International Symposium on Physical Design
sigda

Invited: Navigating the Frontier of Optimality and Complexity: Advanced Design Automation for Wavelength-Routed ONoCs

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Technical University of Munich

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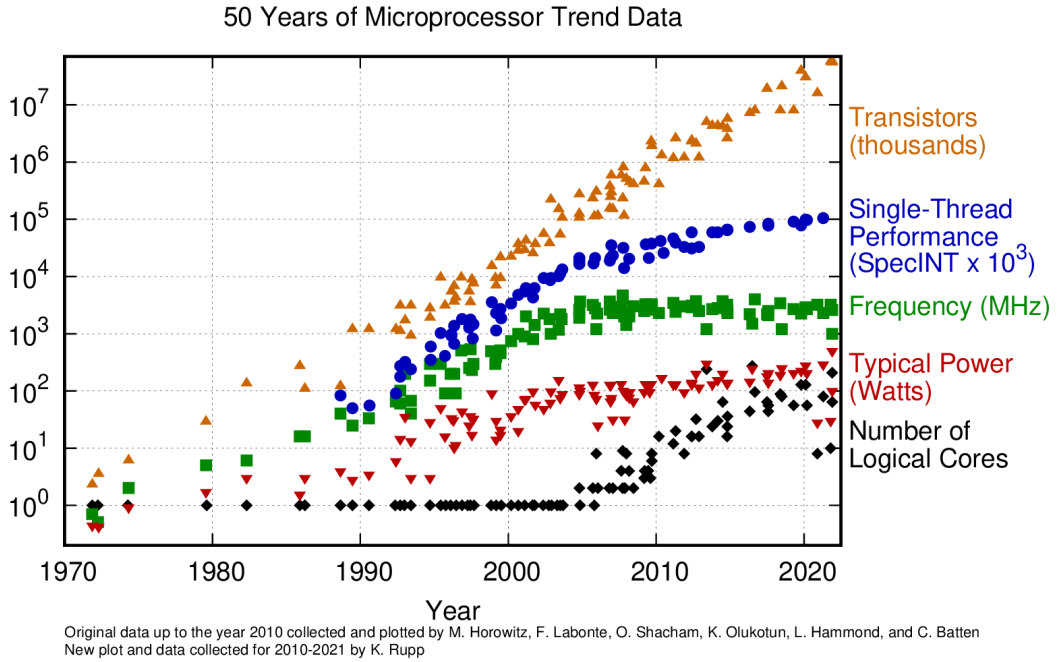
Motivation – The Interconnect Challenge

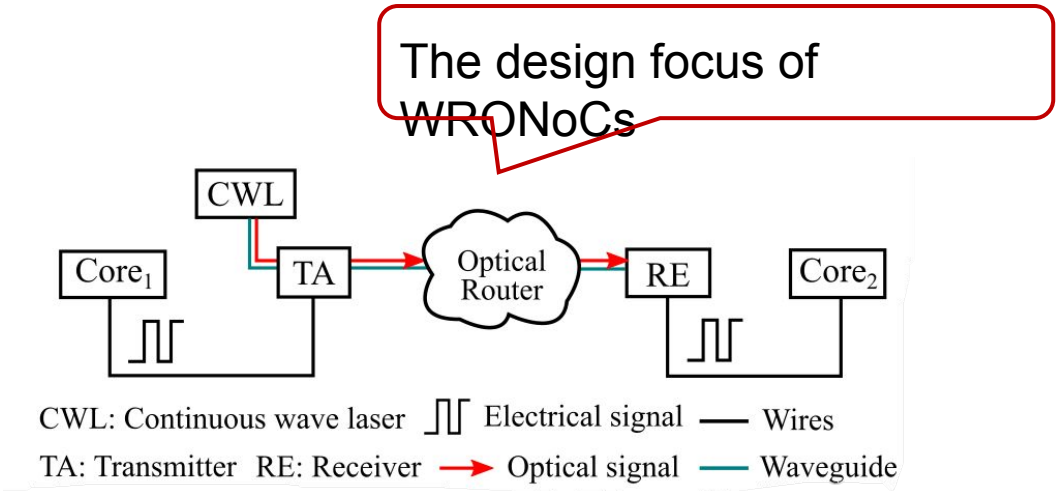
- The Scale-up Era:
  - Modern chips are shifting to many-core.
- The “Interconnect Wall”:
  - Data movement consumes significant power.
  - Conventional electronic networks-on-chip (NoCs) suffer from high power consumption and transmission delay.
- Developing Advanced Interconnect Technologies
  - **Wavelength-Routed Optical NoCs (WRONoCs)** emerge as a promising candidate for supporting on-chip communication with low power and latency.



50 Years of Microprocessor Trend Data
Source: https://github.com/karlrupp/microprocessor-trend-data

The Fundamentals of WRONoCs

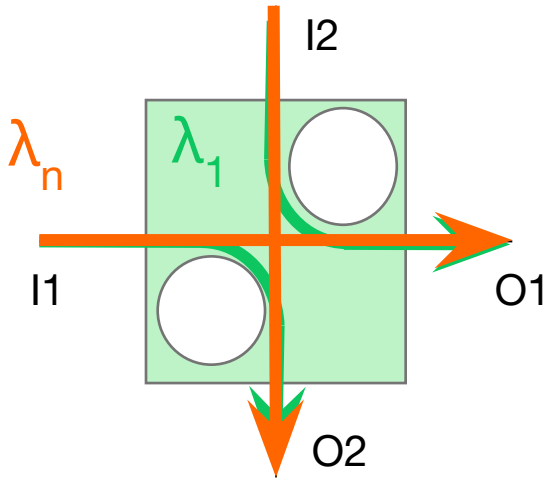
- Key Advantages:
  - High bandwidth with the help of wavelength-division multiplexing (WDM) technology
  - Ultra-low transmission latency (e.g., 10.45 ps/mm[1])
  - No arbitration time and energy consumption[2]
- Basic Components:
  - Laser sources provide multi-wavelength optical carriers.
  - Transmitters and receivers convert signals between electrical and optical domains.
  - Waveguides act as the “optical wires” to guide light across the chip.
  - **An optical router** defines the signal paths for data transmission.



Data transmission between two cores via an optical router.

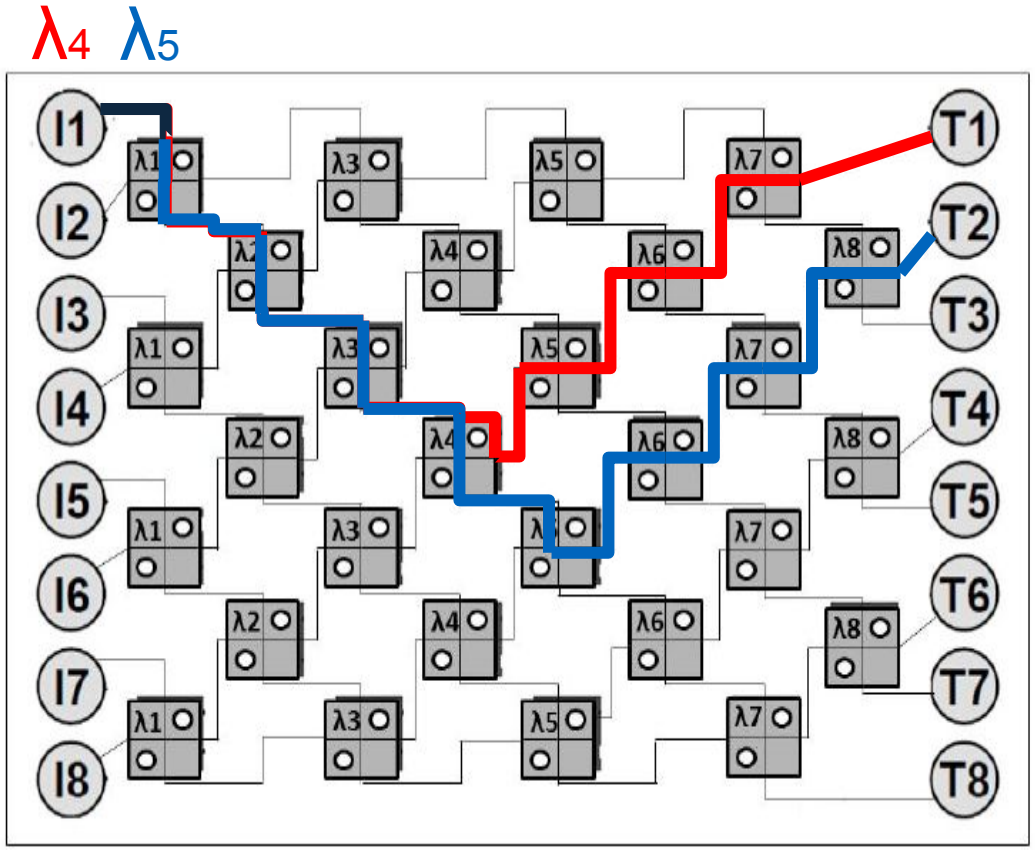
[1] S. V. Winkle et al. “Extending the Power-Efficiency and Performance of Photonic Interconnects for Heterogeneous Multicores with Machine Learning”, in IEEE HPCA, 2018.
[2] T. Tseng, et al. “Wavelength-routed optical NoCs: Design and EDA - state of the art and future directions: Invited paper”, in ICCAD, 2019.

The Fundamentals of WRONoCs



Wavelength λ_1 (resonance) is redirected

Wavelength λ_n crosses



Example: 8x8 λ-Router [Scandurra+ NoCArc'08]

Our WRONoC History

- 2012: Research initiated by contact with Davide Bertozzi, Ferrara
- 2013: ICCAD – PROTON
- 2015: ISPD – Beyond GORDIAN and Kraftwerk: EDA Research at TUM
- 2015: JETC – PROTON
- 2016: ISPD – PLATON (Force-Directed Placement)
- 2019: ISPD – PSION (Template-based Design)
- 2026: ISPD

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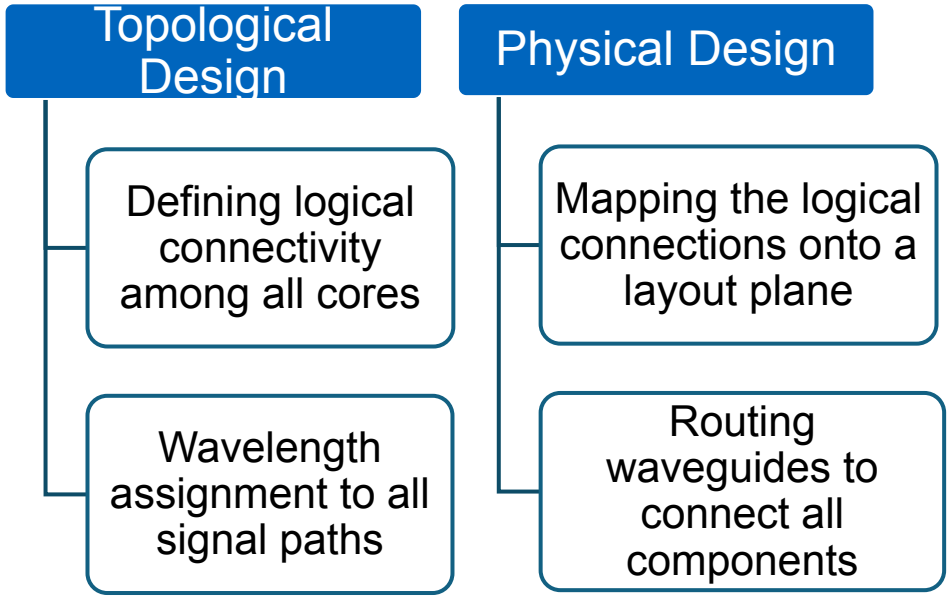
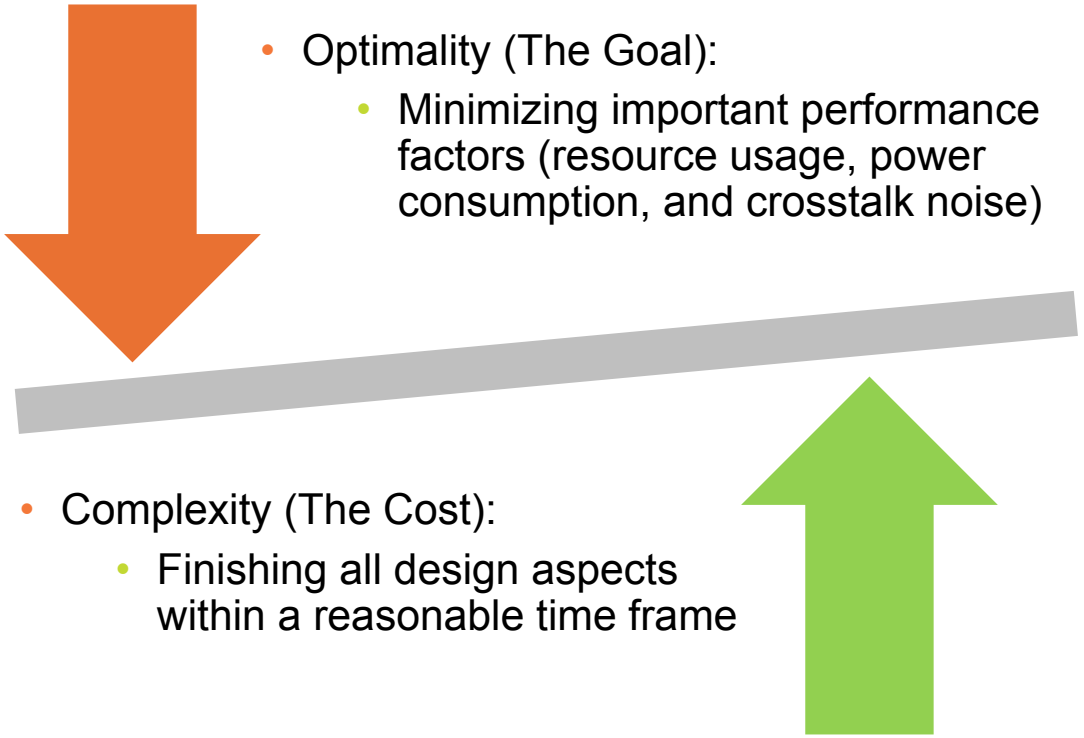
- **2026: ISPD**
- Roughly 35 WRONoC publications so far
- Physical Design Topology / Architecture / Co-Design / Robustness / Crosstalk . . .

Key Design Aspects and Challenges

- Key design aspects

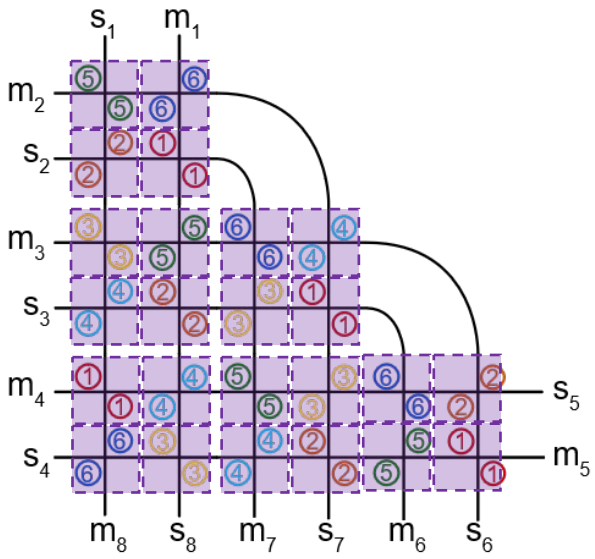


- The core challenge: **optimality vs. complexity**

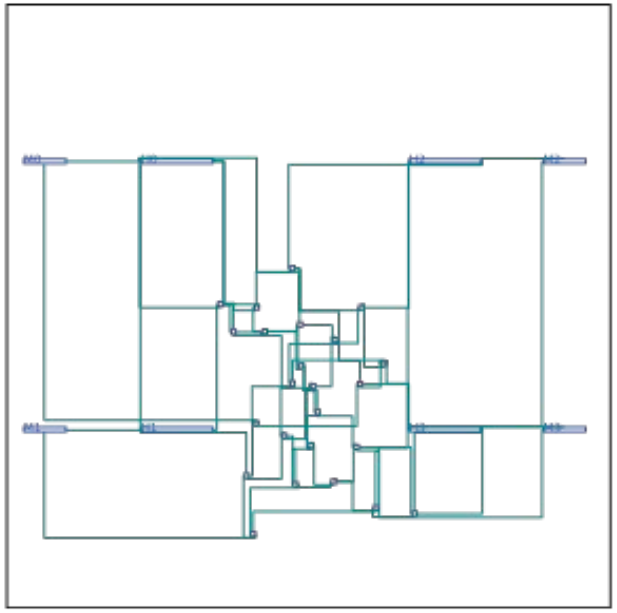


State-of-the-art Designs and Their Limitations

- Sequentially performing topological design and physical design
  - ✚ **Manageable design complexity**: Each stage has a limited search space, and each step is handled by specific methods or tools.
  - ▬ **Suboptimality**: Early-stage decisions made during topological design without layout awareness often lock the design into configurations that are physically suboptimal or even infeasible.



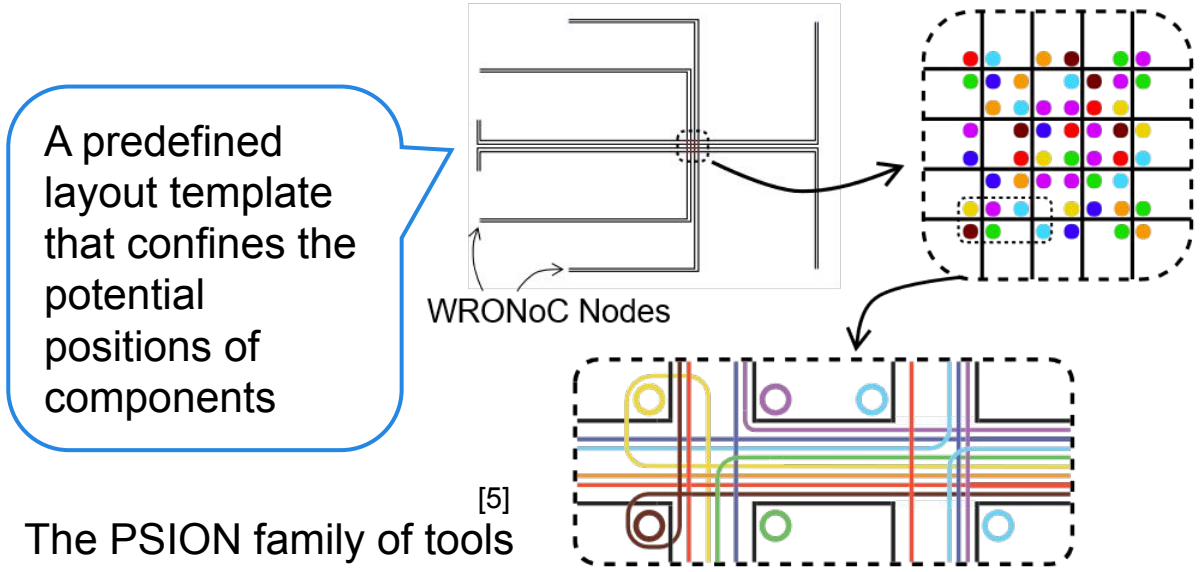
GWOR Logic Scheme[3]


Layout by PROTON+[4]

[3] X. Tan et al. “On a Scalable, Non-Blocking Optical Router for Photonic Networks-on-Chip Designs.”, in SOPO, 2011.
[4] A. V. Beuningen et al. “PROTON+: A Placement and Routing Tool for 3D Optical Networks-on-Chip with a Single Optical Layer”, in JETC, 2015.

State-of-the-art Designs and their Limitations

- Concurrently conducting topological design and physical design
  - ✚ **Holistic optimization:** Jointly optimizes the topology generation and layout synthesis in a single search space.
  - ▬ Exponential growth in complexity: The search space grows exponentially as the number of nodes increases.



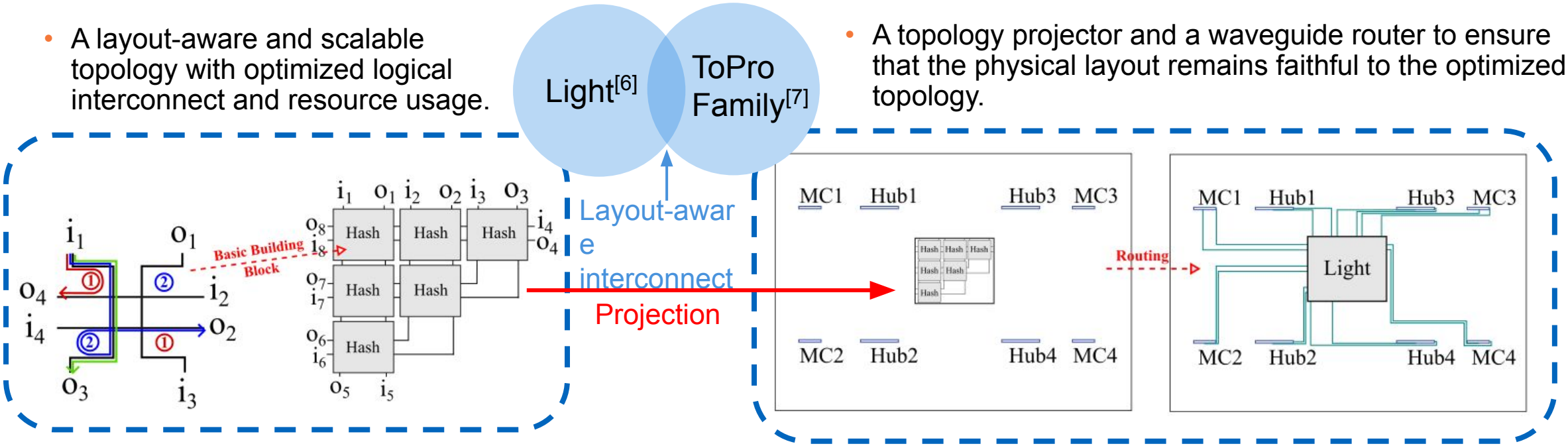
The PSION family of tools [5]

The design of every routing component, the setup of signal paths, and the wavelengths of all components are simultaneously decided

[5] Alexandre Truppel et al., "PSION: Combining Logical Topology and Physical Layout Optimization for Wavelength-Routed ONoCs," in ISPD, 2019.

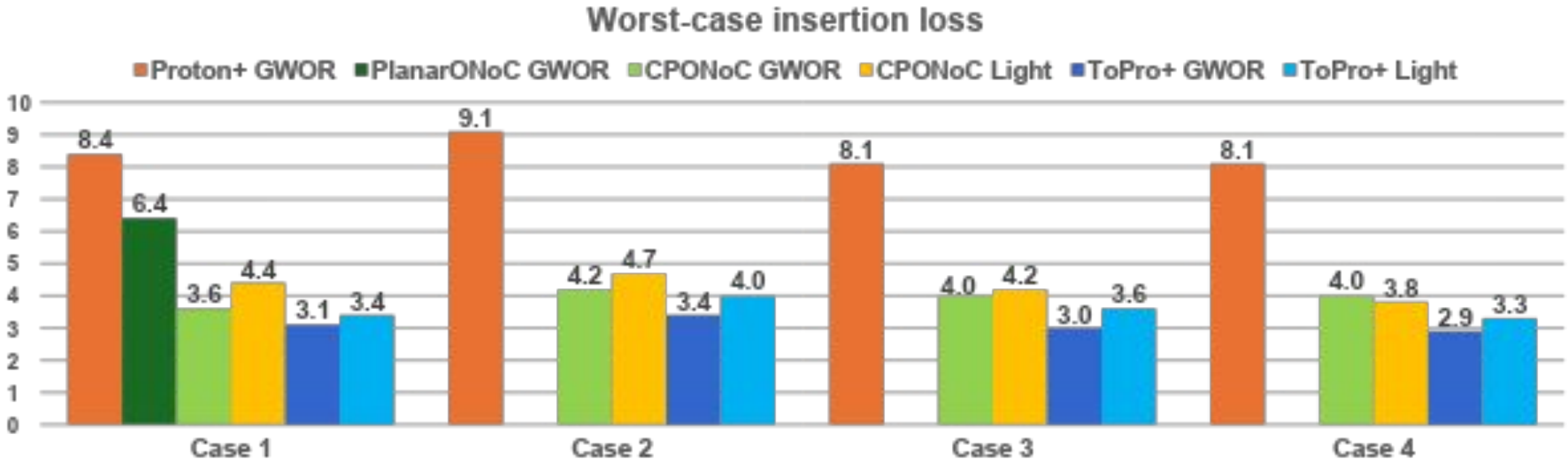
Two Advanced Design Automation Methodologies

- Layout-aware topological design and topology-projection-based physical design
  - A layout-aware and scalable topology with optimized logical interconnect and resource usage.
  - A topology projector and a waveguide router to ensure that the physical layout remains faithful to the optimized topology.



[6] Z. Zheng et al., “Light: A Scalable and Efficient Wavelength-Routed Optical Networks-On-Chip Topology” in ASP-DAC, 2021.
[7] Z. Zheng et al., “ToPro+: A Topology Projector Considering Port Assignment and Waveguide Routing for Wavelength-Routed Optical Networks-on-Chip”, in JOCN, 2025.

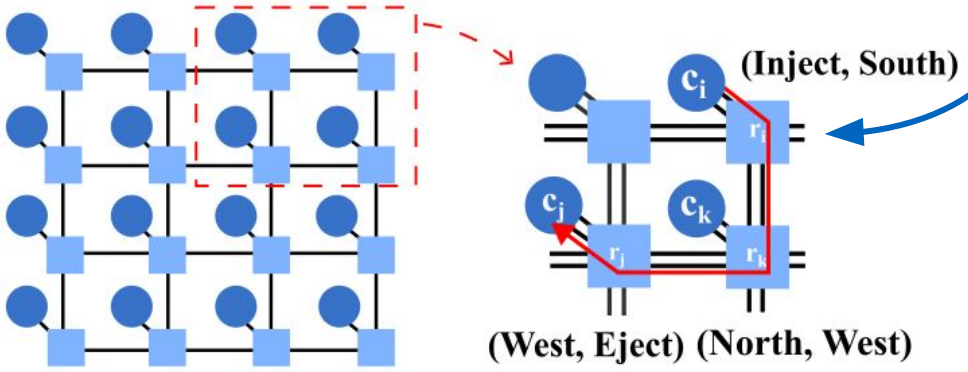
ToPro+ - Comparison Results



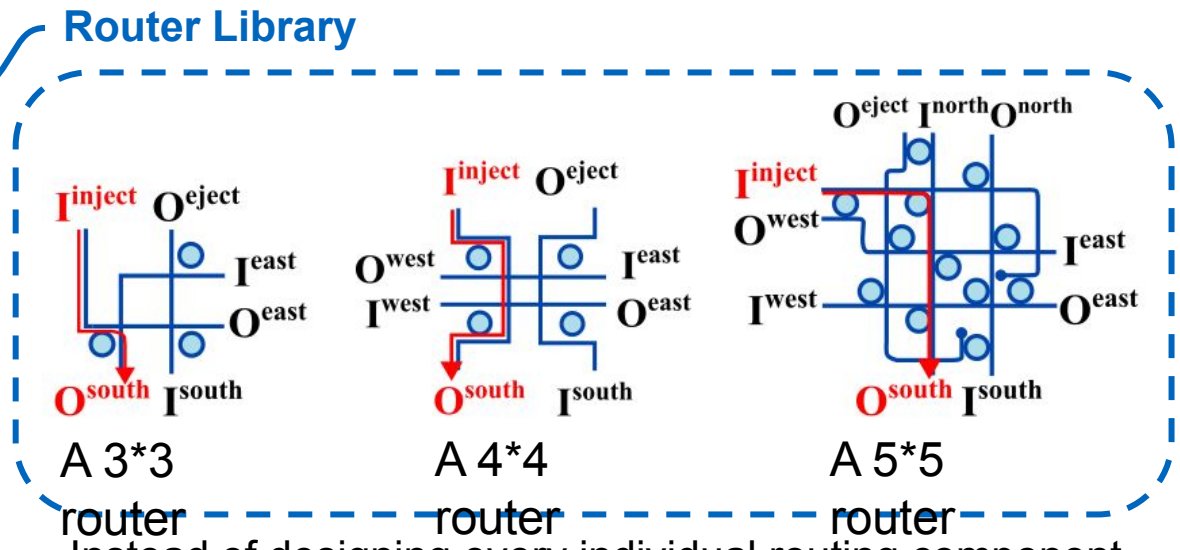
- Compared to the physical design tools in the sequential design flow, ToPro+ **decreases the worst-case insertion loss by about 50%** on average for all cases.

Two Advanced Design Automation Methodologies

- Co-optimization of interconnect design and layout synthesis based on mesh structure [8]



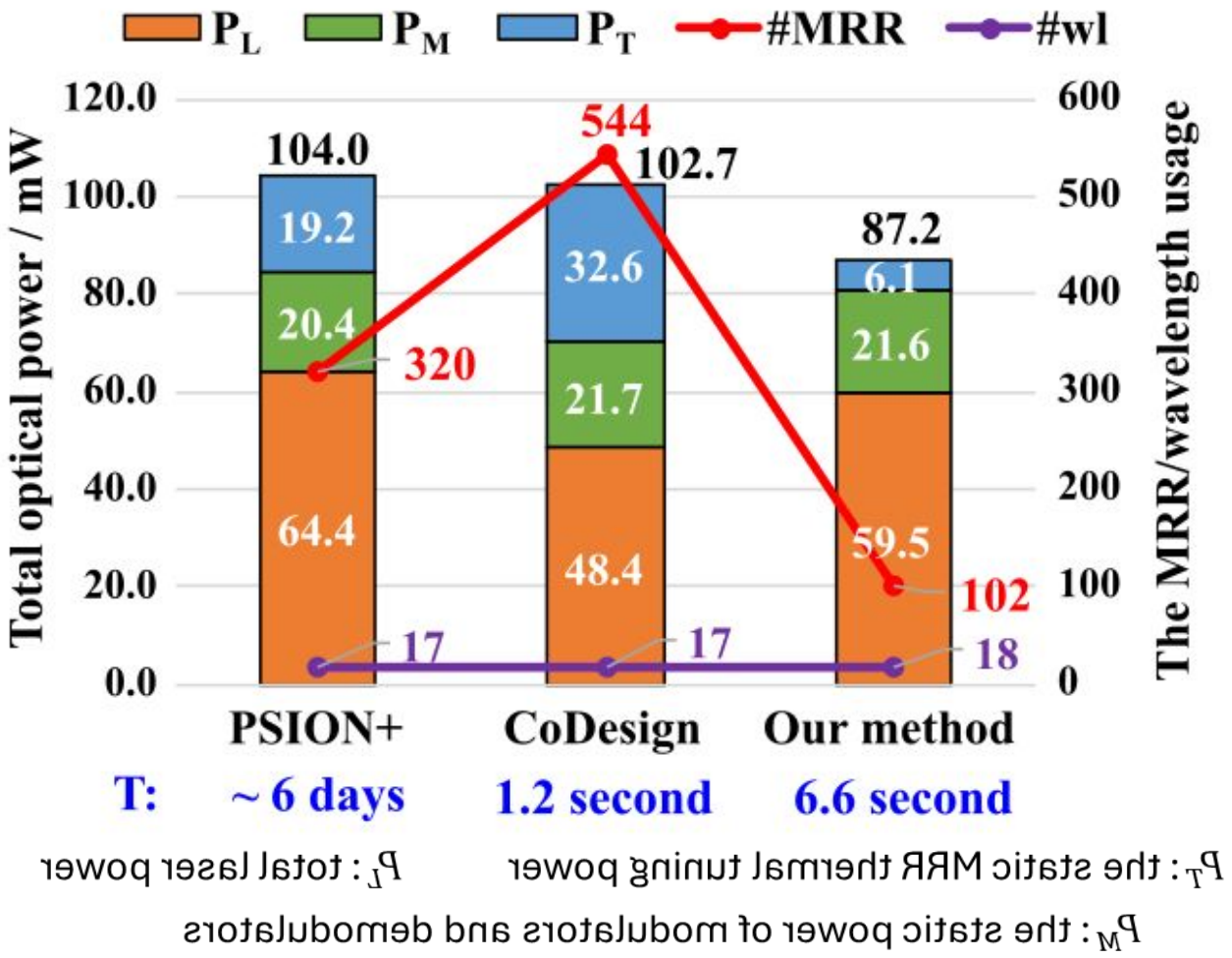
- The connections between cores and optical routers are fixed and extendable.
- Leveraging the regularity of the Mesh structures to prune the search space without sacrificing path diversity.



- Instead of designing every individual routing component from scratch, we apply pre-designed, optimized optical routers.

[8] Z. Zheng et al., "Multi-Resonance Mesh-Based Wavelength-Routed Optical Networks-on-Chip" in DAC, 2024.

Co-Optimization - Comparison Results



- Our method **decreases the total optical power by 14%** compared to PSION+ and CoDesign, two design methods performing concurrent design flow.
- Our method **minimizes the MRR usage** among the three methods.
- Our method can **synthesize the design within a few seconds** without suffering high computational complexity.

Conclusion

- This work provides a viable pathway to navigate the trade-off between **design optimality and computational complexity**.
- Advanced design automation methodologies for WRONoCs:
  - Layout-aware topological design + Interconnect-preserving physical design
  - Co-optimization framework utilizing a mesh structure and efficient optical routers
- Key results
  - Enhanced performance: achieved a significant reduction in insertion loss compared to state-of-the-art design methodologies.
  - Improved computational efficiency: synthesized high-performance WRONoCs for large-scale networks in seconds, outperforming current methods in runtime.
- Future impact
  - Establishing a foundation for the automated design of next-generation, energy-efficient HPC interconnects.

Thank you!

Any Questions?

Backup

ToPro+ - Comparison Results

- For a 16-node network

		#wl	#MRR	il_w	P_L	P_{MD}	P_T	P_{total}	T
PSION+	Center CGT-e10	17	320	n/a	65.6	20.4	19.2	**105.2**	6 days
	Bottom CGT-e10	17	320	4.20	64.4	20.4	19.2	**104.0**	
CoDesign		17	544	n/a	48.4	21.7	32.6	**102.9**	n/a
ToPro+	GWOR	15	224	3.81	45.1	18.0	13.4	**76.5**	14.3
	Light	16	112	3.27	42.6	19.2	6.7	**68.5**	11.5

il_w: the maximum insertion loss value denoted in dB. #MRR: the number of MRRs. $\#wl$: the number of wavelengths.
T: the program runtime denoted in seconds.

- Compared to the state-of-the-art design tools for the concurrent design flow, ToPro+ **decreases the total power consumption by more than 30%** for the large-scale networks.