LiDAR 3.0: Photonics-Aware Planning-Guided Automated Electrical Routing for Large-Scale Active Photonic Integrated Circuits

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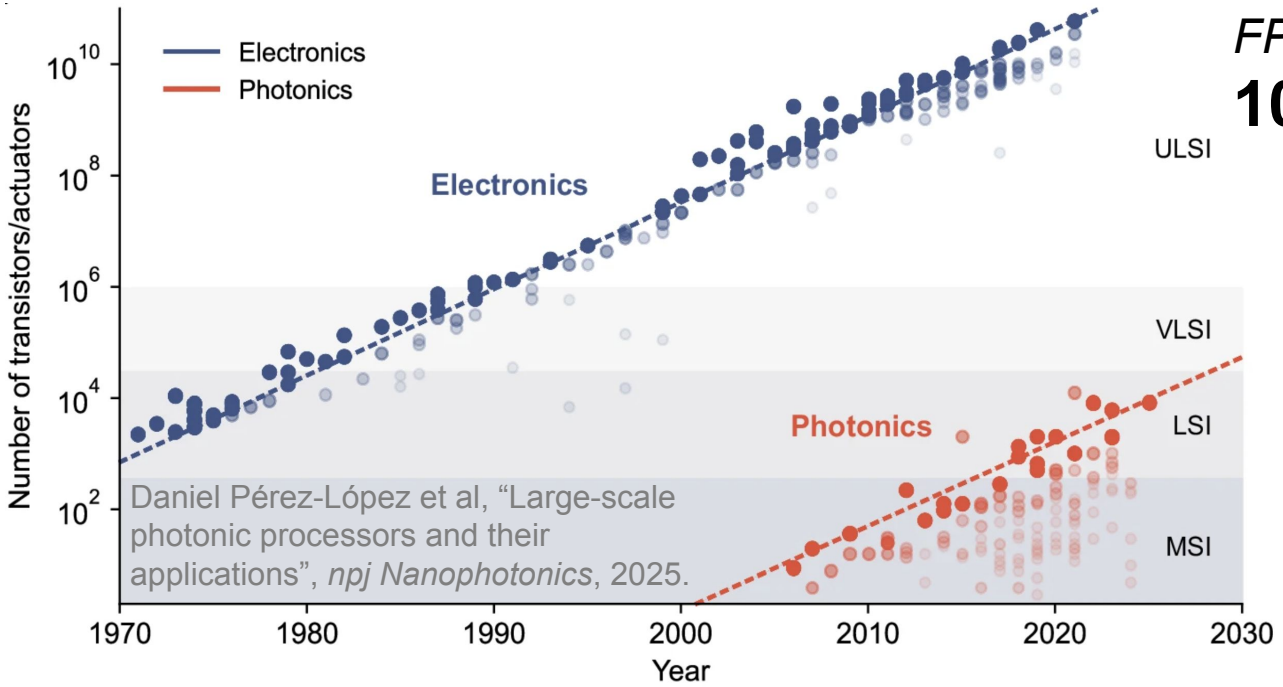
VLPI + EPDA Era



Daniel Pérez-López et al, "Large-scale photonic processors and their applications", *npj Nanophotonics*, 2025.

Very Large-scale Photonic integration (VLPI) Era

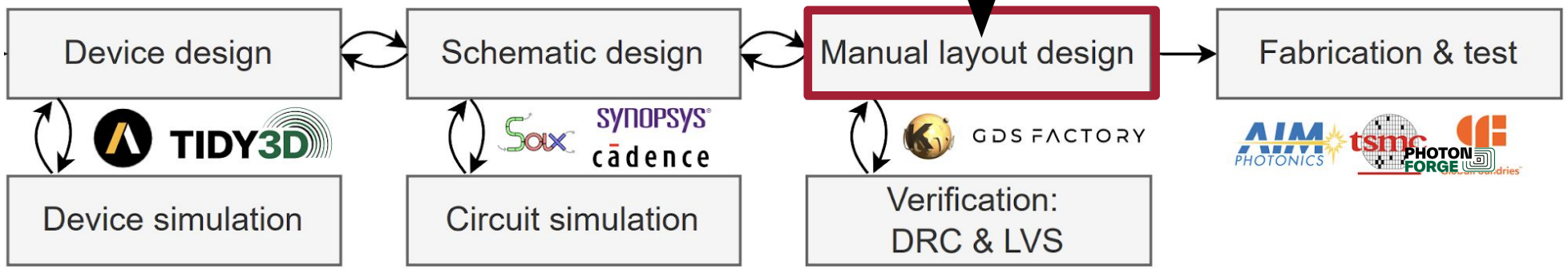
RF, switching, interconnect, LiDAR, beamformer, photonic FPGA, photonic computing, heterogeneous 3D EPIC…

100~10k components and beyond

Electrical wires in active PIC

Heavily relies on manual design in several months!

Time-consuming & Not scalable for large-scale EPICs



3 min per wire

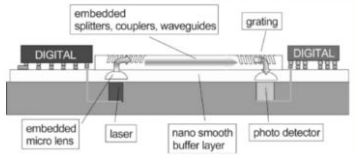
→

Months to route 1k wires

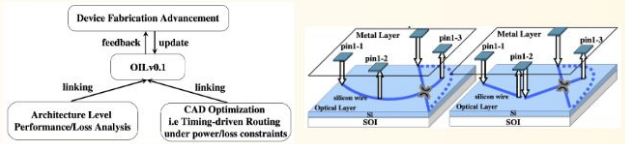
H. Zhou, P. Ma, J. Gu *et al*, "Toward Intelligent Electronic-Photonic Design Automation for Large-Scale Photonic Integrated Circuits: from Device Inverse Design to Physical Layout Generation", *SPIE ODA*, 2025.

LiDAR-series in PIC Layout Literature

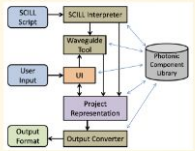
Tools for early stage small-scale optical network-on-chip



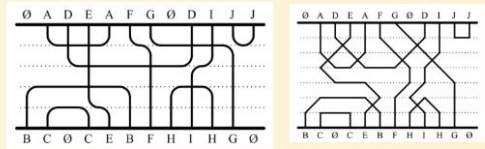
Proposed ***optical routing*** for system on package [Minz+, DATE'06]



OIL: ***Reusable*** optical interconnect library, O-Router: power/loss-aware routing [Ding+, SLIP'09]



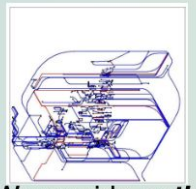
VANDAL: ***scriptable*** layout generation for scalable PIC [Hendry+, DATE"11]



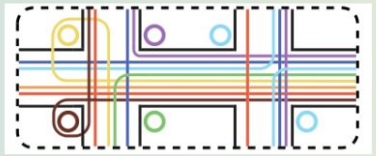
Optical Manhattan/Non-Manhattan ***channel detailed routing*** [Condrat+, SLIP'13]

2007 2009 2011 2012

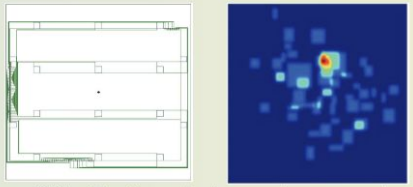
Focus on WRONoC placement & routing, optimize topology and insertion loss



Waveguide ***path length matching*** [Chuang+, ICCAD'21]



PSION: WRONoC logical topology and physical layout ***co-optimization*** [Truppel+, ISPD'19]



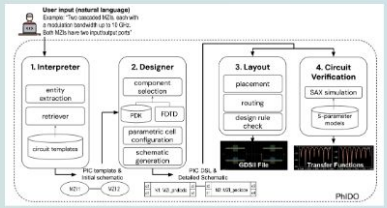
PlanarONoC: Graph-based ***near-planar*** placement [Chuan+, DAC'18]; ***Thermal-aware*** placement [Jiao+, ISCAS'18]

PLATON: ***scalable force-directed*** photonic placement [Beuningen+, ISPD'16]

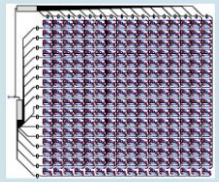
Proton: ***End-to-end*** photonic placement and routing [Boos+, ICCAD'13]

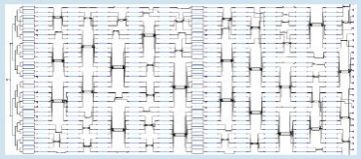
2021 2019 2018 2016 2013

Handle large-scale photonic integrated circuits, generate real GDSII layout

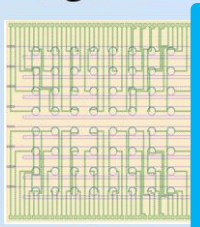


PhiDO: LLM-assisted PIC design [Sharma+, APL'25]

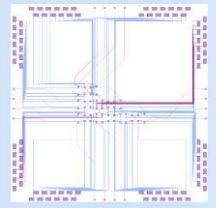




LiDAR/LiDAR2.0: Curvy waveguide detailed routing
Apollo: GPU-accelerated large-scale PIC placement [Zhou+, ISPD'25, ICCAD'25]



PICELF [Jiang+, DATE'25]



iDAR3.0: metal router [Zhou+, ISPD'26]

- *Advanced packaging*
- *Co-packaged optics*
- *3D-HI PIC*
- *Panel/wafer-scale VLPI*
- *...*

Future directions

2025 2026

LiDAR 1.0 / 2.0 → **LiDAR 3.0** Metal Route

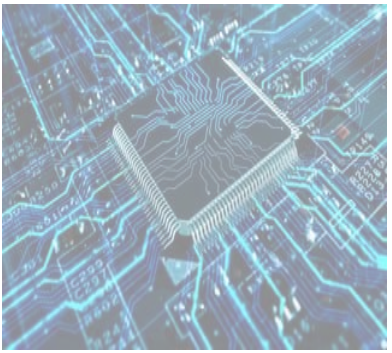
enable

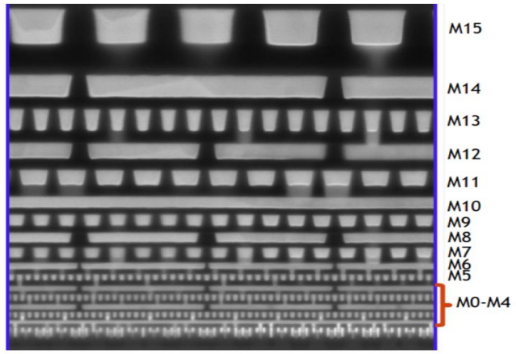
Path finding

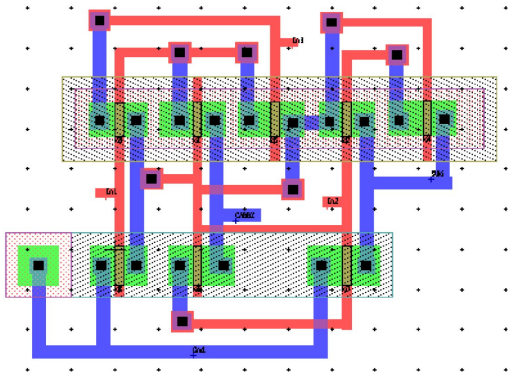
Curvy waveguide routing

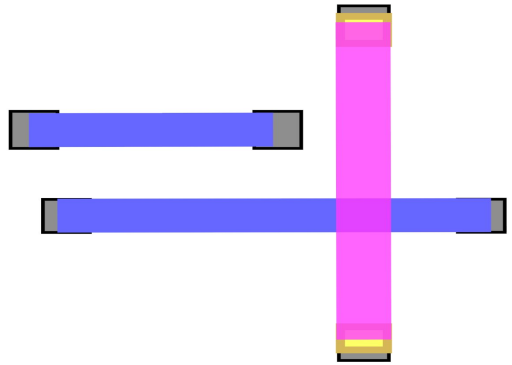
Full PIC place + E-O route

Unique Challenges of PIC Electrical Routing









EIC

15+ metal layers

Many *local* short wires

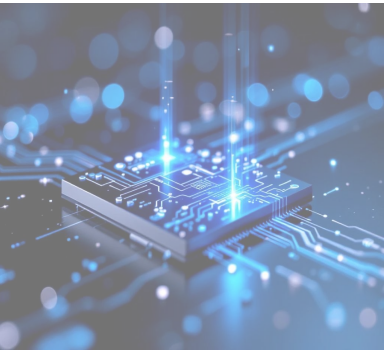
Low contention within layer

PIC

Very few metal layers in current foundry (2 in AIM, 8 in GF)

Many *pin-to-IO* **mm-long** wires

High contention within layer



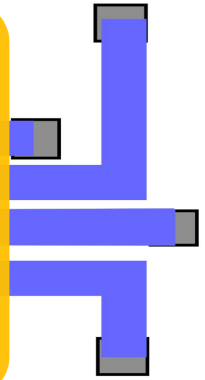
1

Fundamental conflict:

Restricted routing resources

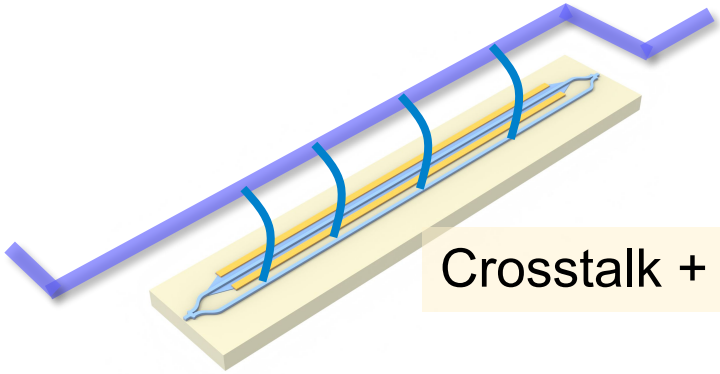
vs.

High routing demand

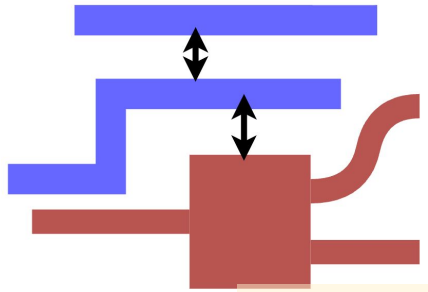


Unique Challenges of PIC Electrical Routing

- *Analog nature* of PIC → performance sensitive to metal routing
- Electrical-photonics interaction
  - Metal near optics induces **crosstalk + loss**!
- Customized rules / user preferences
  - Conservative design style
  - PDK min-pitch 0.5um *vs.* **user-preferred: 3~5um**



Crosstalk + loss



Custom spacing

2

Fundamental challenge 2

Customized **performance-oriented rules / constraints**

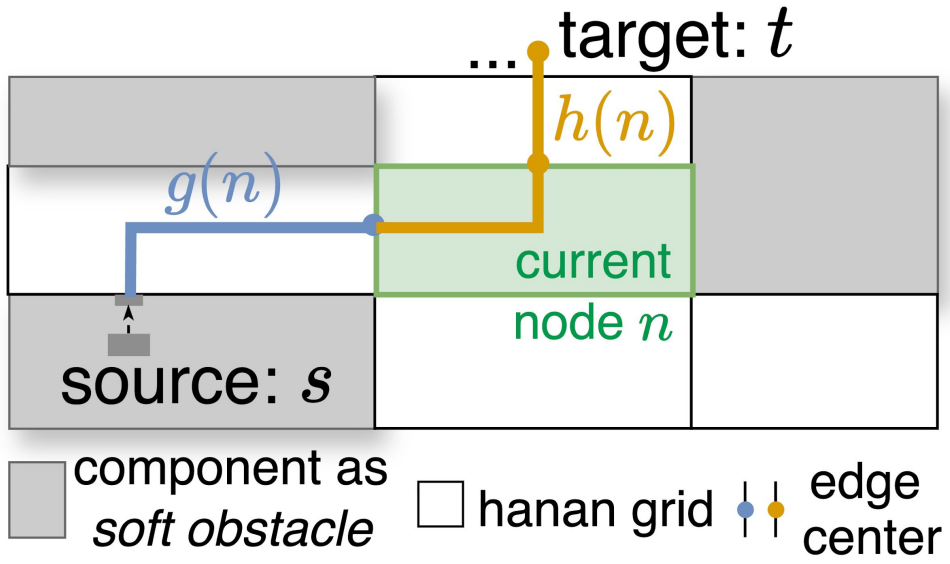
Proposed Framework: LiDAR 3.0

- **Routing grid and routing engine**
  - Hanan grid as routing grid
    - **Avoid** photonic components
  - ***A* search*** as core routing engine
    - f(n) = g(n) + h(n)

g(n): accumulated distance from s to n

h(n): distance from current node n to target t

Edge center is used for cost calculation



- ***How to generate a near-planar solution?***
  - *Sol:* Escape routing + area routing + crossing-aware A* search
- ***How to satisfy user design constraints?***
  - *Sol:* Sequence-consistent track assignment
- ***How to utilize the global routing guidance in detailed routing?***
  - *Sol:* Soft guidance-assisted detailed routing

How to Generate a Near-Planar Solution?

❶ Escape the pins/pads to region boundaries

- Escape order: pins closer to boundary → higher priority
- Boundary side capacity = # I/O pads on that side

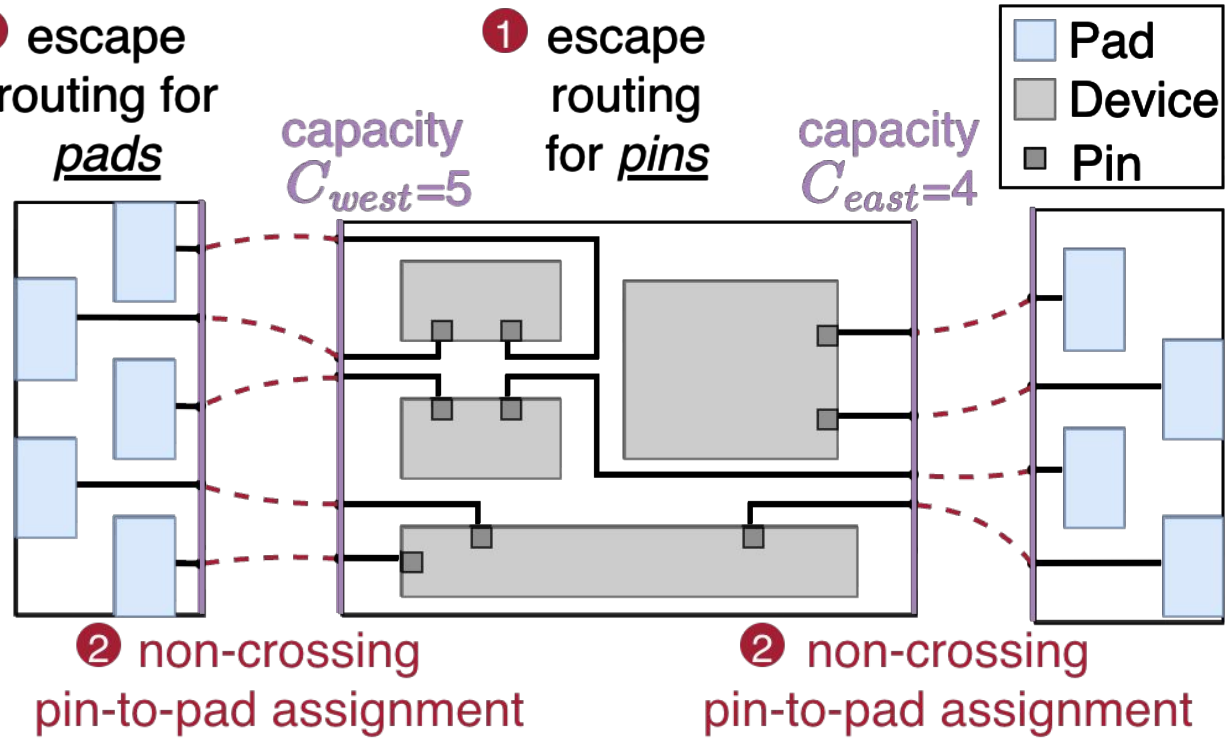
❷ Crossing-aware planar routing "bridges" two ends

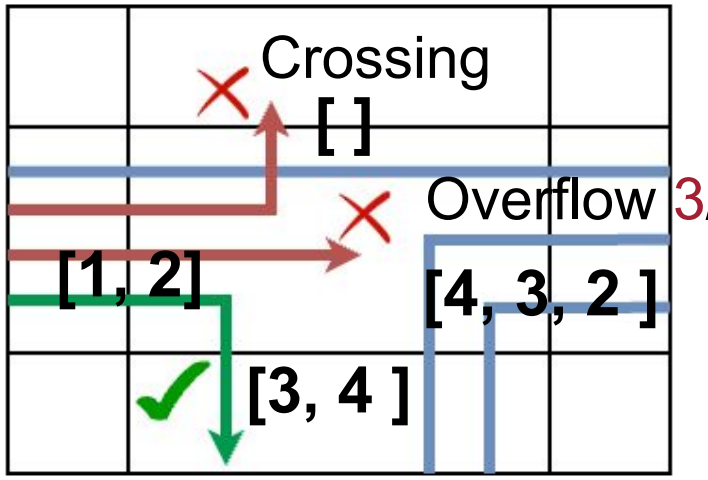
- Avoid crossing by checking net sequence order & edge capacity

Multi-stage planning

(Hard) many-to-many routing

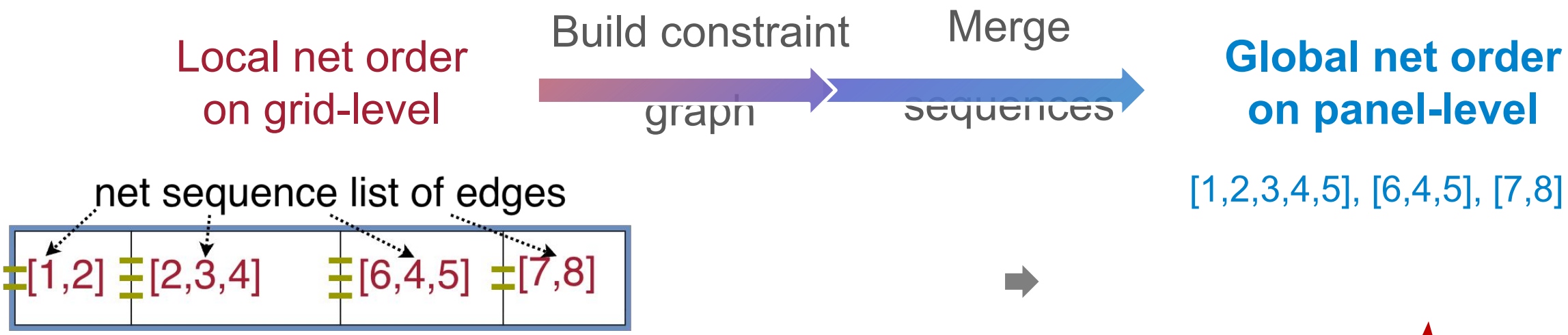
→ **(Easy) 1-to-1 map & route**





How to Satisfy Customized Rules?

- Sequence-consistent track assignment
  - **Key insight**: *joint track assignment with global-view planning*



  - **Which track** to assign the wire segment?
    - min wirelength + honor spacing rules + avoid waveguide overlap

How to Leverage the Global Routing Guidance?

- Global routing adds guidance cost in detailed routing

  $f(n) = g(n) + h(n) + \textbf{cost}$

✗ Hard guidance: once deviate, never come back…

✓ **Soft guidance**: distance-based *attractive force*

→ faster and higher quality

Evaluation Setup

- **Platform**
  - Linux server with a 128-core AMD EPYC 7763 CPU and 512 GB memory
  - Python 3.11 for global routing and C++ for detailed routing
- **Baseline** PIC routers
  - Base-1: Anaroute in MAGICAL [Xu+, ICCAD'19]
    - Supports multiple metal layers and arbitrary routing directions within each layer
  - Base-2: Anaroute* [Xu+, ICCAD'19] with penalty routing over optical devices
- **Benchmark** suits
  - *Computing*: photonic tensor core (PTC)
    - Clements-style MZI arrays [Shen+, NatPhoton'17]
    - ADEPT auto-searched PTC [Jiang+, ASPDAC'25]
  - *Interconnect*: Wavelength-routed Optical NoC [Tan+, JLT'11]

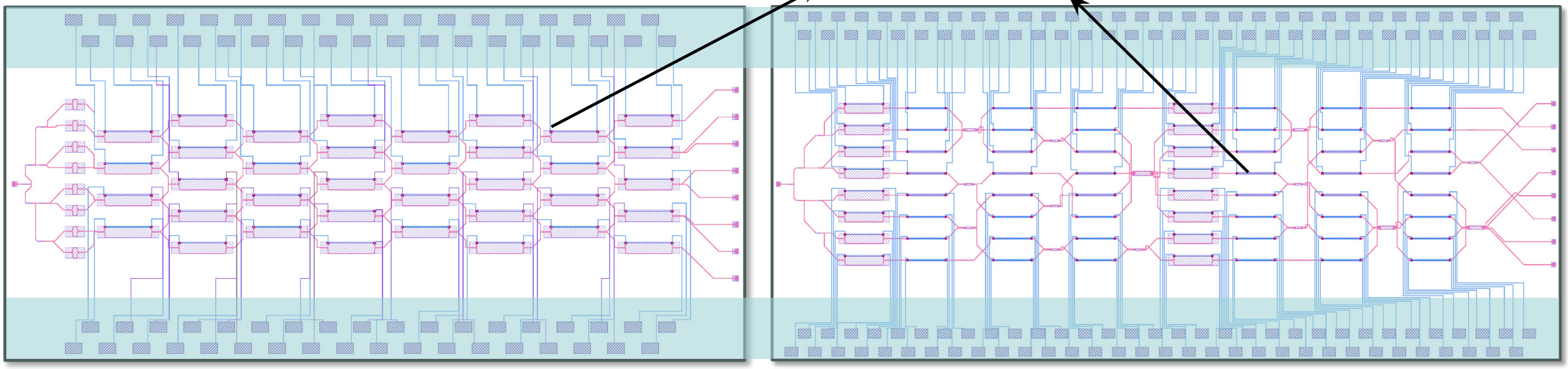
Photonic Computing Benchmarks

Clements: classic MZI-array matrix multiply unit [Shen+, NatPhoton'17]

ADEPT: auto-searched subspace photonic tensor core [Jiang+, ASPDAC'25]

Electrical I/O pads on chip edge

Dense device pins in center to escape



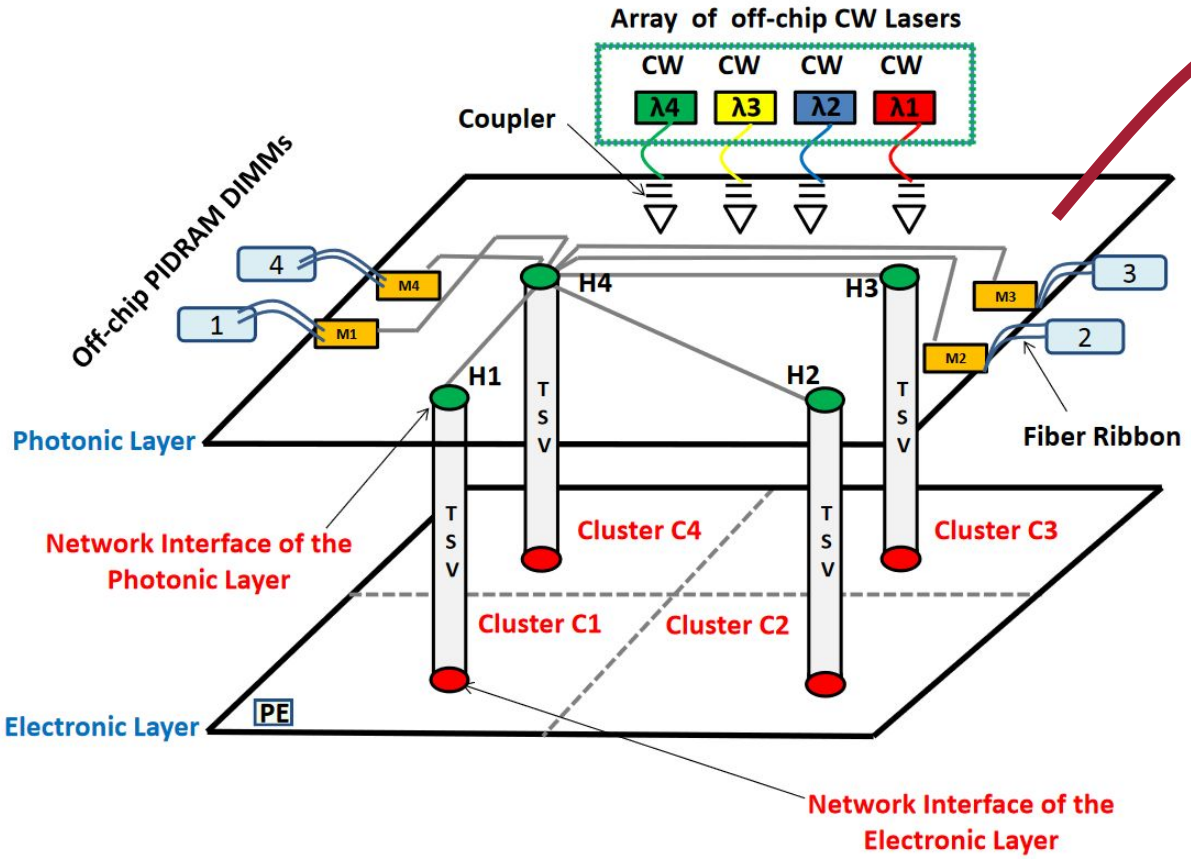
Clements

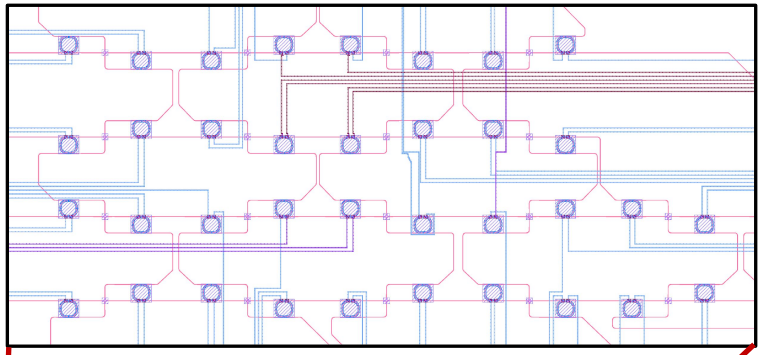
ADEPT

Largest benchmark: 1682 devices, **1056** nets, die size: **14.3mm × 6.1mm**

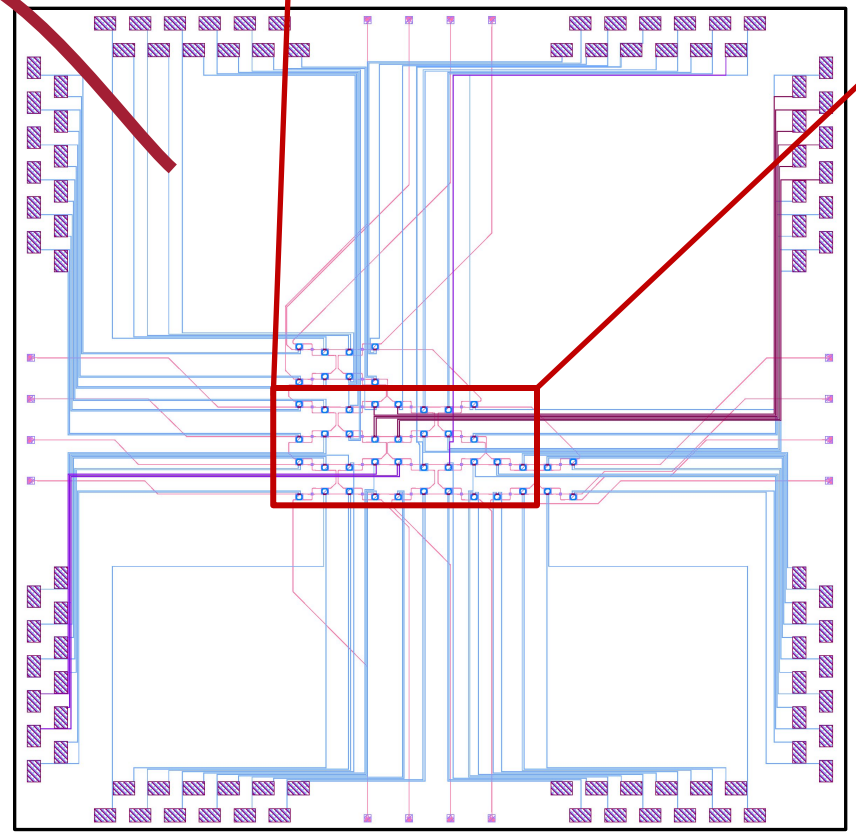
Optical Interconnect Benchmarks

- Wavelength-routed Optical Network-on-Chip
- I/O pads on four edges
- High pin density in micro-ring arrays



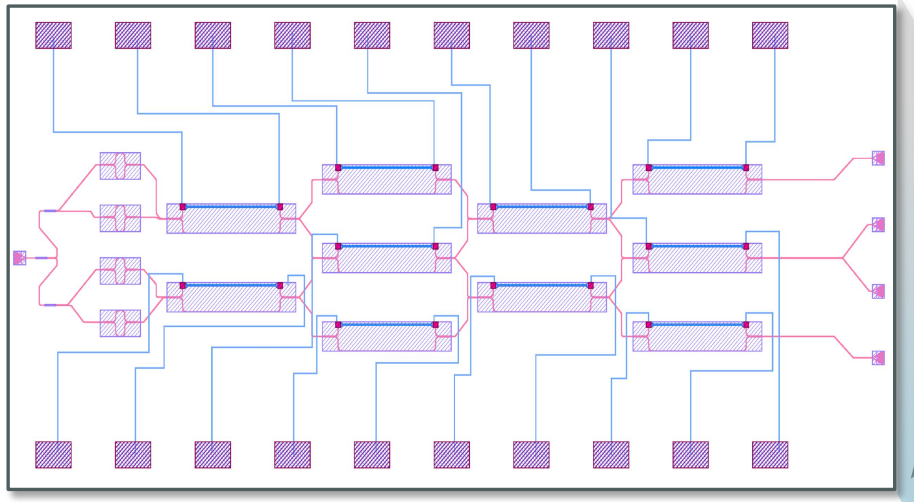


Escape Routing Using Multi-layer



LiDAR 3.0 Matches Manual Routing Well

Manual Layout Reference

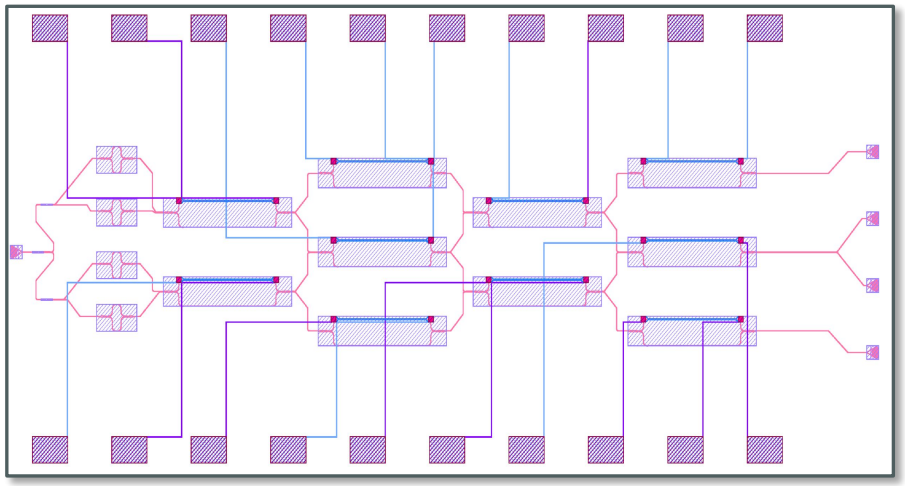


✓ # Layer: 1

✓ # Violation: 0

✗ Time: ~1 hour

Match well

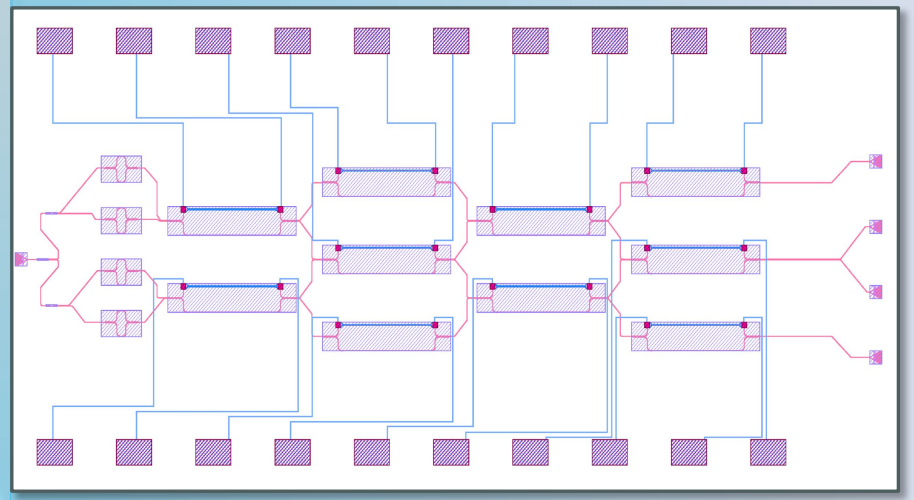


Anaroute

⚠ # Layer: 2

✗ # Violation: 23

⚠ Time: 50 s



LiDAR 3.0

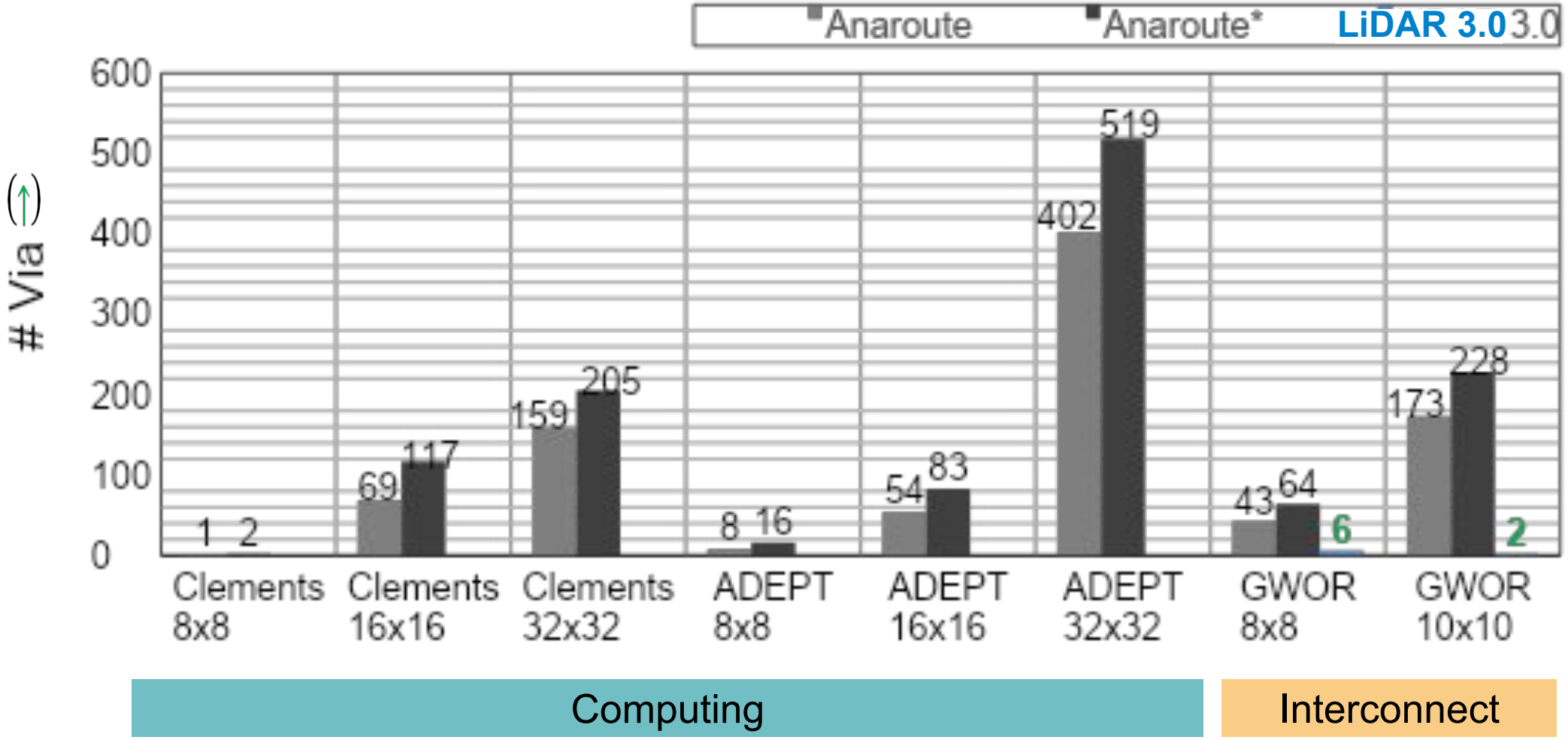
✓ # Layer: 1

✓ # Violation: 0

✓ Time: 8 s

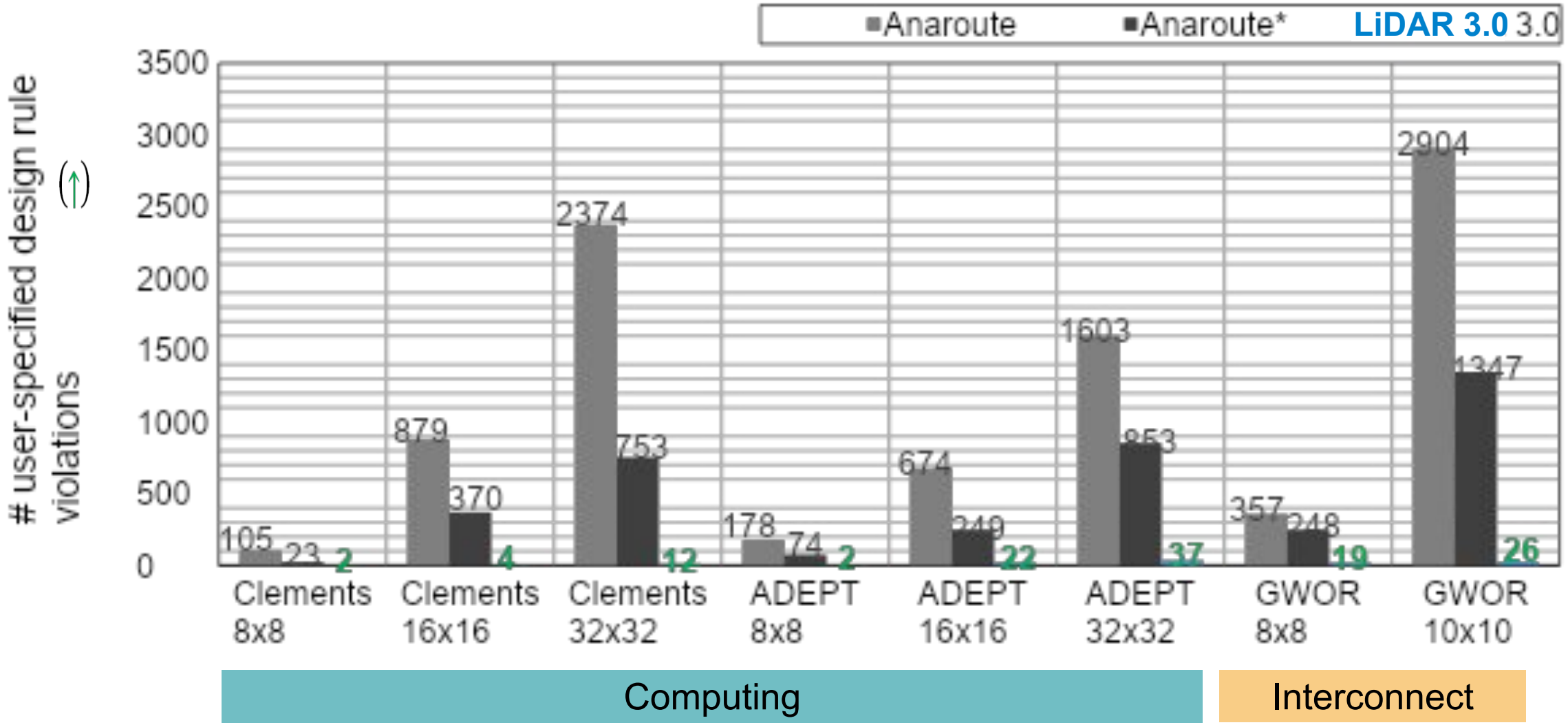
Via Usage Reduction

- **LiDAR 3.0** reduces Via count by **99%** vs. Anaroute
- Achieves **0** routing Via on computing benchmarks.



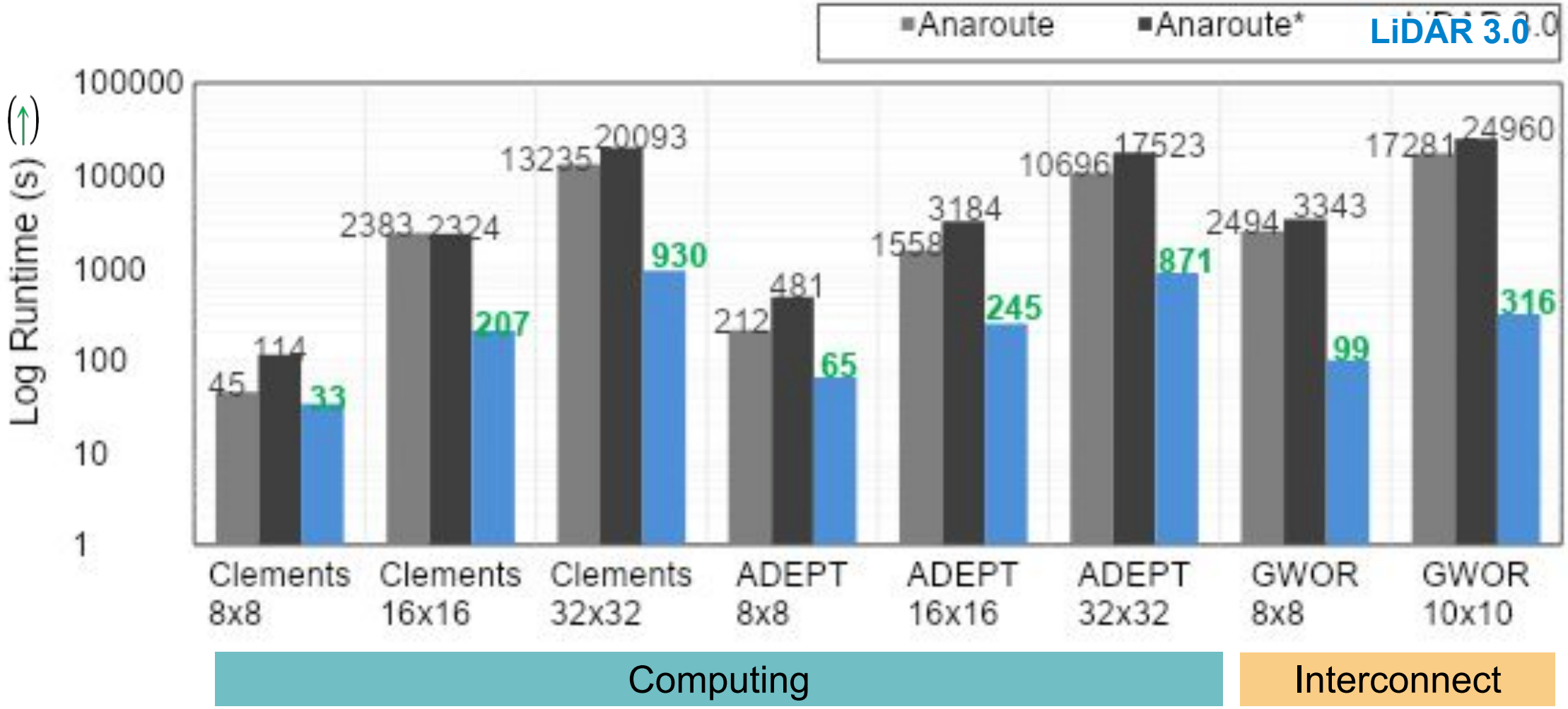
User-Specified Design Rule Violation Comparison

- **LiDAR 3.0** better satisfies the user-specified design rules
  - **98%** fewer violations than Anaroute; **96%** fewer than Anaroute*.



Runtime Comparison

- **LiDAR 3.0** is **17× / 25×** faster than Anaroute / Anaroute*
  - Routing guidance significantly reduces the searching space

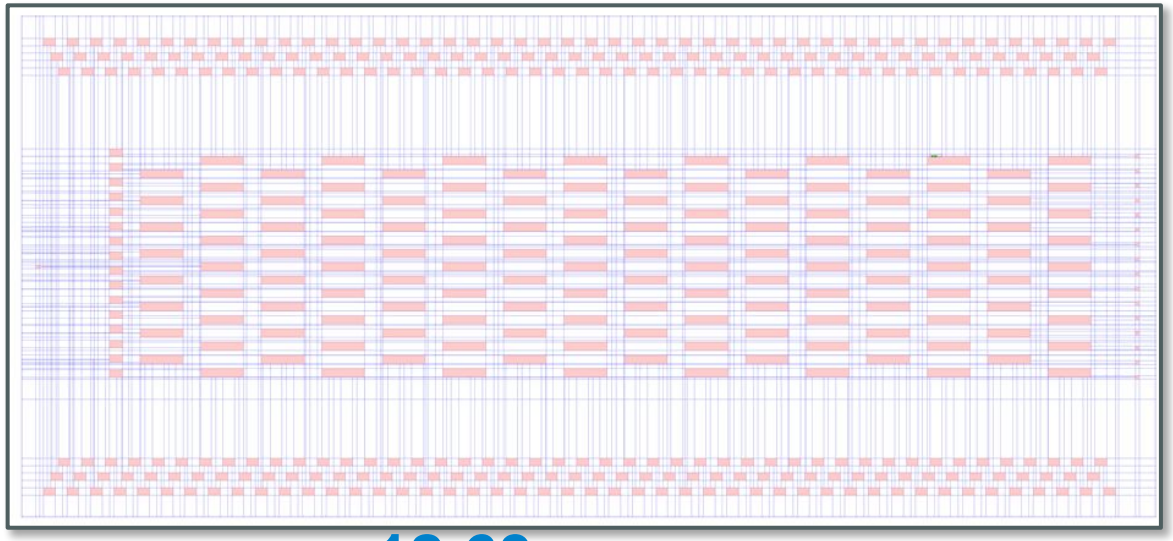


Animation of Global Routing and Track Assignment

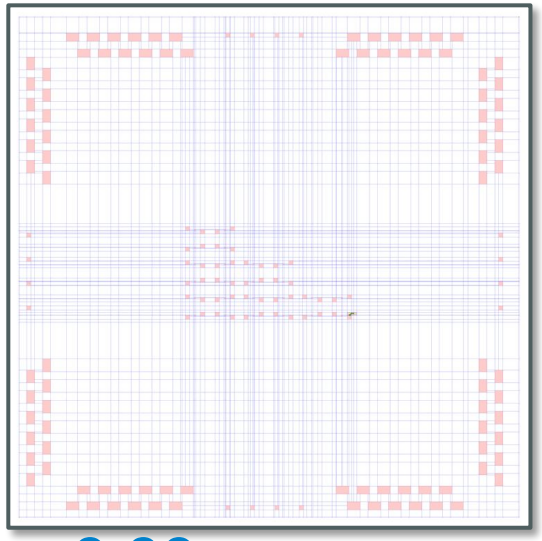
Clements_16×16 (#metal wires: **271**)

GWOR_8×8 (#metal wires: **95**)

Global planning

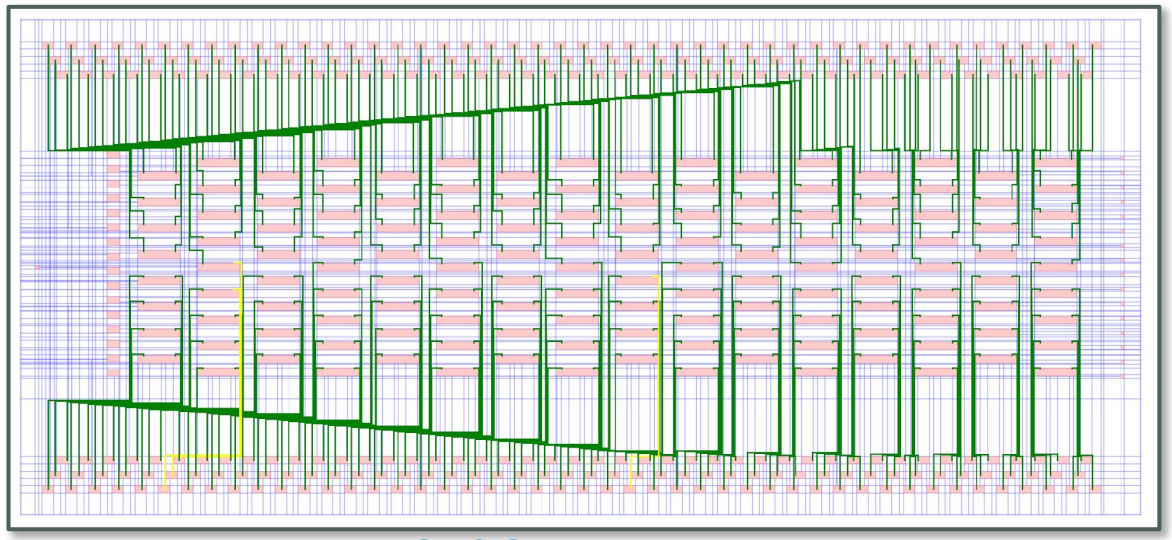


12.63s to finish

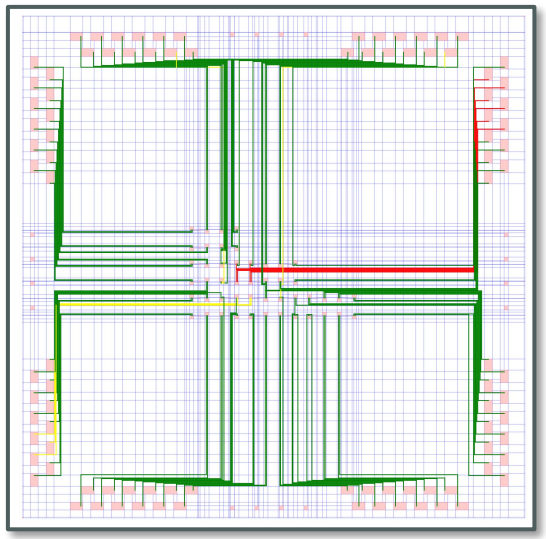


3.33s to finish

Track assignment



0.62s to finish



0.03s to finish

Low congestion

High congestion

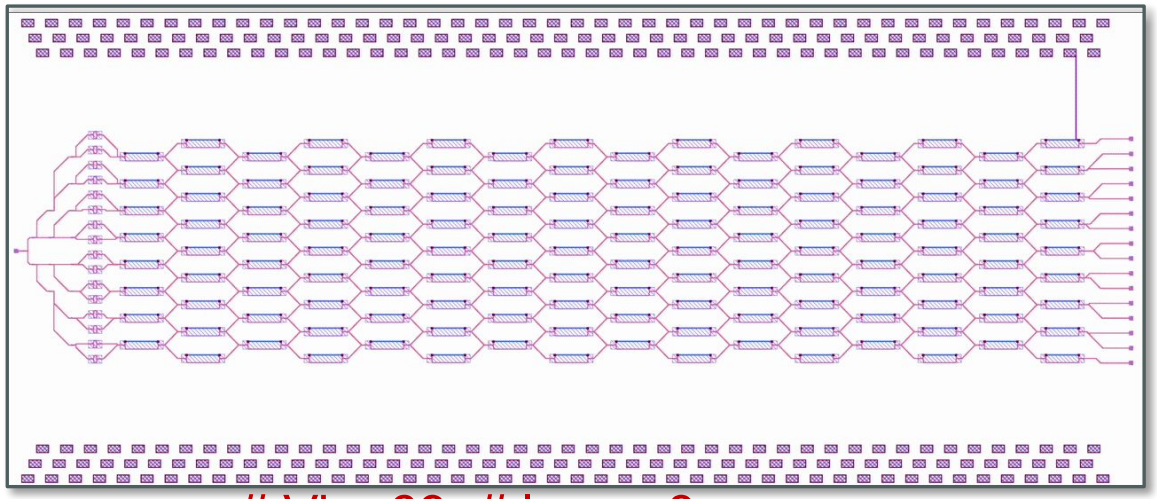
Animation of PIC Electrical Detailed Routing

Clements_16×16 (#metal wires: **271**)

GWOR_8×8 (#metal wires: **95**)

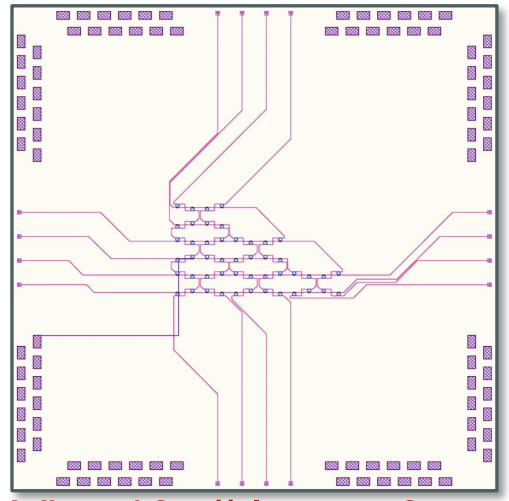
Anaroute

w/o routing guidance



Via: 69, # layer: 3

Violation: 879, Time: 2383s

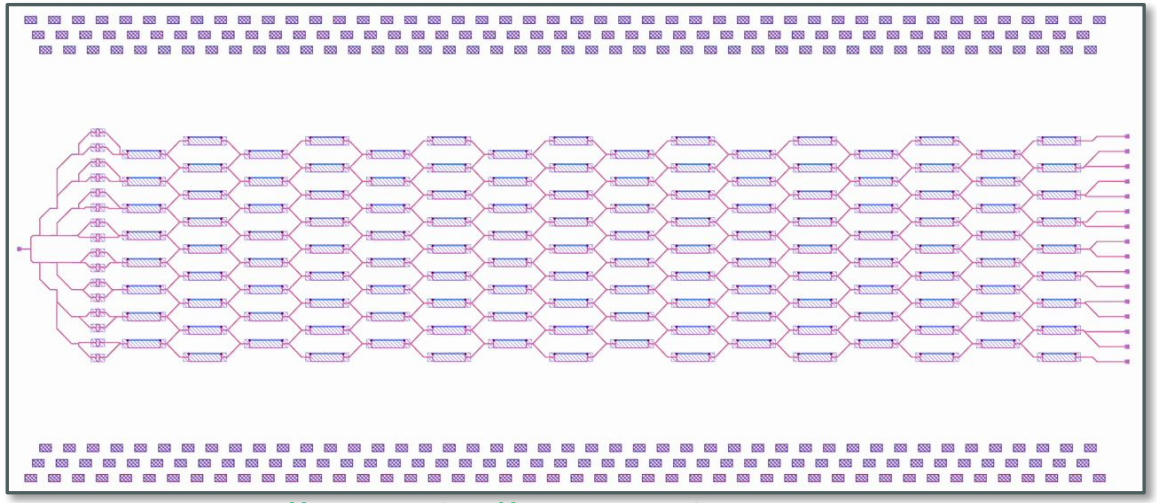


Via: 43, # layer: 3

Violation: 357, Time: 2494s

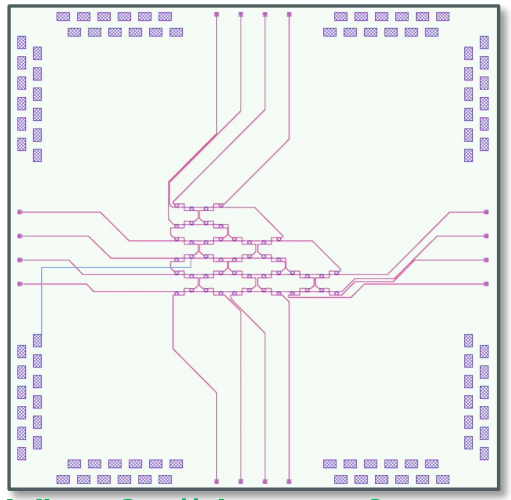
LiDAR 3.0

w/ routing guidance



Via: 0, # layer: 1

Violation: 4, Time: 207s



Via: 6, # layer: 3

Violation: 19, Time: 99s

Thank you!
Q & A?

LiDAR 3.0: Photonics-Aware Planning-Guided Automated Electrical Routing for Large-Scale Active Photonic Integrated Circuits

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Open-Source
PIC Router LiDAR

arXiv Preprint

PIC router for auto waveguide routing & metal routing

Seamless w/ GDSFactory 8

Arizona State University

ASU Center for Semiconductor Microelectronics (ACME)

SCOPE