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Multi-Level Interconnect Planning for Signal-Power-Thermal Integrity in 2.5D/3D Integration

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  - Influence of interconnects on SI/PI/TI
- Our MIP-SPT framework
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- Experimental Results

Background: Chiplets and Package Interconnects

- Chiplet: a small chip that contains a well-defined subset of functionality

- Vertical interconnects (VIC):
  - Micro-bumps (µbumps), C4 bumps and solder balls
  - Through-silicon vias (TSV), through-package vias (TPV) and vias in redistribution layer (RDL)

- Planar interconnects (PIC):
  - Wires in RDL on interposer
  - Planes in RDL on substrate

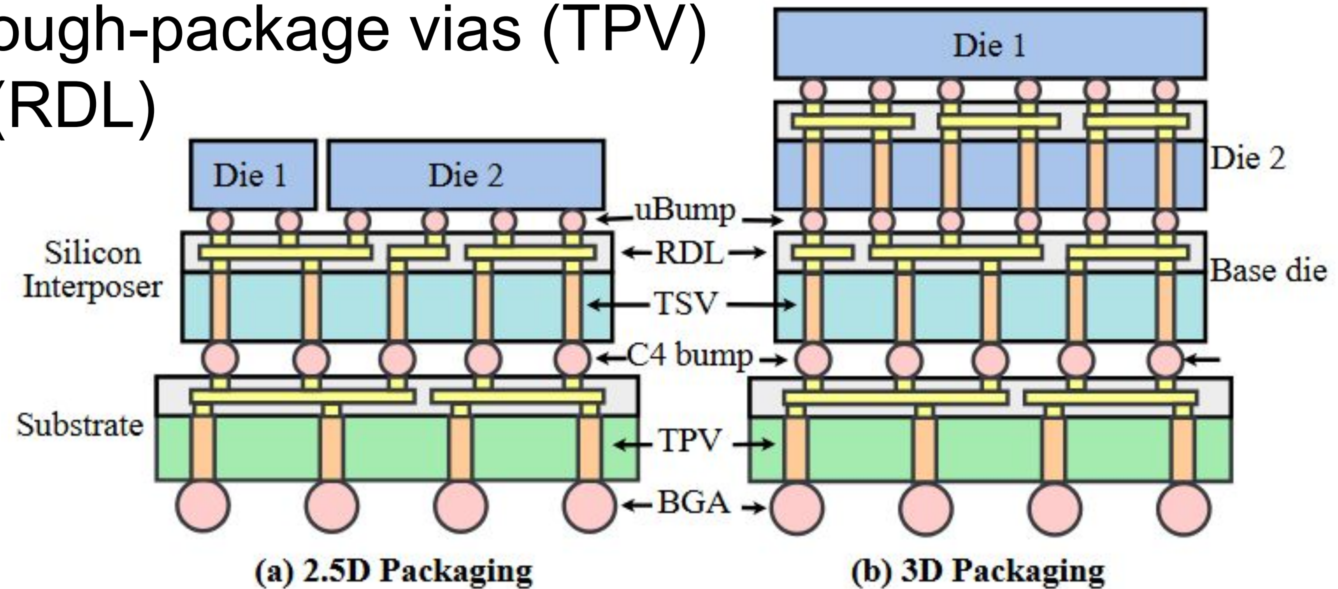

Figure 1: Structure of (a) 2.5D packaging (b) 3D packaging. Some VICs are aligned only for illustration; they can be unaligned when manufacturing.

Motivation: Interconnects Influence PI, SI and TI

- **Die to die SI:** Large number of parallel transmission lines -> add ground guarded tracks
- **DC PI:** Interconnects are considered as a resistive network -> determined by their density and geometric shape
- **TI:** Vertical interconnects form heat transfer channels and become hot spots

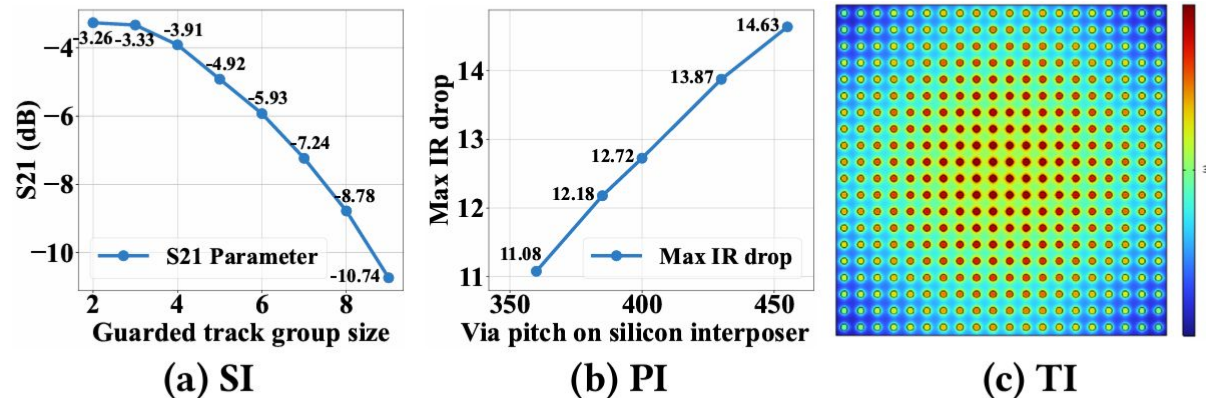

Figure 2: Examples of effects on (a) SI (b) PI and (c) TI

MIP-SPT: Challenges in interconnect planning

- The design space of interconnects in interposer and substrate is too large.
  - 15 dimensions in total, 25 billion combinations -> 25 billion physical simulations
  - Distinct design rules in interposer and substrate

- The multiphysics criterions (SI, PI, TI) and routability requirements are coupled.
  - Nonlinearities are introduced in the planning/optimization
  - Lack of quantitative SI/PI/TI analysis in previous works

MIP-SPT: Framework Overview

- We propose MIP-SPT, a multi-phase Bayesian optimization (MPBO) framework for multiphysics and route-driven interconnect planning

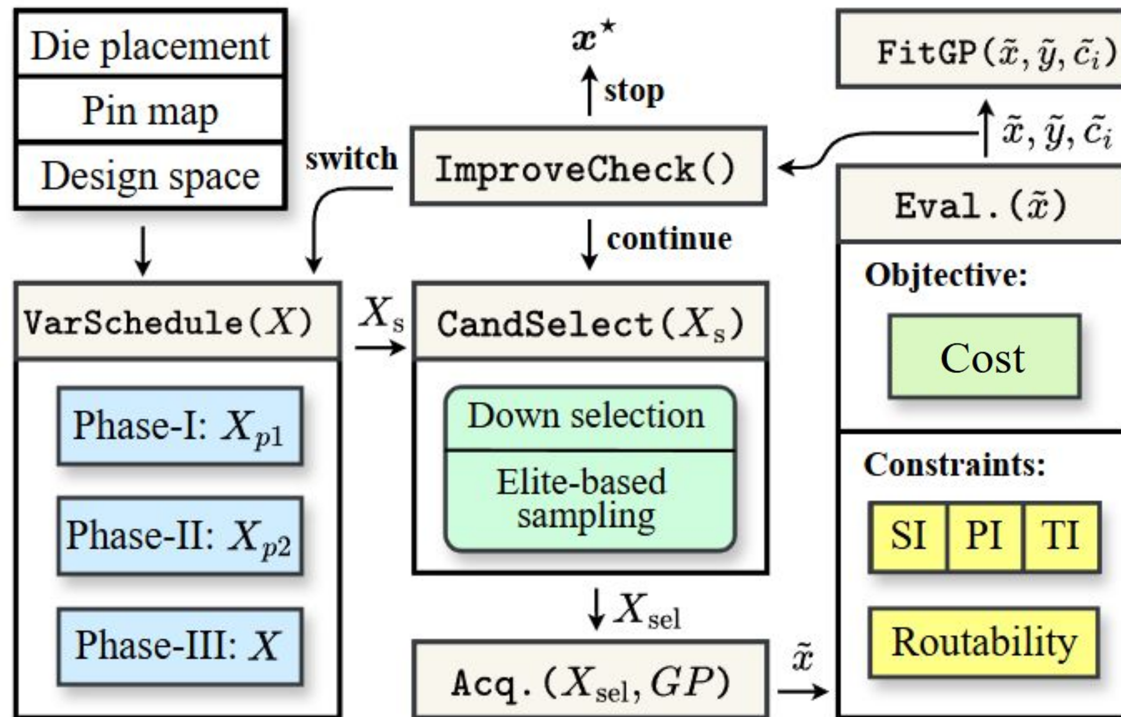

Figure 3. Overview of MIP-SPT framework. "Acq." denotes acquisition

MIP-SPT: Multi-phase Bayesian Optimization

- Objective and constraints

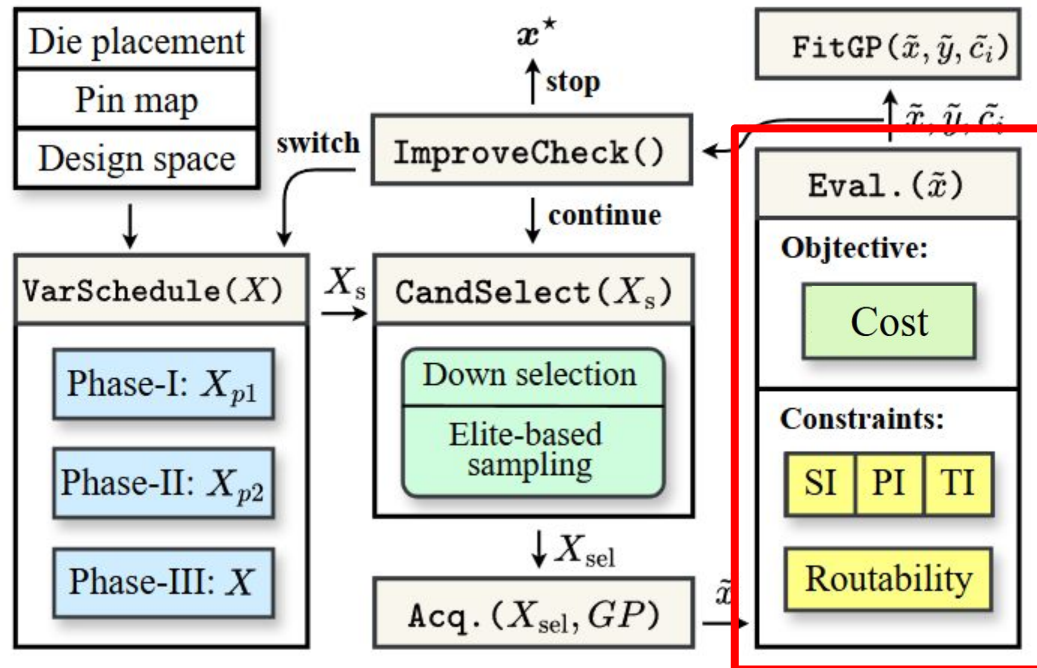

Figure 5. Overview of MIP-SPT framework

- Objective: interconnect cost
- Constraints
  - **SI:** Insertion loss of inter-die connection below threshold
  - **PI:** Maximum IR drop at die ports below threshold
  - **TI:** Maximum temperature below threshold
  - **Routability:** the chiplets are routable given the optimized design parameters

MIP-SPT: Framework Overview

- Hierarchical Variable Scheduling Strategy

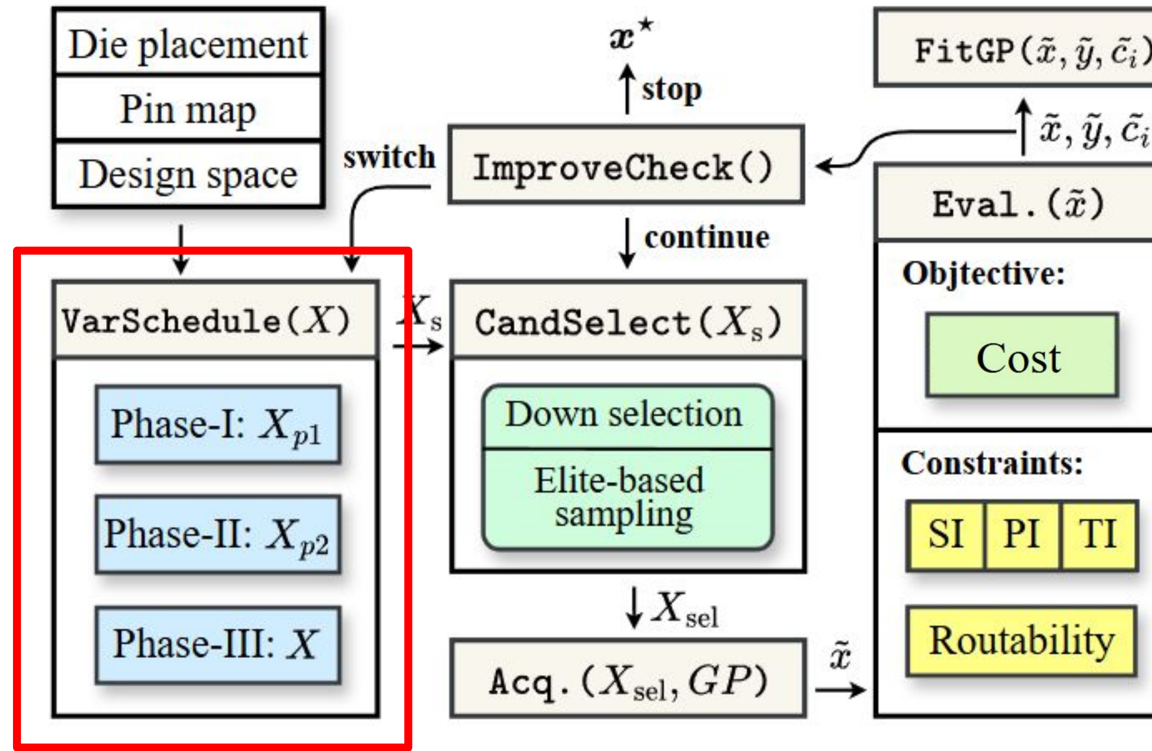

Figure 3. Overview of MIP-SPT framework

MIP-SPT: Hierarchical Variable Scheduling Strategy

- We decouple the design variables across the interposer/substrate based on their physical correlations -> optimize them in separate phases

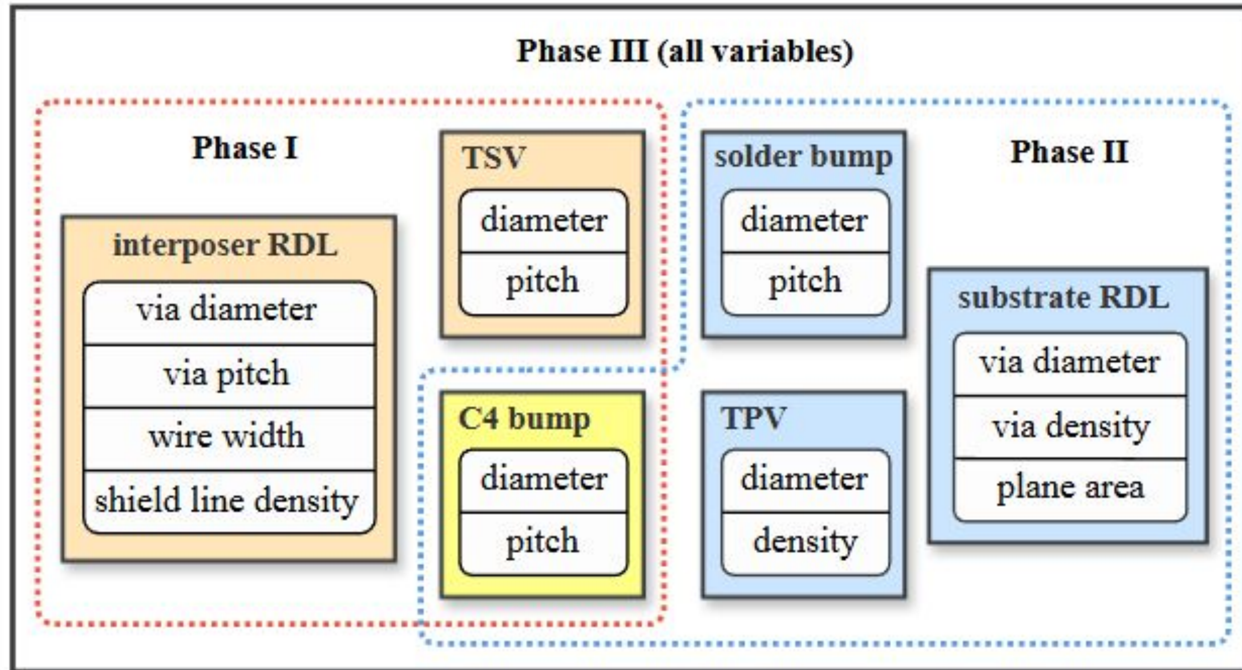

Figure 4: Variables scheduled in different phases

- Phase I: interposer and C4 bump
- Phase II: C4 bump and substrate
- Phase III: all variables, optimized based on the information from phase I and phase II

MIP-SPT: Hierarchical Variable Scheduling Strategy

- Physical logics behind the hierarchical scheduling
  - **SI**: die-to-die signal connections are routed on the interposer and are irrelevant to the substrate.
  - **PI**: the package PDN can be decomposed into to cascaded sub-networks. The total IR drop is roughly the summation of that in the interposer and substrate.
  - **TI**: similar to PI, the overall thermal resistance can be approximated as a series combination of the interposer and substrate components.

MIP-SPT: Multi-phase Bayesian Optimization

- Candidate selection

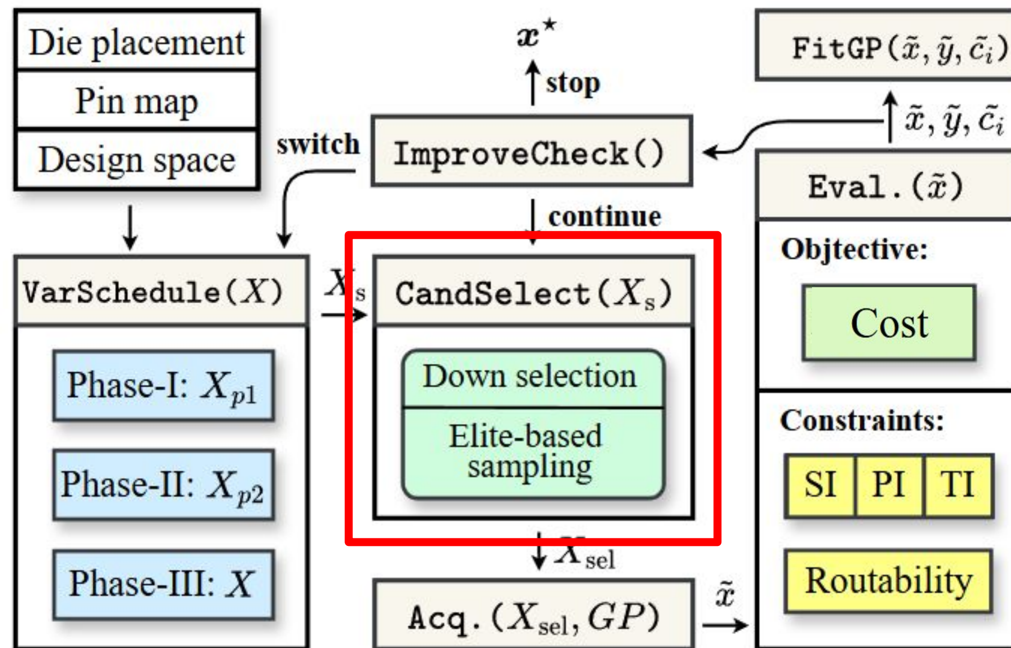

Figure 3. Overview of MIP-SPT framework

- Too many points in design space -> select most promising candidates for acquisition

- Techniques in different phases
  - Phase I and II: multi-score down selection
  - Phase III: down selection + elite-based sampling

MIP-SPT: MPBO - Multi-Score Down-Selection

- **Multi-score down-selection:**
  - Exploitation score: exploits the feasible regions for high objective value

$$S_E(x) = \mu_o(x)\, P_{\text{feas}}(x), \qquad P_{\text{feas}}(x) = \prod_{j=1}^{3} \Phi\left(\frac{-\mu_{c_j}(x)}{\sigma_{c_j}(x)}\right)$$

  - Exploration score: explores uncertain yet promising regions

$$S_A(x) = \mu_o(x) + \beta\, \sigma_o(x)$$

  - Boundary-learning score: selects points near the boundary of feasible region

$$S_{c_i}(x) = -\frac{|\mu_{c_i}(x)|}{\sigma_{c_i}(x)}, \quad i = 1, 2, 3$$

  - Random selection as fallback

$\mu_o(x), \sigma_o(x)$, $\mu_{c_i}(x), \sigma_{c_i}(x)$: objective and constraint posterior predictions

$\Phi(\cdot)$: cumulative distribution function (CDF) of the standard normal distribution

MIP-SPT: MPBO - Elite-based sampling

- Still too many points in Phase III (the entire design space)! Fortunately, we have historically good feasible points (elites) from Phase I and II, so we concentrate around the elites and sparsely sample the rest of the space.

- **Elite-based sampling**:
  - The distance to the elite set is:

$$D_{\mathbb{E}}(x) = \min_{e_i \in \mathbb{E}} \|x - e_i\|,$$

  - For each point, the probability of being selected is:

$$q(x) = (1 - \alpha) \frac{\exp(-D_{\mathbb{E}}(x)/\tau)}{\sum_{x_i \in \mathbb{X}} \exp(-D_{\mathbb{E}}(x_i)/\tau)} + \alpha/N,$$

near elites

uniform

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MIP-SPT: MPBO – Ablation Study of Candidate Selection

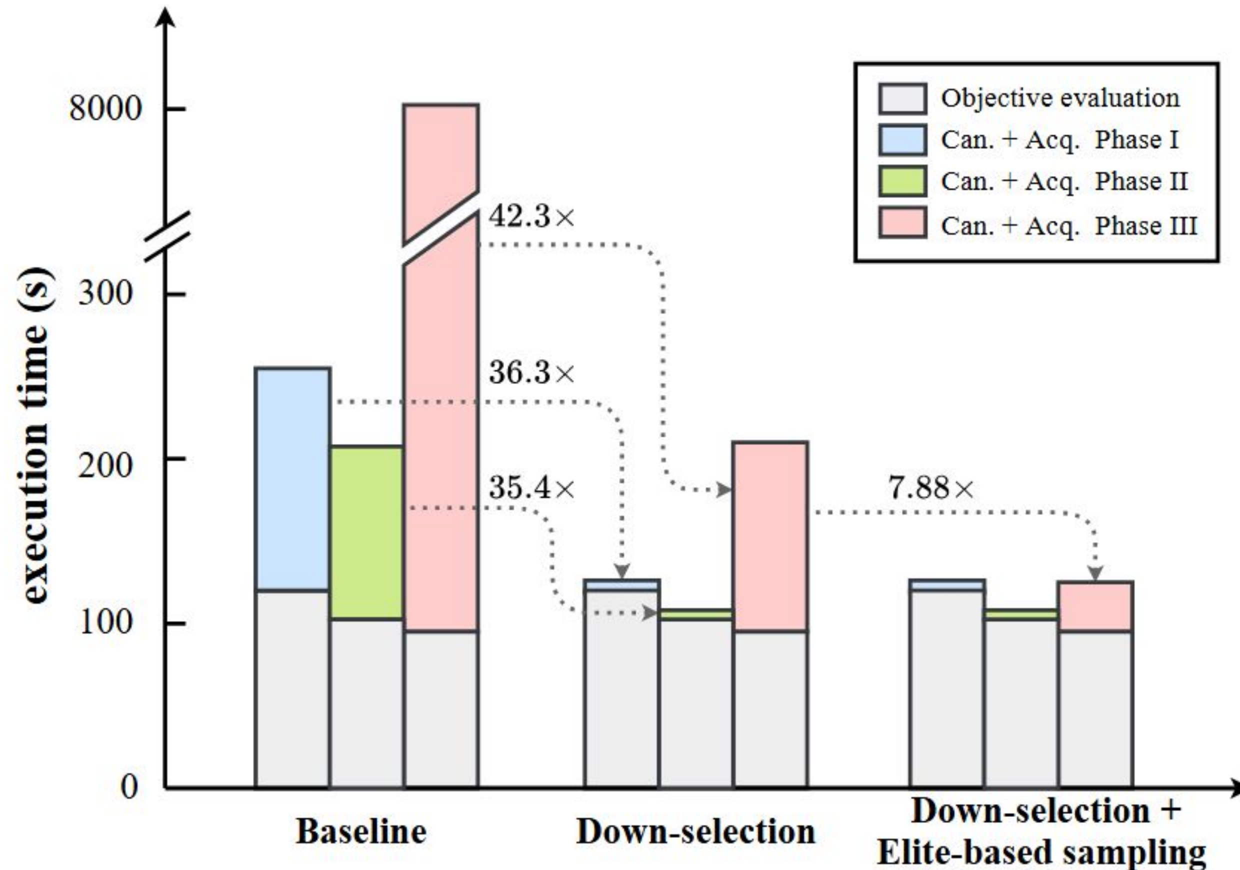

Figure 6: Ablation study of down-selection and elite-based sampling on execution time breakdown of MPBO phases. "Can." denotes candidate selection; "Acq." denotes acquisition.

- Multi-score down selection: 38x speedup on average in Phase I and II
- Elite-based sampling: additional 7.8x speedup in Phase III

MIP-SPT: Multi-phase Bayesian Optimization

- Acquisition function (abbreviated as Acq.)

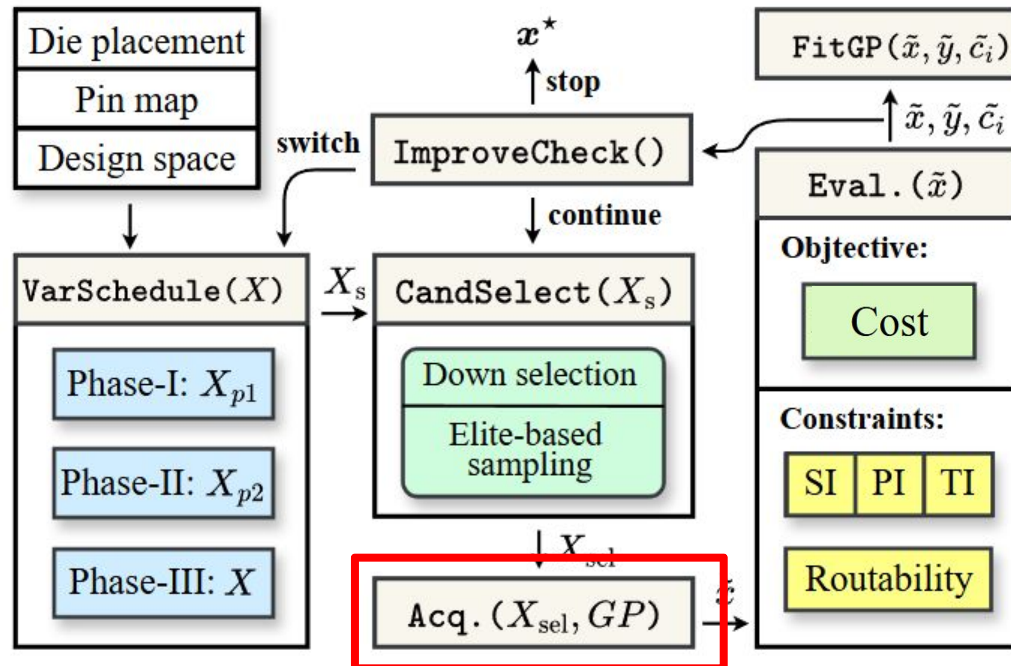

Figure 3. Overview of MIP-SPT framework

- At the beginning with few feasible points:
  - probability of feasibility *LogPoF*

$$\text{LogPoF}(x) = \log P_{\text{feas}}(x) = \sum_{j=1}^{3} \log \Phi(-\mu_{c_j}(x)/\sigma_{c_j}(x))$$

- Normal cases:
  - expected improvement *LogEI*

$$\text{logEI}(x) = \log\left[(\mu(x) - f^\star - \epsilon)\,\Phi(z(x)) + \sigma(x)\,\phi(z(x))\right]$$

$$z(x) = \frac{\mu(x) - f^\star - \epsilon}{\sigma(x)} \qquad f^\star = \max_{j=1,\dots,t} f(x_j)$$

$\Phi(\cdot)$: cumulative distribution function (CDF) of the standard normal distribution

$\phi(\cdot)$: probability density function (PDF) of the standard normal distribution

MIP-SPT: MPBO – Acquisition Function

- Tuning constraint stringency in acquisition function
  - Constraints are considered as a multiplicative weight in acquisition function:

$$W_p = \prod_{j=1}^{3} \Phi\left(\frac{-\mu_{c_j}(x)}{\eta \sigma_{c_j}(x)}\right)$$

    η controls the softness

  - η is determined by recent feasible rate r
    large r -> too conservative -> increase η -> softer constraints
    small r -> too adventurous -> decrease η -> harder constraints

MIP-SPT: MPBP - Phase Switching and Termination

- Phase Switching and Termination Criteria

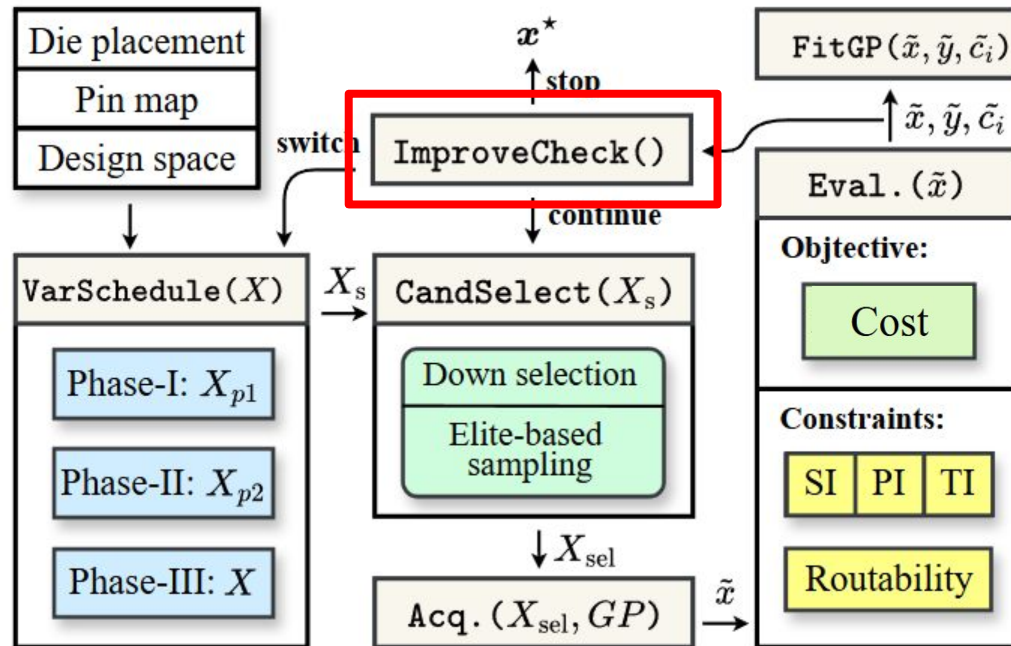

Figure 3. Overview of MIP-SPT framework

- Termination criteria for each phase:
  - Consecutive non-improvement trials > threshold

- Phase switching:
  - Phase I -> Phase II
  - Phase II -> Phase III
  - Phase III -> Stop

MIP-SPT: Experiment setup

- Experiment setup

Architecture:	MCore-OPU[4]
Packaging:	Two 2.5D cases + one 3D case
Fixed structural parameters:	Listed below
SI constraints:	Insertion loss < 10dB (S_{21} > -10dB)
PI constraints:	Maximum IR drop < 3%, 5%, 8%, 10%
TI constraints:	Maximum temperature < 343K, 348K

Table 1. Fixed structural parameters of 2.5D/3D cases

Cases	Die layer	μBumps		Interposer† RDL		TSVs	C4 bumps	Substrate RDL		TPVs	Solder Balls
	height	height	diameter	#layers	height	height	height	#layers	height	height	height
Case-1 (2.5D)	200μm	40μm	45μm	6 layers	120μm	200μm	100μm	4 layers	160μm	200μm	200μm
Case-2 (2.5D)	200μm	40μm	45μm	6 layers	120μm	200μm	100μm	4 layers	160μm	200μm	200μm
Case-3 (3D)	200+720μm‡	40μm	60μm	6 layers	120μm	200μm	120μm	4 layers	160μm	200μm	220μm

† Base-die in 3D integration shares the same parameters with interposer in 2.5D integration.
‡ 200μm for ASIC, 720μm for HBM.

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MIP-SPT: Experiment – Comparison with BO baseline

- Comparison between our MPBO and baseline single-phase BO (SPBO)

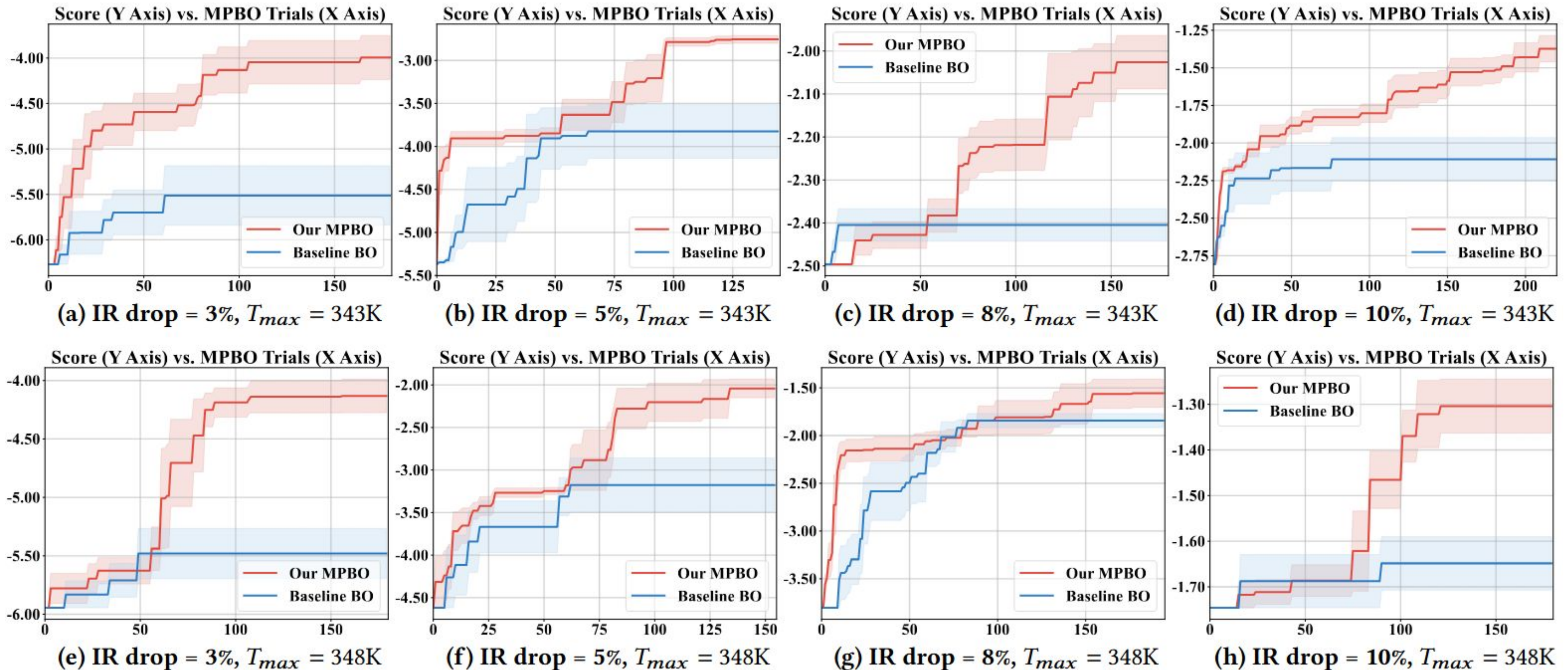

Figure 5. Comparison of Convergence between MIP-SPT and baseline BO on Case-1 (first row) and Case-3 (second row)

MIP-SPT: Experiment – Comparison with BO baseline

- Quantitative Comparison between our MPBO and baseline SPBO

Table 2. Mean and standard deviation of the best scores across eight experimental settings for MPBO and the baseline

Best score statistics		Case-1 IR3	Case-1 IR5	Case-1 IR8	Case-1 IR10	Avg.	Imp.
Mean	Ours	-4.7442	-2.7550	-2.1227	-2.0260	-2.9120	24.12%
	Baseline	-6.2621	-3.8249	-2.8581	-2.4047	-3.8375	-
Std. Dev.	Ours	0.2423	0.0450	0.0877	0.0620	0.1092	0.53×
	Baseline	0.3272	0.3130	0.1441	0.0376	0.2055	-
Best score statistics		**Case-3 IR3**	**Case-3 IR5**	**Case-3 IR8**	**Case-3 IR10**	**Avg.**	**Imp.**
Mean	Ours	-4.8816	-2.7909	-2.3065	-2.0539	-3.0082	20.57%
	Baseline	-6.2311	-3.9265	-2.5932	-2.3985	-3.7873	-
Std. Dev.	Ours	0.1435	0.1094	0.1478	0.0591	0.1149	0.69×
	Baseline	0.2151	0.3182	0.0742	0.0584	0.1665	-

†Imp. (%) for improvement: cost reduction and ratio of standard deviation

- We outperform the baseline on both final converged value and standard deviation

MIP-SPT: Experiment – Comparison with Previous Works

- We reproduce and compare with the previous works[6][7].
- On average, we reduce the manufacturing cost by 23.1% and 18.1% percent, respectively
- The advantage comes from the effective exploration of the design space and careful treatment of physical constraints.

Table 3. Comparison of our interconnect planning against previous works

Case	#RDL vias			#TSVs			Cost Reduction	
	[15]	[9]	Ours	[15]	[9]	Ours	v.s.[15]	v.s.[9]
Case1-2.5D	6423	5945	5430	280	264	190	-25.6%	-17.8%
Case2-2.5D	9887	9694	8338	432	420	293	-23.6%	-22.5%
Case3-3D	6619	6209	5585	549	528	440	-20.1%	-14.1%
Average	-	-	-	-	-	-	-23.1%	-18.1%

Conclusions

- We proposed a hierarchical variable scheduling strategy that decoupled interposer and substrate design variables and optimized them in separate phases

- To improve the convergence and efficiency of our MPBO, we employed score-based down-selection and elite-based sampling.

- Under the same SI/PI/TI constraints, our MPBO achieves a manufacturing cost of 22.4% lower than the baseline SPBO. Compared to two previous works, MIP-SPTreduces interconnect cost by 23.1% and 18.1%, respectively.

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Thank You