Toward Sustainable and Transparent Benchmarking for Academic Physical Design Research

Heterogeneous Integration, VLSI physical design, Benchmarking

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Outline

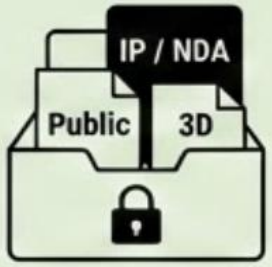
1 Introduction

2D and 3D Physical Design Research

2D & 3D Physical Design Research

Poor Reproducibility

2D & 3D Physical Design Research



Too Few Shareable Testcases

- Industrial testcases hard to share (IP / NDA)
- Public testcases limited in scale & diversity

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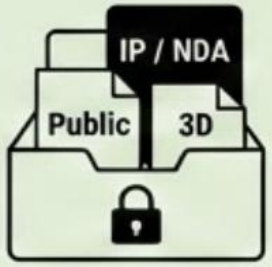
2D & 3D Physical Design Research



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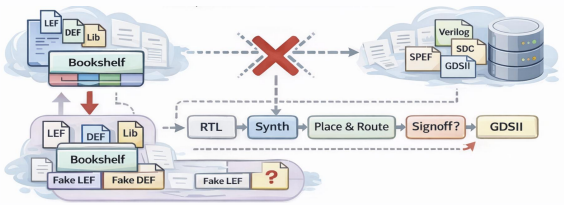
Format & Interface Fragmentation

- Academic testcases not standardized
- Interfaces across tools (bookshelf, fake lef, def)



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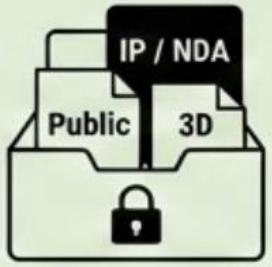

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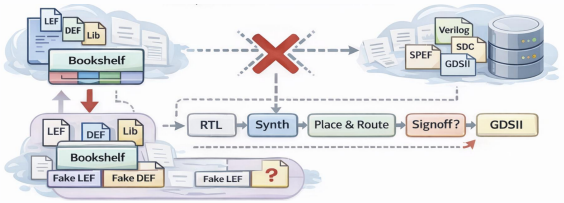
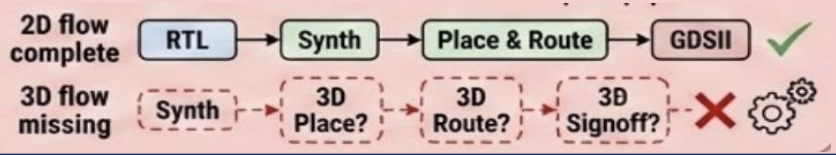
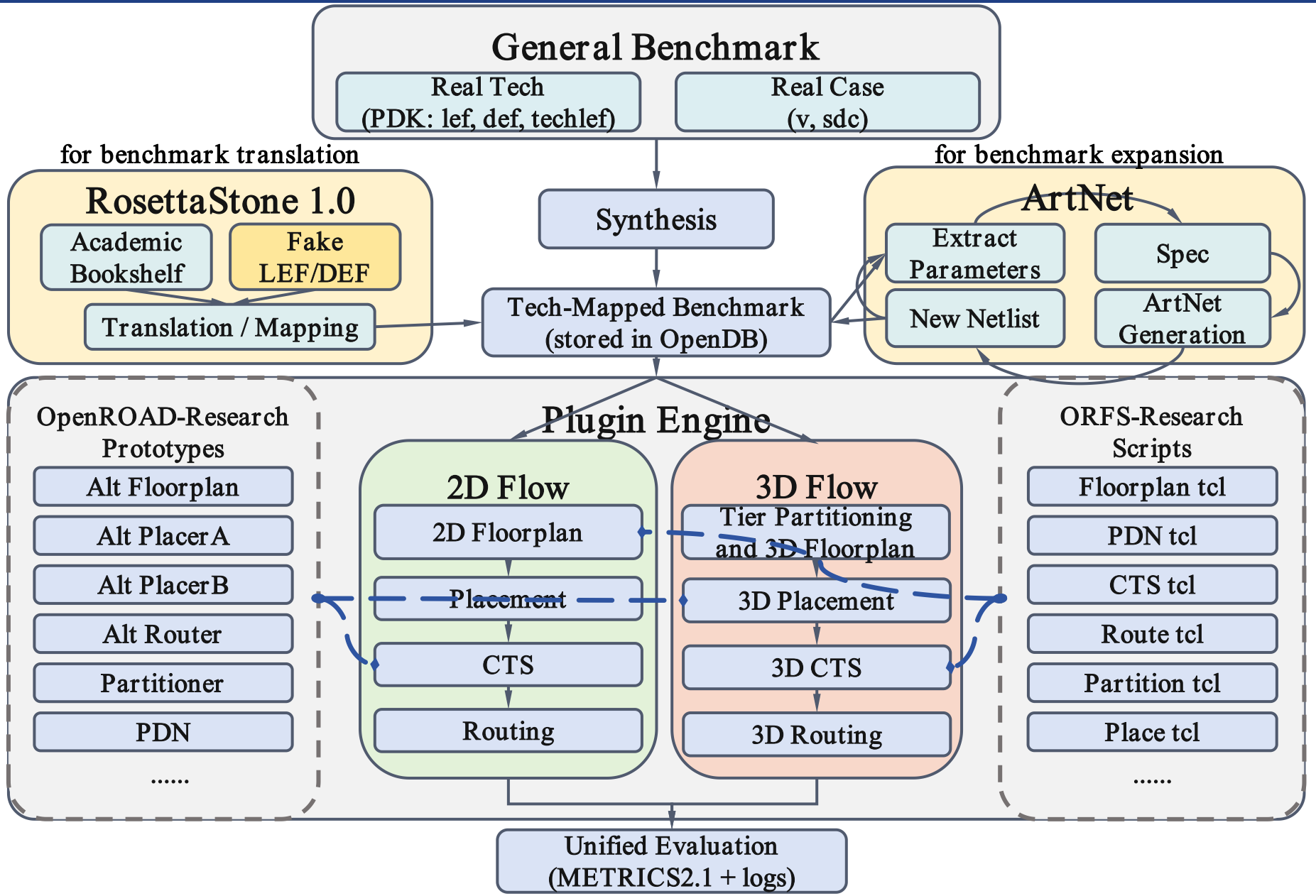


Flow Incompleteness & Evaluation

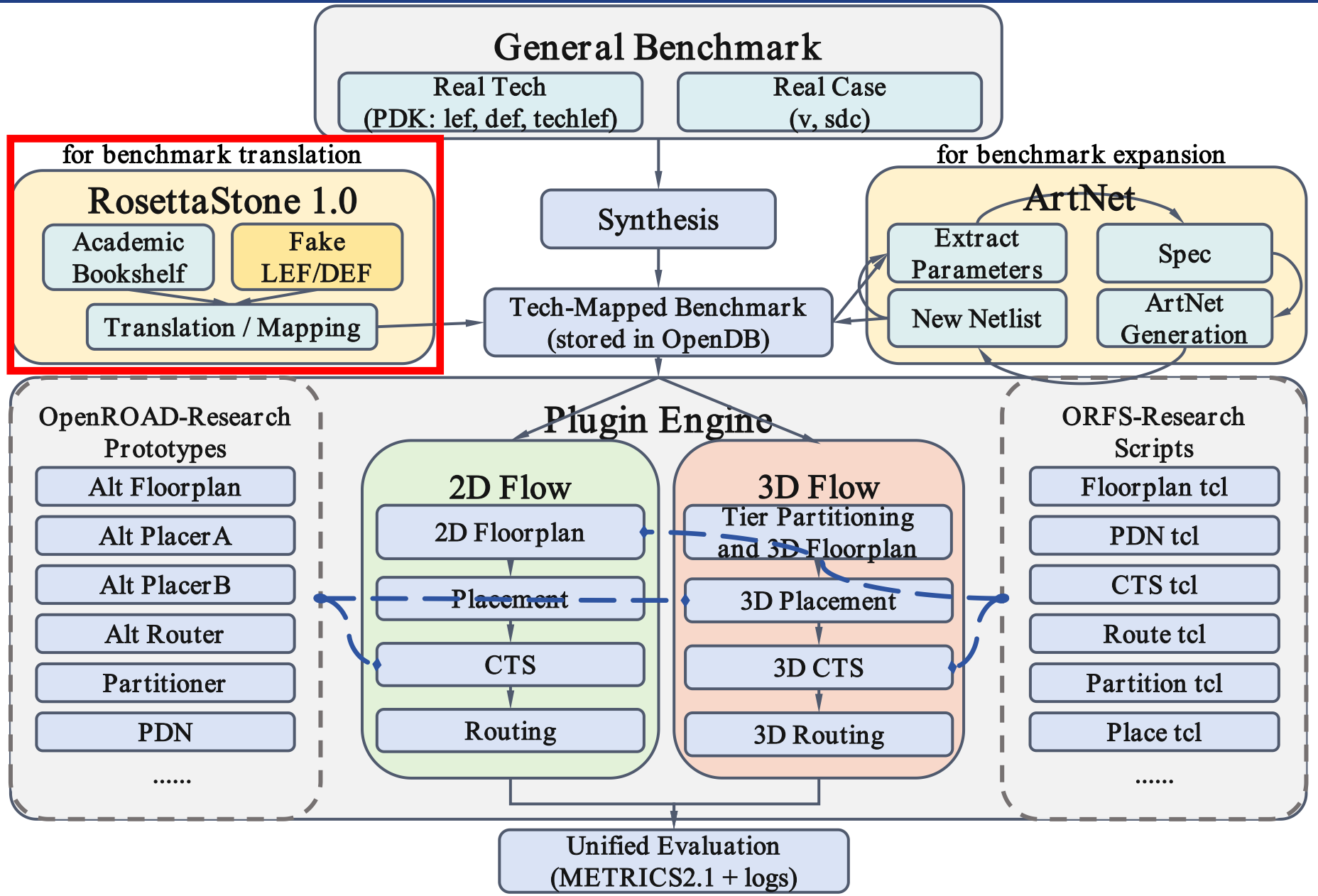
- Benchmark Inputs Incomplete (LEF/Lib/RC)
- End-to-end RTL-to-GDS flows often incomplete
- Metrics and reporting differ



RosettaStone 2.0:



RosettaStone 2.0: backplane



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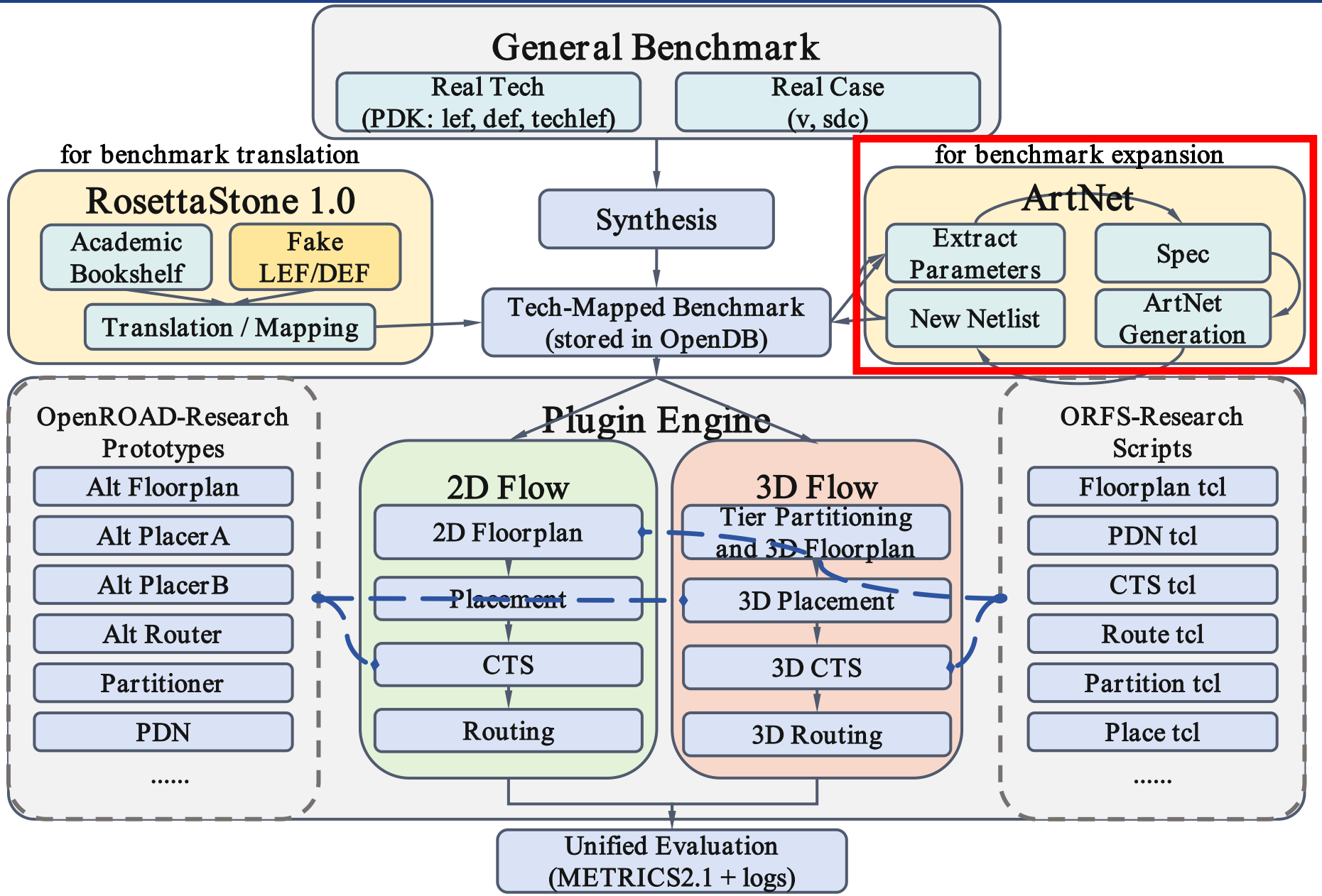

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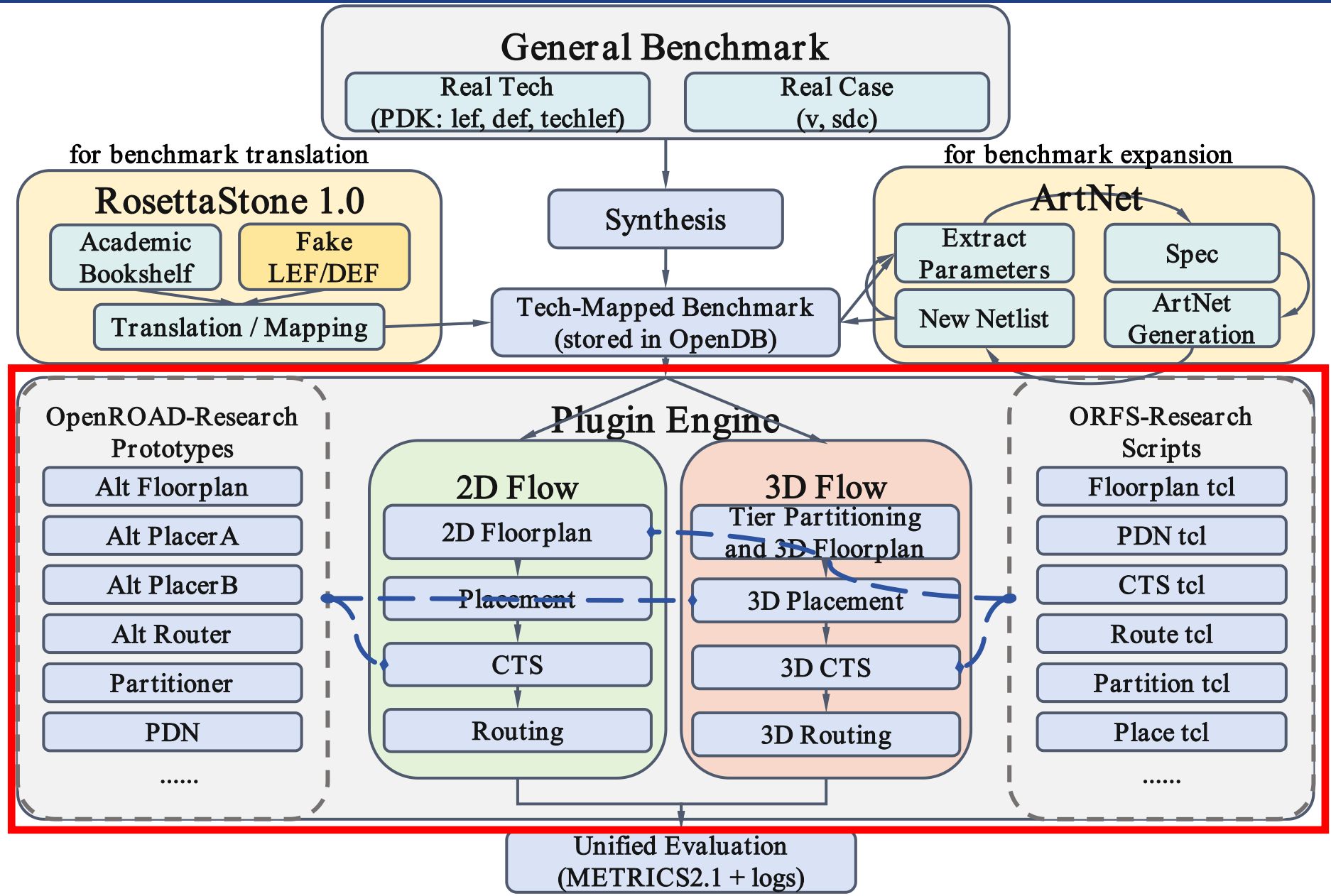
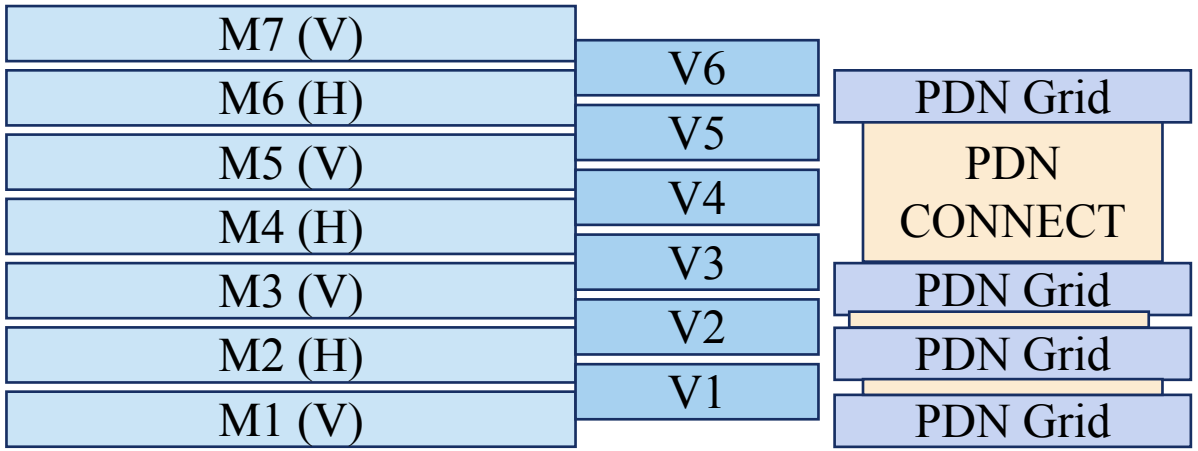


2 Pin-3D Enablement and Flow

Use 2D tools to implement 3D VLSI designs

Pin-3D Enablement (1/2): 2D Abstraction for F2F Stacks

Homogeneous Integration: ASAP7 3D



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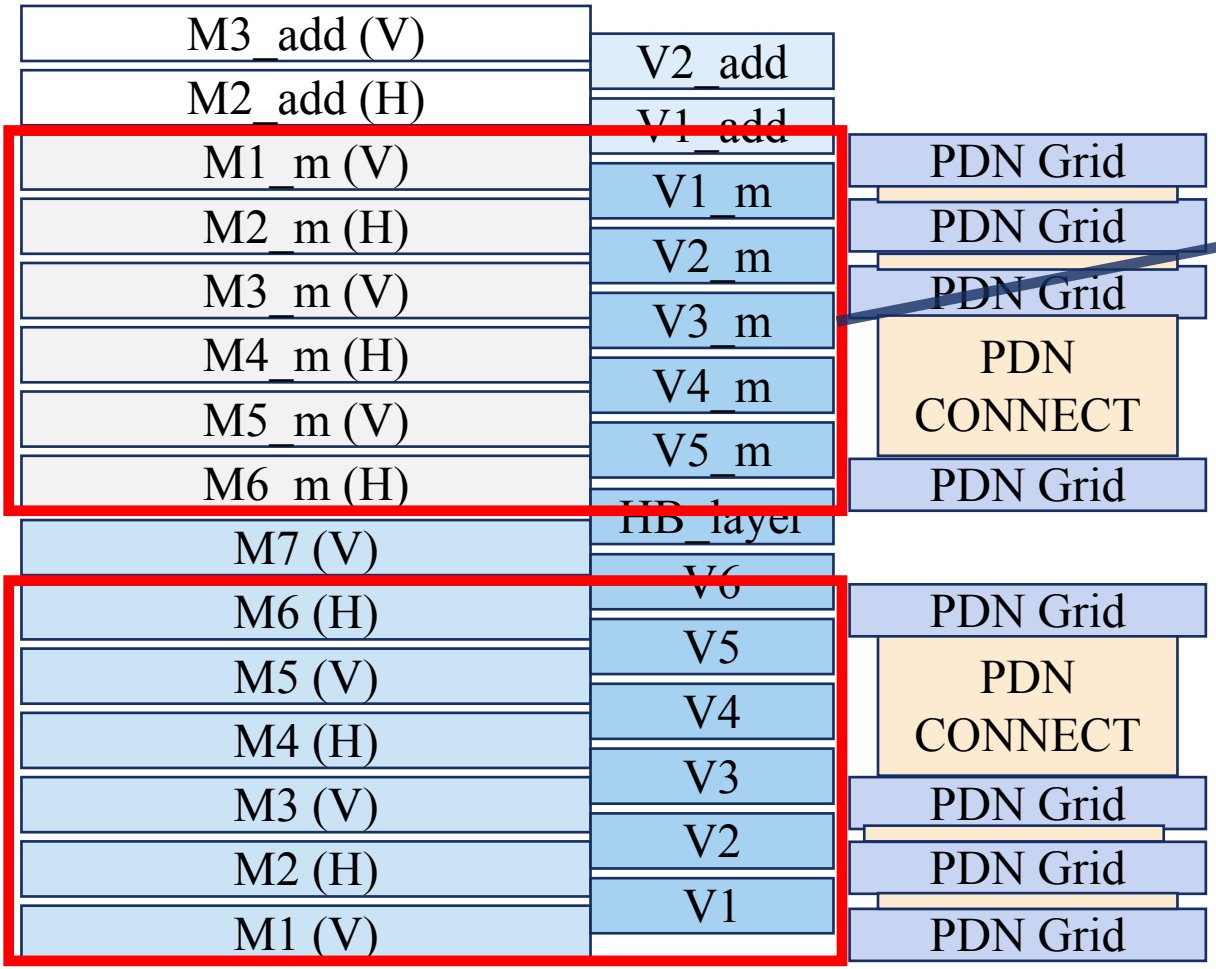

Mirror the 2D metal stack with _m layers and _m vias to form a unified stack

Pin-3D Enablement (1/2): 2D Abstraction for F2F Stacks

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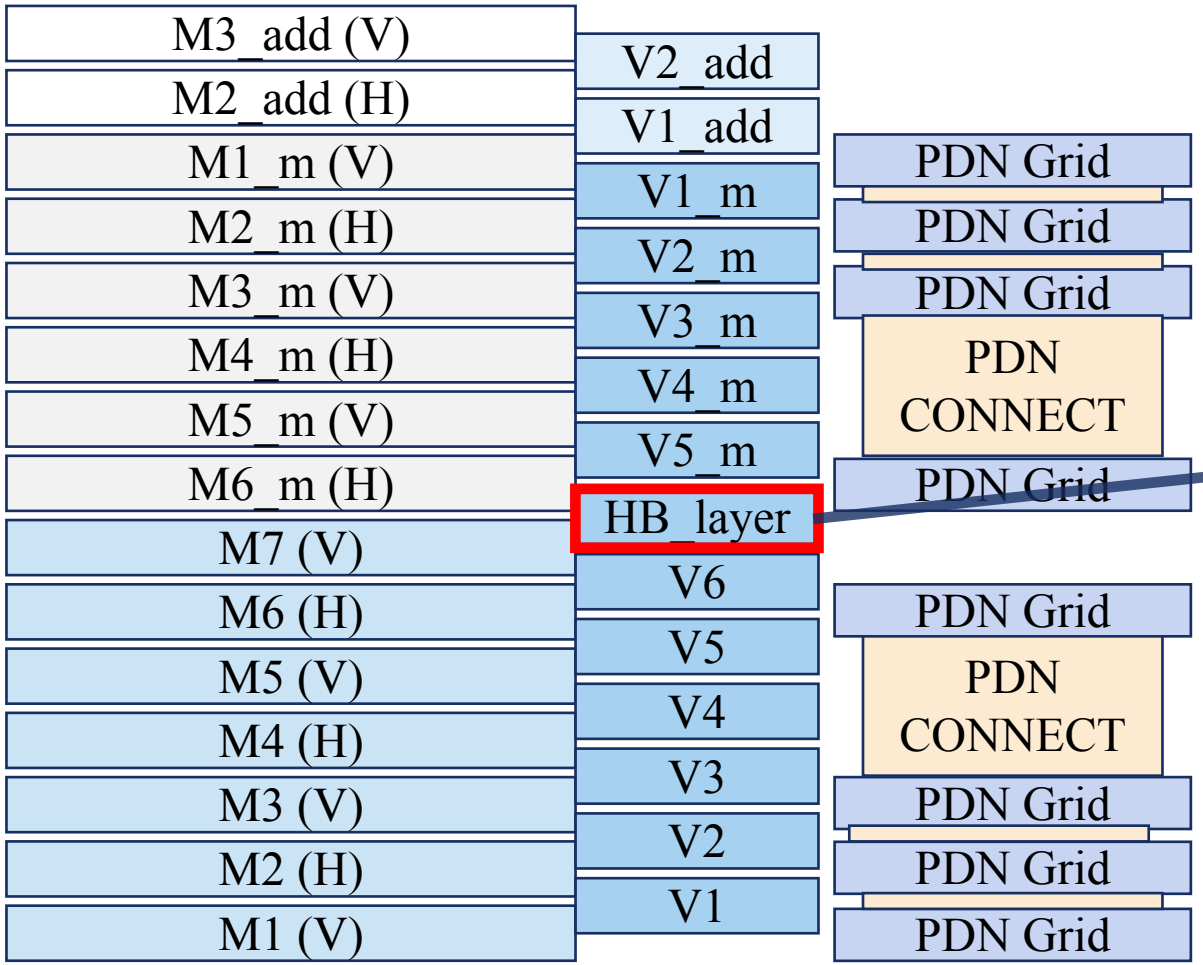
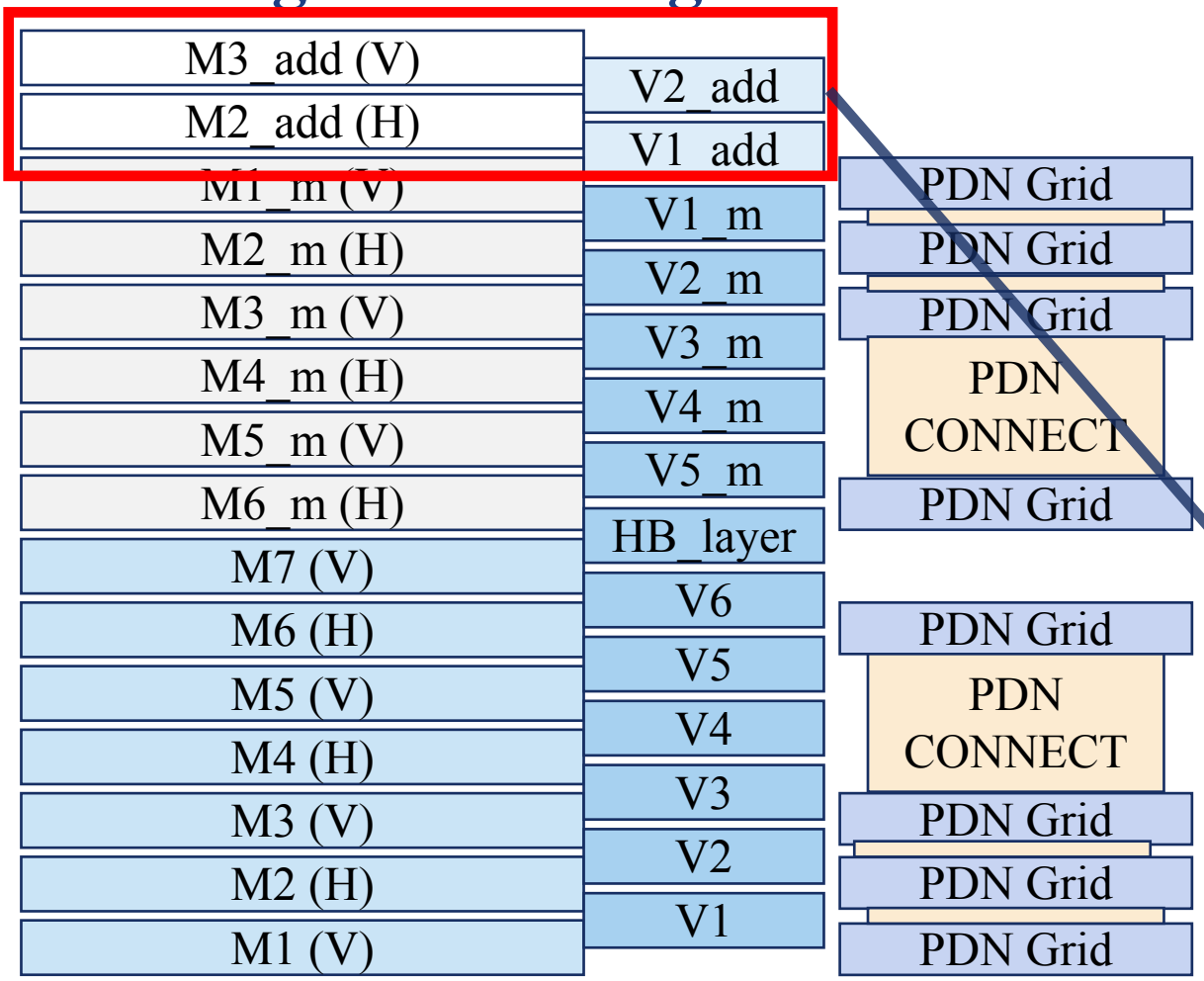


Model Hybrid Bonding Terminals (HBTs) as vertical vias on the HB layer

Pin-3D Enablement (1/2): 2D Abstraction for F2F Stacks

Homogeneous Integration: ASAP7 3D



MAX_ROUTING_LAYER M2_m/M3_add
MIN_ROUTING_LAYER M2

For OpenROAD Tool specific pin access logic, we cannot set layer below M1_m for routing

Pin-3D Enablement (1/2): 2D Abstraction for F2F Stacks

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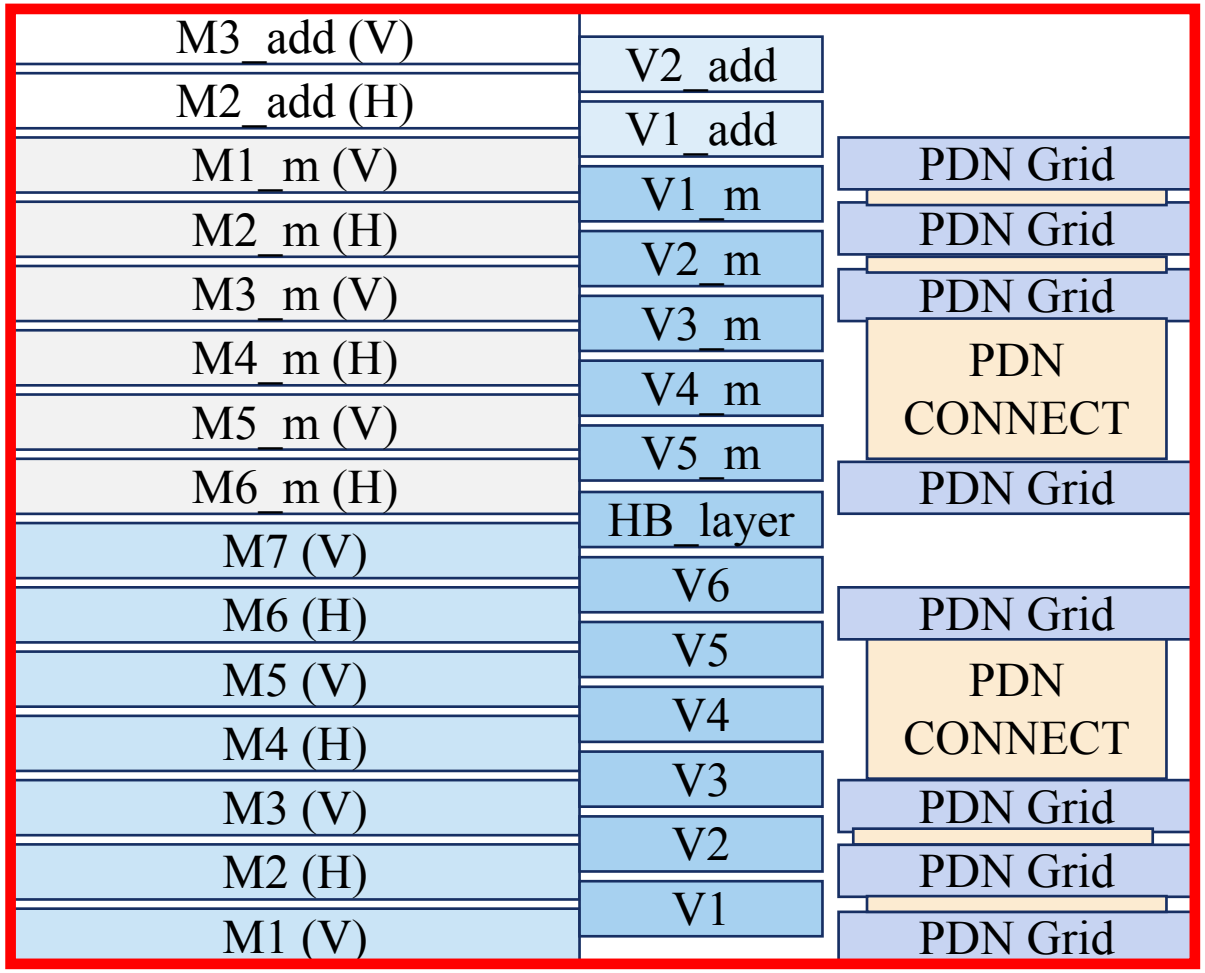
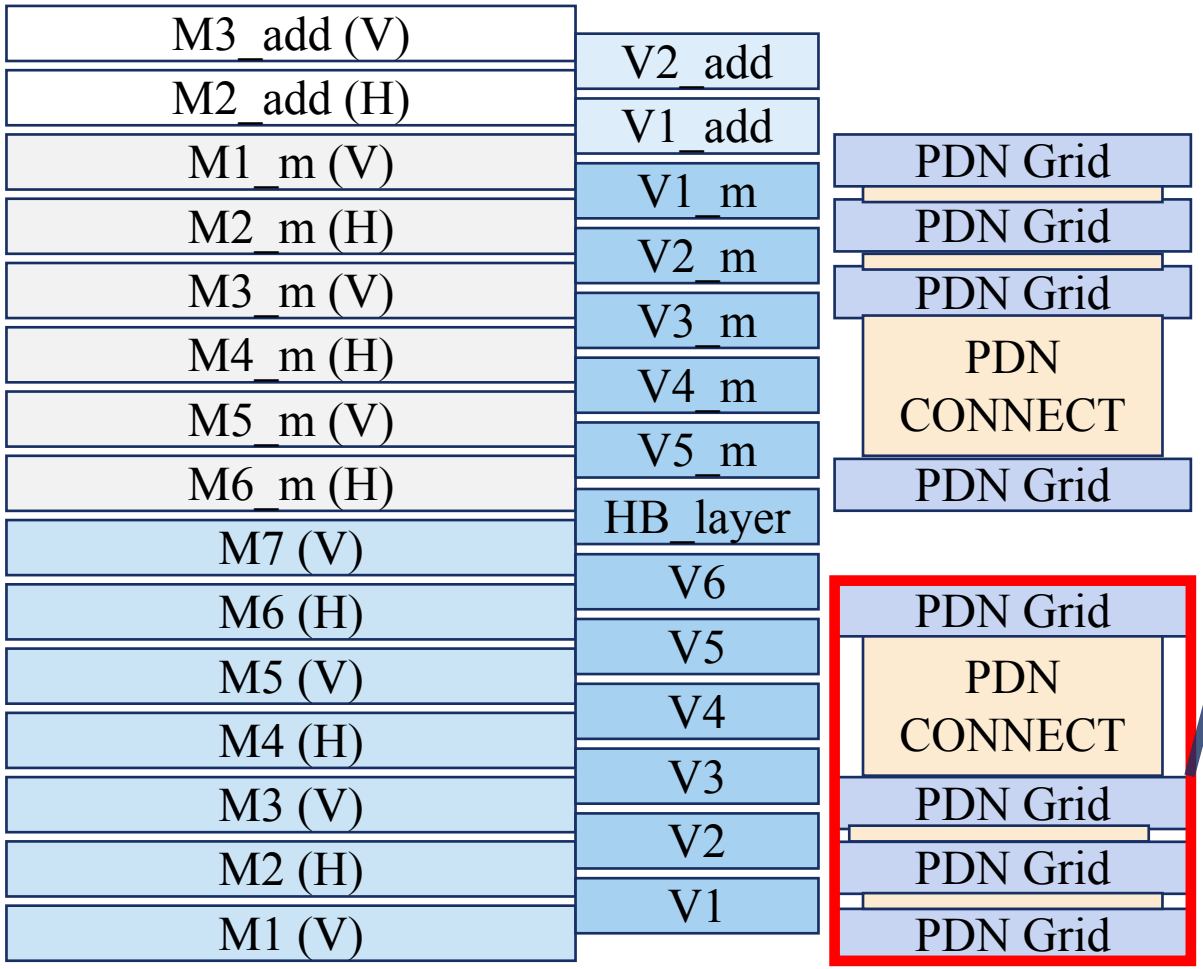


Make 3D designs appear as one unified 13-layer routing environment to unmodified 2D engines

Pin-3D Enablement (2/2): How to optimize one tier?

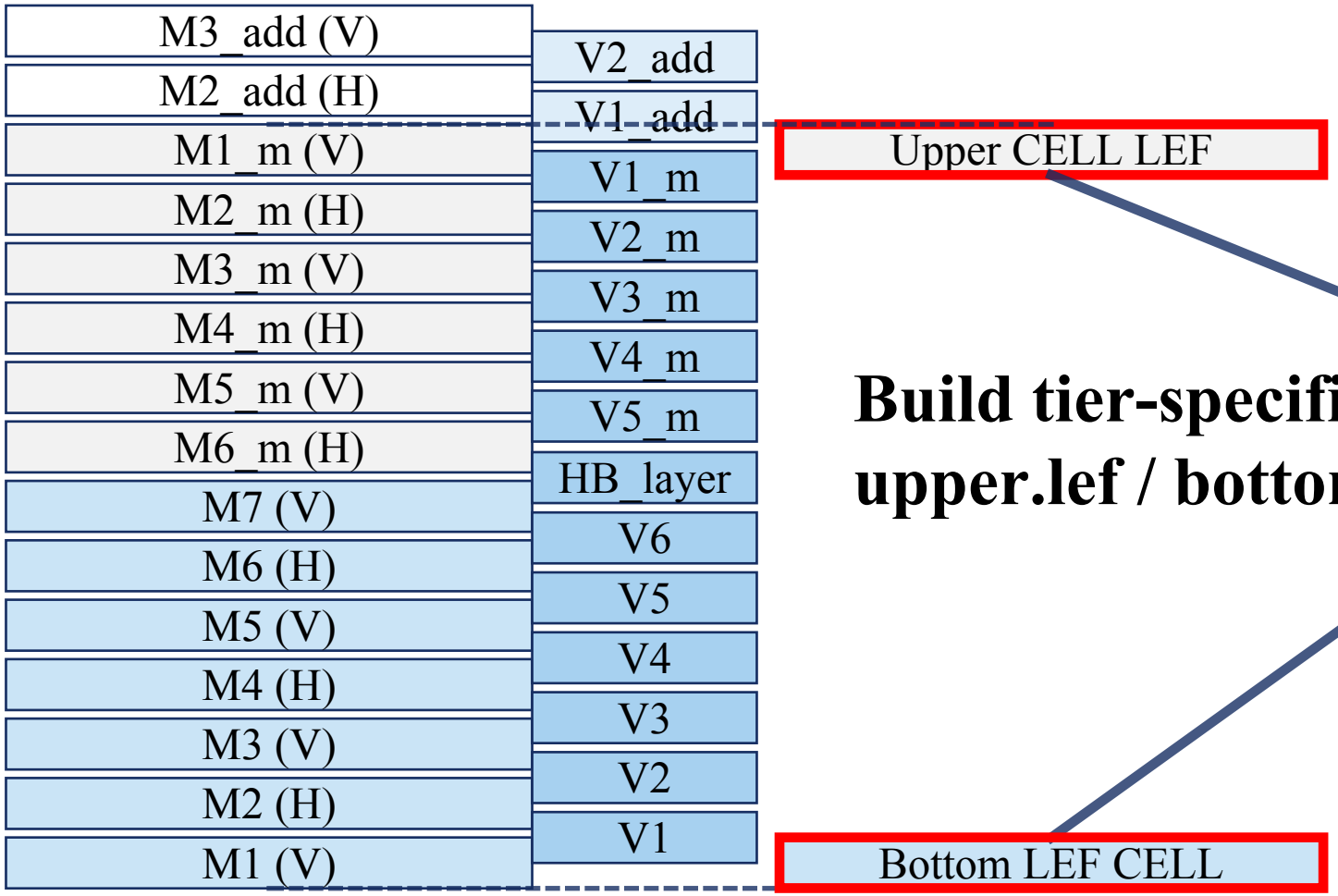
Homogeneous Integration: ASAP7 3D

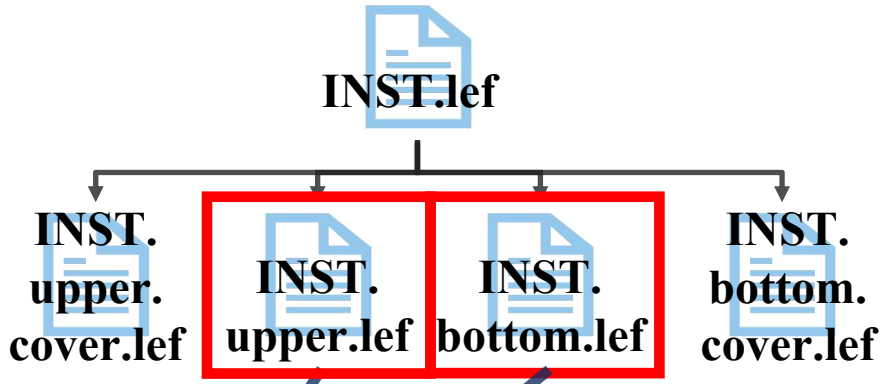


Use tier-specific PDN grids (BOT_VDD/VSS vs. TOP_VDD/VSS) to keep supplies isolated

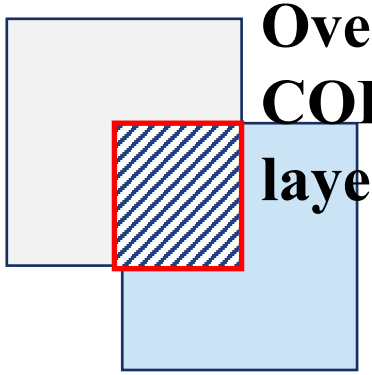
Pin-3D Enablement (2/2): How to optimize one tier?

Homogeneous Integration: ASAP7 3D





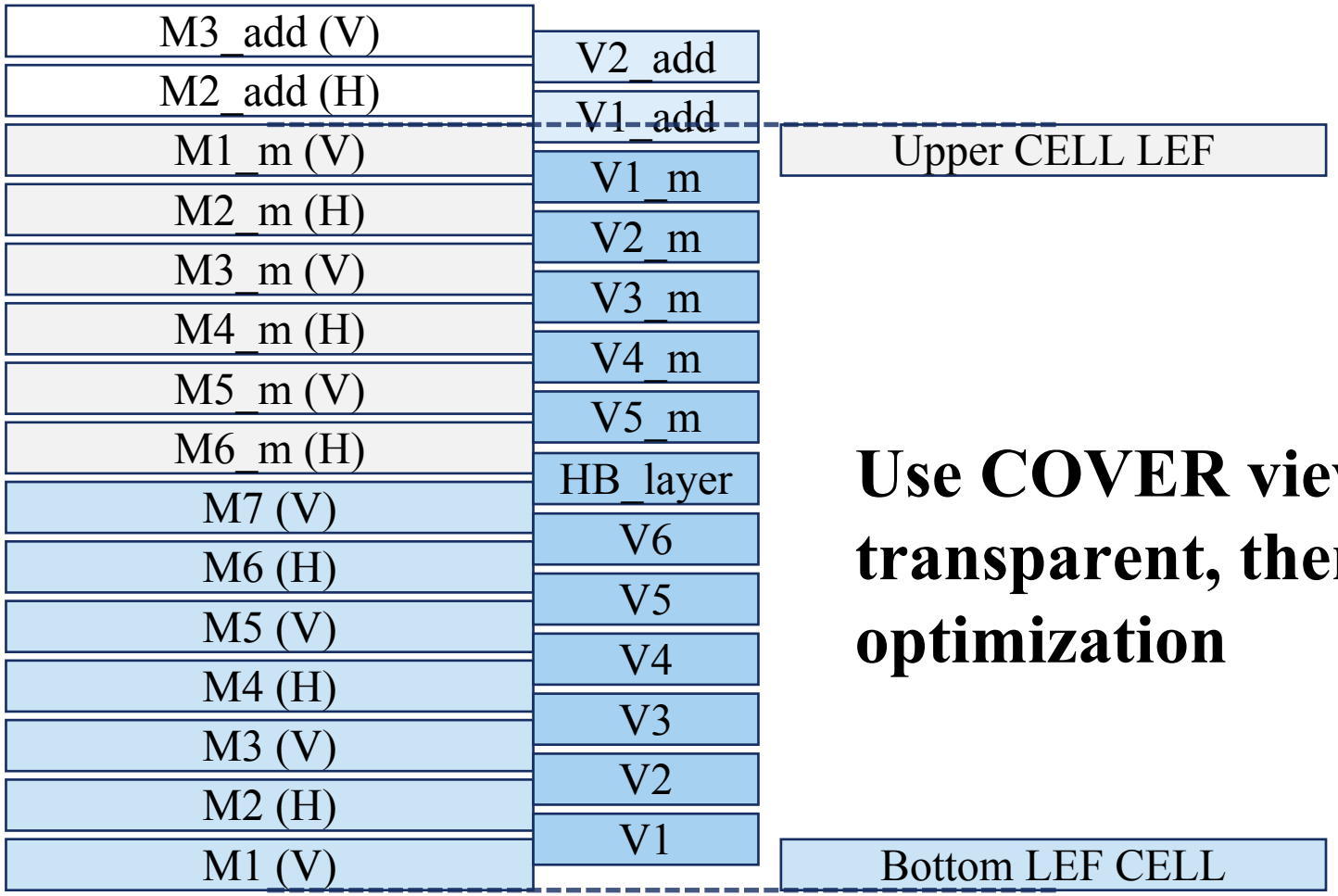
Build tier-specific physical masters: upper.lef / bottom.lef (CORE Views)

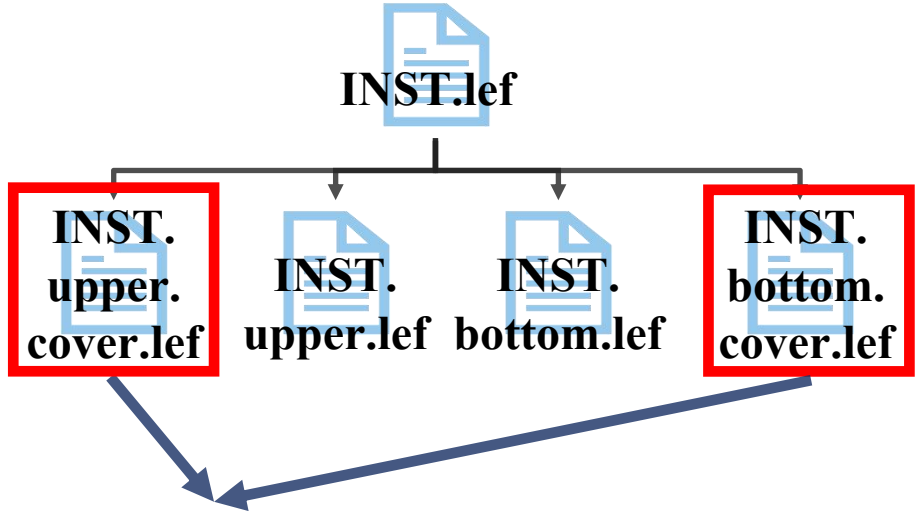


However:
Overlaps Detected between CORE cells on different layers using 2D Tools

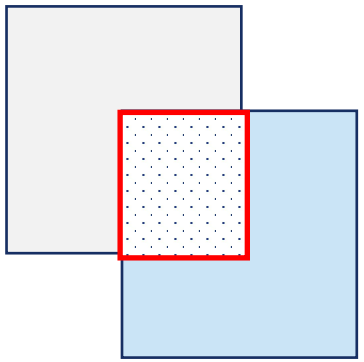
Pin-3D Enablement (2/2): How to optimize one tier?

Homogeneous Integration: ASAP7 3D





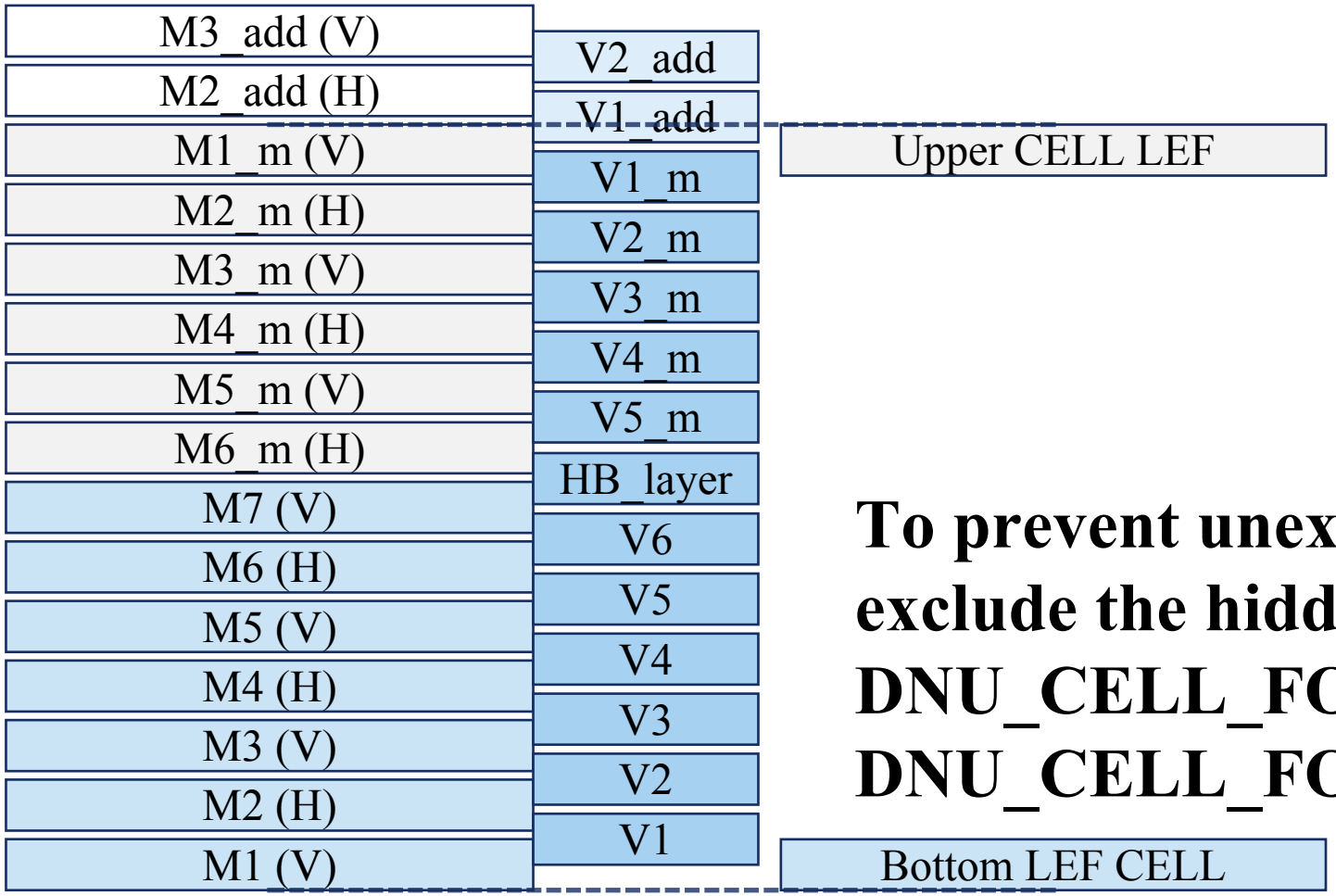
Use COVER views to make the opposite tier transparent, then FIX the hidden tier during optimization

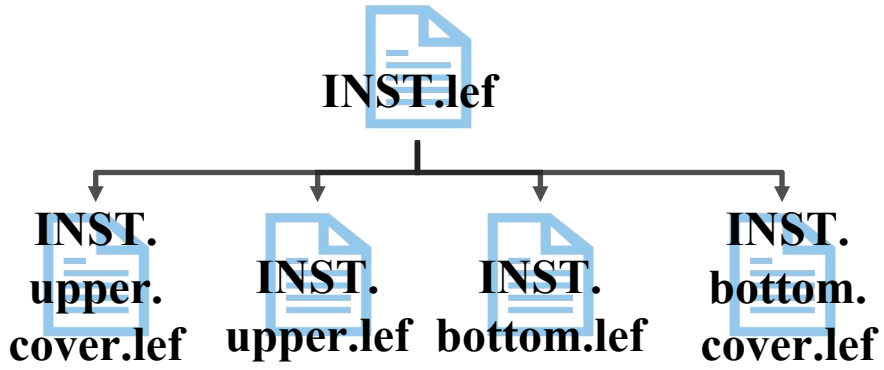


Overlaps will be ignored between COVER cells and CORE cells using 2D Tools

Pin-3D Enablement (2/2): How to optimize one tier?

Homogeneous Integration: ASAP7 3D





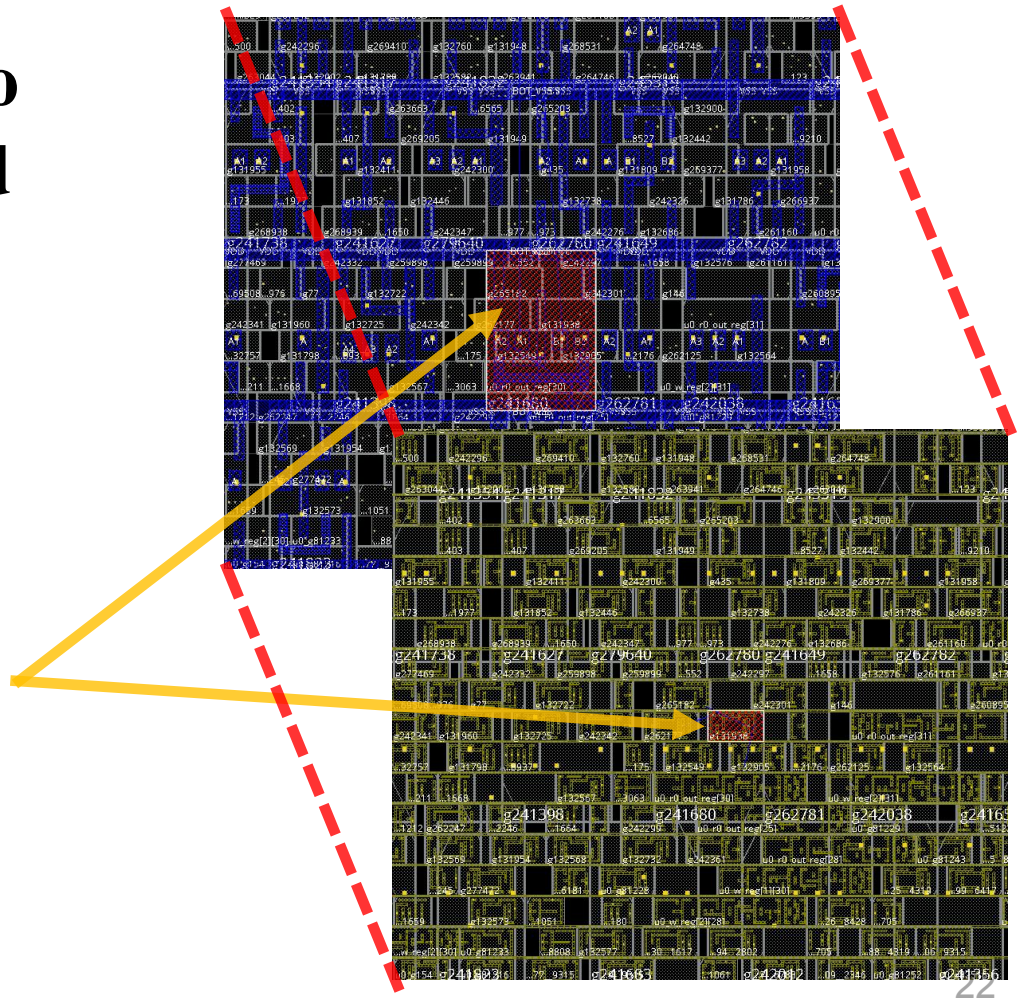
To prevent unexpected cell insertion, exclude the hidden tier using DNU_CELL_FOR_UPPER / DNU_CELL_FOR_BOTTOM

Heterogeneous Enablement (1/2): Tier Map

Tier Map for Cross-Die Cell Movement

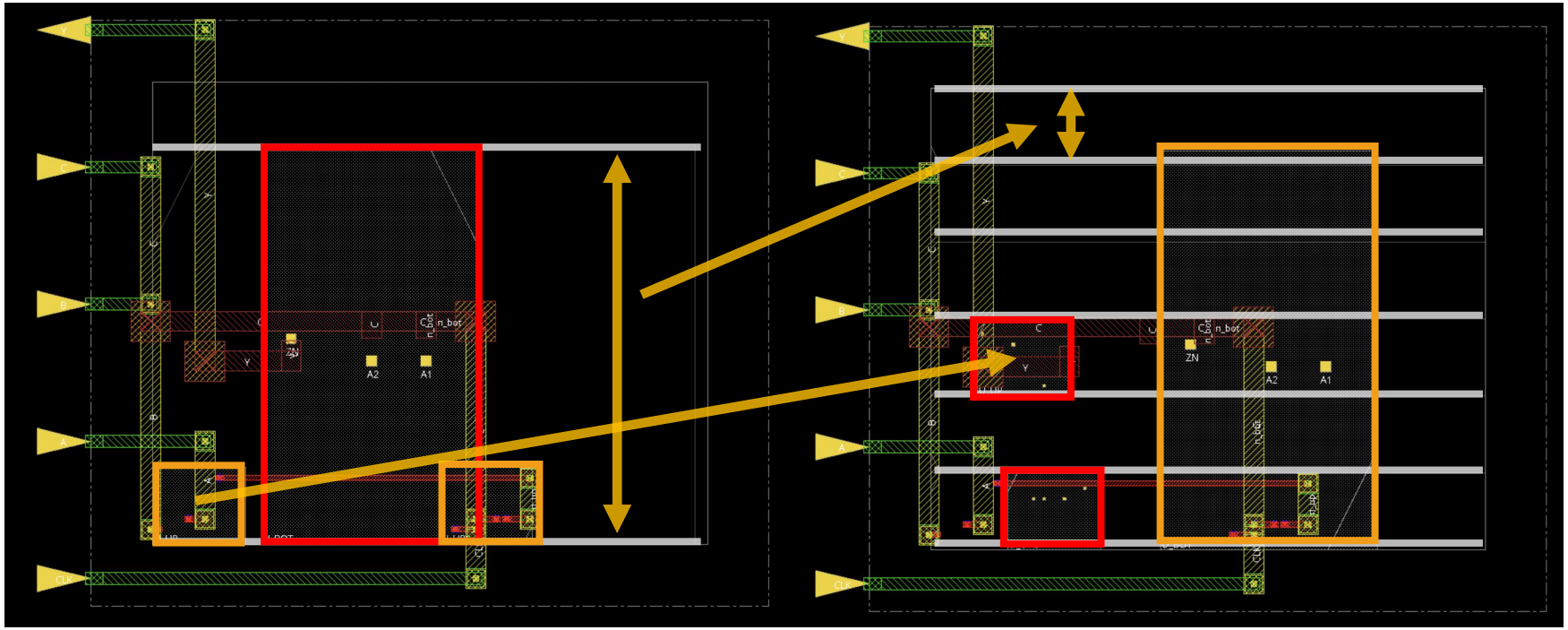
For heterogeneous integration, we need a one-to-one cell mapping across libraries so that cells can move across tiers legally and consistently.

- **Site legality**: row, PDN, orientation, etc.
- **Physical/Logical**: physical pin, area map, logical function map, etc.



Heterogeneous Enablement (2/2): Tier legalization

For tier legalization: Reconstruct rows

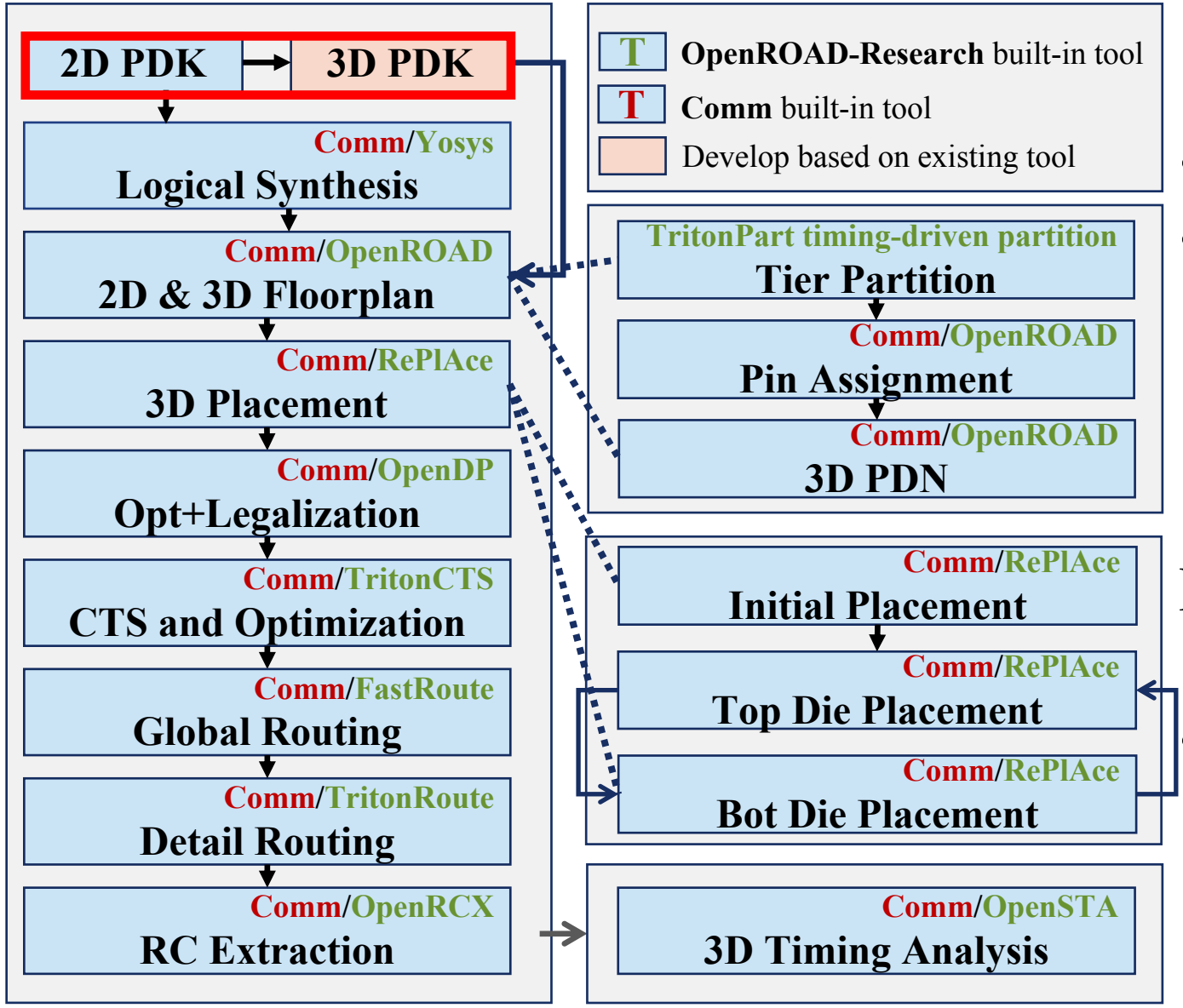


Site Bottom && Place Design

Site Upper && Place Design

- Heterogeneous cells have different **height** and different **site definitions / row constraints**.
- We **reconstruct rows** when activating a tier to ensure standard 2D placers can run legalization across mixed PDKs.

Pin-3D Flow: Step-by-Step Execution Flow



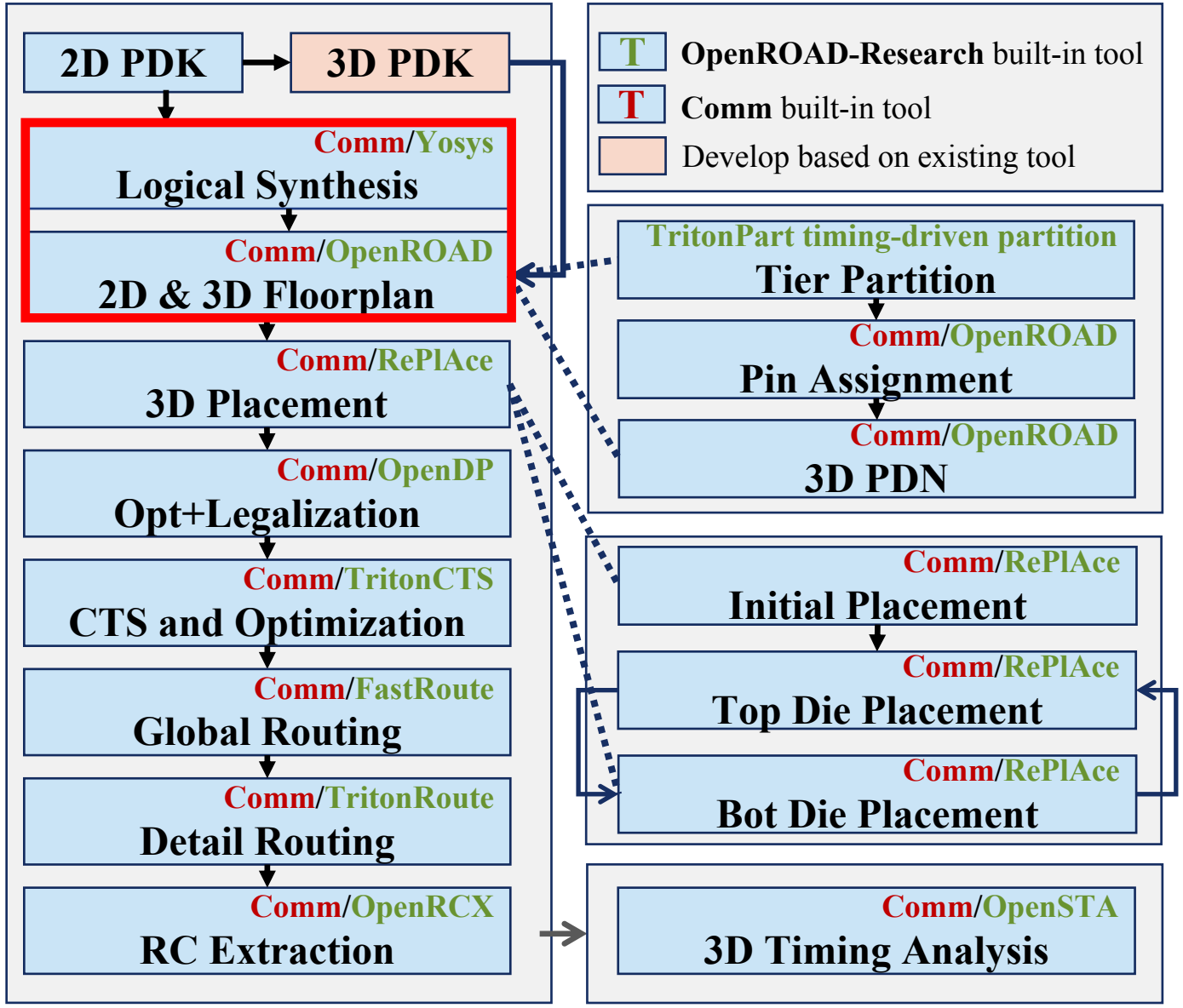
What we mentioned above:

- **2D → 3D PDK & tier-strategy**
- **3 PDKs:**
  - **NG45_3D**
  - **ASAP7_3D**
  - **ASAP7 + NanGate45**

Now we are introducing:

- **A fully automated RTL-to-GDS flow for F2F 3D stacks by reusing mature 2D engines**

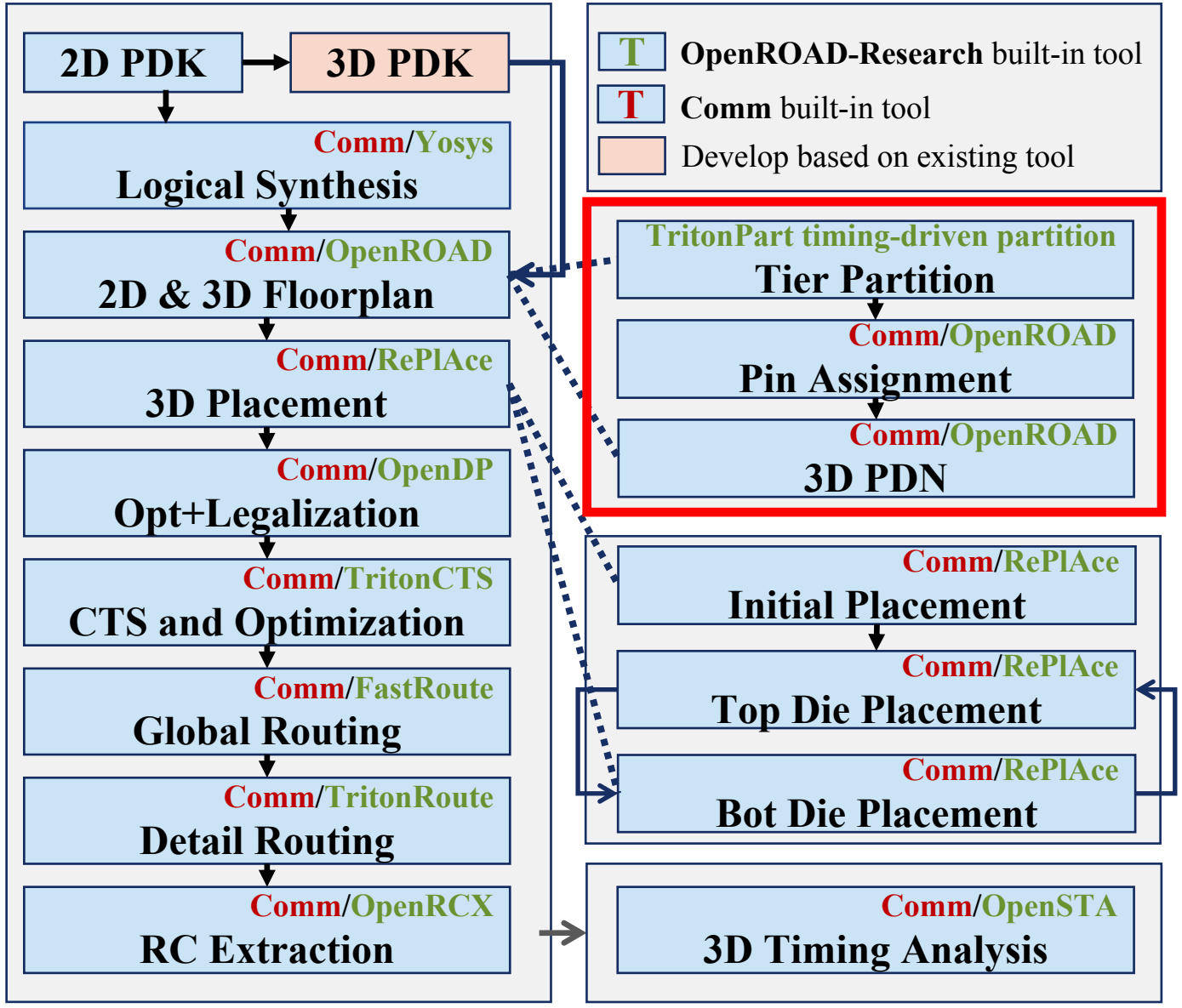
Pin-3D Flow: Step-by-Step Execution Flow

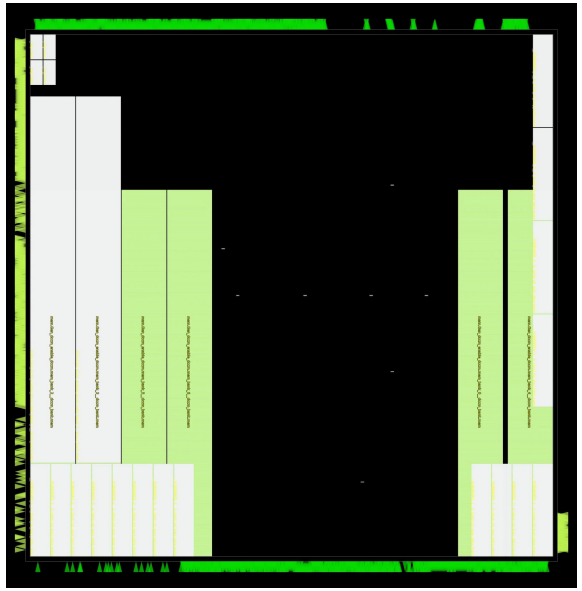


2D logical synthesis using 2D PDK

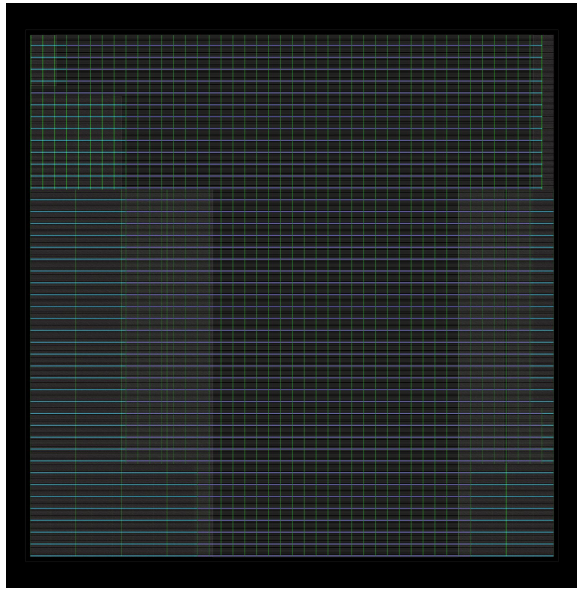
Partition First with TritonPart

Pin-3D Flow: Step-by-Step Execution Flow



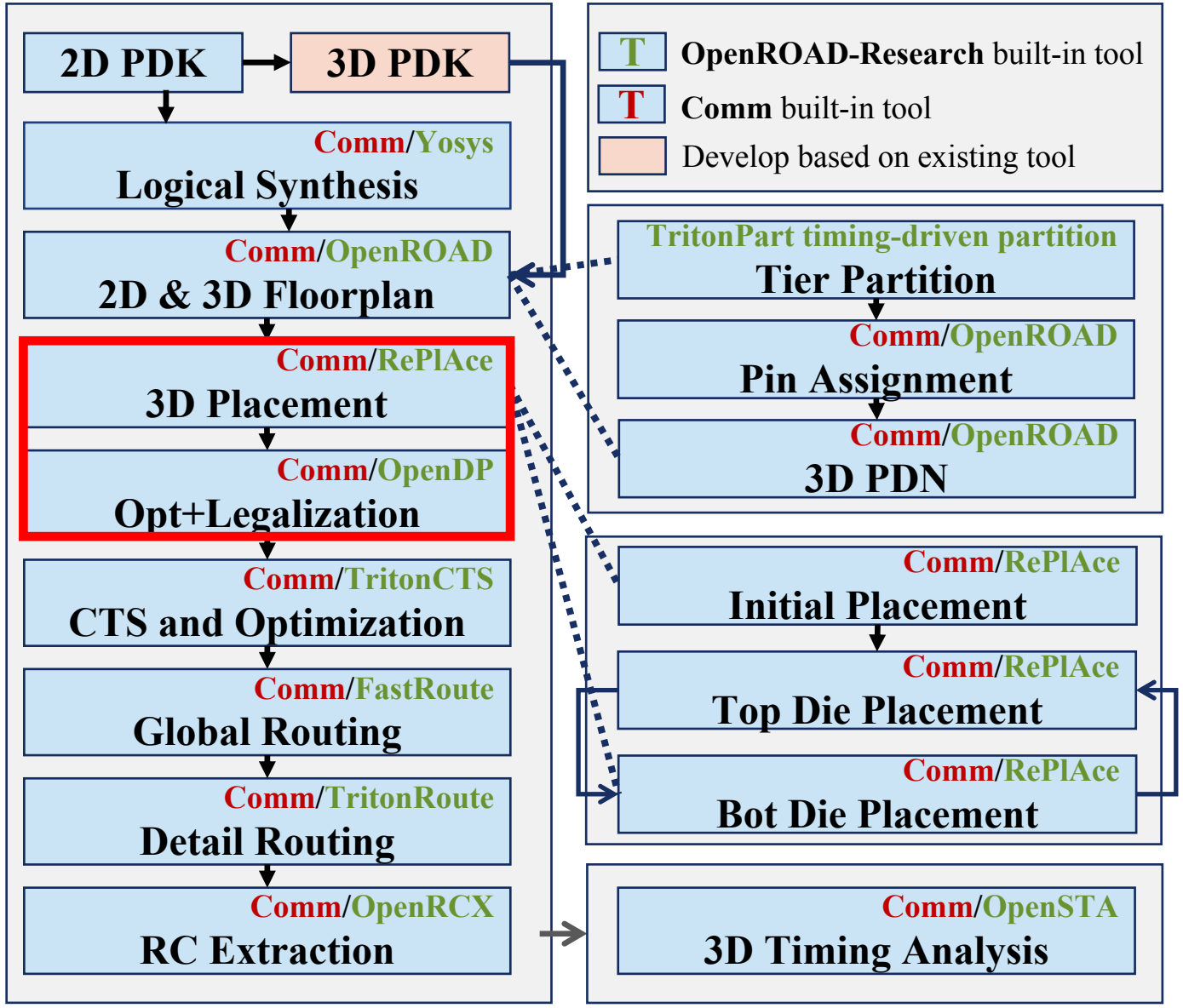


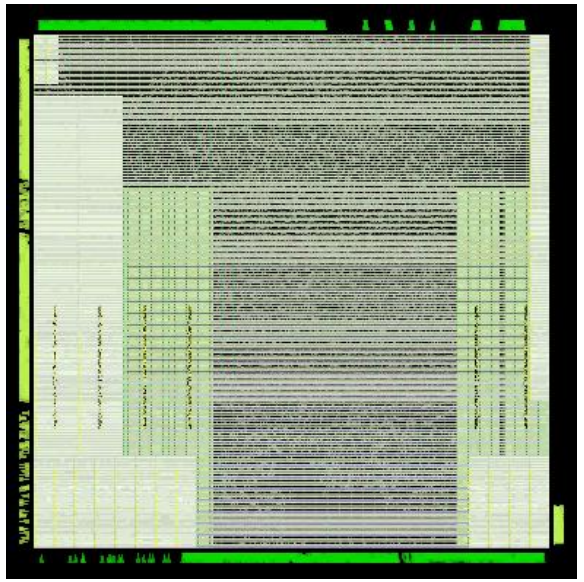
Macro Place



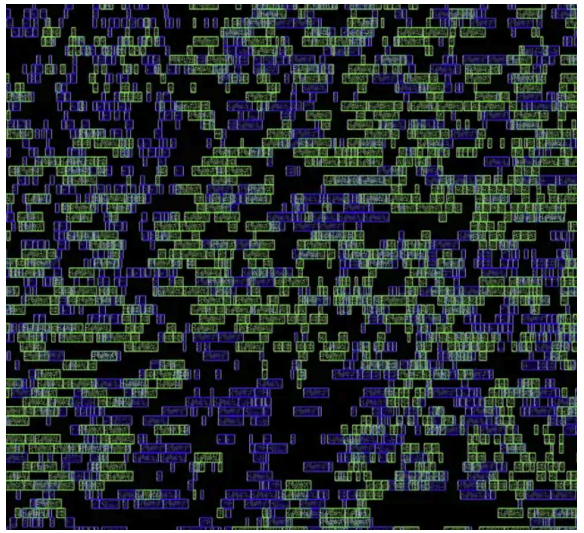
PDN

Pin-3D Flow: Step-by-Step Execution Flow





Global Place



Opt + Legalize

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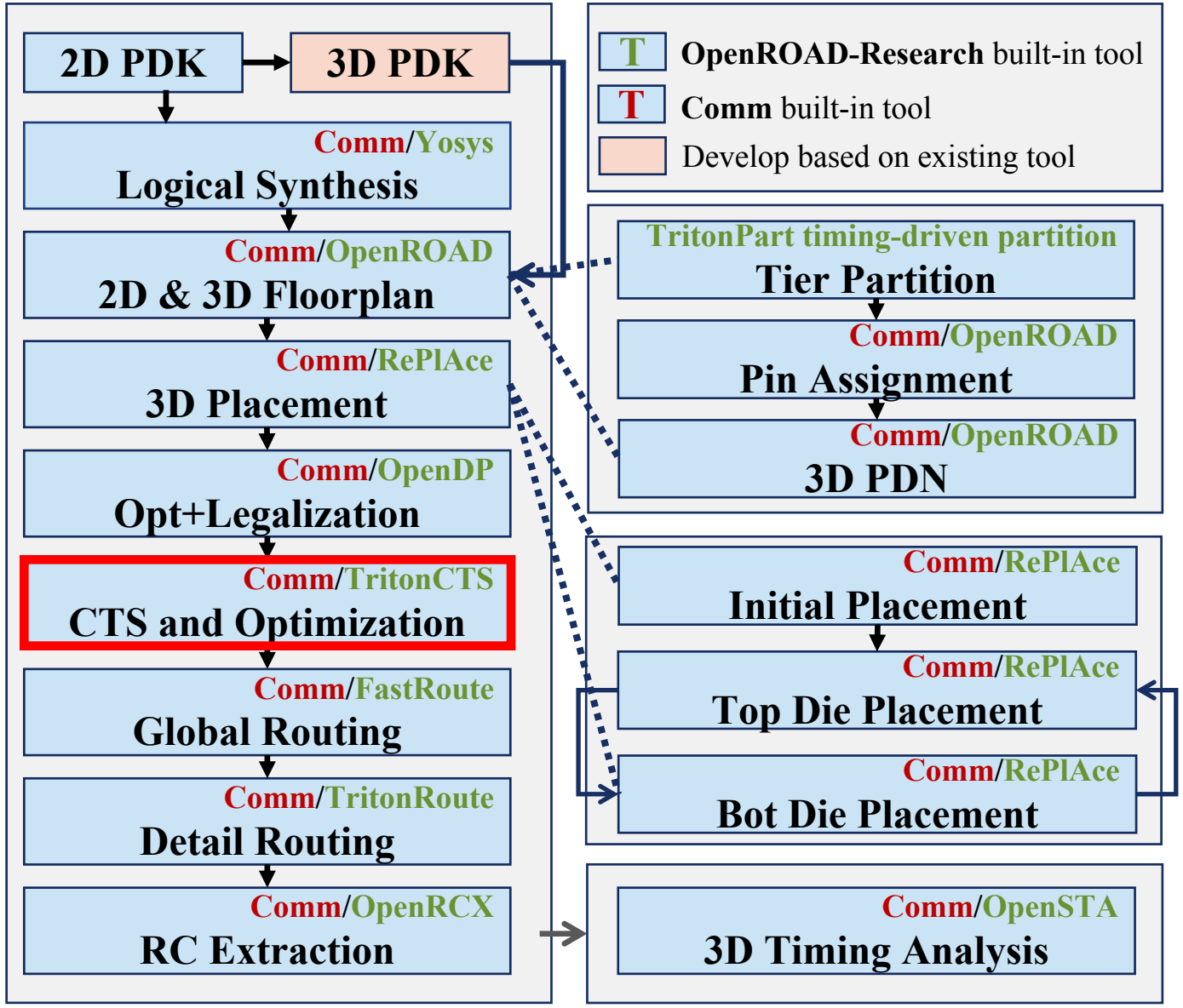
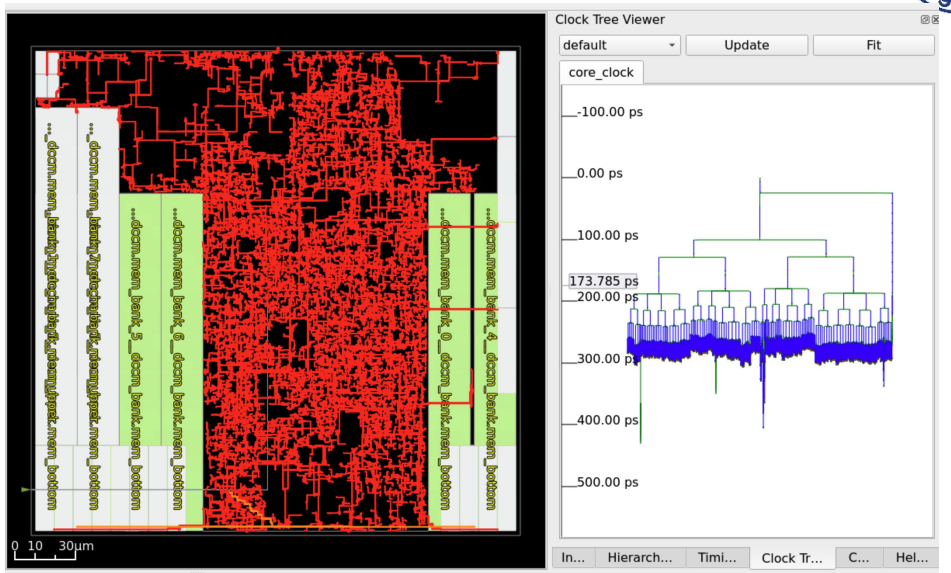
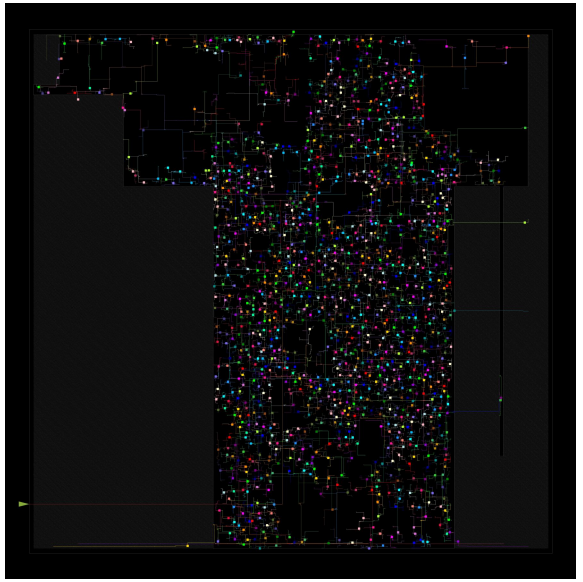


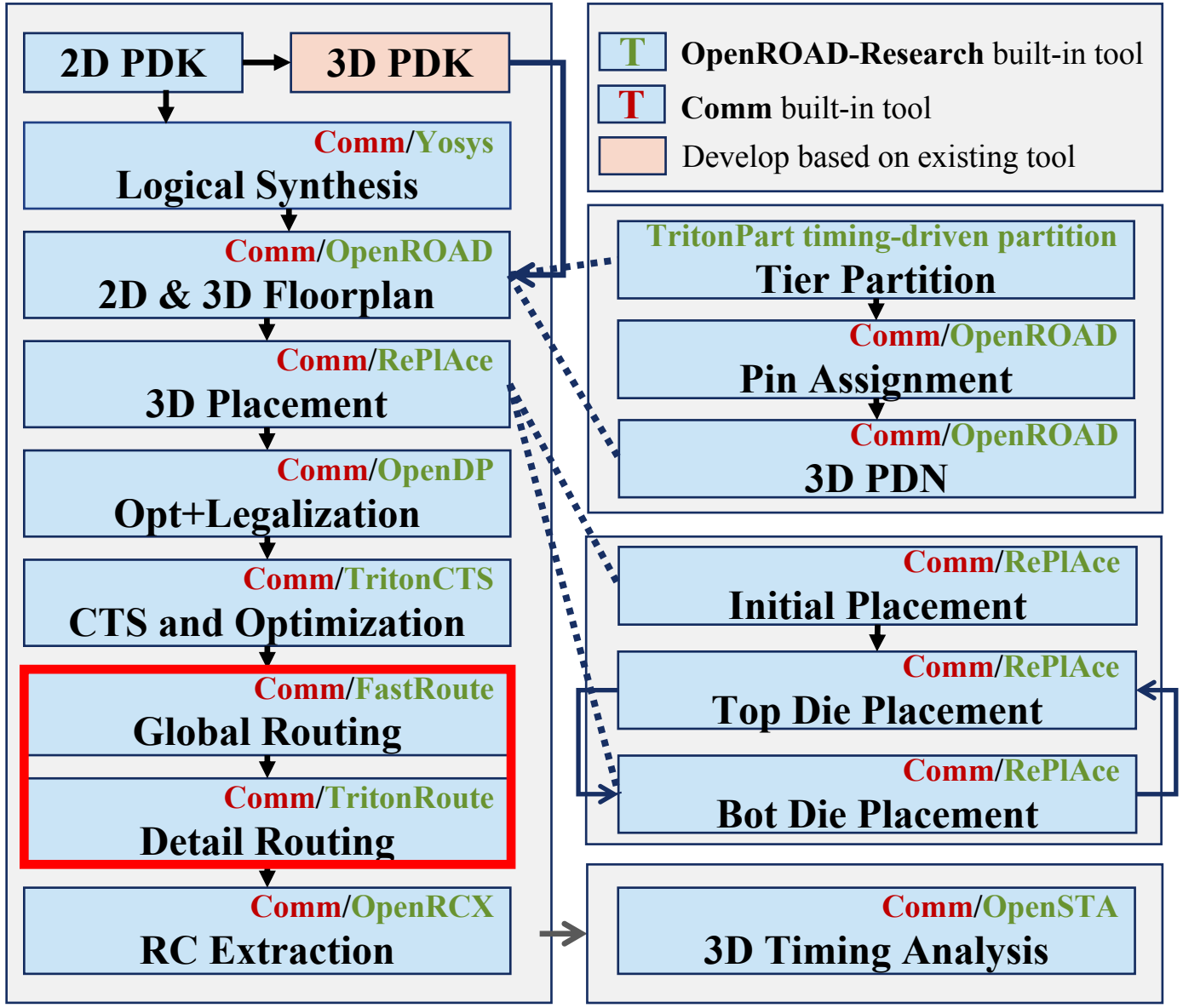


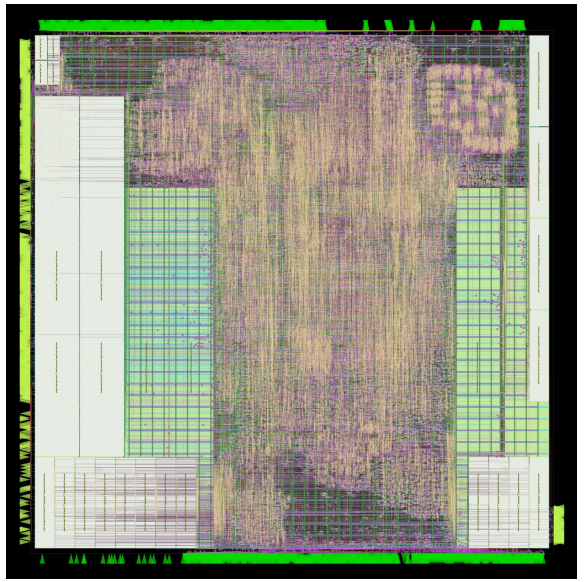
CTS



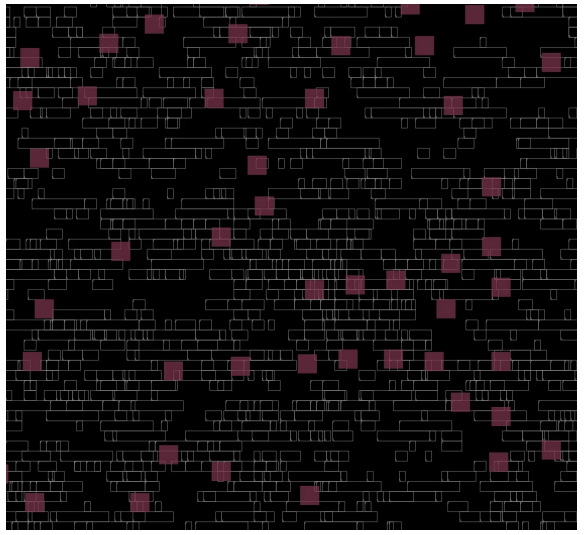
Clock Net

Pin-3D Flow: Step-by-Step Execution Flow



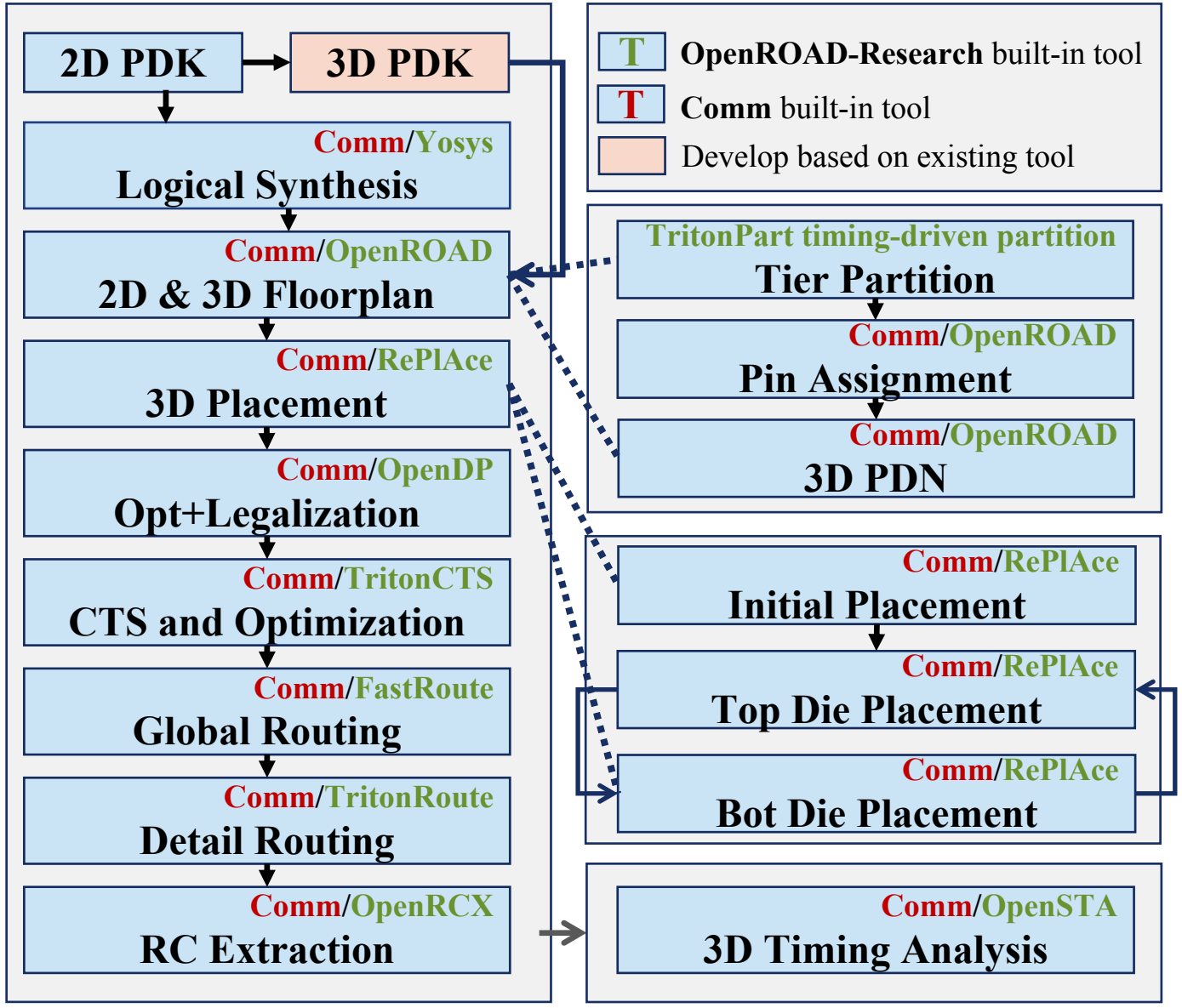


Routed layout



HBTs

Pin-3D Flow: Step-by-Step Execution Flow



Handoff Outline:

- Read and write .v and .def, use .lef and .lib to mark different tier cell master
- Synthesis → 1_synth.{v,sdc}
- 2D Floorplan + IO → 2_2_floorplan_io.{v,def}
- Partition → partition.txt → DEF/Verilog → DESIGN_NAME_3D.fp.{v,def}
- 3D Floorplan→ 2_floorplan.{v,def,sdc}
- 3D Placement → 3_placed.{v,def,sdc}
- CTS → 4_cts.{def,v,sdc}
- Routing → 5_route.{def,v,sdc}
- Eval → post-route STA/RC extraction

3 Pin-3D Validations

Enable fair and reproducible PD comparisons

Mixed flow: The "Synthesis Gap"

(Detailed Routing: fixed at 20 iterations for runtime)

Toolchain Configuration (Synthesis + Backend)	StdCell Area (µm2)	Power (mW)	rWL (mm)	WNS (ns)	DRVs	FEPs	HBT
Commercial Synthesis + Commercial Backend	16,446.5	20.33	232.2	-0.016	3	6	904
Commercial Synthesis + OpenROAD Placement + Commercial CTS/Routing	16,510.1	22.50	237.5	-0.040	0	54	1,031
Commercial Synthesis + OpenROAD Backend	16,193.3	24.58	209.8	-0.135	153	144	522
Yosys Synthesis + Commercial Backend	17,604.7	38.77	195.2	0.012	0	0	982
Yosys Synthesis + Commercial Placement + OpenROAD CTS/Routing	17,664.3	45.25	189.7	-0.094	0	87	915
Yosys Synthesis + OpenROAD Backend	18,100.8	46.33	193.4	-0.064	8	55	650

Mixed flow: The "Routing & CTS Gap"

(Detailed Routing: fixed at 20 iterations for runtime)

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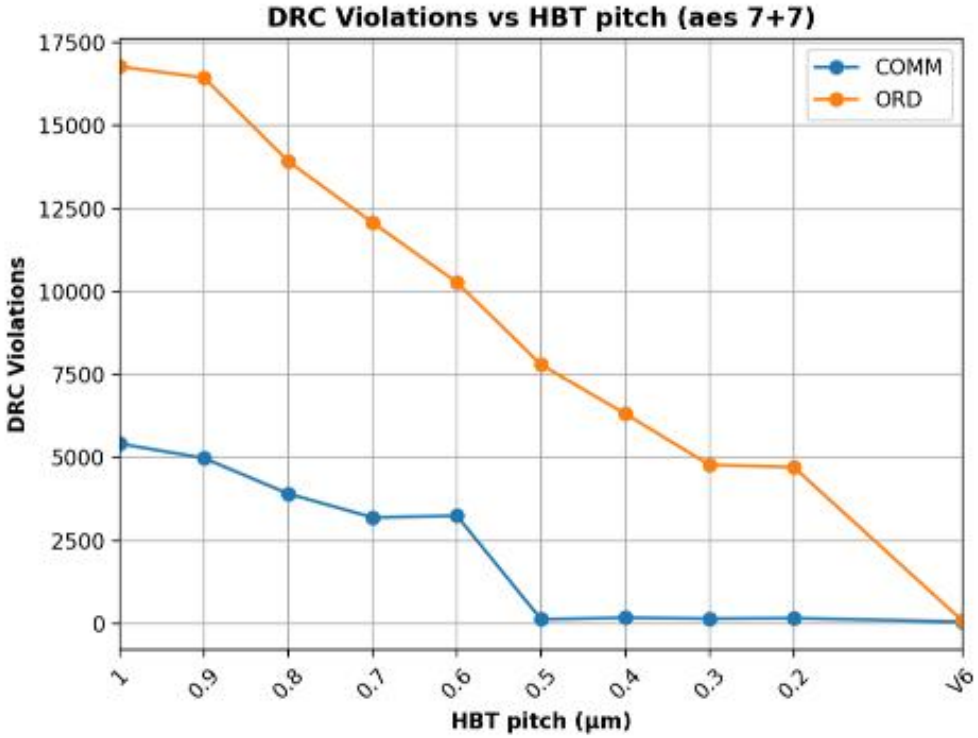
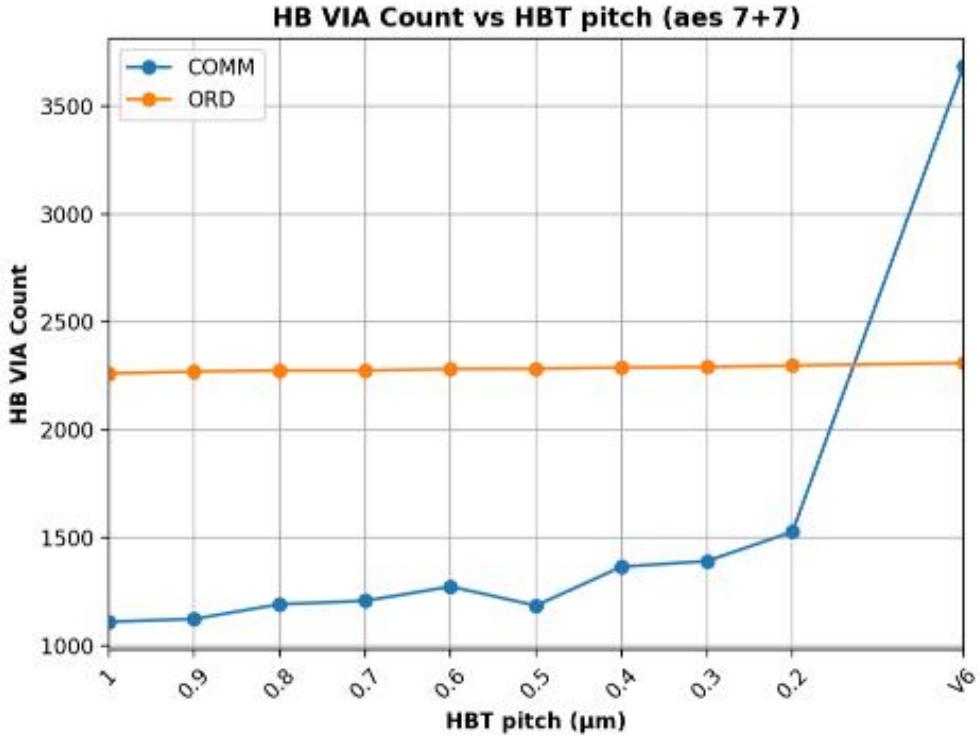
Effect on HBT Pitch size





With a larger pitch, HBTs lead to more shorts and spacing issues.

As the pitch becomes closer to via-scale, these violations drop quickly.

4 Key Takeaway

ORFS-Research enabled F2F 3D flow

Why This Flow Matters (Beyond Any Single QoR Number)

01

Problem Addressed

Reproducibility gap:

missing PDK details and fragile scripts make results hard to reproduce.

02

Core Value

Explicit evaluation contract:

consistent stage I/O and metrics, even when tools are swapped.

03

Community Impact

Drop-in extensibility:

plug in a new tool without rebuilding the RTL-to-GDS pipeline.

Key Takeaway

A maintained, audit-ready benchmarking harness making 3D PD research **reproducible**, **comparable**, and **extensible**.

https://github.com/ieee-ceda-datc/ORFS-Research/tree/maple/pin3Dflow/flow-Pin3D

QR code for our ORFS-Research Pin 3D

ORFS-Research maple/pin3Dflow (legacy)

https://github.com/CODA-Team/TaiWei-Pin-3D