Technische Universität Dresden

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Layout Design Automation: From Academia to Industry and Back

Jens Lienig

Prof. Dr.-Ing. Dr. h.c. Dieter A. Mlynski
1932 – 2024


Atlantic Ocean
Pacific Ocean
Indian Ocean

Starting in Academia: My First Paper (EDAC, 1992)

Routing Algorithms for Multi-Chip Modules

Jens Lienig, K. Thulasiraman, M. N. S. Swamy

Department of Electrical and Computer Engineering
Concordia University
1455 de Maisonneuve Blvd. West
Montreal, Quebec H3G 1M8, Canada

Abstract

We present routing algorithms for multi-chip modules. Two routing strategies, a channel routing and a grid-based routing, are discussed. The channel routing enables the designer to examine an effective routing during the placement phase. The grid-based routing calculates the net ordering with a new cost function and includes an effective rip-up and reroute procedure. The paper concludes with the presentation of some routing results.

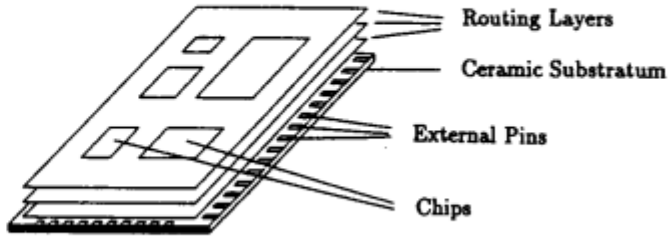
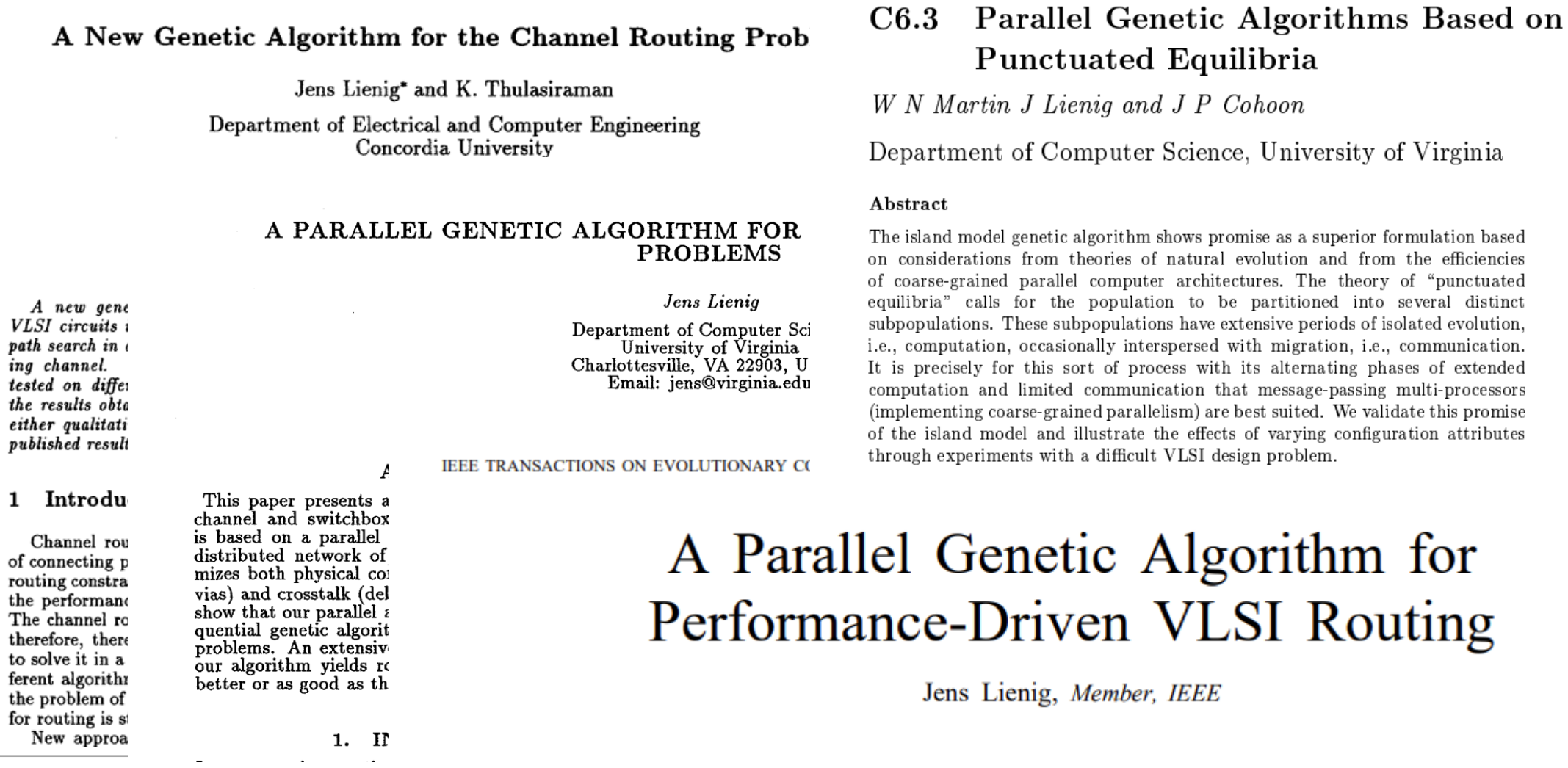


Figure 1: A multi-chip module

Starting in Academia: Moving into Evolutionary Algorithms



A New Genetic Algorithm for the Channel Routing Prob

Jens Lienig* and K. Thulasiraman

Department of Electrical and Computer Engineering
Concordia University

A PARALLEL GENETIC ALGORITHM FOR PROBLEMS

Jens Lienig

Department of Computer Sci
University of Virginia
Charlottesville, VA 22903, U
Email: jens@virginia.edu

IEEE TRANSACTIONS ON EVOLUTIONARY C

C6.3 Parallel Genetic Algorithms Based on Punctuated Equilibria

W N Martin J Lienig and J P Cohoon

Department of Computer Science, University of Virginia

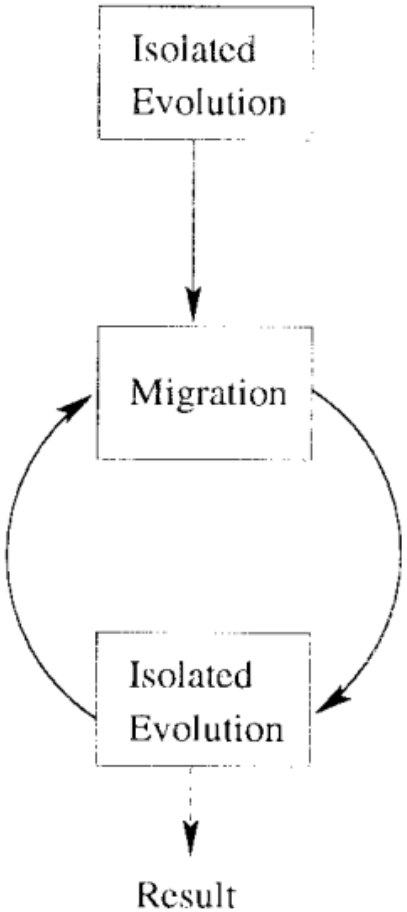
Abstract

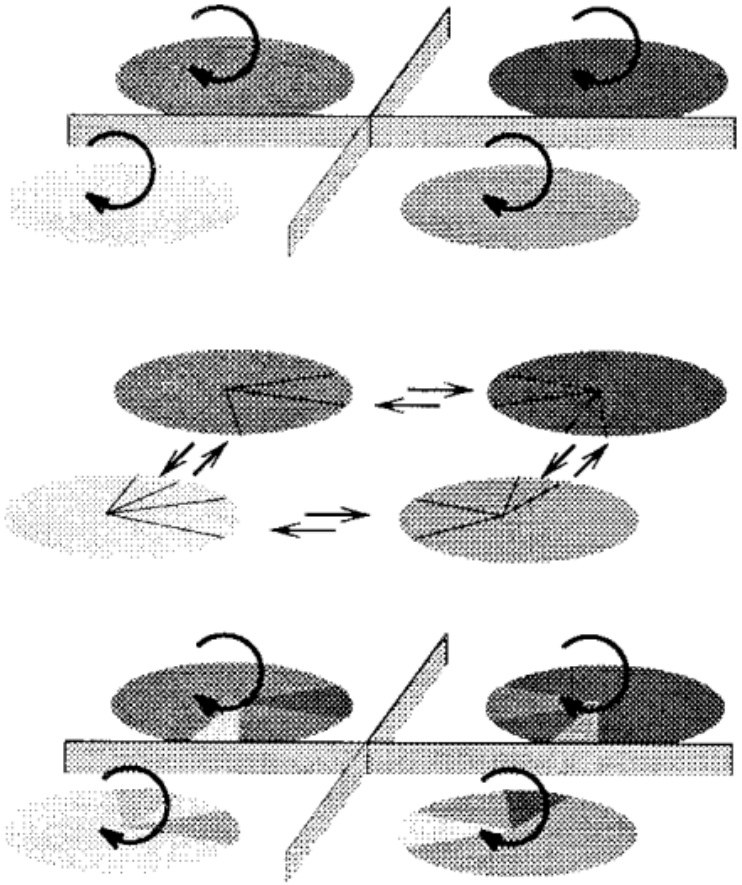
The island model genetic algorithm shows promise as a superior formulation based on considerations from theories of natural evolution and from the efficiencies of coarse-grained parallel computer architectures. The theory of "punctuated equilibria" calls for the population to be partitioned into several distinct subpopulations. These subpopulations have extensive periods of isolated evolution, i.e., computation, occasionally interspersed with migration, i.e., communication. It is precisely for this sort of process with its alternating phases of extended computation and limited communication that message-passing multi-processors (implementing coarse-grained parallelism) are best suited. We validate this promise of the island model and illustrate the effects of varying configuration attributes through experiments with a difficult VLSI design problem.

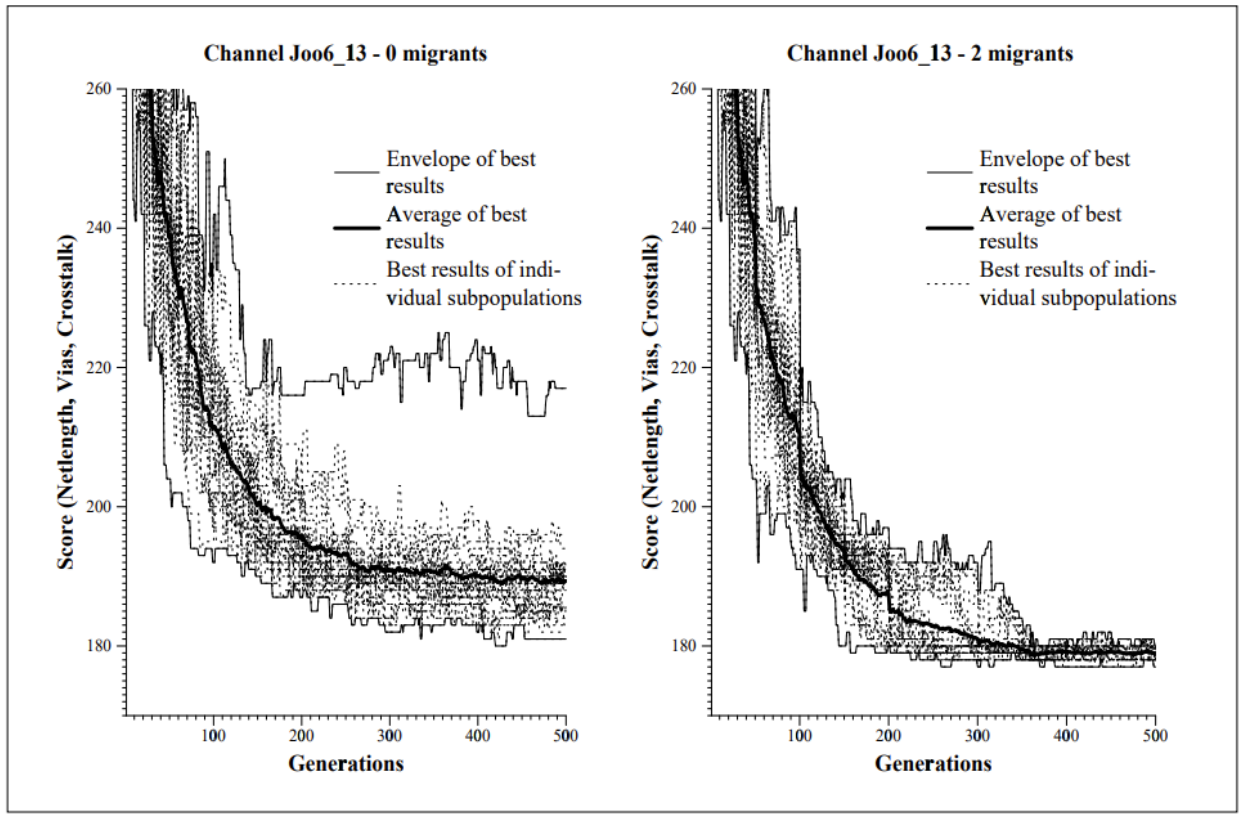
A Parallel Genetic Algorithm for Performance-Driven VLSI Routing

Jens Lienig, *Member, IEEE*

Parallel Genetic Algorithms Based on Punctuated Equilibria



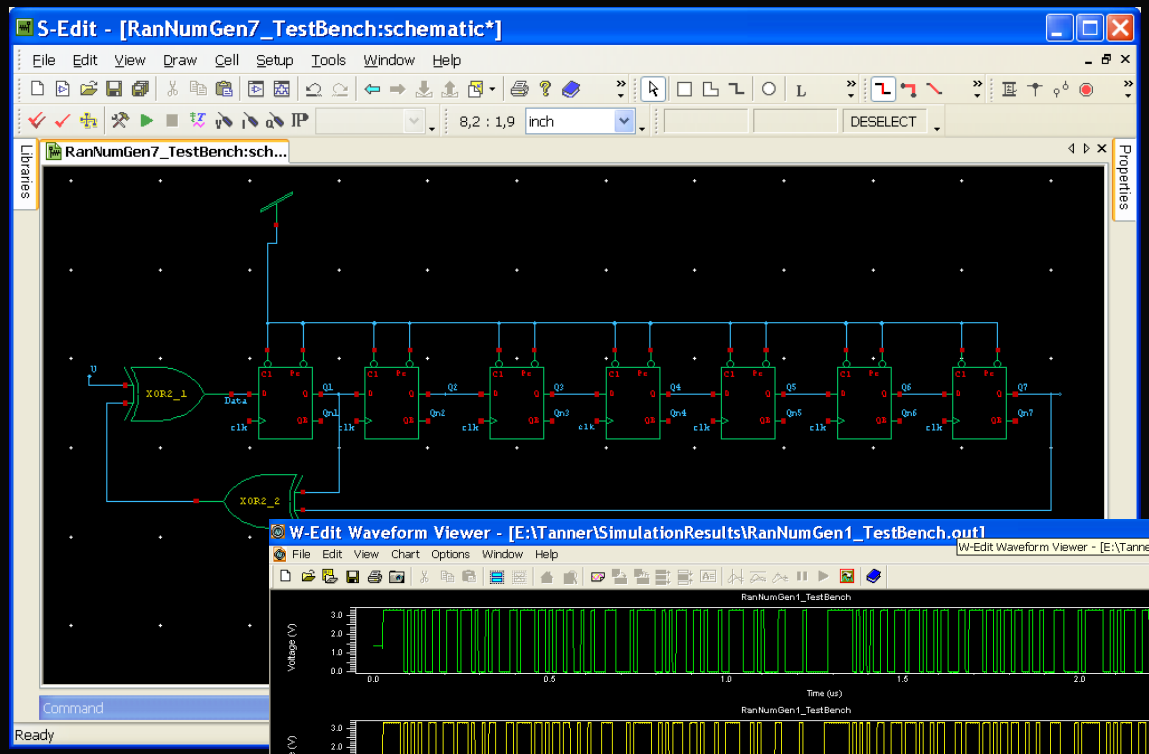




It is Time for Industry…


U-HAUL


Tanner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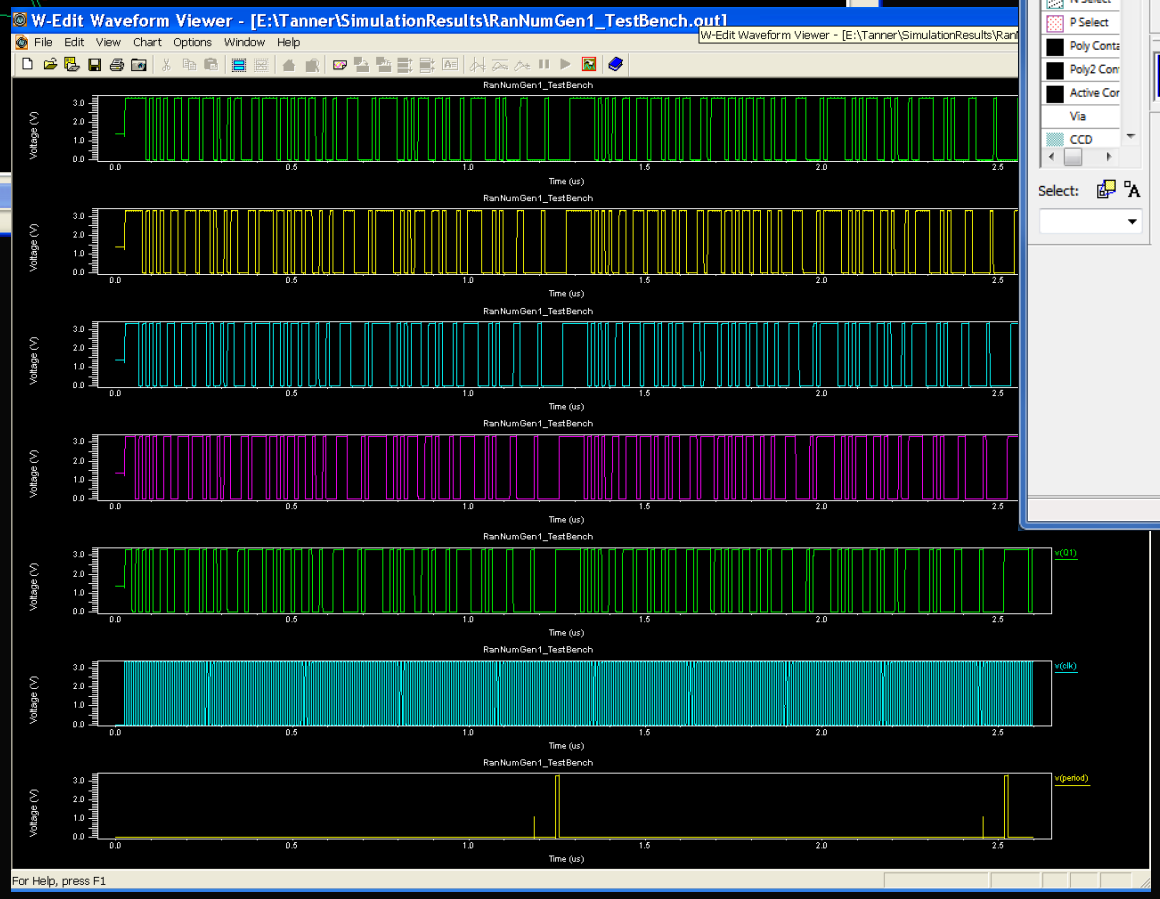
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RanNumGen1_TestBench
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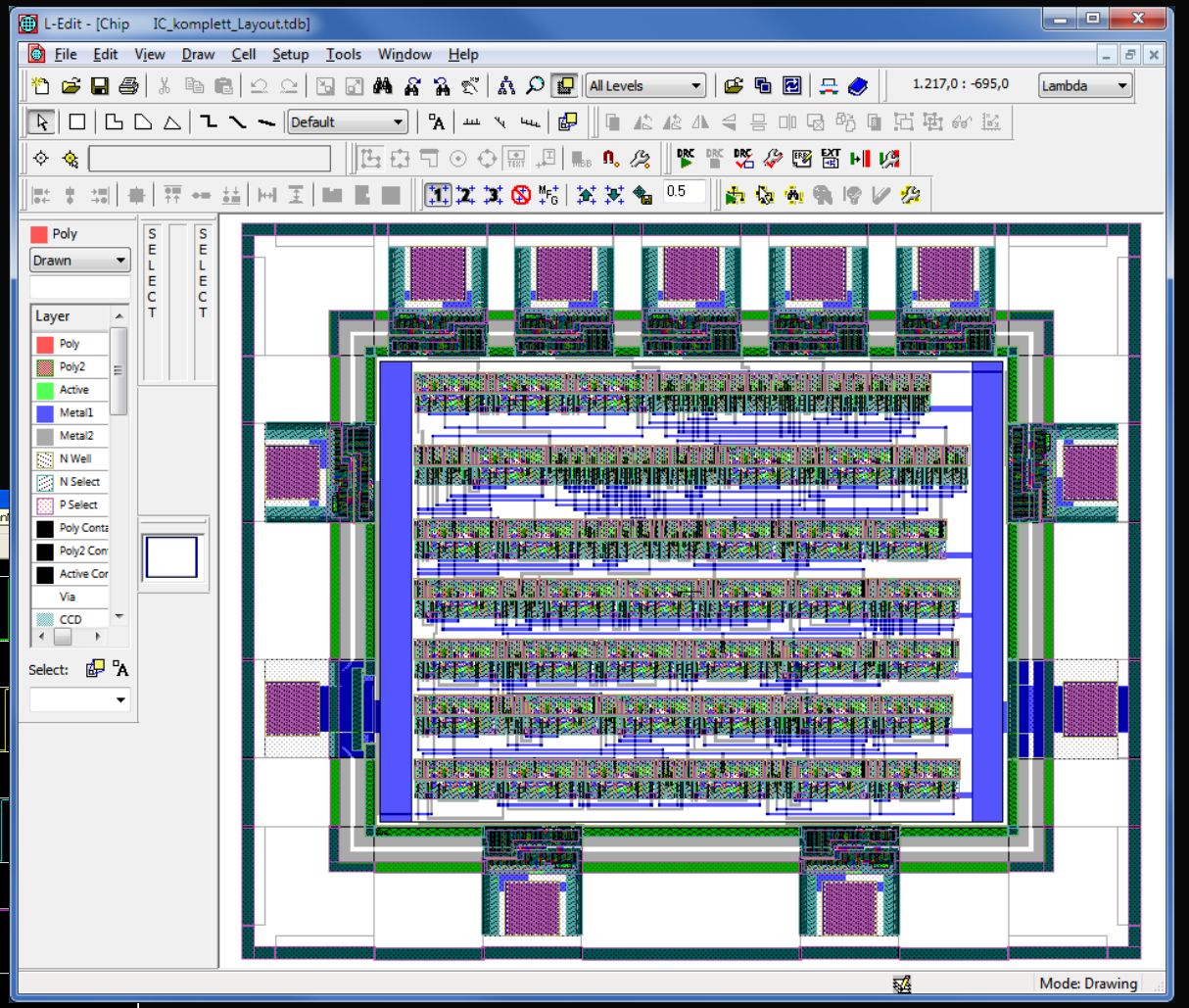
For Help, press F1


L-Edit - [Chip IC_komplett_Layout.tdb]
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DESIGNLINES | AUTOMOTIVE DESIGNLINE

EDA software Designs Camera ICs on Mars Rovers

By EETimes 03.15.2004 0

Integrated circuits (ICs) designed using software from Tanner EDA are ensuring the successful operation of the cameras on the NASA Mars Exploration Rovers Opportunity and Spirit. Tanner is a leading developer of EDA (electronic design automation) software for integrated circuit designers.

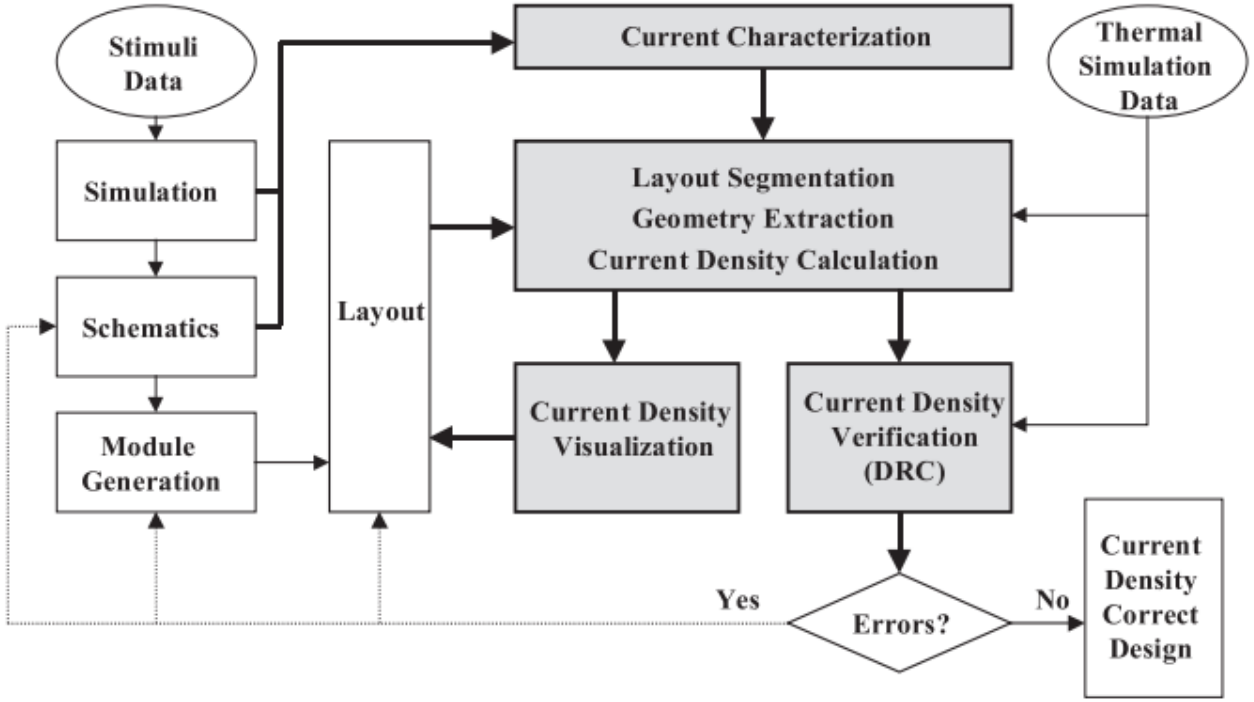
Scientists and designers at NASA's Jet Propulsion Laboratory (JPL) in Pasadena, California, used L-Edit Pro, Tanner's layout and verification software and T-Spice Pro, Tanner's design entry and simulation software, to design a 1024×1024 CCD (charge coupled device). This effectively shutters, or 'grabs' the images and reads them out to the camera electronics. The CCD design is in use in each of Opportunity and Spirit's different camera systems, which are producing the highest-resolution images ever taken of another planet.

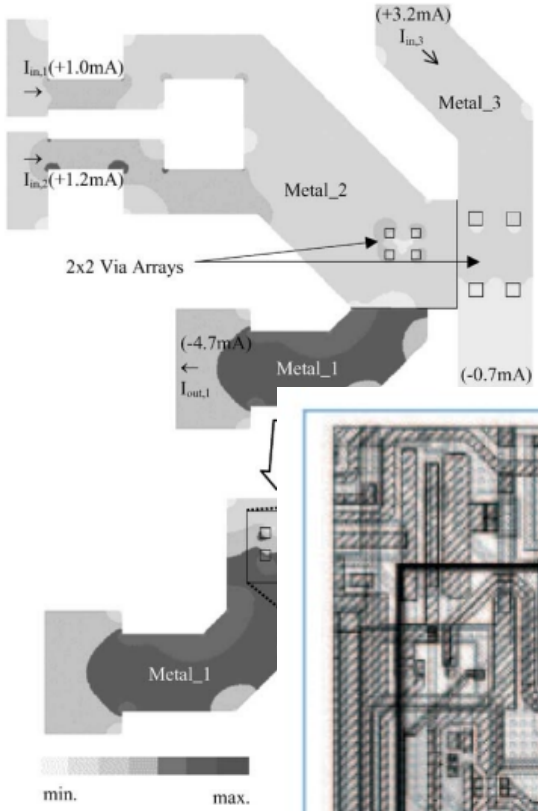

Atlantic Ocean
Pacific Ocean
Indian Ocean

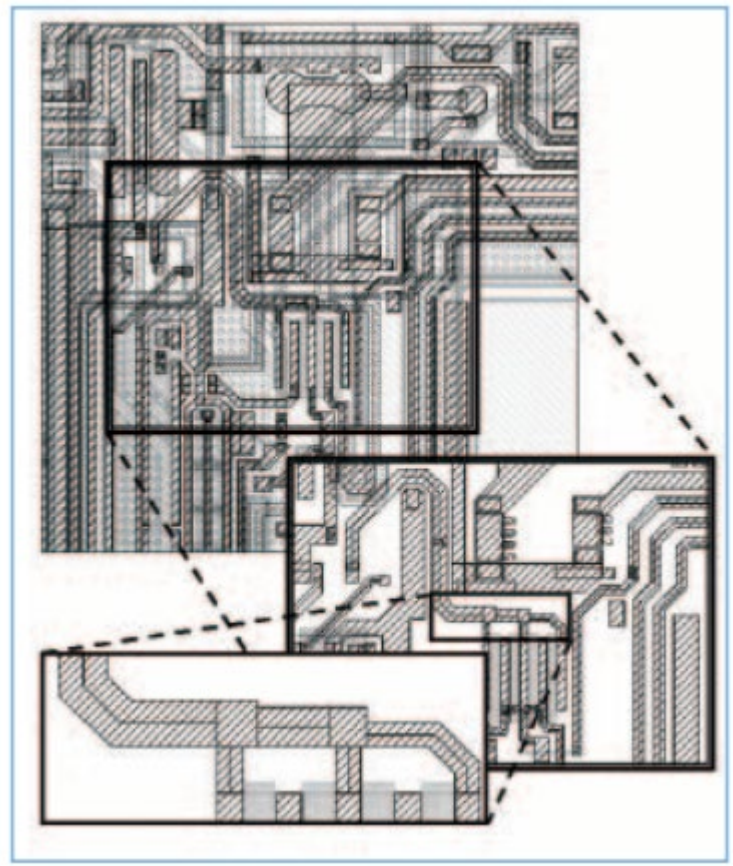

BOSCH

Hierarchical Current-Density Verification in Arbitrarily Shaped Metallization Patterns of Analog Circuits

Göran Jerke, *Student Member, IEEE,* and Jens Lienig, *Member, IEEE*








Sweden
North Frisian Islands
North Sea
Lubek
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Magdeburg
Arnhem
Hartz Mountains
Dortmund
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Dresden
Aachen
Weimar
Liege
Bonn
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Belgium
Koblenz
Czech Republic
Trier
Frankfurt
Pizen
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Luxembourg
Heidelberg
Nuremburg
Nancy
Baden-Baden
Stuttgart
Strasbourg
Passau
Tubingen
BAVARIA
Linz
Freiburg
Munich
Salzburg
France
Basel
Konstanz
Mittenwald
Berchtesgaden
Zurich
Fussen
Bregenz
Innsbruck
Austria
Lucerne
Lech
Switzerland


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Nancy
Baden-Baden
Stuttgart
Strasbourg
Passau
Tubingen
BAVARIA
Linz
Freiburg
Munich
Salzburg
France
Basel
Konstanz
Mittenwald
Berchtesgaden
Zurich
Fussen
Bregenz
Innsbruck
Austria
Lucerne
Lech
Switzerland

Dresden University of Technology
Institute of Electromechanical and Electronic Design

- Professor of Electromechanical and Electronic Design

Dresden University of Technology
Institute of Electromechanical and Electronic Design

- Professor of Electromechanical and Electronic Design
- Director of the Institute
- Five main research areas

Electronic Design Automation	Design of Electronic Systems	Electro-mechanical Systems	Simulation and Optimization	Medical Device Engineering

Overview

From Academia to Industry and Back

Academia: Evolutionary algorithms – the quest for applicability

Industry: From software development to EDA tool management

Academia: Electromigration avoidance and (many) other topics

Overview

From Academia to Industry and Back

Academia: Evolutionary algorithms – the quest for applicability

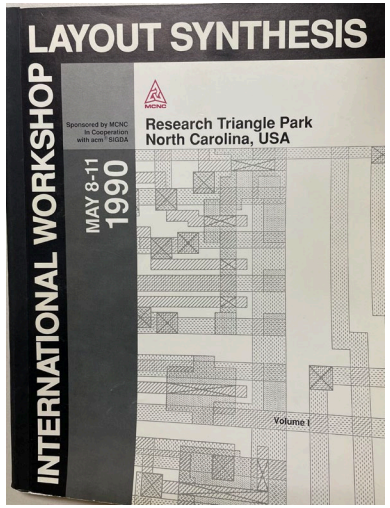
Industry: From software development to EDA tool management

Academia: Electromigration avoidance and (many) other topics

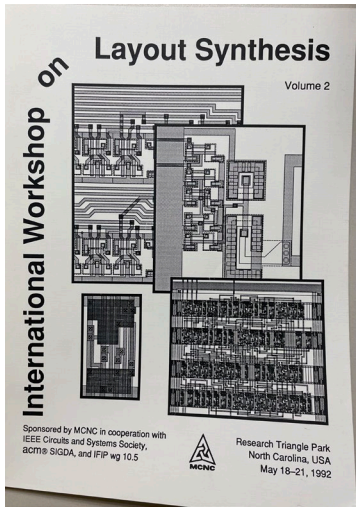
ISPD – More Than an Annual Symposium

International Symposium on Physical Design (ISPD)
Predecessors

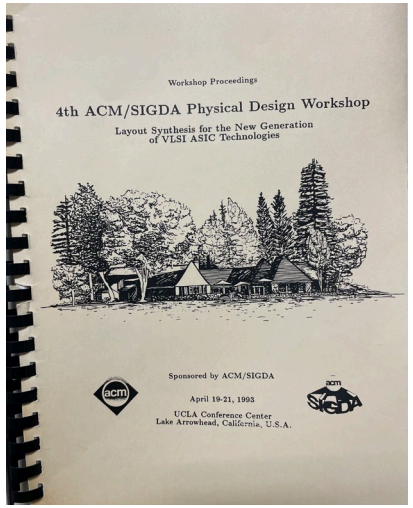
- ACM SIGDA Physical Design Workshop: 1987, 1989, 1991, 1993, 1996
- MCNC Layout Synthesis Workshop: 1988, 1990, 1992



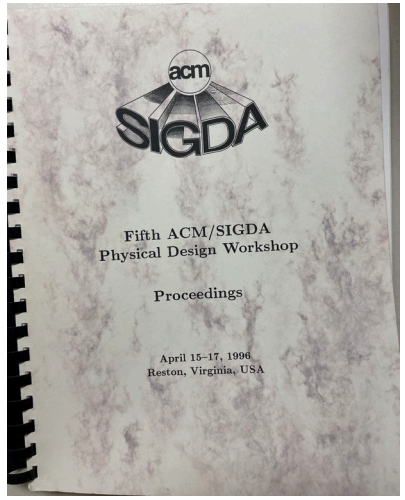
1990



1992

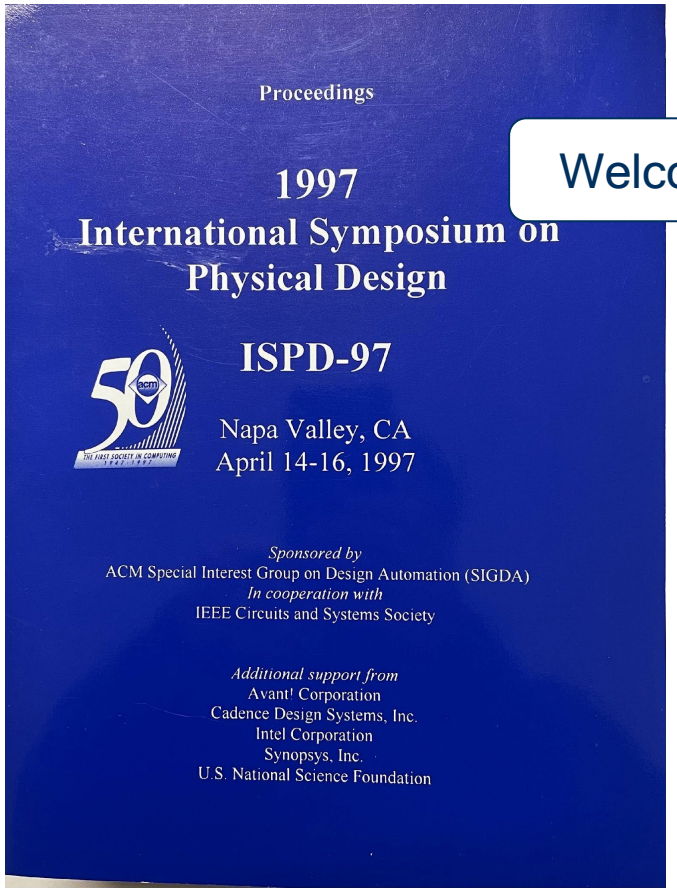


1993



1996

International Symposium
First ISPD 1997



Foreword

Welcome to the first International Symposium

1997 will be reme ed as yet another year
industry. Lithog gn complexity, and
than predicted ago: 0.18-micr
microprocesso reach their n
have been e ndustry
of system d cir
synthesis

1987-1996. Its scope includes all aspects of ph
logic-level synthesis, to back-end performance

This year's inaugural Symposium focuses on
design, as well as the necessary interactions be
cation tasks. The 15-member Technical Progra
technical papers; a total of 69 papers were subi
accepted for poster presentation. These researc
that set forth contexts and visions for the key ar
design and design methodology – with an emp
design. A number of the invited presentations
proceedings. The Symposium concludes with
unique perspectives as to the critical R&D nee

Thanks are due to the ACM Special Interest G
ISPD-97 in cooperation with the IEEE Circuits
has also been provided by Avant! Corporatior
Synopsys, Inc. and the U.S. National Science

On behalf of the Organizing and Technical Prog
useful and enjoyable. Again, welcome!

Andrew B. Kahng
General Chair

Welcome to the first International Symposium on Physical Design, ISPD-97!

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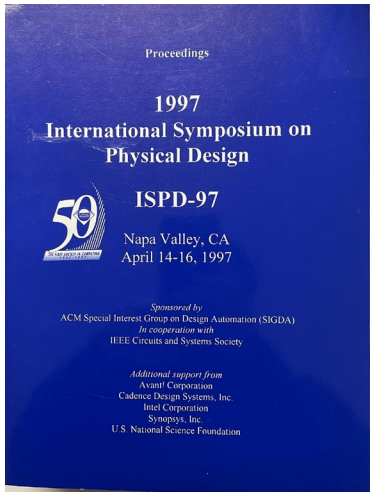
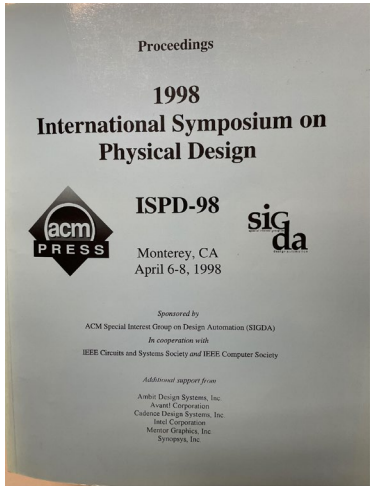
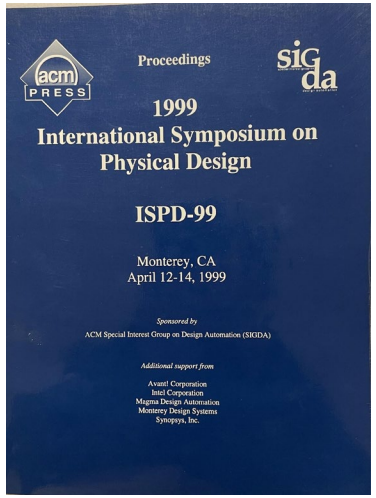
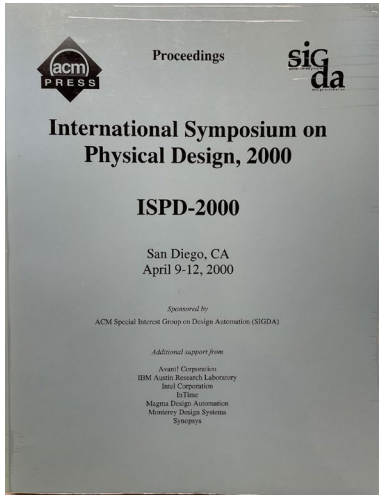
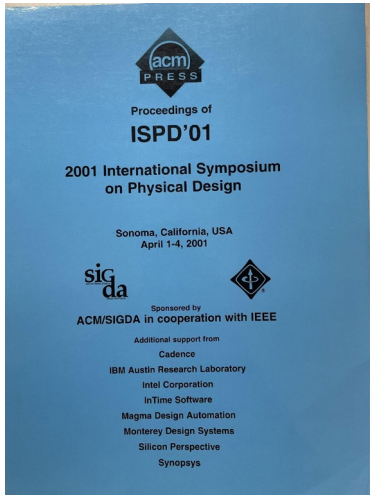
International Symposium on Physical Design (ISPD)
Annual Symposium 1997 - present

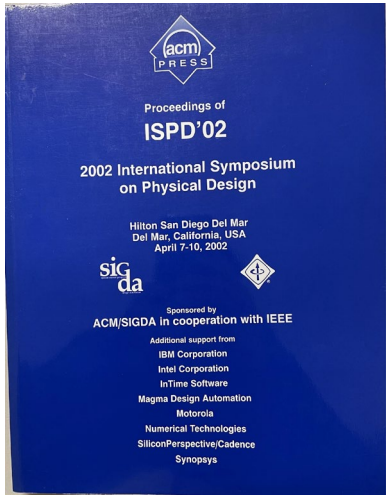


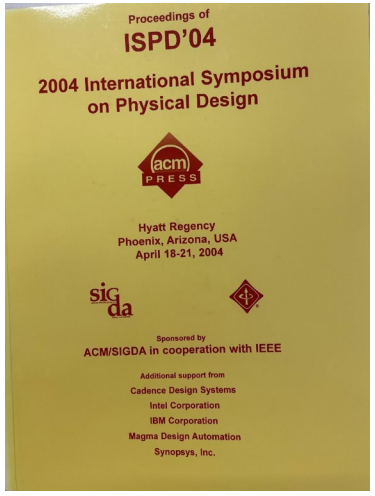


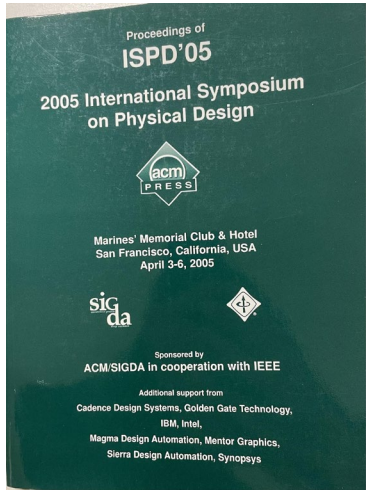


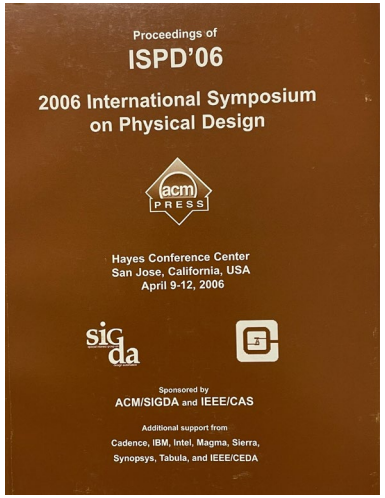


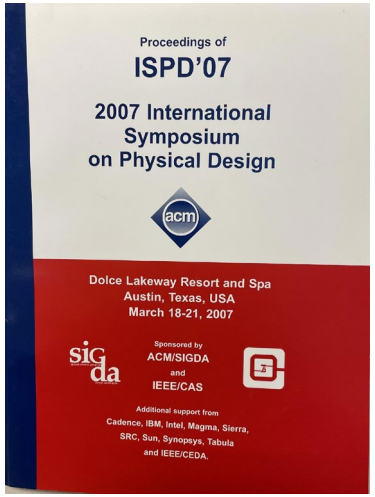


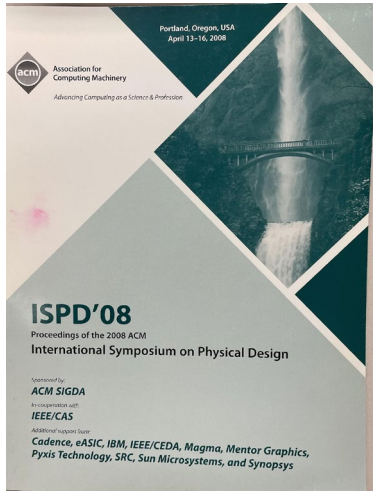




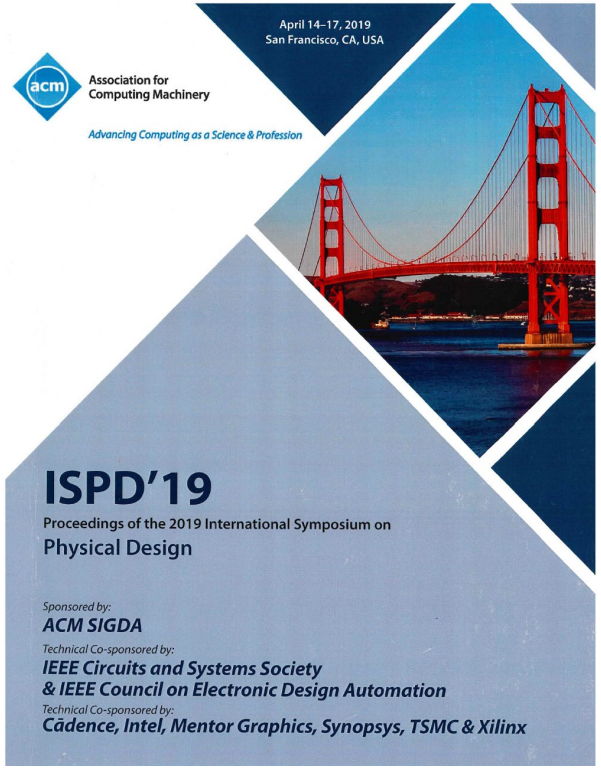








International Symposium on Physical Design
Annual Symposium 1997 - present



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International Symposium on Physical Design (ISPD)
ISPD 2020

TPC meeting Nov. 2019
Westminster/Denver, CO

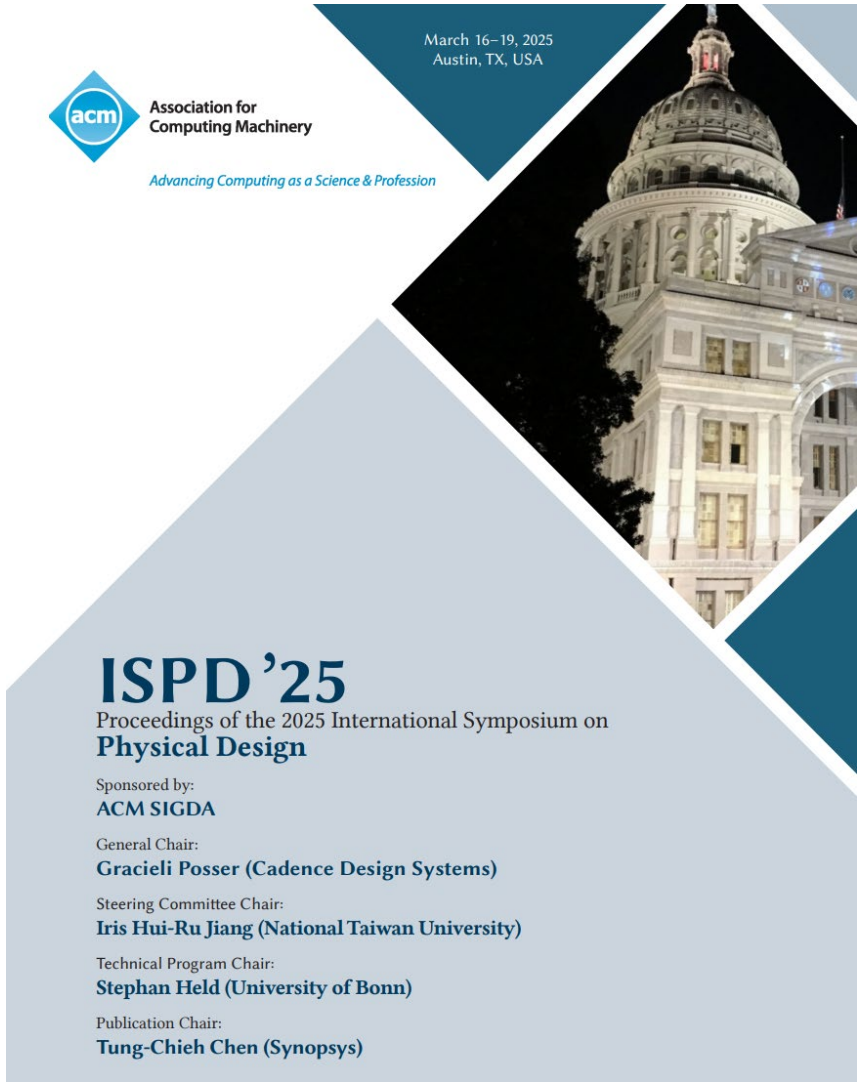
International Symposium on Physical Design (ISPD)
ISPD 2020: Cancelled by COVID-19

International Symposium on Physical Design (ISPD)
COVID-19: Online ISPD 2021, 2022, 2023

International Symposium on Physical Design (ISPD)
COVID-19: Online ISPD 2021, 2022, 2023

International Symposium on Physical Design (ISPD)
Back to normal: 2024, 2025 …

International Symposium on Physical Design (ISPD)
Back to normal: 2024, 2025 …



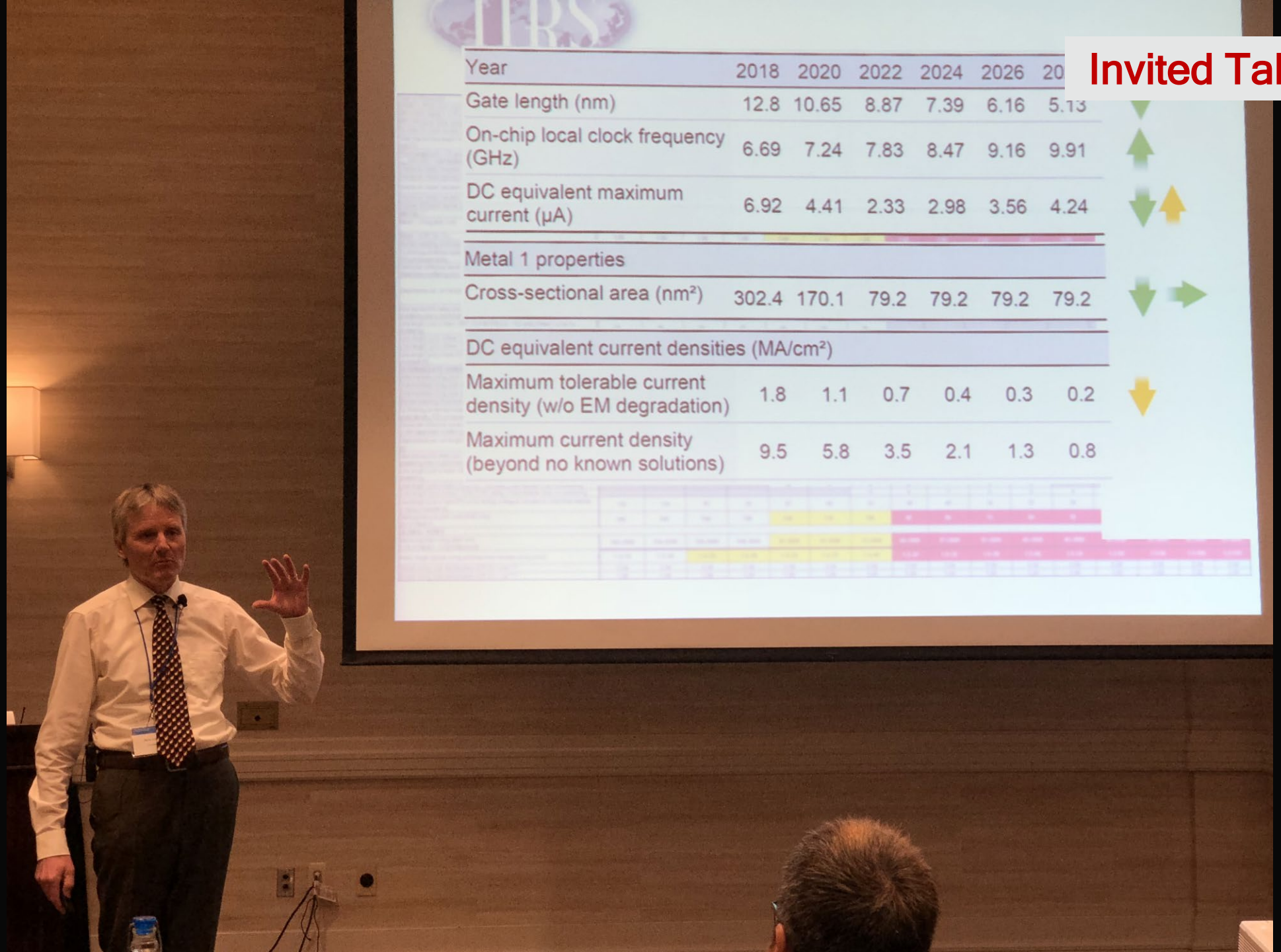
International Symposium on Physical Design (ISPD) Locations

1997	Napa Valley, CA
1998	Monterey, CA
1999	Monterey, CA
2000	San Diego, CA
2001	Sonoma, CA
2002	San Diego, CA
2003	Monterey, CA
2004	Phoenix, AZ
2005	San Francisco, CA
2006	San Jose, CA
2007	Austin, TX
2008	Portland, OR
2009	San Diego, CA
2010	San Francisco, CA
2011	Santa Barbara, CA
2012	Napa Valley, CA
2013	Stateline, NV
2014	Petaluma, CA
2015	Monterey, CA
2016	Santa Rosa, CA
2017	Portland, OR
2018	Monterey, CA
2019	San Francisco, CA
2021	Online
2022	Online
2023	Online
2024	Taipei, Taiwan
2025	Austin, TX
2026	Bonn, Germany

ISPD‘14: Petaluma, CA

ISPD‘16: Hilton, Sonoma, CA

ISPD‘18: Monterey, CA



Invited Talks

Participation statistics

- 12 teams initially participated from Canada, China, France, Germany, Hong Kong, Taiwan, USA
- 7 final placer binary submissions

Rank	Prize
1st	$2,000
2nd	$1,000
3rd	$500

ID	University	Team Lead and Members	Advisor
1	University of Calgary and University of Waterloo	Nima Karimpour Darav, Aysa Fakheri Tabrizi, David Westwick	Lalah Behjat Andrew Kennings
2	Dresden University of Technology	Andreas Krinke,Sergii Osmolovskyi, Johann Kenctel, Matthias Thiele, Steve Bigalke	Jens Lienig
4	Chinese University of Hong Kong	Wing-Kai Chow, Peisahn Tu, Jian Kuang, Zhiqing Liu	Evangeline Young
5	University of Illinois	Chun-Xun Lin, Zigang Xiao, Haitong Tian, Daifeng Guo	Martin Wong
7	National Taiwan University	Chau-Chin Huang, Sheng-Wei Yang, Chin-Hao Chang, Hsin-Ying Lee, Szu-To Chen, Bo-Qiao Lin	Yao-Wen Chang
10	National Chiao Tung University	Ching-Yu Chin	Hung-Ming Chen
11	National Chung Cheng University	Xin-Yuan Su	Mark Po-Hung Lin

International Symposium on Physical Design (ISPD) Contests

2005	Placement
2006	Placement
2007	Global Routing
2008	Global Routing
2009	Clock Network Synthesis
2010	Clock Network Synthesis
2011	Routability-Driven Placement
2012	Discrete Gate Sizing Contest
2013	Discrete Gate Sizing Contest
2014	Detailed Routing-Driven Placement
2015	Detailed Routing-Driven Placement
2016	Routability-Driven FPGA Placement
2017	Clock-Aware FPGA Placement
2018	Initial Detailed Routing
2019	Initial Detailed Routing
2020	Wafer-Scale DL Accelerator Placement
2021	Wafer-Scale Physics Modeling Contest
2022	Security Closure of Physical Layouts
2023	Security Closure of Physical Layouts
2024	GPU/ML-Enhanced Global Routing
2025	Performance-Driven Global Routing
2026	Post-Placement Buffering and Sizing

International Symposium on Physical Design (ISPD)
First Lifetime Achievement Award: 2011 Santa Barbara

Prof. Ernest Kuh (1928-2015)
University of California at Santa Barbara

International Symposium on Physical Design (ISPD)
Lifetime Achievement Award Recipients

2011	Prof. Ernest Kuh
2012	Prof. C.-L. Liu
2013	Prof. Yoji Kajitani
2014	Dr. Bryan Preas
2015	Prof. Kurt Antreich
2016	Prof. Ralph Otten
2017	Prof. Satoshi Goto
2018	Prof. Te C. Hu
2019	Prof. Alberto Sangiovanni-Vincentelli
2021	Dr. Louis K. Scheffer (postponed from ISPD 2020)
2022	Prof. Ricardo Augusto Da Luz Reis
2023	Prof. Malgorzata Marek-Sadowska
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Thank you very much!