Technische Universität Dresden

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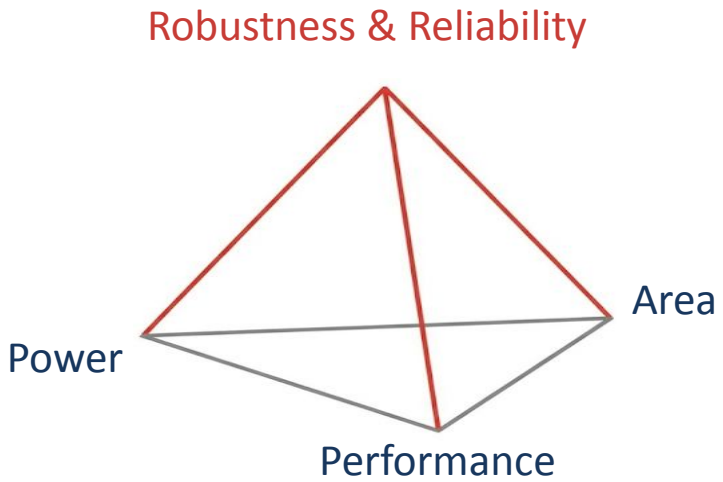
From Evolutionary Algorithms to Analog Design, Electromigration, 3D Integration, and Beyond: On Jens Lienig's Contributions to Advance Physical Design

Johann Knechtel, Susann Rothe, Robert Fischbach,
Matthias Thiele, Tilo Meister, Andreas Krinke

ISPD 2026 – Lifetime Award
Bonn (Germany), March 17th 2026

Core Philosophy

- PPA is meaningless if the chip fails in the field
- Robustness and reliability as overarching objectives
- Lienig's work bridges the gap between established design practices with the *physical* reality for physical design

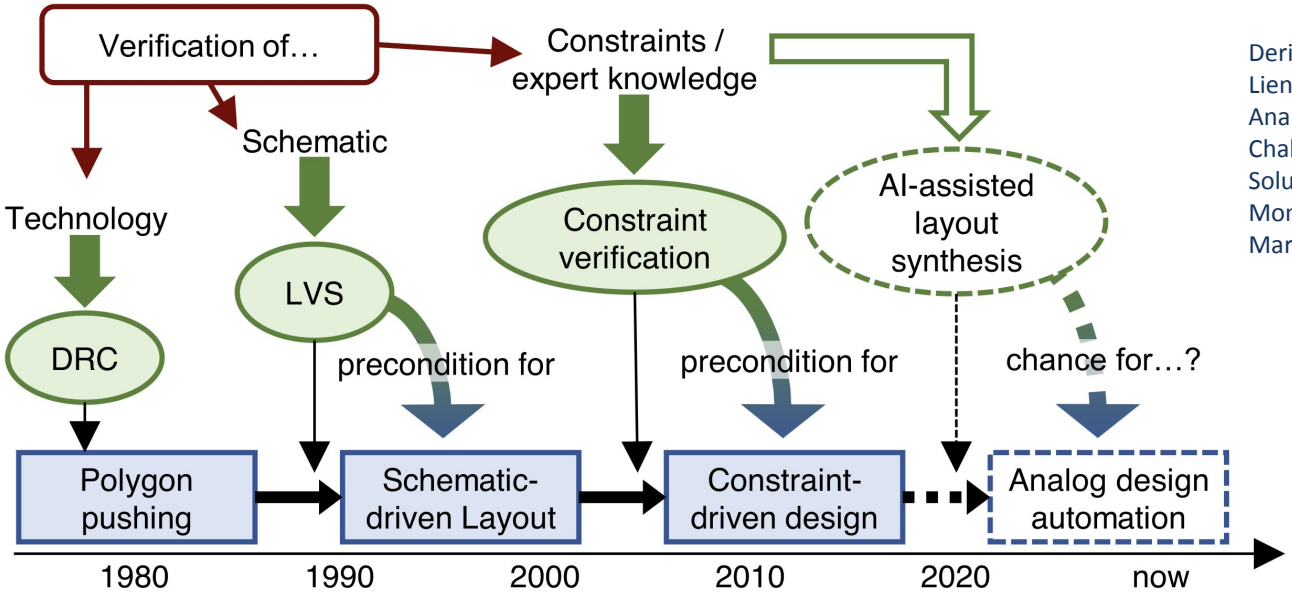


Analog Design Automation (2000 – Present)

Around 2000, Lienig expanded his research to analog design automation hindered by complex constraints: paradigm shift from schematic-driven design toward **constraint-driven design**

Context and Timeline

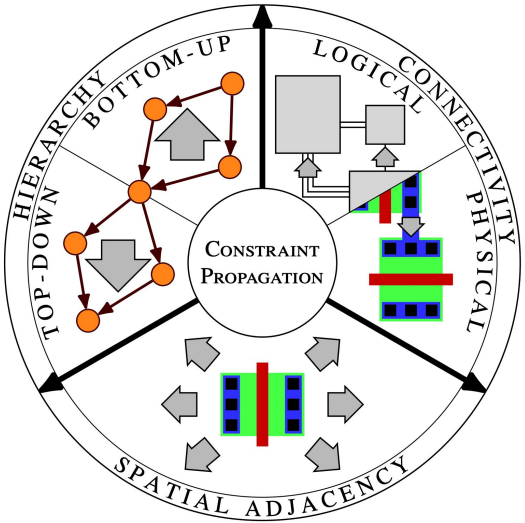
- Analog design was (and remains) more difficult than digital design: complex constraints
- Proposed a paradigm shift from schematic-driven layout toward constraint-driven design



Derived from: J. Scheible, J. Lienig. Automation of Analog IC Layout – Challenges and Solutions, Proc. ISPD'15, Monterey, CA, pp. 33-40, March 2015.

Constraint-Driven Analog Design

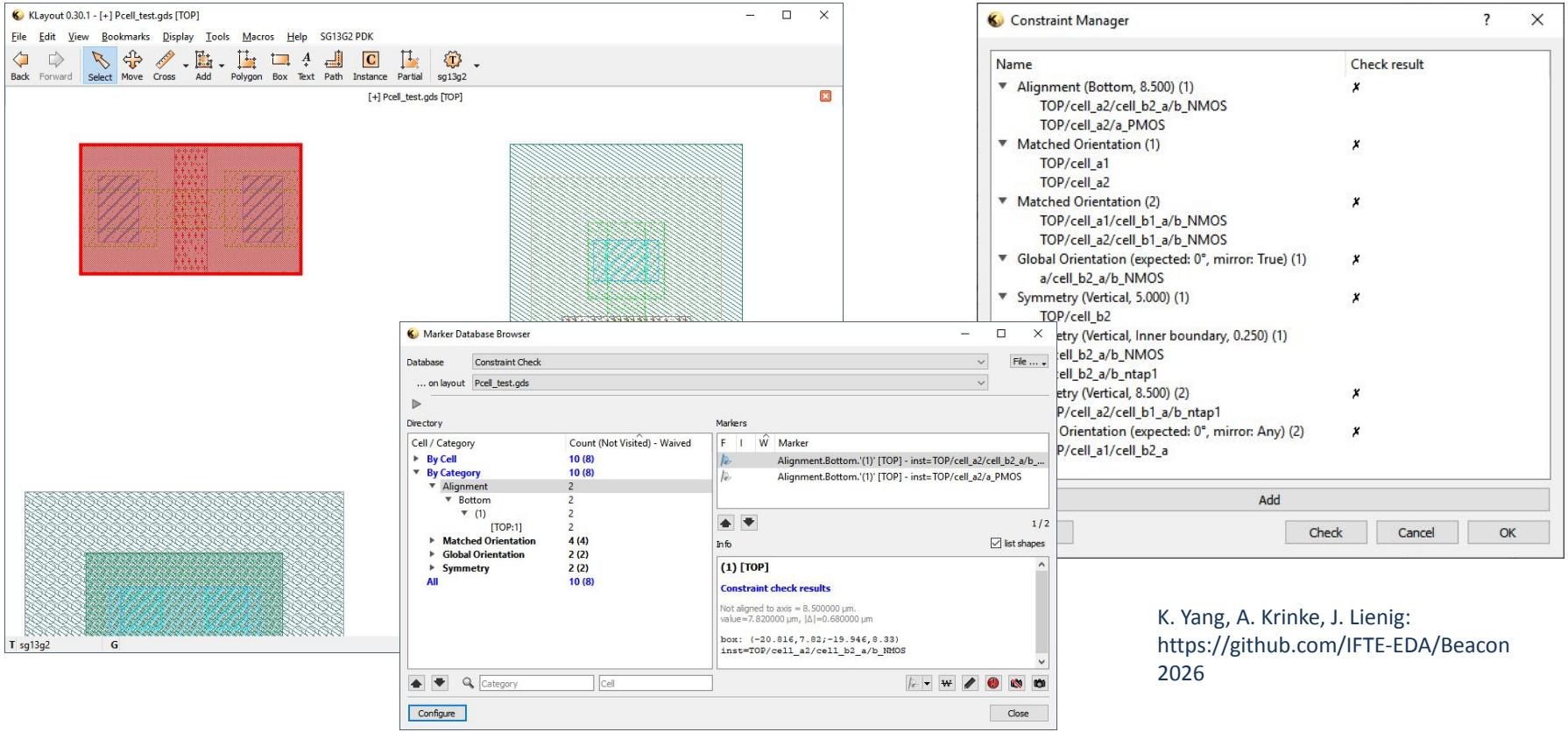
Involves formal definition, propagation, and verification of constrainst, to ensure requirements are met throughout the design flow



A. Krinke, G. Jerke, J. Lienig, Constraint Propagation Methods for Robust IC Design, GMM-Fachbericht 83, VDE Verlag, pp. 7-14, Sept. 2015

G. Jerke, J. Lienig, Constraint-driven Design - The Next Step Towards Analog Design Automation, in Proc. ISPD'09, pp. 75-82, 2009

Constraint-Driven Design with Open-Source Tools



K. Yang, A. Krinke, J. Lienig: https://github.com/IFTE-EDA/Beacon 2026

Analog Design with Open-Source Tools

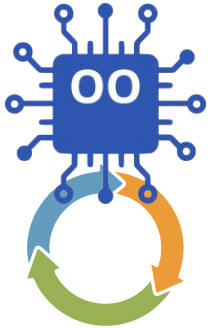
Open
Design Rule Format

Automatic Generation of
Design Manuals

R. Fischbach, A. Krinke, J. Lienig, research project DI-Meta-X, funded by BMFTR under grant 16ME0973K

Schematic-driven Layout
with **OpenOrchestrator**

Automatic Generation &
Verification of **DRC Runsets**



Calibre4KLayout

PyCell Editor

Constraint-driven
Layout Design

M. Paulenz, A. Krinke, J. Lienig, OpenOrchestrator: Schematic-Driven Layout with Open-Source EDA Tools, to be presented at Free Silicon Conference (FSiC), 2026

Electromigration-Aware Physical Design (2000 – Present)

Work began during Lienig's time in industry at Robert Bosch GmbH (1999–2002) and continues to be a primary research focus today:

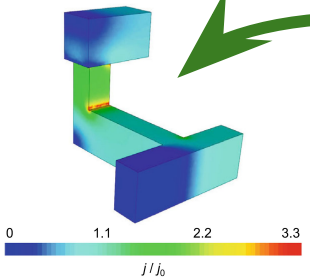
– Current-density verification and interconnect optimization (for analog circuits, integrated into commercial flows)

– Around 2017, shift to physics-based models (for precise assessment of interconnects)

– EM-aware routing, characterization of stress evolution models

R&D Approach for EM-Aware Physical Design

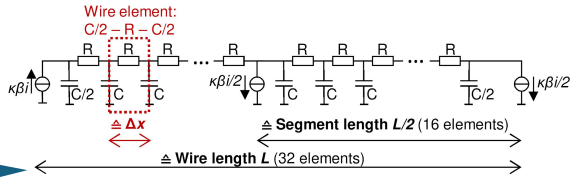
Current-density Simulation



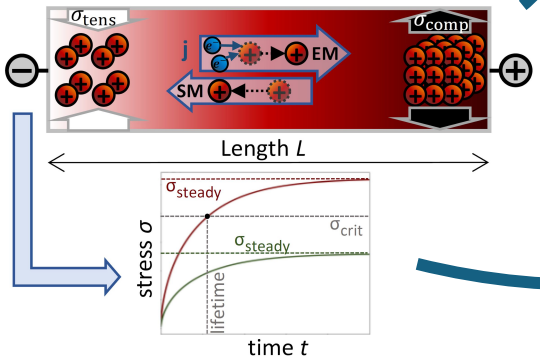
Semiconductor Industry

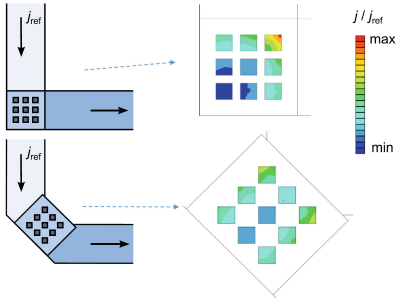
Technology Characterization

Designer-friendly Interconnect Verification

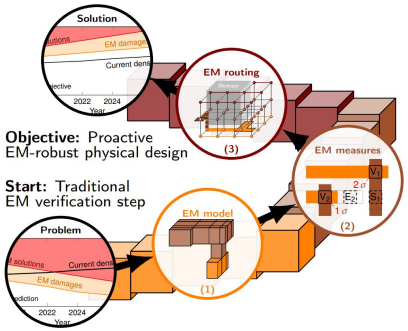


Physics-based Models





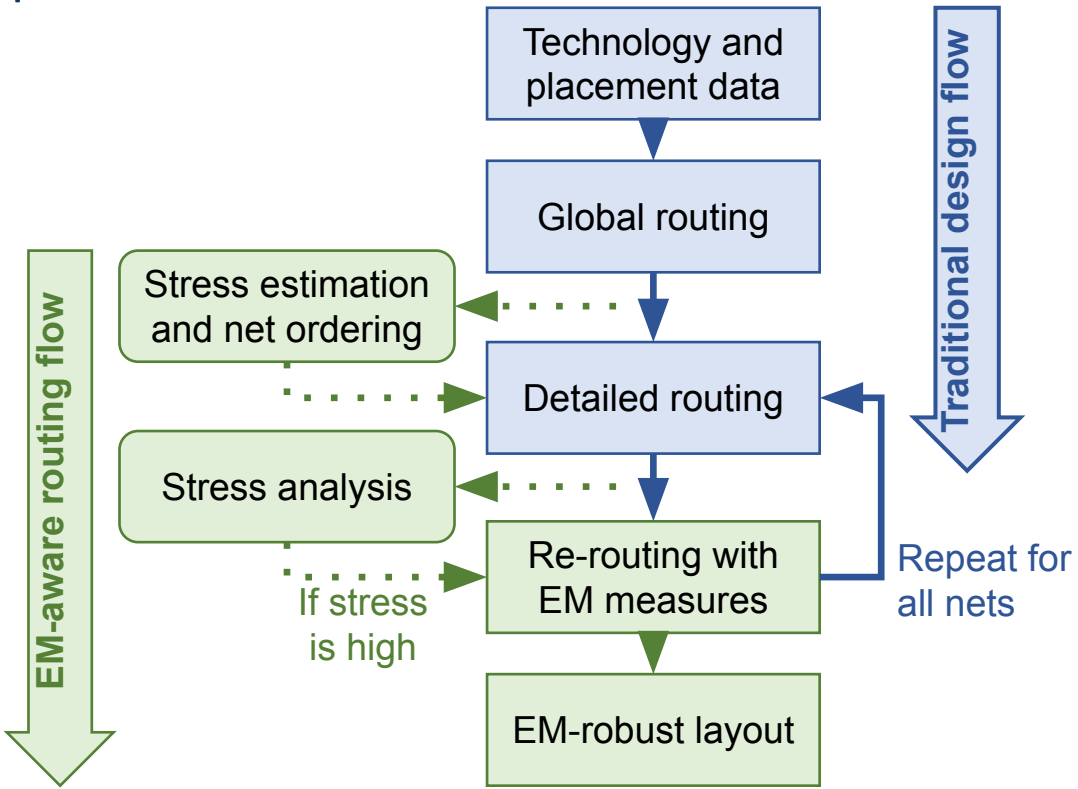
Interconnect Optimization



EM-robust Routing

EM Robustness from Design Perspective

- Design stages for EM consideration:
  - **Routing Proactive mitigation**
  - Verification Finding violations
  - Repair Fixing violations
- Two parallel approaches: avoidance vs. repair



S. Bigalke, J. Lienig, Avoidance vs. Repair: New Approaches to Increasing Electromigration Robustness in VLSI Routing, Integration, the VLSI Journal, vol. 65, ISSN 0167-9260, June 2020, DOI: 10.1016/j.vlsi.2020.04.009

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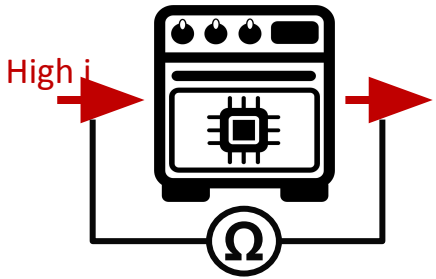
Prerequisite: Model parameter characterization



Physics-based models

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\underbrace{\frac{DB\Omega}{k_B T}}_{=\kappa}\left(\frac{\partial \sigma}{\partial x} - \underbrace{\frac{e\rho Z j}{\Omega}}_{=\beta j}\right)\right]$$

S. Rothe, J. Lienig, S. S. Sapatnekar, Temperature-aware Stress-based Migration Modeling in IC Design: Moving from Theory to Practice, AEU - International Journal of Electronics and Communications, 155909, ISSN 1434-8411, June 2025.

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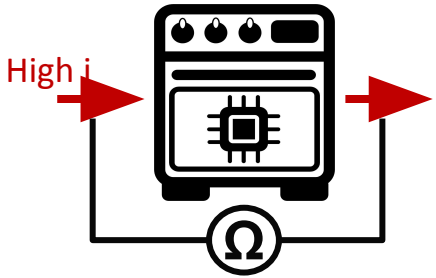

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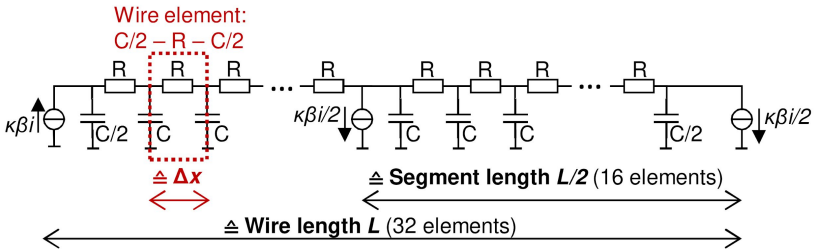
Designer-friendly modeling strategies



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System-Level Design Automation (2008 – Present)

As industry moved toward "More than Moore," Lienig fostered research and development system-level automation:

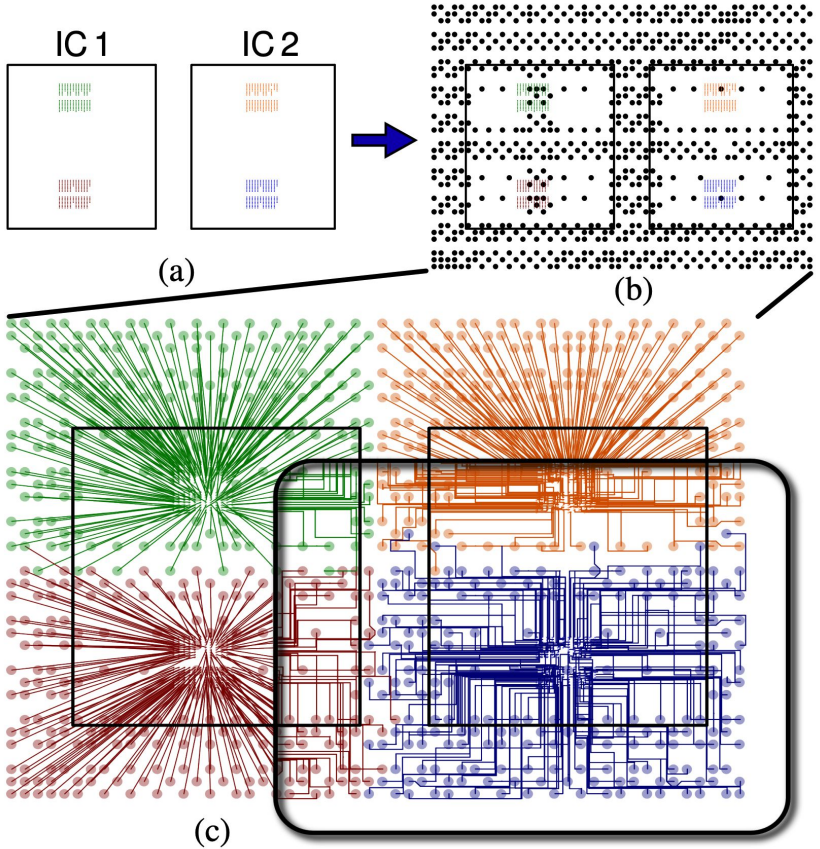
– Pin assignment and probabilistic routing models (to manage congestion across hierarchical systems)

– Data structures and floorplanning for 2.5D and 3D ICs

– WaferPlanner for chiplet integration

Pin Assignment

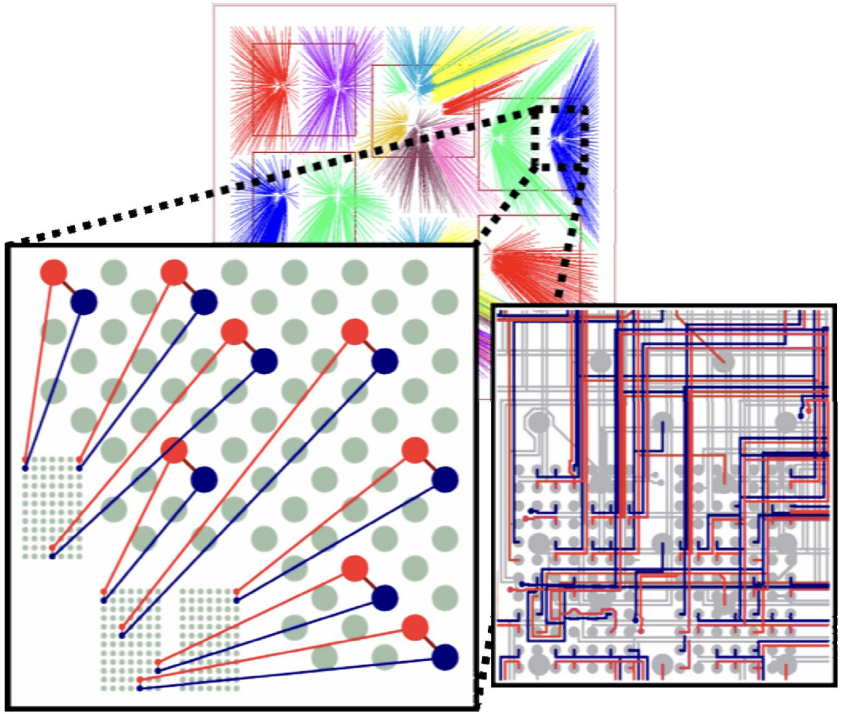
- Simultaneous consideration of interfaces across all hierarchy levels
- Optimization algorithms for pin assignment



T. Meister, J. Lienig, G. Thomke, Interface Optimization for Improved Routability in Chip-Package-Board Co-Design, Proc. 13th ACM/IEEE Int. Workshop SLIP 2011, San Diego, CA, pp. 1-8, June 2011.

Pin Assignment

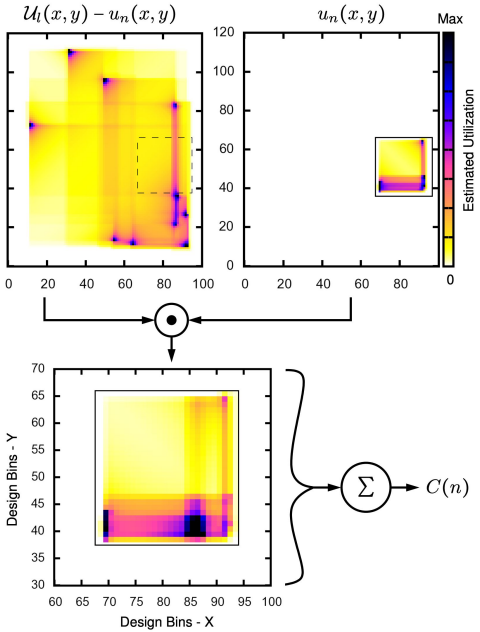
- Simultaneous consideration of interfaces across all hierarchy levels
- Optimization algorithms for pin assignment
- Supports differential pairs for signal integrity through pairings of pins
- Implemented in commercial design flow, along with routing prediction models

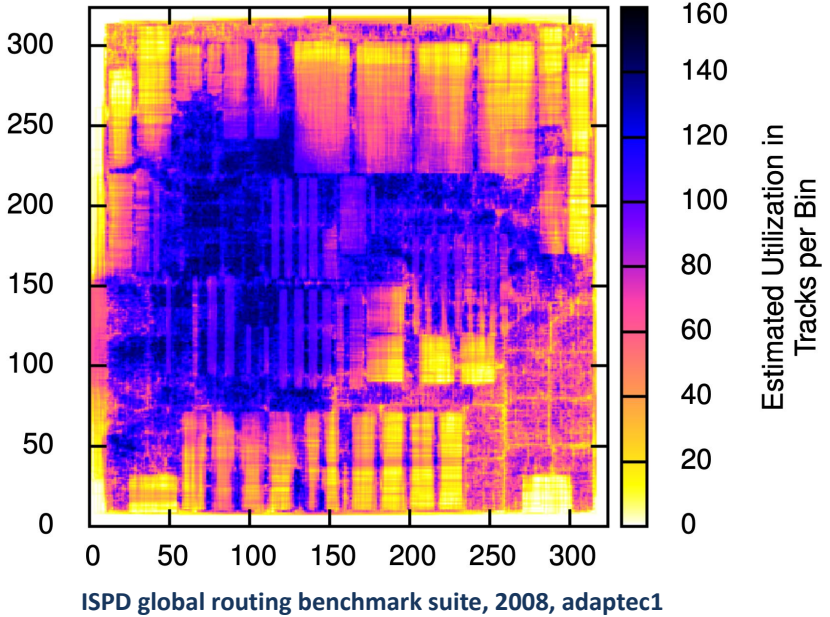


T. Meister, J. Lienig, G. Thomke, Universal Methodology to Handle Differential Pairs During Pin Assignment, Proc. 16th IFIP/IEEE VLSI-SoC 2008, Rhodes Island, Greece, pp. 347-352, Oct. 2008.

Routing Prediction

- Probabilistic models with heuristics for scalable routability assessment
  - Flexible consideration of routing patterns, detours, blockages, etc.
  - Additive and adaptive: built-in modeling of over-congested regions



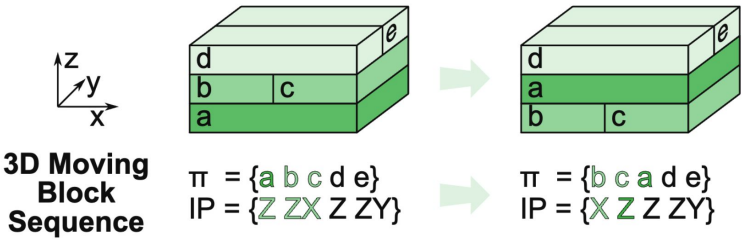


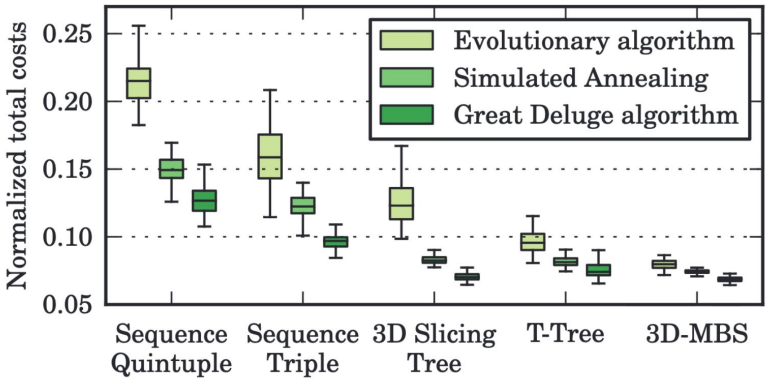
ISPD global routing benchmark suite, 2008, adaptec1

T. Meister, J. Lienig, G. Thomke, Interface Optimization for Improved Routability in Chip-Package-Board Co-Design, Proc. 13th ACM/IEEE Int. Workshop SLIP 2011, San Diego, CA, pp. 1-8, June 2011.

Data Structures and Floorplanning for 3D ICs

- Data structures are fundamental to design flows
  - Systematic investigation of 2D, 3D data structures
  - Development of advanced 3D data structures





R. Fischbach, J. Knechtel, J. Lienig, Utilizing 2D and 3D Rectilinear Blocks for Efficient IP Reuse and Floorplanning of 3D-Integrated Systems, Proc. ACM ISPD'13, Stateline, Nevada, pp. 11-16, March 2013.

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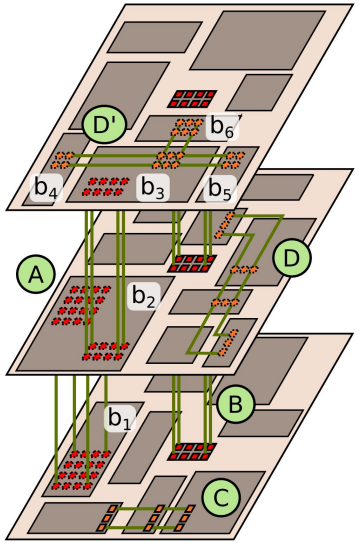
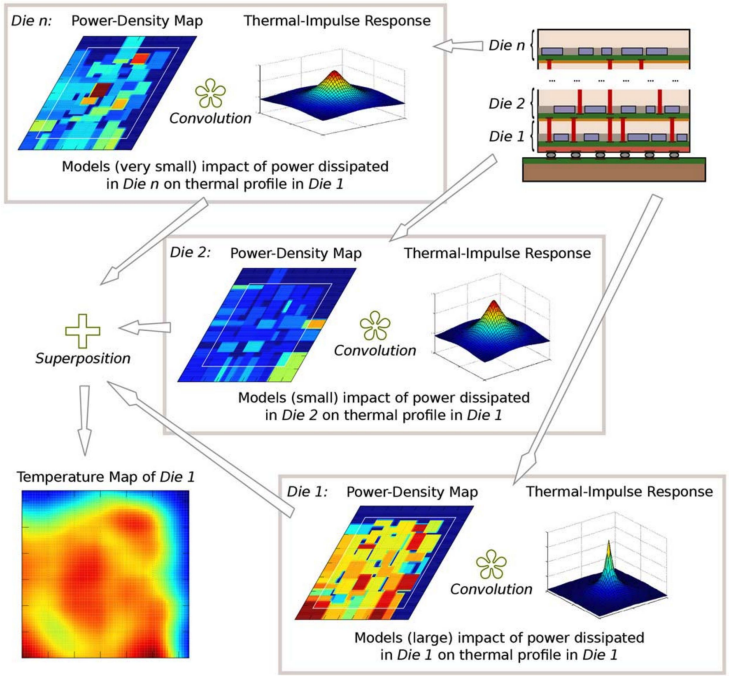
- Floorplanning for 3D ICs and 2.5D interposer
  - Multi-objective optimization: thermal management, power-domain planning, interconnects, etc.

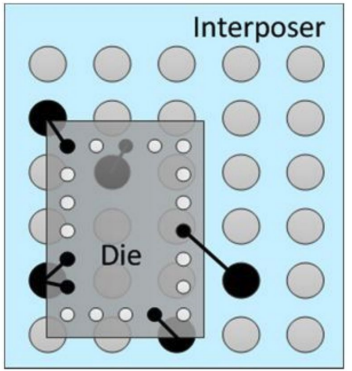


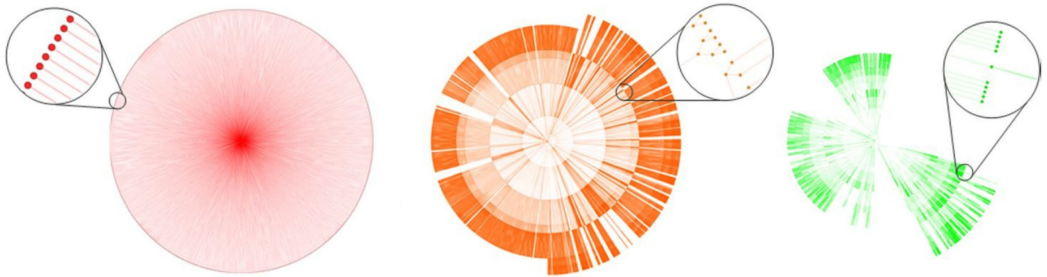


J. Knechtel, E. F. Y. Young, J. Lienig, Planning Massive Interconnects in 3D Chips, IEEE TCAD, vol. 34, no. 11, pp. 1808-1821, ISSN 02780070, Nov. 2015.

Data Structures and Floorplanning for 3D ICs

- Data structures are fundamental to design flows
  - Systematic investigation of 2D, 3D data structures
  - Development of advanced 3D data structures
- Floorplanning for 3D ICs and 2.5D interposer
  - Multi-objective optimization: thermal management, power-domain planning, interconnects, etc.
  - Efficient design-space exploration toward optimal chiplet placement





S. Osmolovskyi, J. Knechtel, I.L. Markov, J. Lienig, Optimal Die Placement for Interposer-Based 3D ICs, Proc. 23rd ASP-DAC, pp. 513-520, Jan. 2018

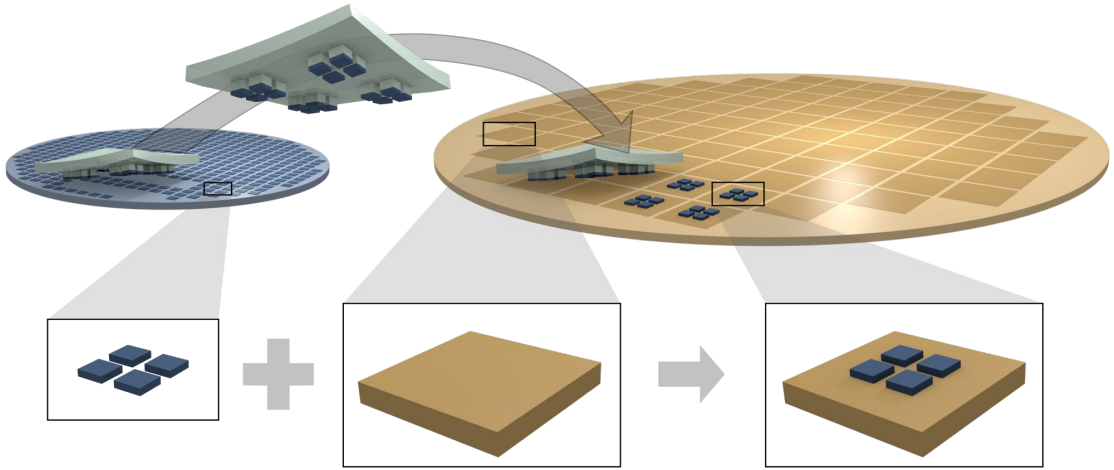
Brute Force
~$4{,}4 \cdot 10^{12}$ nodes
~43 days

Native Branch & Bound
263 million nodes
~10 min

Advanced B & B
350 thousand nodes
~0.25 sec

WaferPlanner for Stamp-Based Chiplet Integration

- Micro-transfer printing: elastomer stamp transfers dies from source to target wafers
  - Managing new cross-die/wafer-level dependencies: constraints induced by stamp and wafers
  - Die printing location has strong impact on utilization, yield at the wafer level



R. Fischbach, T. Horst, J. Lienig, A Graph-Based Model of Micro-Transfer Printing for Cost-Optimized Heterogeneous 2.5D Systems, Proc. 3DIC 2019, Sendai, Japan, Oct. 2019.

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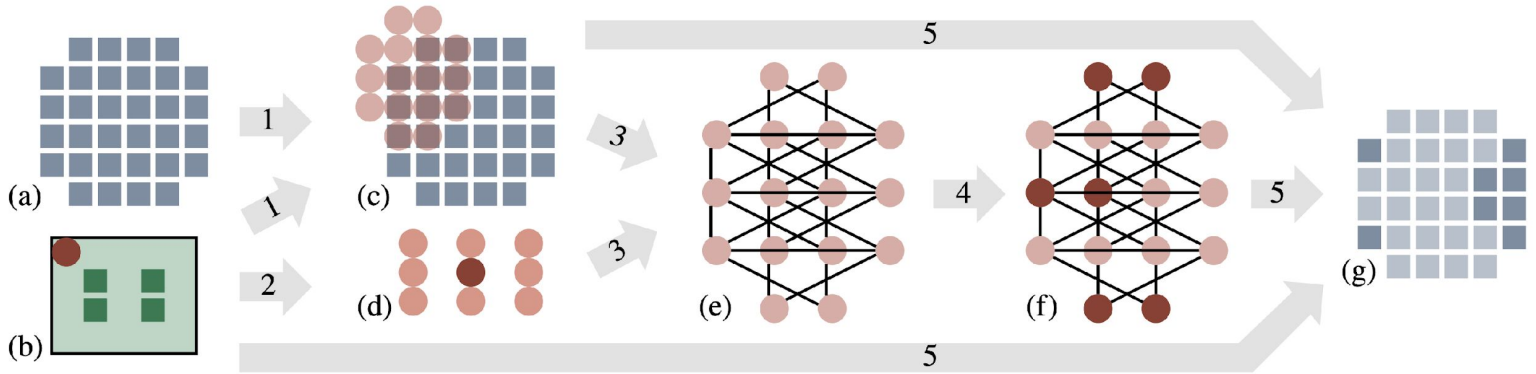
  - Managing new cross-die/wafer-level dependencies: constraints induced by stamp and wafers
  - Die printing location has strong impact on utilization, yield at the wafer level
- Graph-based modeling and optimization
  - Tool demonstrator with industry partners



R. Fischbach, T. Horst, J. Lienig, A Graph-Based Model of Micro-Transfer Printing for Cost-Optimized Heterogeneous 2.5D Systems, Proc. 3DIC 2019, Sendai, Japan, Oct. 2019.

Beyond: Further Domains and Technologies (2010 – Present)

Lienig and collaborators extended the notion of robustness and reliability to further domains:

– Thermal modeling and simulation

– Security closure of physical layouts

– Flexible printed circuits, automotive wiring

– Electronic systems design and precision engineering

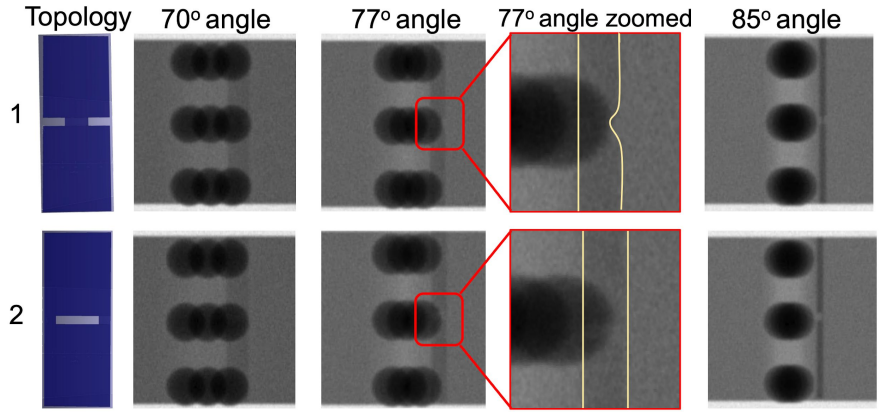
Security Closure of Physical Layouts

- Treat physical effects as potential attack surfaces
  - Transistor aging impacts delays; side-channel attacks
  - Migration effects-based Trojans in interconnects

J. Lienig, S. Rothe, M. Thiele, N. Rangarajan, M. Nabeel, H. Amrouch, O. Sinanoglu, J. Knechtel, Toward Security Closure in the Face of Reliability Effects, Proc. ICCAD, 2021

Security Closure of Physical Layouts

- Treat physical effects as potential attack surfaces
  - Transistor aging impacts delays; side-channel attacks
  - Migration effects-based Trojans in interconnects
  - Elevated risks in advanced packages



K. Yahyaei, S. Rothe, M. Vawoo Dawood Naina, A. Roy, M. Shafkat, M. Khan, O. Sinanoglu, J. Lienig, J. Knechtel, N. Asadizanjani, Lurking in the Shadows: Challenges for X-Ray Inspection to Uncover Electromigration-Based Hardware Trojans in Advanced Packaging, Proc. IEEE 2025 Int. Conf. on Physical Assurance and Inspection of Electronics (PAINE 2025)

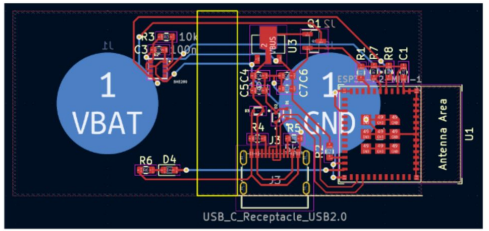
Security Closure of Physical Layouts

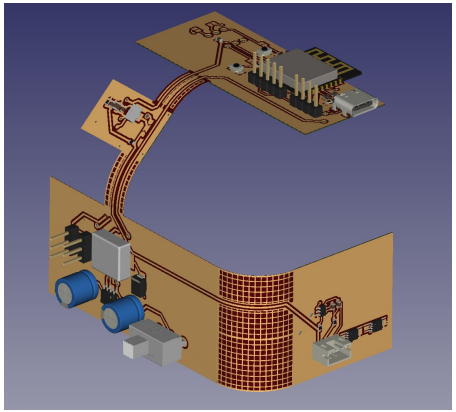
- Treat physical effects as potential attack surfaces
- Extend design flows to hinder exploitation of reliability mechanisms; clear synergies with reliability-aware design
  - Aging-aware logical and physical synthesis
  - Migration-aware routing rules and algorithms
  - Inspection-aware design of advanced packages, e.g., routing keep-out zones under microbumps
  - Layout compaction (against digital Trojans)

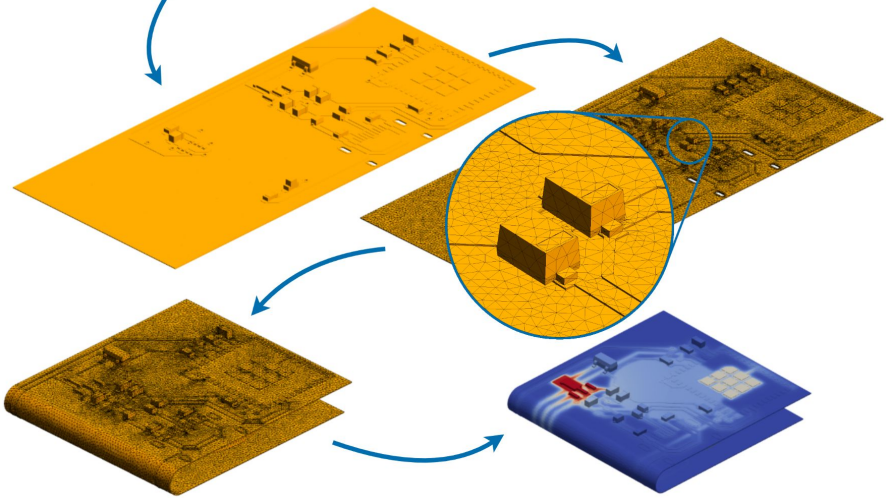
J. Lienig, S. Rothe, M. Thiele, N. Rangarajan, M. Nabeel, H. Amrouch, O. Sinanoglu, J. Knechtel, Toward Security Closure in the Face of Reliability Effects, Proc. ICCAD, 2021

Modeling and Simulation of Flexible Electronics

- Complete design flow based on open-source tools
- Starting from classical 2D PCB design in KiCad
  - Additional definition of bends and angles
  - Maintain interfaces between components
- Transformation into 3D bent meshes
  - Ready for FEM simulation



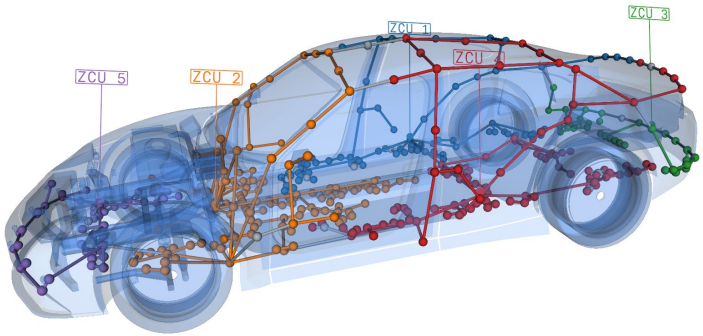


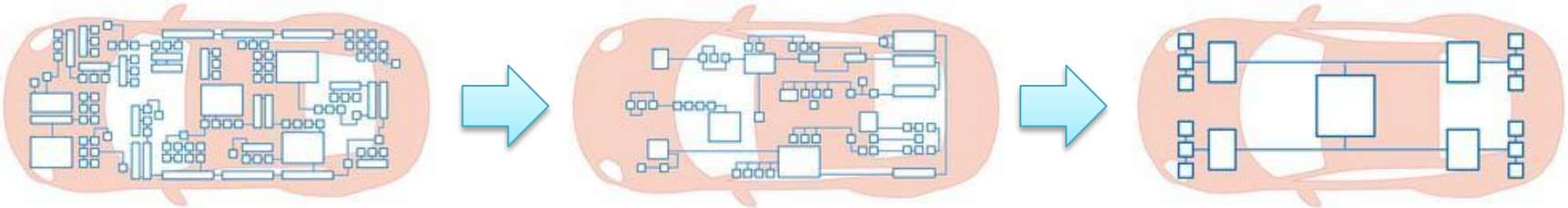


N. Arnold, A. Krinke, M. Dietrich, J. Lienig, An Open-Source Tool for FEM Modeling of Bent Flexible Circuits, IEEE Journal on Flexible Electronics, vol. 4, no. 8, pp. 333-341, Aug. 2025.

Architecture Planning of Automotive Wiring Harnesses

- Challenges:
  - Number and locations of zone controllers?
  - Assignment of components to zone controllers?
- ARANEA: Efficient architecture planning tool, based on EDA experiences
  - Optimal routing
  - Creation of zonal architectures by partitioning





P. Näke, F. Stein, A. Krinke, J. Lienig, Efficient Architecture Evaluation and Generation of Automotive Wiring Harnesses, Proc. of the IEEE Transportation Electrification Conf. and Expo, Asia-Pacific (ITEC Asia-Pacific), Singapur, pp. 1-5, November 2025.

Electronic Systems Design and Precision Engineering at IFTE

Custom devices for heating and cooling

Innovative LED systems

Medical devices

Mechanical devices and integration solutions

Pictures from www.ifte.de

Technische Universität Dresden

ifte

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Education and Textbooks (2002 – Present)

Lienig dedicated himself to teaching algorithms and physical realities to generations of students:

– Reformed the curriculum at IFTE

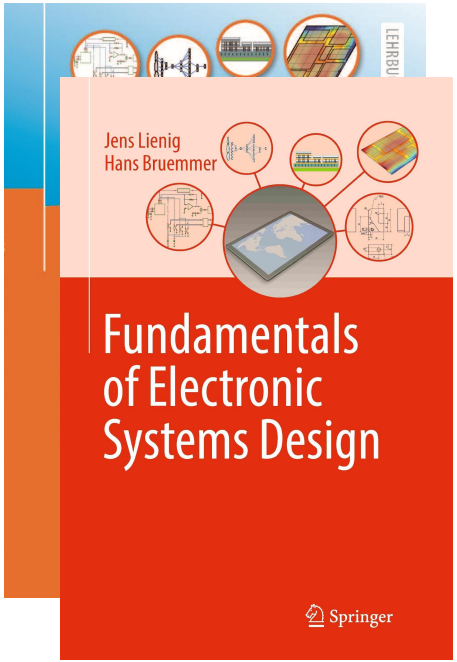
– Led and co-authored several foundational textbooks

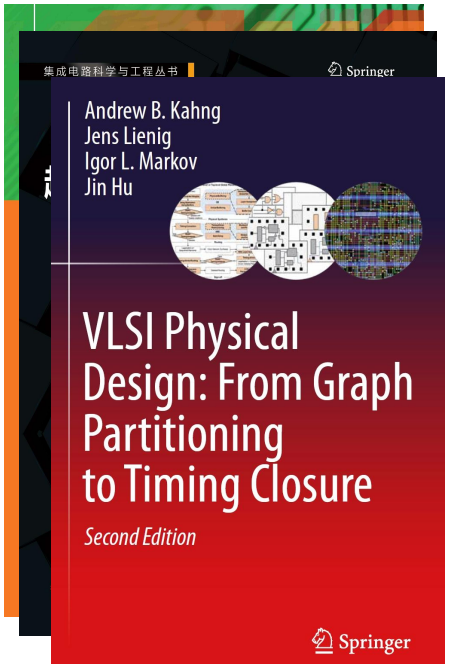
Reformed Curriculum

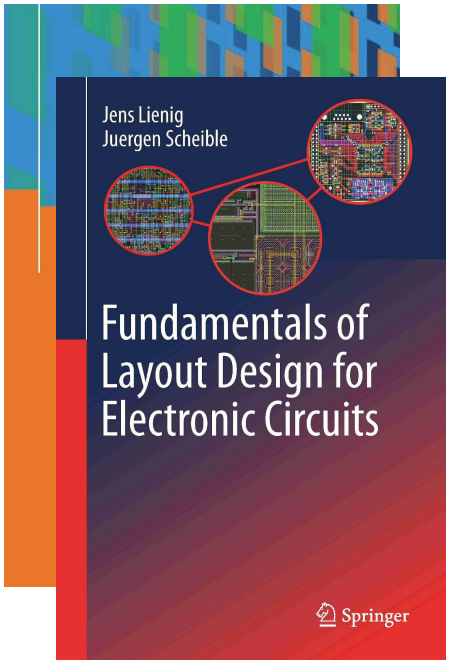
- Integrated electronic design education with systems design and precision engineering
- Program spans from undergraduate level to advanced electives.
- Covers both theory and practical experience in CAD, PCB design, and IC layout synthesis

Textbooks

- Several foundational textbooks, defining modern physical design curriculum
- Guides readers to understand algorithms and physics problems behind design efforts







Textbooks

- Several foundational textbooks, defining modern physical design curriculum
- Guides readers to understand algorithms and physics problems behind design efforts

Conclusion

Jens Lienig's Contributions to Advance Physical Design

- His commitment to grounding algorithmic abstractions in the physical realities, underpinned by industrial collaborations, enabled real-world advances.
- He pioneered vital paradigm shifts for reliable and robust design, primarily through constraint-driven analog design and electromigration-aware design.
- He demonstrated foresight in tackling system-level complexities for robust design, for both classical and emerging applications.
- Through his leadership, mentorship, and comprehensive textbooks, he has codified the principles of robust physical design for the next generation of engineers.

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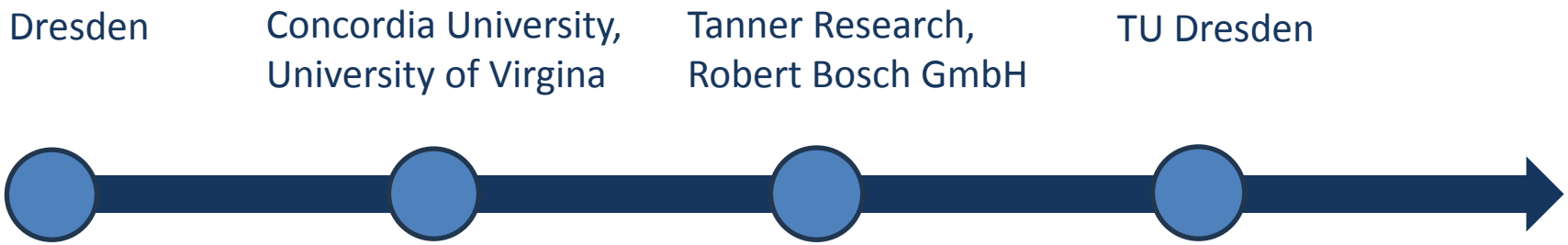
Congratulations to Prof. Jens Lienig for the ISPD 2026 Lifetime Achievement Award !

Biographical Sketch



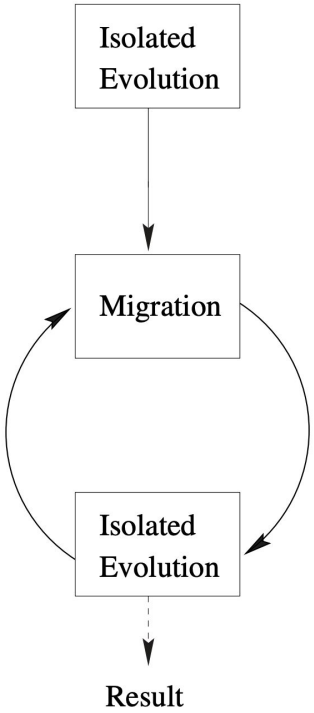
Evolutionary Algorithms (1990s)

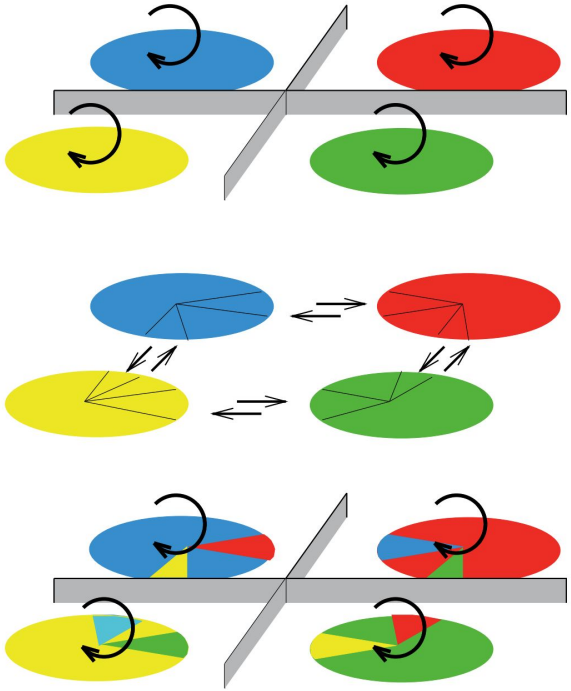
During the first decade of his career, Lienig applied nature-inspired techniques to solve NP-hard routing problems through:

– GASBOR (Genetic Algorithm for Switchbox Routing)
– Multi-objective optimization, crosstalk minimization
– Handling of multi-chip modules
– Parallelization efforts, **“island model”**

Island Model for Evolutionary Routing Algorithms

- Distributed genetic algorithms
- Sub-populations (islands) evolve independently
  - Preserves genetic diversity

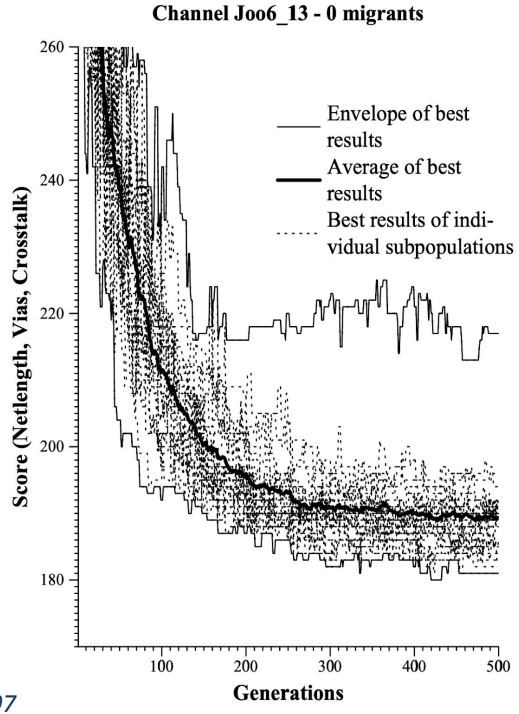


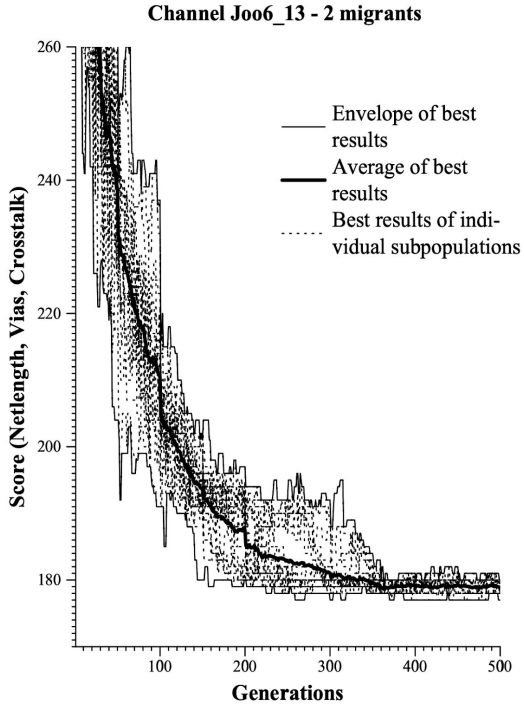


J. Lienig, Physical Design of VLSI Circuits and the Application of Genetic Algorithms, E*volutionary Algorithms in Engineering Applications, Springer, 1997*

Island Model for Evolutionary Routing Algorithms

- Distributed genetic algorithms
- Sub-populations (islands) evolve independently
  - Preserves genetic diversity
  - Prevents premature converging to local optima

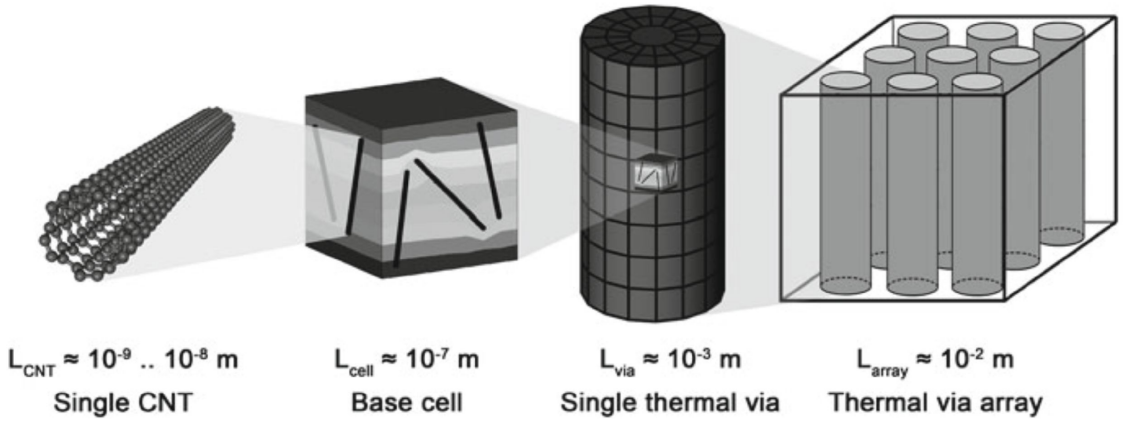




J. Lienig, Physical Design of VLSI Circuits and the Application of Genetic Algorithms, E*volutionary Algorithms in Engineering Applications, Springer, 1997*

Thermal Analysis for Carbon Nanotubes

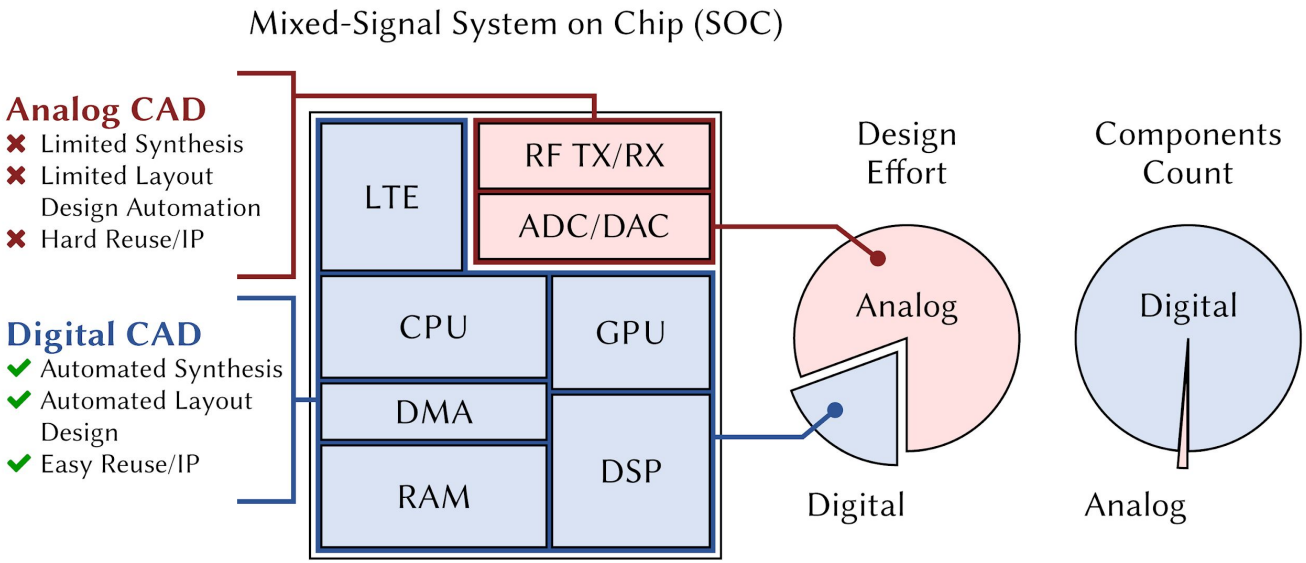
- Thermal vias are essential for dense integration, e.g., in 3D stacks
- Carbon nanotubes and composites allow for excellent heat conduction
- Hierarchical modeling approach for various technological configurations



J. Hertwig, H. Neubert, J. Lienig, A Hierarchical Modeling Approach of Thermal Vias Using CNT-Based Composites. In: Bio and Nano Packaging Techniques for Electron Devices, Springer, 2012

Context and Timeline

- Analog design was (and remains) more difficult than digital design: complex constraints



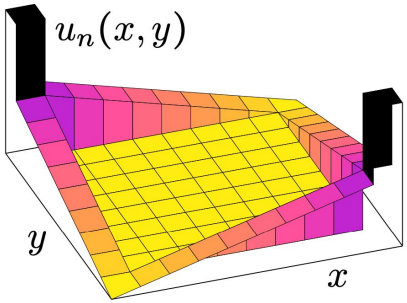
Derived from: N. Lourenço, R. Martins, N. Horta, Automatic Analog IC Sizing and Optimization Constrained with PVT Corners and Layout Effects, Springer 2016

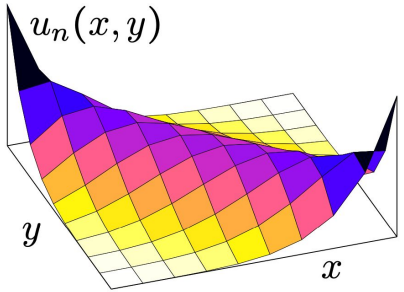
Constraint-Driven Analog Design: Examples

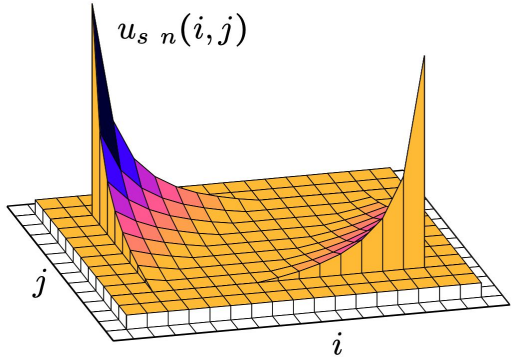
G. Jerke, J. Lienig,
Constraint-driven Design - The Next Step Towards Analog Design Automation, in Proc. ISPD'09, pp. 75-82, 2009

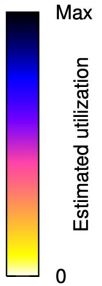
Routing Prediction

- Probabilistic models with heuristics for scalable routability assessment
  - Flexible consideration of routing patterns, detours, blockages, etc.





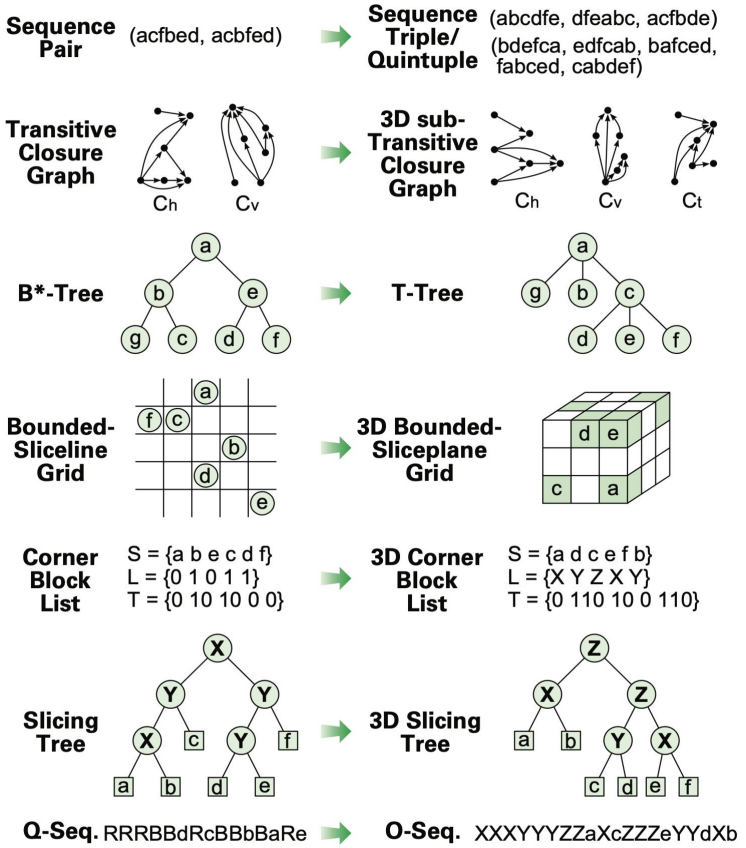




T. Meister, J. Lienig, G. Thomke, Interface Optimization for Improved Routability in Chip-Package-Board Co-Design, Proc. 13th ACM/IEEE Int. Workshop SLIP 2011, San Diego, CA, pp. 1-8, June 2011.

Data Structures and Floorplanning for 3D ICs

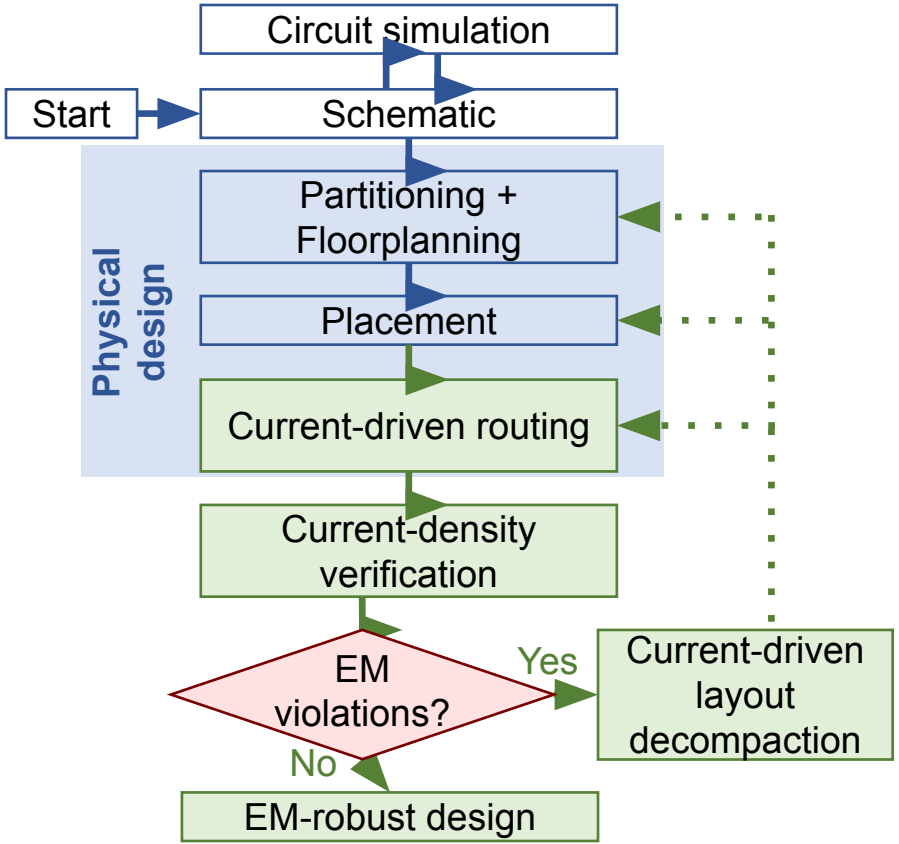
- Data structures are fundamental to design flows
  - Systematic investigation of 2D, 3D data structures



R. Fischbach, J. Lienig, T. Meister, From 3D Circuit Technologies and Data Structures to Interconnect Prediction, Invited Talk, Proc. 2009 Int. Workshop SLIP, San Francisco, CA, pp. 77-84, July 2009.

EM Robustness from Design Perspective

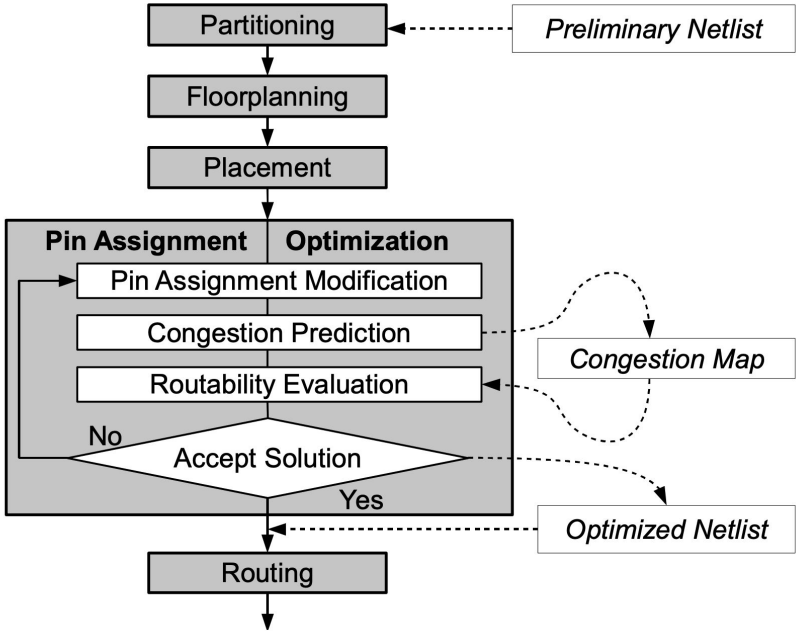
- Design stages for EM consideration:
  - Routing Proactive mitigation
  - Verification Finding violations
  - Repair Fixing violations
- Two approaches:
  avoidance vs. repair
- Underlying strategies can be transferred to physics-based EM modeling



J. Lienig, Introduction to Electromigration-Aware Physical Design, Invited Talk, Proceedings of the International Symposium on Physical Design (ISPD'06), San Jose, CA, pp. 39–46, April 2006.

Routing Prediction

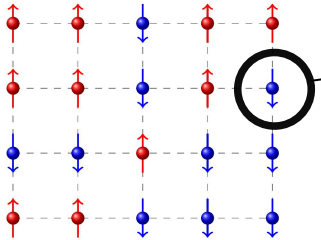
- Probabilistic models with heuristics for scalable routability assessment
  - Flexible consideration of routing patterns, detours, blockages, etc.
  - Additive and adaptive: built-in modeling of over-congested regions
- Combined with pin assignment for hierarchical systems
  - Integrated into commercial design flows

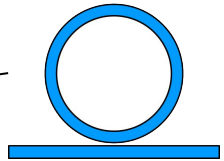


T. Meister, J. Lienig, G. Thomke, Interface Optimization for Improved Routability in Chip-Package-Board Co-Design, Proc. 13th ACM/IEEE Int. Workshop SLIP 2011, San Diego, CA, pp. 1-8, June 2011.

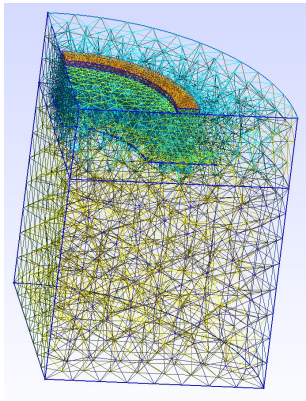
Thermal Analysis for Coherent Ising Machines

Spatially Multiplexed CIM





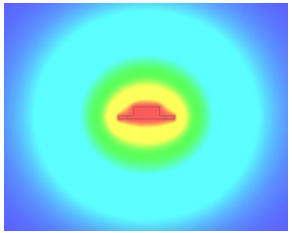
Microring Oscillator



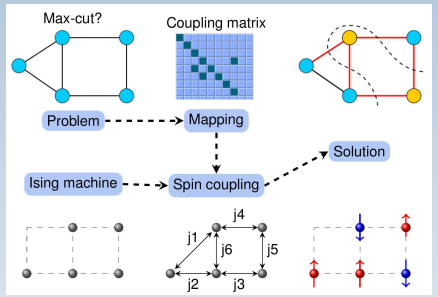
Simulation Model

Design rules

Scaling



Thermal Simulation



Solver for complex mathematic problems

M. Thiele, J. Lienig, M. He and K. Jamshidi: Thermal Modeling of Silicon Photonic Waveguides, Proc. SMACD 2025, Istanbul, Turkiye, Jul 2025.

Reformed Curriculum

- Integrated electronic design education with systems design and precision engineering
- Program spans from undergraduate level to advanced electives, providing students with both theory and practical experience in CAD, PCB design, and IC layout synthesis

Textbooks

- Several foundational textbooks, defining modern physical design curriculum
- For readers to understand both the algorithms and physics problems behind design efforts