A History of Influences

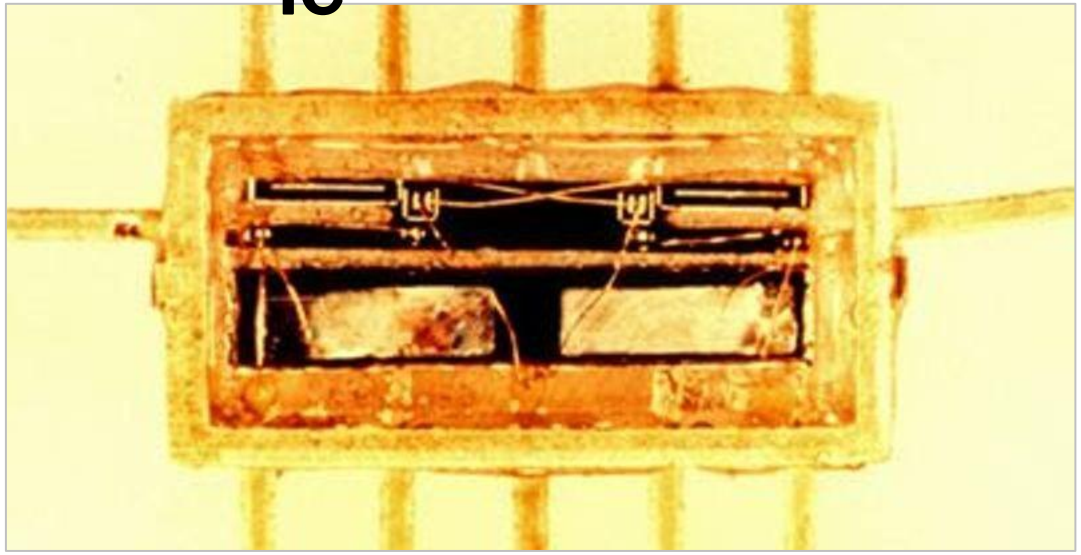
Jürgen Scheible, Reutlingen University

A Tribute to Jens Lienig

The Birth of Microelectronic

Electronics & Drives
Reutlingen University

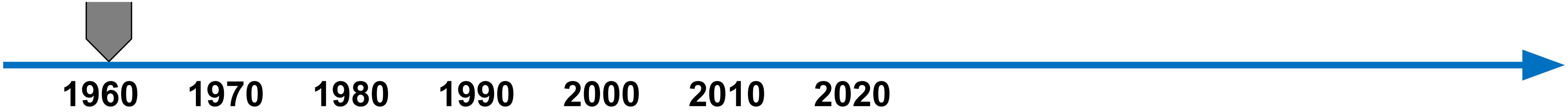
First commercial IC



1960

Type 502: „Bistable Multivibrator Solid Circuit“

Texas Instruments (Jack Kilby)



Two German Engineers

Electronics & Drives

Reutlingen University

Jens

Jürgen

Bor
n

1960 1970 1980 1990 2000 2010 2020

A History of Influences

Electronics & Drives

Reutlingen University

Jens

Jürgen

Study of Electrical Engineering

PhD in Physical Design Automation

TECHNISCHE UNIVERSITÄT DRESDEN

Universität (TH) Karlsruhe

Germany

Born

Early Years

1960 1970 1980 1990 2000 2010 2020

Two German Engineers

Electronics & Drives

Reutlingen University

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Study of Electrical Engineering

PhD in Physical Design Automation

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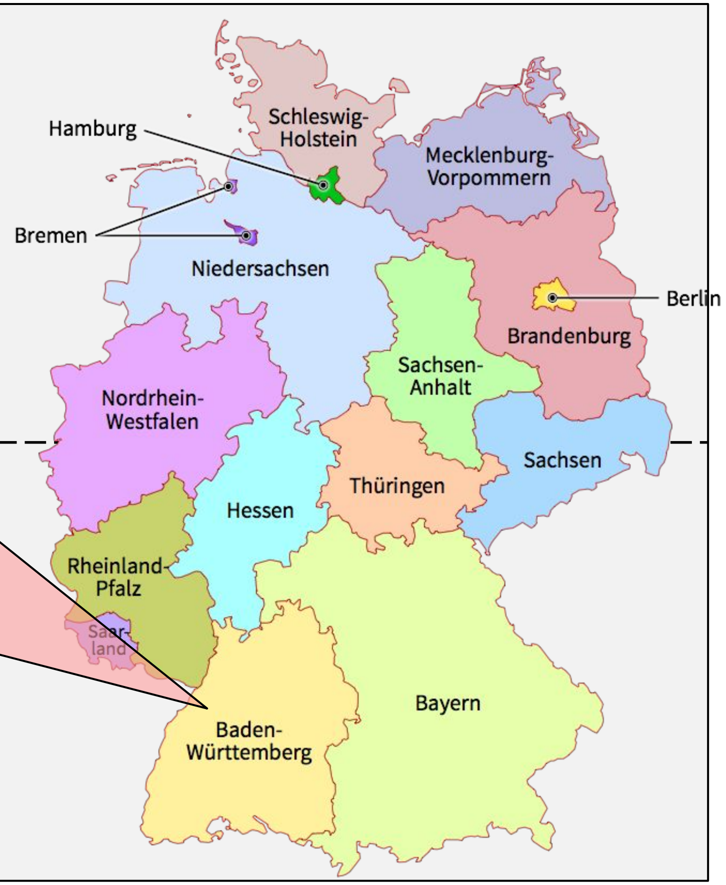

Early Years

1960 1970 1980 1990 2000 2010 2020

Two German Engineers

Electronics & Drives
Reutlingen University

Jens

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Study of Electrical Engineering

PhD in Physical Design Automation


FORTSCHRITT-BERICHTE VDI

Dipl.-Ing. Jens Lienig, Dresden

Ein Verdrahtungssystem für den rechnergestützten Layoutentwurf von Multichipträgern

Reihe 9: Elektronik

Nr. 119

VDI VERLAG

Routing Strategies for the Computer-Aided Design of Multi-Chip Modules

Concepts of genetic algorithms


FORTSCHRITT-BERICHTE VDI

Dipl.-Ing. Jürgen Scheible, Karlsruhe

Ein Softwarepaket zur vollautomatischen Plazierung von Bauteilen auf Leiterplatten für den industriellen Einsatz

Reihe 20: Rechnerunterstützte Verfahren

Nr. 59

VDI VERLAG

Autoplacement Package for Industrial PCB-Layout

Born

Early Years

1960 1970 1980 1990 2000 2010 2020

Two German Engineers

Electronics & Drives

Reutlingen University

Jens

Jürgen

Study of Electrical Engineering

PhD in Physical Design Automation

Postdoc

Assistant

Lead

EDA

Toolmanager

Concordia University Montréal,

University of Virginia Charlottesville, VA, USA

Tanner Research Pasadena, CA, USA

Habilitation 1996:
Evolutionary Algorithms Applied to VLSI Physical Design

P&R for standard cells, interfaces

- **Trainee**
- **ASIC Layout Designer**
- **Project Manager Layoutflow**
- **Group Manager EDA Tools**
- **Head of Dept. IC Layout**

BOSCH

Automotive Electronics

Born

Early Years

Industrial Years

1960 1970 1980 1990 2000 2010 2020

What is Automotive Electronics?

Electronics & Drives
Reutlingen University

Modern cars contain

- 100 ECUs
- > 1000 chips

Safety critical systems

Active

- Brake-by-wire
- Steer-by-wire
- Drive-by-wire

Passive

- Airbags, seat belts
- ABS, ESP

Covenience features

- Adaptive cruise control
- High beam assist
- Auto steering

Automotive Electronics

Electronics & Drives
Reutlingen University

Two major Challenges

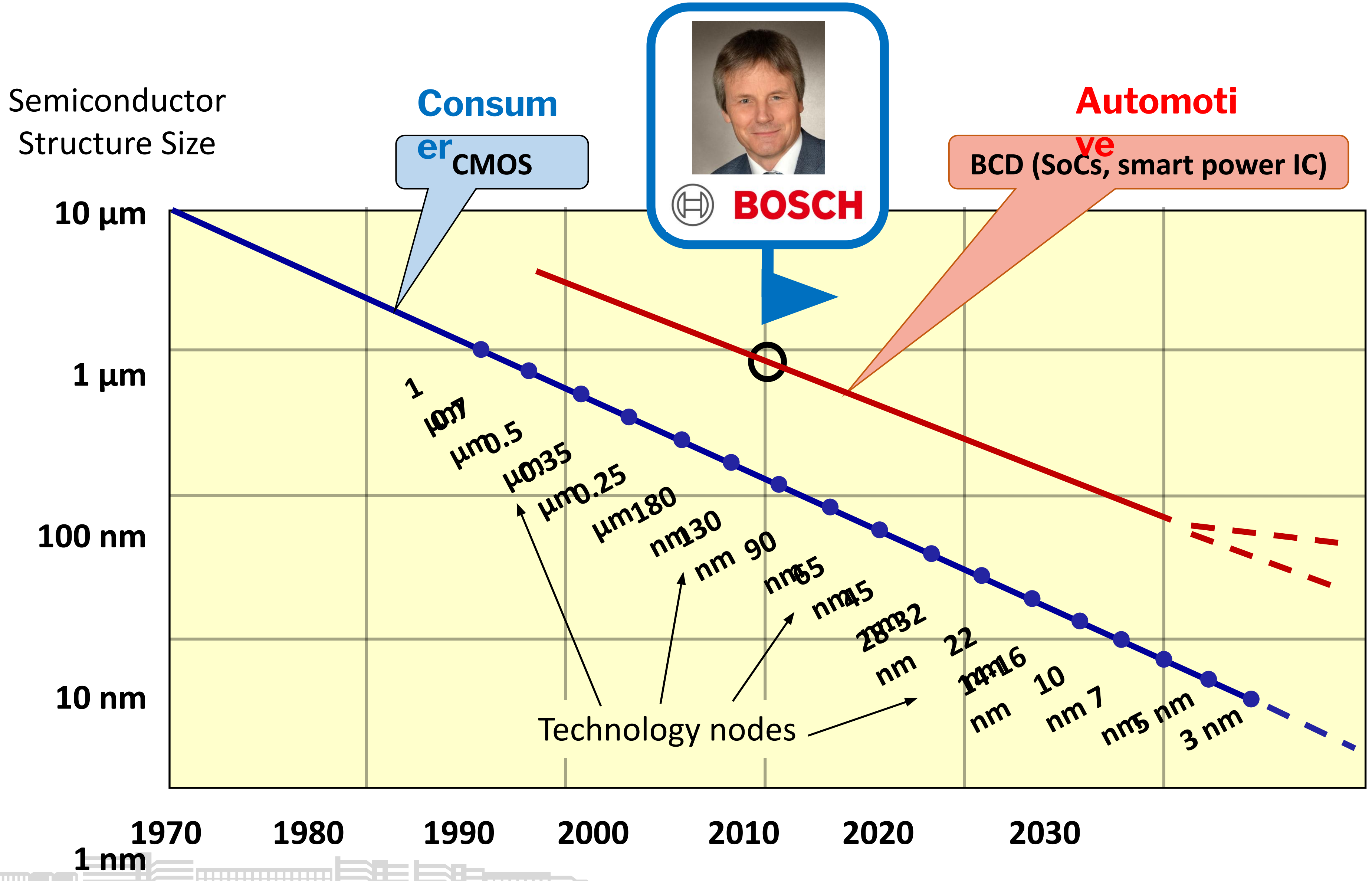
Reliability

Analog Design

Technology Roadmaps: Consumer vs. Automotive

Electronics & Drives

Reutlingen University



Automotive Electronics

Electronics & Drives
Reutlingen University

Two major Challenges

Reliability

Analog Design

Requirements for Automotive Electronics

Electronics & Drives

Reutlingen University

Automotive

Temperature range	-40 °C ... +165°C
Lifetime	10 – 15 years
Vibration	0–2000 Hz
Acceleration	500 m/s²
ESD safety	up to 15 kV
Acceptable field failures	Goal: zero failure
Failure documentation (effect / cause)	yes
Long-term supply	up to 30 years

Very harsh environment al conditions

Long service life

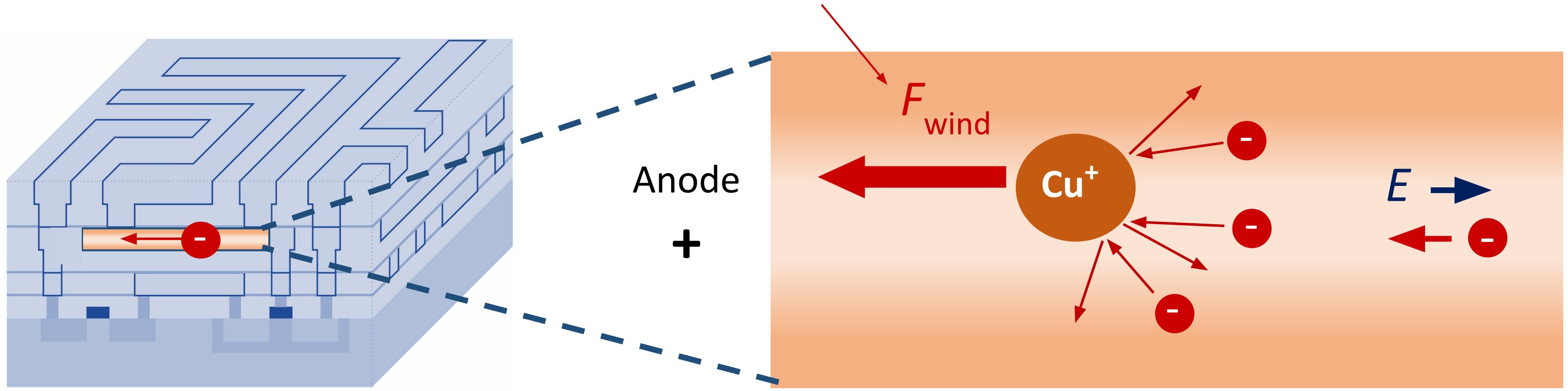
Extreme reliability requirements (zero failure)

Source: Volkswagen

Electromigration (EM)

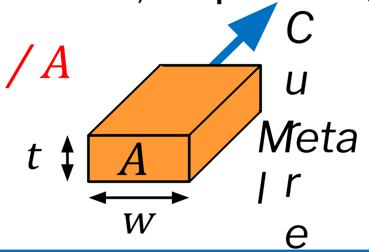
Electronics & Drives
Reutlingen University

Force on metal ions (Cu^+)
resulting from momentum transfer
from the conduction electrons



Above a critical current density j_{crit}, the atoms **migrate** in a metal conductor, depending on

- Current density $j = I / A$
- Temperature T



Black's equation

$$MTF = \frac{a}{j^n} \cdot \exp\left(\frac{E_a}{k \cdot T}\right)$$

Const. (a, E_a, k)

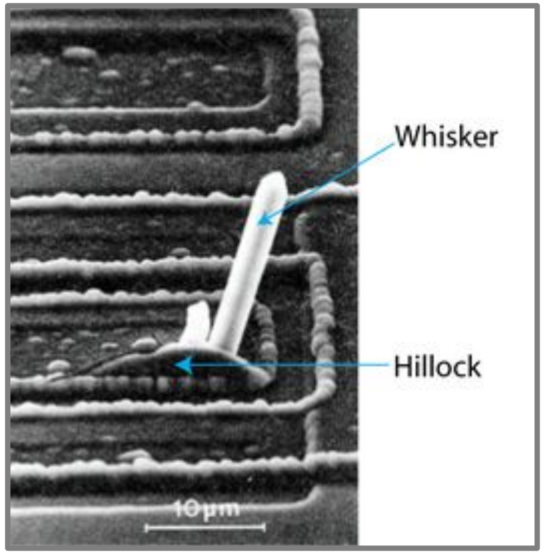
$n \approx 2$

Electromigration (EM)

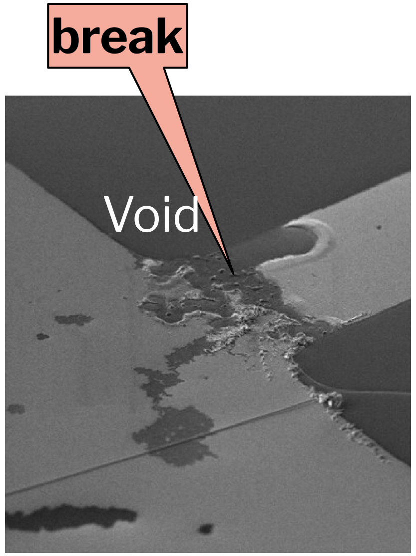
Electronics & Drives
Reutlingen University

This material transport can lead to two types of failure:

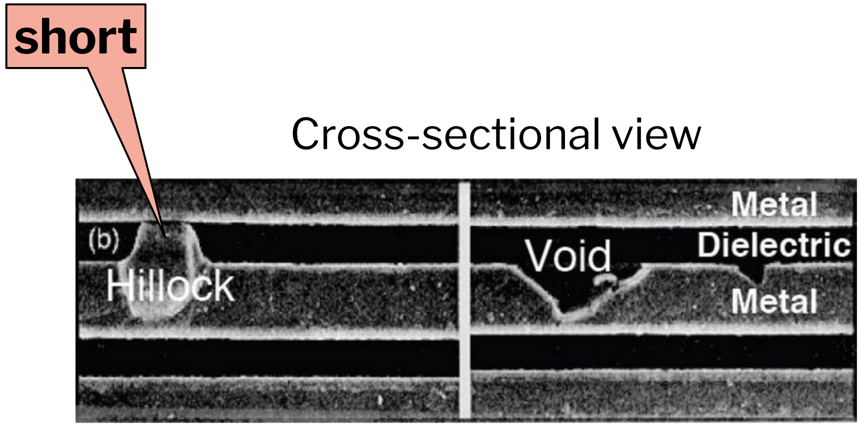
- Reduction in conductor cross-section ("voids") □ interconnect breaks
- Increase in the conductor cross-section („hillocks, whiskers, spikes“) □ short circuits



Source: Microelectronic Materials by CRM Grovenor, IOP Publishing Ltd



Source: Bosch



Source: E. Yantak et.al., Koc University, Istanbul CHI Workshop 2019

Electromigration (EM)

Electronics & Drives

Reutlingen University

Problems

- EM is a long-term effect vulnerable metal lines cannot be identified by chip testing.
- EM is a positive feedback effect failure in field

A nightmare for automotive !!

Electromigration (EM)

Electronics & Drives

Reutlingen University

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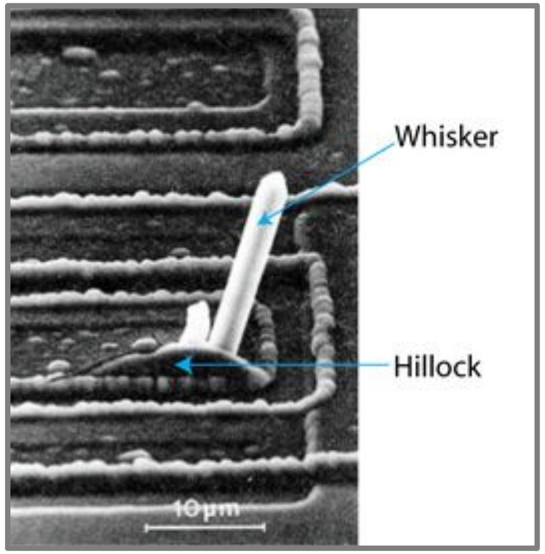

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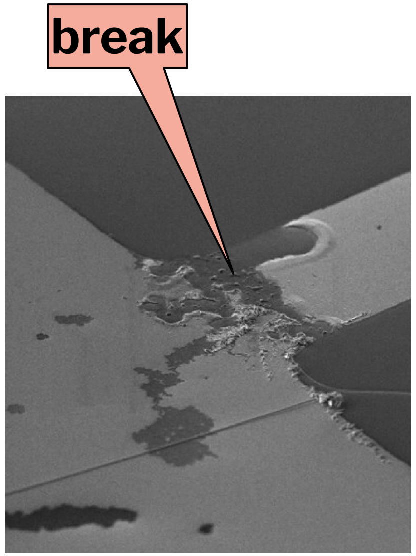
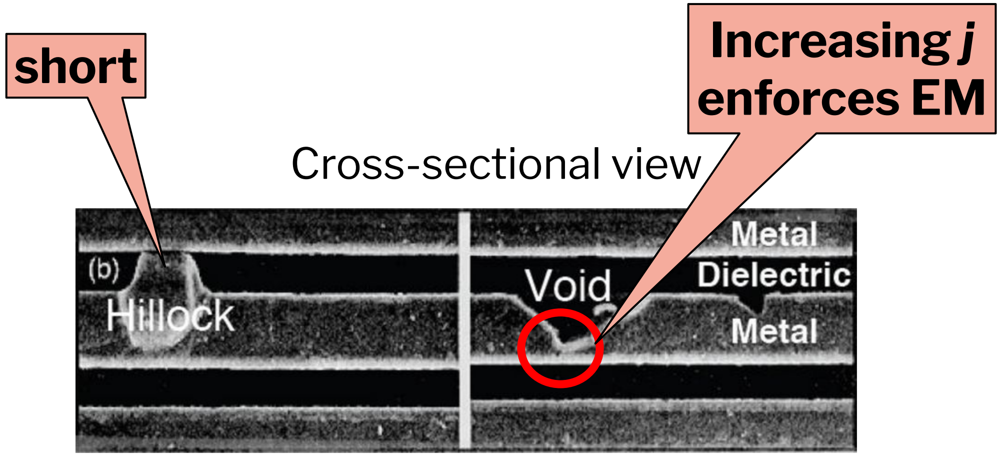


Source: Bosch



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Electromigration (EM)

Electronics & Drives
Reutlingen University

Problems

- EM is a long-term effect vulnerable metal lines cannot be identified by chip testing.
- EM is a positive feedback effect failure in field

 EM must be reliably prevented in the layout design!

Next problem: In 2000 there was no tool from EDA industry to protect layouts against EM effects.

What does not work: Net properties. Each net segment must be adapted individually.

Our solution at Bosch: We decided to developed our own tool to identify vulnerable spots in the wires.

 EMSIM (Electromigration Simulator)

FEM-based calculation of current density in entire metallization structure

EMSIM – Example 1

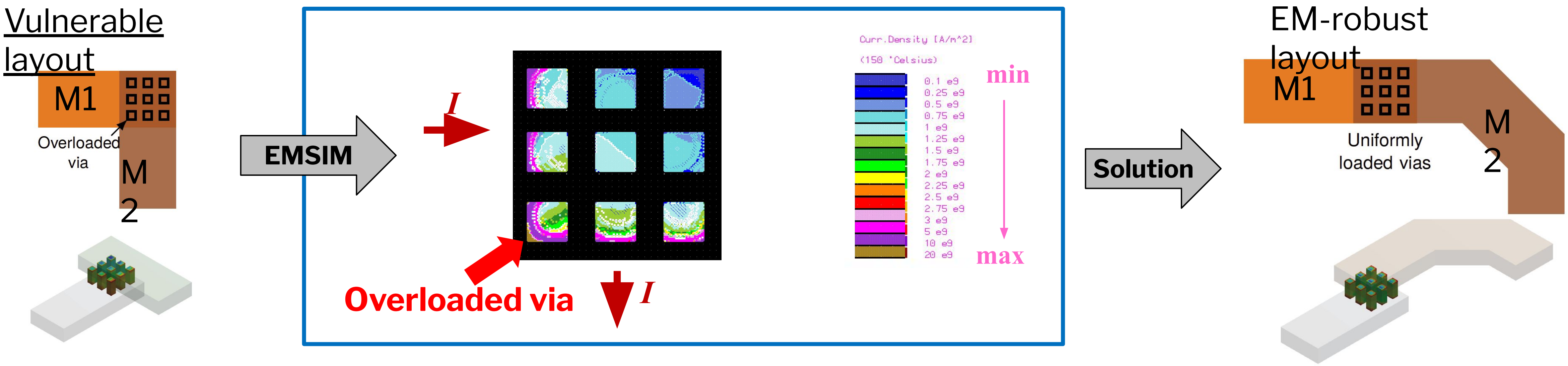
Possible Current Density Problem

Solution

Star point

Wire widening

EMSIM – Example 2



EMSIM (Electromigration Simulator)

EMSIM became a mandatory check tool for all automotive chips at Bosch.

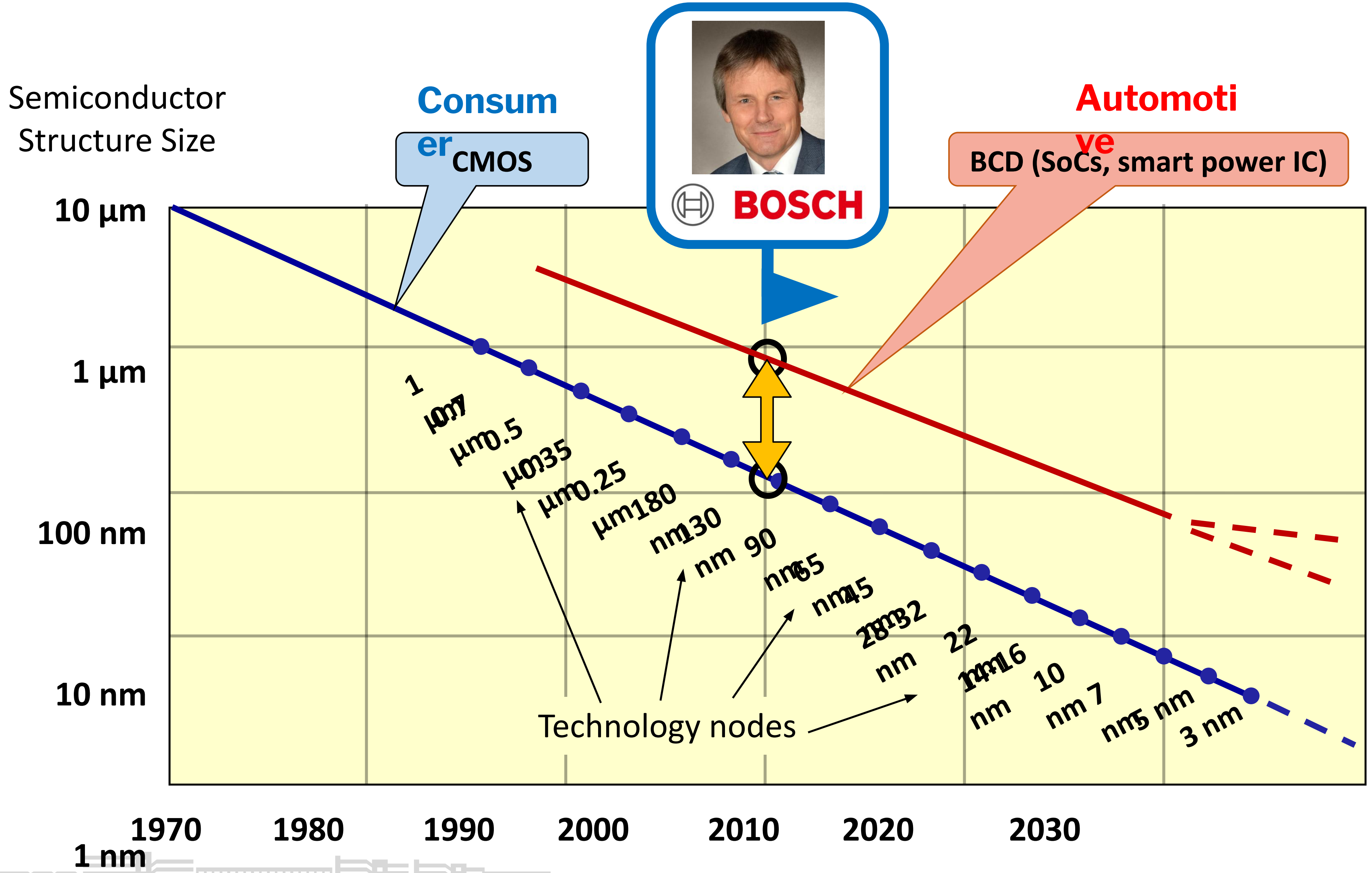
EMSIM was developed by **Göran Jerke,** who received the **EDA Achievement Award 2004** for this work.

Source: edacentrum, Hanover

With the EDA Achievement Award, the edacentrum (Hanover) honors and rewards significant, excellent R&D contributions in the area of EDA, that have resulted in a measurable improvement or acceleration of the design process and thus have demonstrated industrial benefits.

Technology Roadmaps: Consumer vs. Automotive

Electronics & Drives
Reutlingen University



Requirements for Automotive Electronics

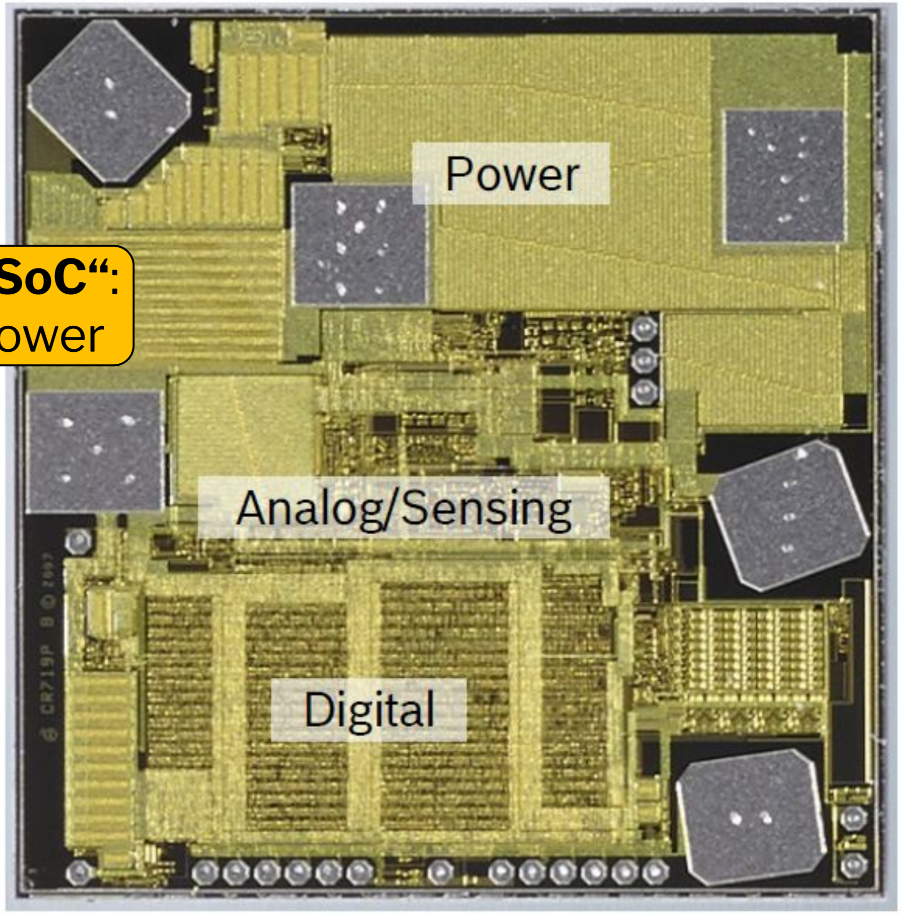
Electronics & Drives
Reutlingen University

about 7 orders of magnitude

- Currents: 1µA … >10A DC, AC, pulse (*)
- Voltages: <1mV … >100V (*)
- Temperatures: -55˚C … >175˚C
- Lifetime: 10 … 15 years
- Failure rate: <1ppm
- High system integration (analog, digital, RF, power, *MEMS*)
- Highly cost-driven
- Relatively small number of metallization layers
- Up to 100 controllers, 500 … 3,000 semiconductors / car

(*) at P/G *and* signal lines

Systen on Chip „SoC“:
Mixed Signal + Power



Source: Bosch (Alternator Regulator ASIC)

Automotive Electronics

Two major Challenges

Reliability

Analog Design

Electronic Systems needs Analog!

Electronics & Drives

Reutlingen University

Real World

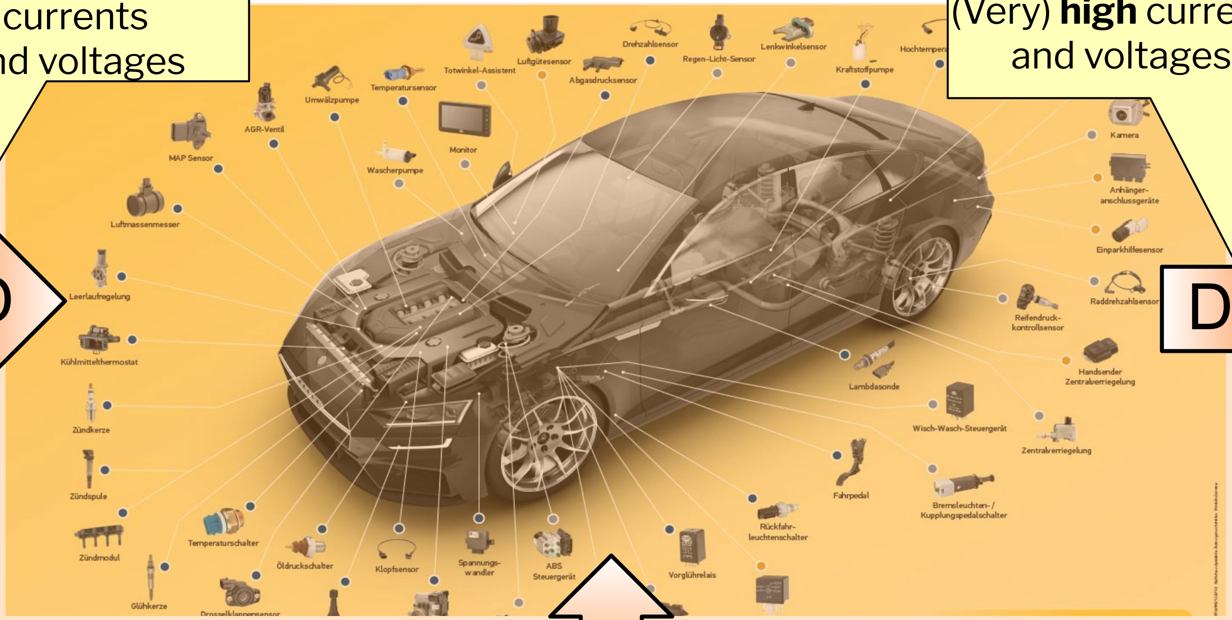
Sensors:

- Sound
- Position
- Light
- Pressure
- Temperature
- Humidity
- …

Analog

(Very) **small** currents and voltages

A/D



(Very) **high** currents and voltages

D/A

Real World

Actuators:

- Speaker
- Display
- Motor
- Lamp
- Heater
- …

Analog

DC/DC

AC/DC

Power management

Analog

DC/DC, AC/DC, DC/AC, AC/AC

DC/DC, AC/DC, DC/AC, AC/AC

System on Chip (SoC)

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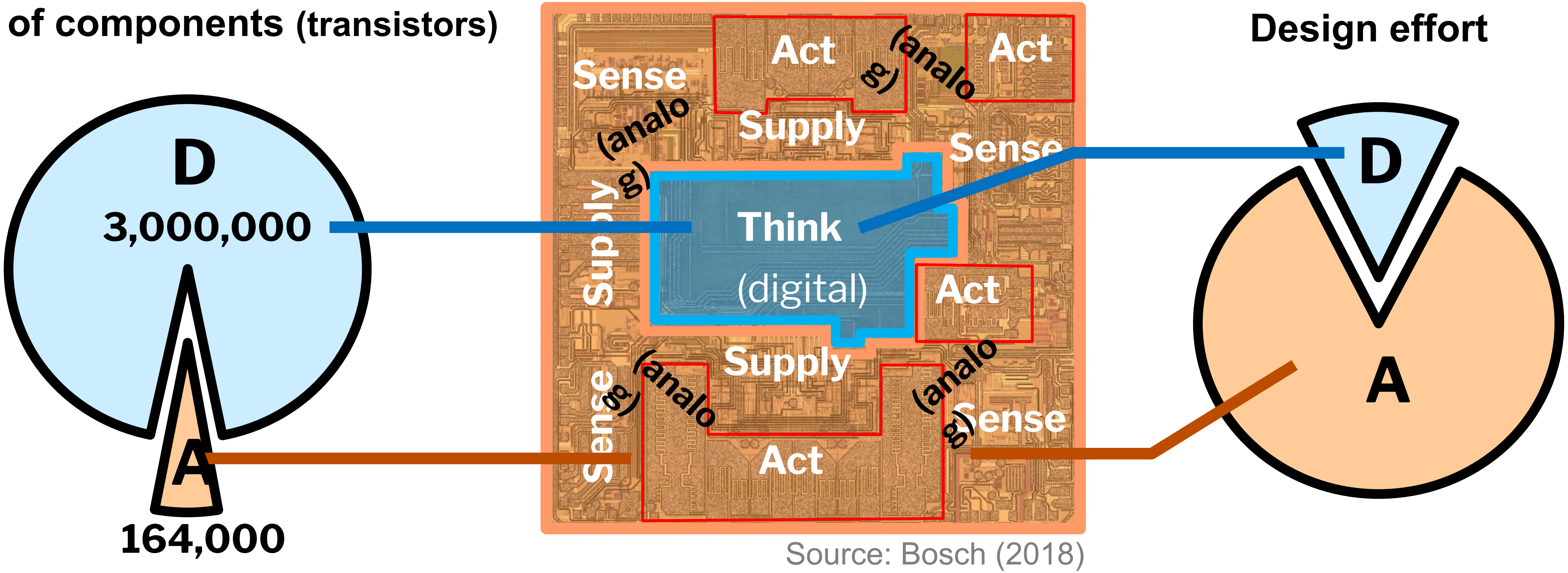
Reutlingen University

Number of components (transistors)

Design effort



Source: Bosch (2018)

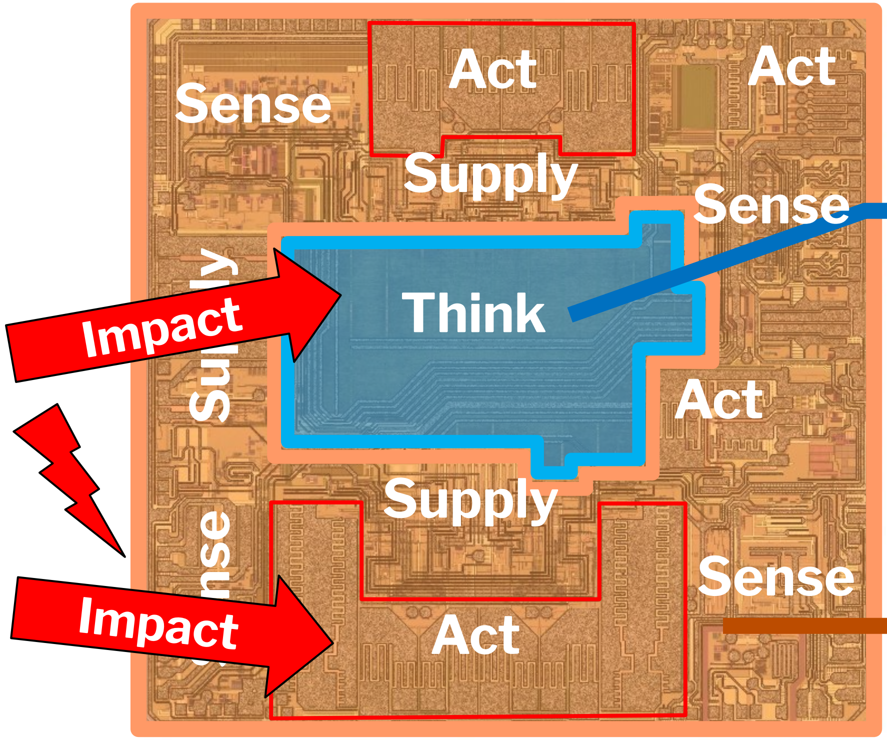
Analog design productivity lags behind **digital** design productivity by **orders of magnitude**!

System on Chip (SoC)

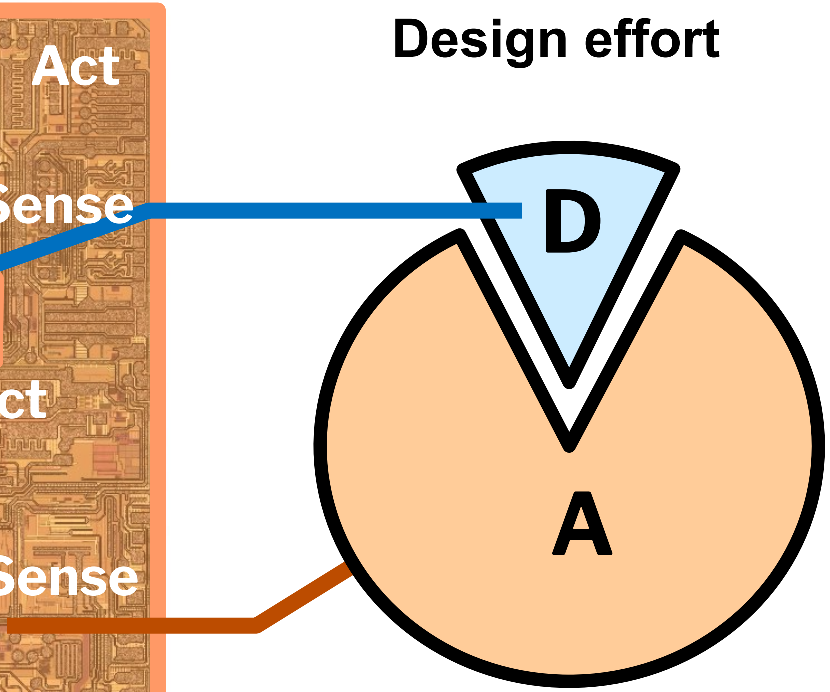
Electronics & Drives
Reutlingen University

Circuits are exposed to many disturbances:

- **Fabrication tolerances**: variations of ±10% … ±50%
- **Temperature effects**: variations of R, V_t, V_D …
- **Mechanical stress effects**: variations of carrier mobilities
- **Parasitic effects**:
  - R, C, L IR-drop, coupling, loss …
  - diodes, bips substrate effects: carrier injection, latch up …
  - thick-field threshold shorts
- **Additional sources of noise …**



Source: Bosch (2018)



System on Chip (SoC)

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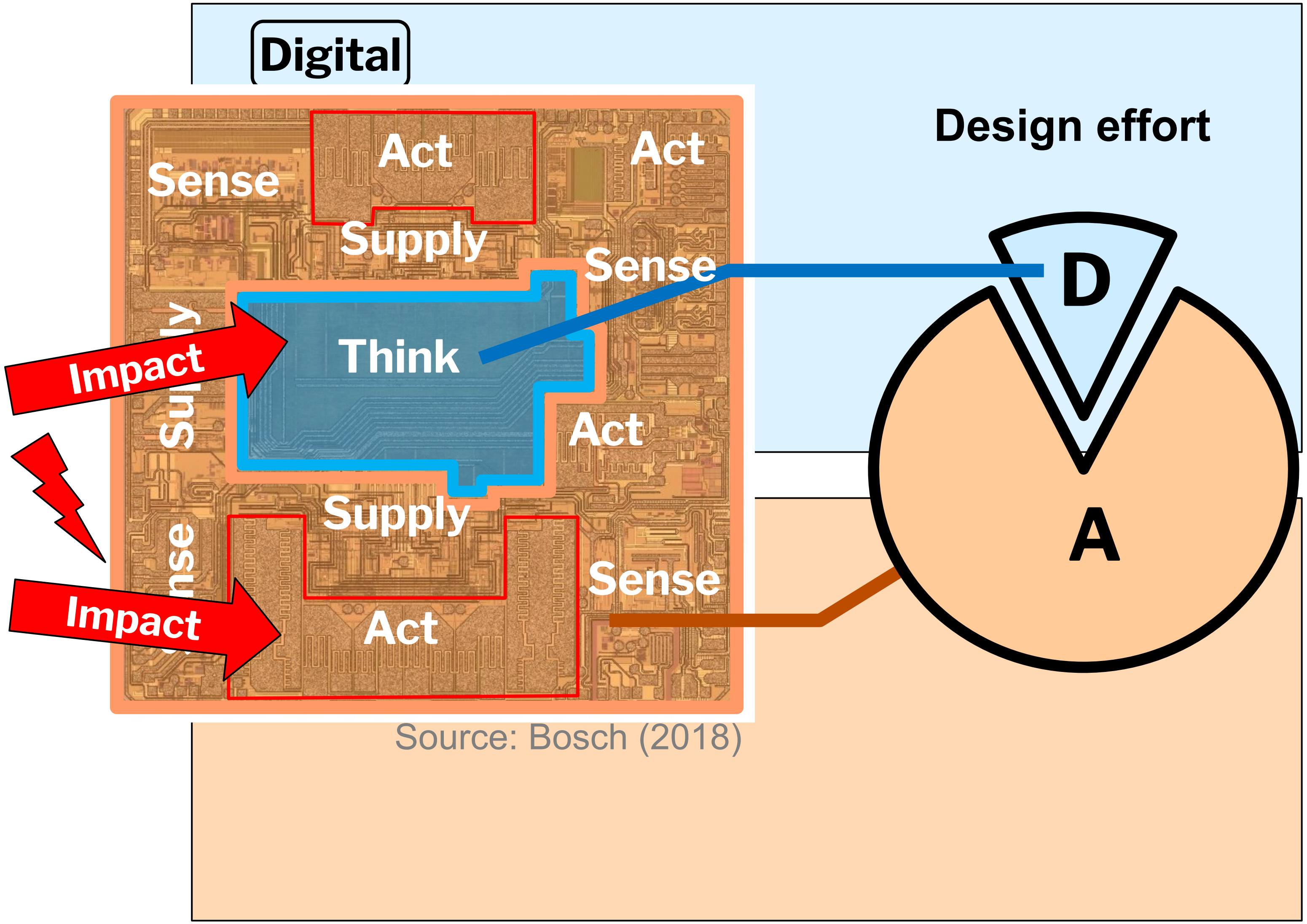

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Analog vs. Digital: the Big Difference

Electronics & Drives

Reutlingen University

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  - thick-field threshold □ shorts
- **Additional sources from outside**

Quantitative complexity

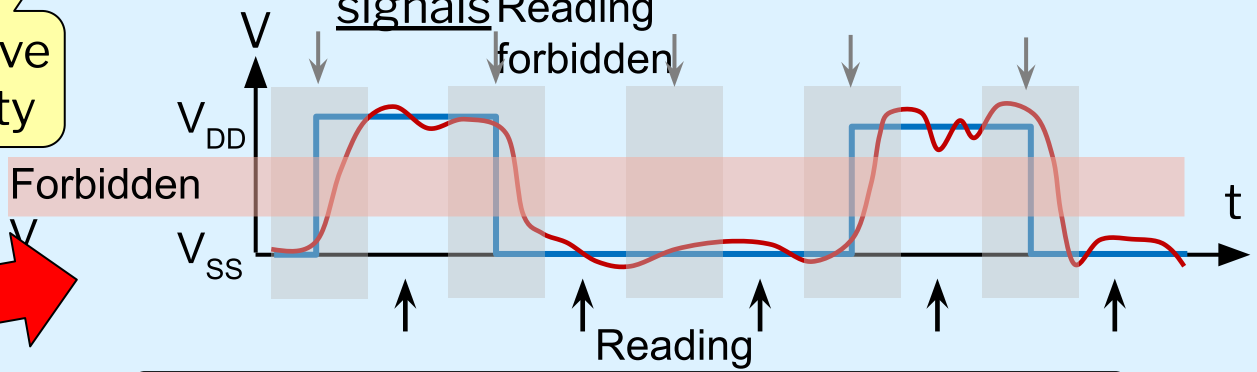
Impact

Impact

Qualitative complexity

Digital

Value- and time-discrete signals



Effects can be controlled by „timing“ (basically)

Analog

Value and time-continuous signals

Every effect has a direct impact on signal quality!

All effects must be considered directly and individually!

Analog vs. Digital: the Big Difference

Electronics & Drives

Reutlingen University

Circuits are exposed to many disturbances:

- **Fabrication tolerances**:
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Analog

Value and **time-continuous** signals

All effects must be considered directly and individually!

Challenges in Analog Design

Electronics & Drives

Reutlingen University

Circuits are exposed to many disturbances:

- **Fabrication tolerances**: variations of ±10% ... ±50%
- **Temperature effects**: variations of R, V_t, V_D ...
- **Mechanical stress effects**: variations of carrier mobilities
- **Parasitic effects**:
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  - diodes, bips substrate effects: carrier injection, latch up ...
  - thick-field threshold shorts
- **Additional sources of noise ...**

Analog

Value and time-continuous signals

The "Art" of Analog Circuit Design

Analog circuits utilize the *symmetrical behavior* of components to manage / control these effects

 The "Art" of Analog Layout Design

"Matching components"

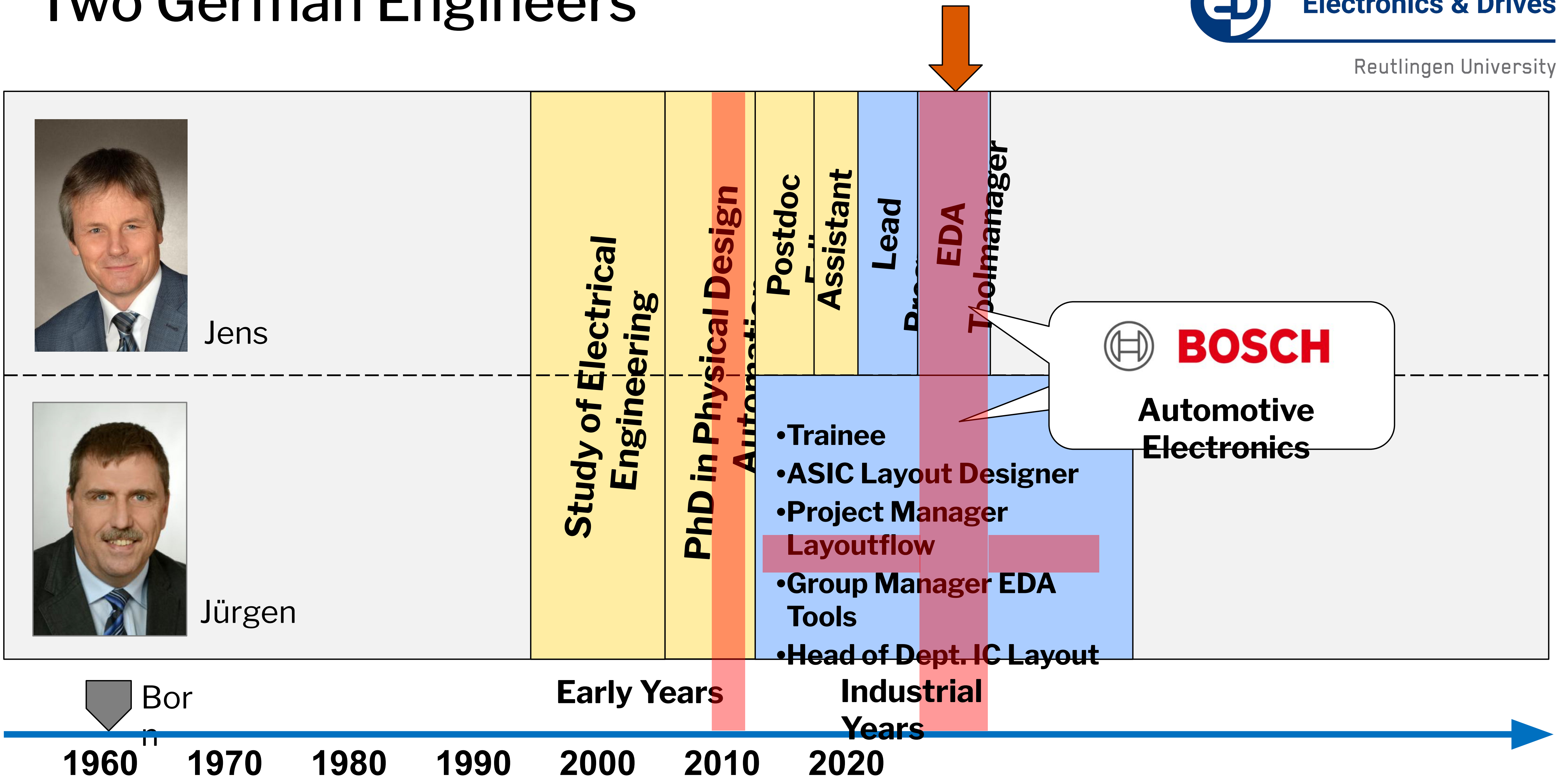
These effects require **specific layout measures** (e.g. guard rings, shielding, star routing ...)

Alle requirements can be handled as

constraints

Two German Engineers

Electronics & Drives
Reutlingen University



Handling of Constraints in Analog Layout

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Reutlingen University

The "classic" way of dealing with constraints:

- Notes in the schematics
- Tables
- Circuit/layout handover meeting
- Phone calls ...

- time-consuming
- error-prone

Increasing complexity required a new approach:

- Data-based processing
  - Completeness
  - Reliability
  - Transparency
  - Flexibility
- Enabling of automation
  - Checks
  - Synthesis approaches

Improvement of

- Design productivity
- Design reliablity

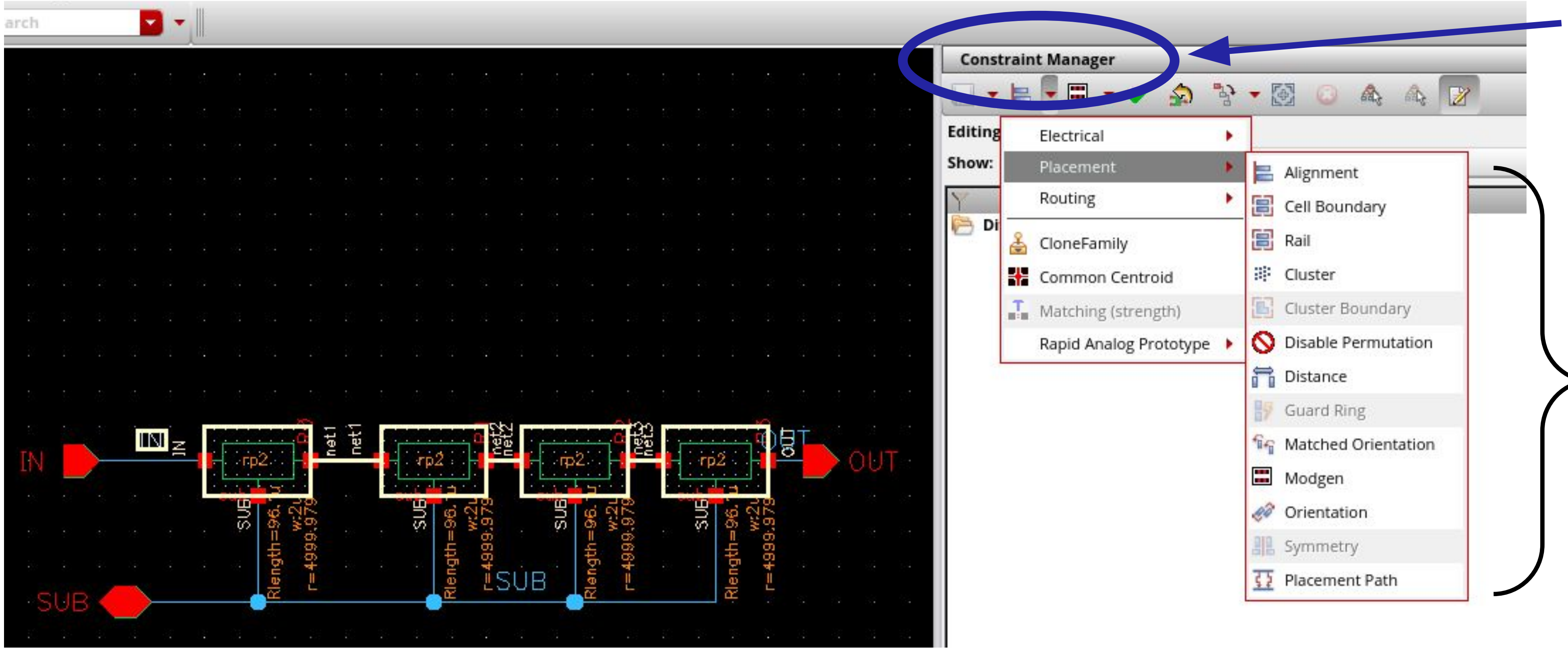
Steps to a **„constraint-driven design"** ...

Constraint Management

Electronics & Drives
Reutlingen University

Development of constraint management mechanisms for IC design environments

- Publicly funded project LEONIDAS, later LEONIDAS II
- Consortium with automotive electronics industry, EDA industry, universities



„Constraint Manager“

Constraint types

Constraint Manager

Electronics & Drives

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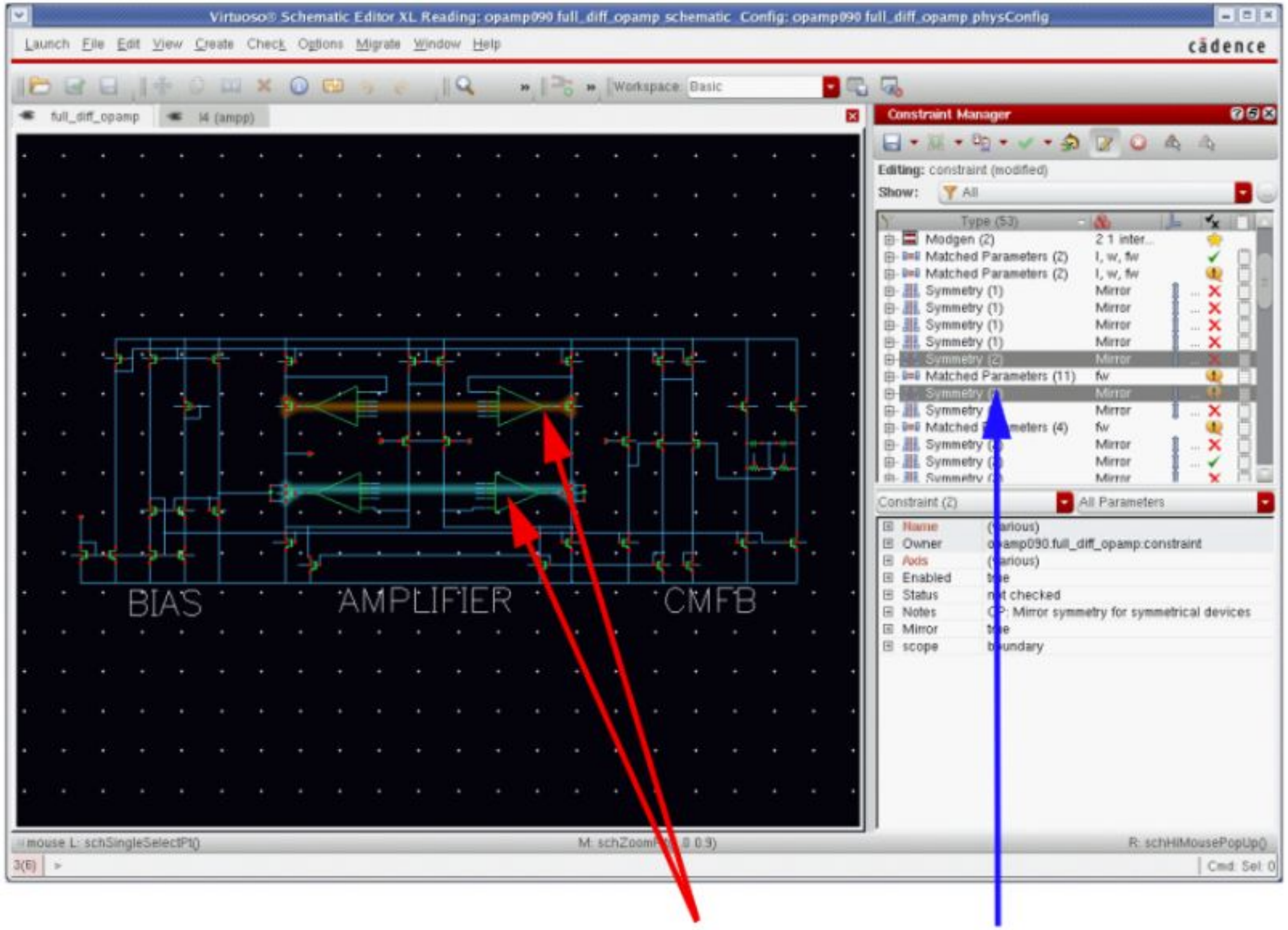


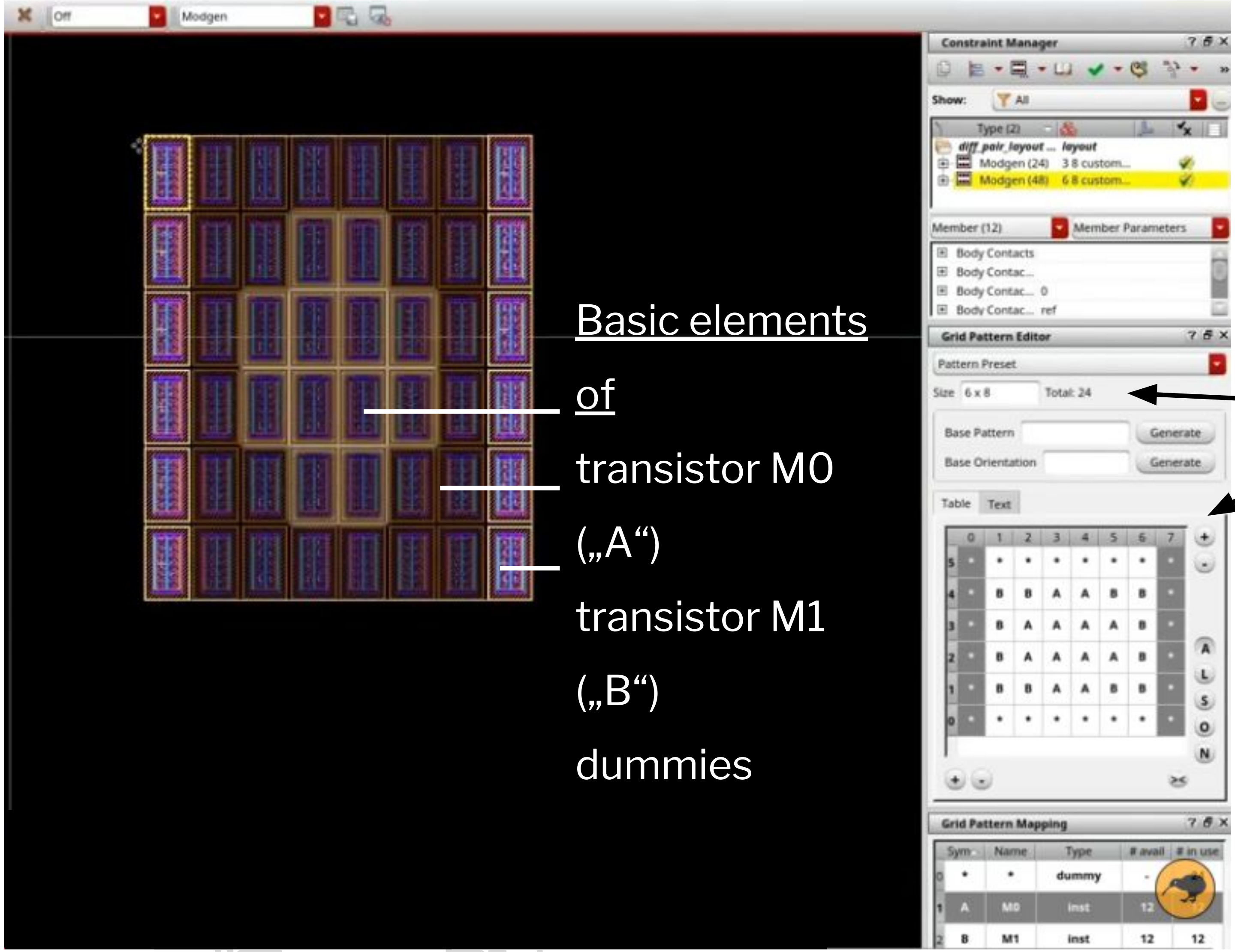
Constraint browser

Two symmetry constraints selected in the Constraint browser and highlighted in the design canvas.

Constraint Manager

Electronics & Drives

Reutlingen University



Autoplacement of matching patterns

„Modgen“ function

Easy specification options for layout patterns

Mapping of devices incl. dummies

Two German Engineers

Electromigration
Costraint-driven
Design

Electronics & Drives

Reutlingen University

Jens

Study of Electrical Engineering

PhD in Physical Design Automation

Postdoc

Assistant

Lead

EDA

Full Professor
Director of

ifte

Technische Universität Dresden

BOSCH

Automotive Electronics

Jürgen

- Trainee
- ASIC Layout Designer
- Project Manager Layoutflow
- Group Manager EDA Tools
- Head of Dept. IC Layout

Born

Early Years

Industrial Years

Late Years

1960 1970 1980 1990 2000 2010 2020

Jens‘ Works on Constraint-driven Design

Electronics & Drives

Reutlingen University

Until 2010

J. Scheible. **„Constraint-driven Design– Eine Wegskizze zum Designflow der nächsten Gene-ration“,** ANALOG’08, VDE, 2008.

A. Nassaj, J. Lienig, G. Jerke **"A Constraint-driven Methodology for Placement of Analog and Mixed-signal Integrated Circuits,"** *Proc. of the 14th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Malta, pp. 770-773, Aug. 2008.

A. Nassaj, J. Lienig, G. Jerke, J. Freuer **"Constraint-geführte Floorplan-Generierung von integrierten Analog- und Mixed-Signal-Schaltungen,"** *GMM-Fachbericht ANALOG '08*, Siegen, pp. 159-164, April 2008.

A. Nassaj, J. Lienig, G. Jerke **"A New Methodology for Constraint-Driven Layout Design of Analog Circuits,"** *Proc. of the 16th IEEE Int. Conference on Electronics, Circuits and Systems (ICECS 2009)*, Hammamet, Tunisia, pp. 996-999, Dec. 2009.

G. Jerke, J. Lienig **"Constraint-driven Design — The Next Step Towards Analog Design Automation,"** Invited Talk, *Proc. of the Int. Symposium on Physical Design (ISPD'09)*, San Diego, CA, pp. 75-82, March 2009.

G. Jerke, J. Lienig, J. B. Freuer **"Constraint-Driven Design Methodology: A Path to Analog Design Automation„.** In: *Analog Layout Synthesis — A Survey of Topological Approaches,* H. Graeb (ed.) Springer Verlag, New York, ISBN 978-1-4419-6931-6 , pp. 271-299, 2011.

Since 2011

A. Krinke, J. Lienig, **Neuartige Entwurfsmethodik zur Berücksichtigung des IR-Drop bei der Power-Verdrahtung analoger Schaltungen** [PDF] *Tagungsband Dresdner Arbeitstagung Schaltungs- und Systementwurf (DASS)*, Fraunhofer, 2011.

A. Krinke, J. Lienig **"An Ontology for Constraints in Custom IC Design,"** *ECCTD,* 2011.

M. Mittag, A. Krinke, G. Jerke, W. Rosenstiel, **Hierarchical Propagation of Geometric Constraints for Full-Custom Physical Design of ICs,** *DATE,* 2012.

A. Krinke, M. Mittag, G. Jerke, J. Lienig, **Propagierung und Transformation von Randbedingungen für den AMS-IC-Entwurf,** *edaWorkshop 13*, VDE, 2013.

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Krinke, M. Mittag, G. Jerke, J. Lienig **"Extended Constraint Management for Analog and Mixed-Signal IC Design“,** *21th ECCTD,* 2013.

A. Krinke, G. Jerke, J. Lienig **"Constraint Propagation Methods for Robust IC Design“** *GMM-Fachbericht 83, Reliability by Design (ZuE 2015)*, VDE, 2015.

A. Krinke, G. Jerke, J. Lienig, **Entwurf analoger und analog-digitaler ICs: Kenne die Grenzen,** *Elektronik*, WEKA Fachmedien, Ausgabe 4/2016, S. 8, Februar 2016

A. Krinke, L. Lei, J. Lienig **"Predictive System-Level Constraint Verification and Optimi-zation** *GMM-Fachbericht 274, ZuE 2017*, VDE, 2017.

A. Krinke, B. Prautsch, J. Lienig, et. al. **"From Constraints to Tape-Out: Towards a Continuous AMS Design Flow,"** *Proc. 22nd DDECS, 2019*.

A. Krinke, **Constraint Propagation for Analog and Mixed-Signal Integrated Circuit Design,** Dissertation, *Fortschritt-Berichte VDI, Reihe 20, Nr. 474*, VDI 2020.

Jens‘ Works on Constraint-driven Design

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Dissertation Andreas Krinke

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Generic approach for substantial improvements in the design flow of analog and mixed-signal ICs with regard to constraint handling

Propagation of constraints

- along design flows (forward, backward)
- across hierarchy boundaries (up, down)

Support for the creation of

- new constraints during design
- novel constraint types

Jens‘ Work on Migration Effects

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Moving migration modeling into IC design flow

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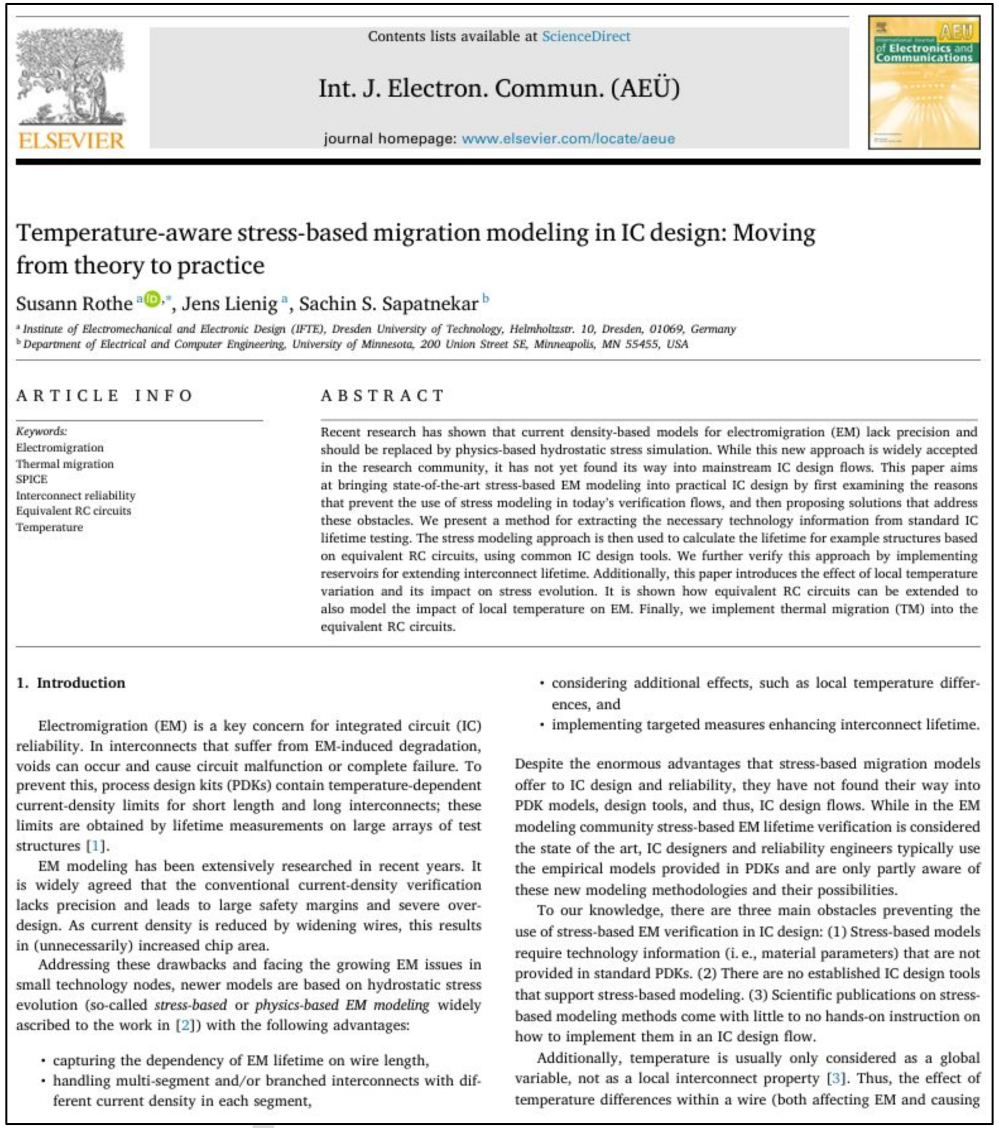

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Temperature-aware stress-based migration modeling in IC design: Moving from theory to practice

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Keywords:
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ABSTRACT

Recent research has shown that current density-based models for electromigration (EM) lack precision and should be replaced by physics-based hydrostatic stress simulation. While this new approach is widely accepted in the research community, it has not yet found its way into mainstream IC design flows. This paper aims at bringing state-of-the-art stress-based EM modeling into practical IC design by first examining the reasons that prevent the use of stress modeling in today's verification flows, and then proposing solutions that address these obstacles. We present a method for extracting the necessary technology information from standard IC lifetime testing. The stress modeling approach is then used to calculate the lifetime for example structures based on equivalent RC circuits, using common IC design tools. We further verify this approach by implementing reservoirs for extending interconnect lifetime. Additionally, this paper introduces the effect of local temperature variation and its impact on stress evolution. It is shown how equivalent RC circuits can be extended to also model the impact of local temperature on EM. Finally, we implement thermal migration (TM) into the equivalent RC circuits.

1. Introduction

Electromigration (EM) is a key concern for integrated circuit (IC) reliability. In interconnects that suffer from EM-induced degradation, voids can occur and cause circuit malfunction or complete failure. To prevent this, process design kits (PDKs) contain temperature-dependent current-density limits for short length and long interconnects; these limits are obtained by lifetime measurements on large arrays of test structures [1].

EM modeling has been extensively researched in recent years. It is widely agreed that the conventional current-density verification lacks precision and leads to large safety margins and severe over-design. As current density is reduced by widening wires, this results in (unnecessarily) increased chip area.

Addressing these drawbacks and facing the growing EM issues in small technology nodes, newer models are based on hydrostatic stress evolution (so-called *stress-based* or *physics-based EM modeling* widely ascribed to the work in [2]) with the following advantages:

- capturing the dependency of EM lifetime on wire length,
- handling multi-segment and/or branched interconnects with different current density in each segment,
- considering additional effects, such as local temperature differences, and
- implementing targeted measures enhancing interconnect lifetime.

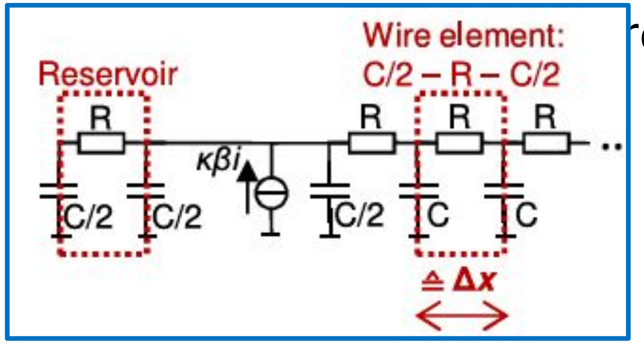
Despite the enormous advantages that stress-based migration models offer to IC design and reliability, they have not found their way into PDK models, design tools, and thus, IC design flows. While in the EM modeling community stress-based EM lifetime verification is considered the state of the art, IC designers and reliability engineers typically use the empirical models provided in PDKs and are only partly aware of these new modeling methodologies and their possibilities.

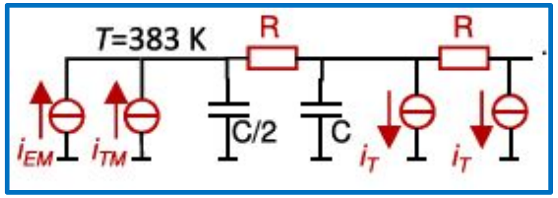
To our knowledge, there are three main obstacles preventing the use of stress-based EM verification in IC design: (1) Stress-based models require technology information (i. e., material parameters) that are not provided in standard PDKs. (2) There are no established IC design tools that support stress-based modeling. (3) Scientific publications on stress-based modeling methods come with little to no hands-on instruction on how to implement them in an IC design flow.

Additionally, temperature is usually only considered as a global variable, not as a local interconnect property [3]. Thus, the effect of temperature differences within a wire (both affecting EM and causing

Contributions

- Method for estimating material parameters from standard lifetime testing
- Method for stress-based EM simulation with SPICE-like simulators based on equivalent RC circuits
  - Modeling of reservoirs for lifetime improvement
  - Consideration of local temperature and ...re migration





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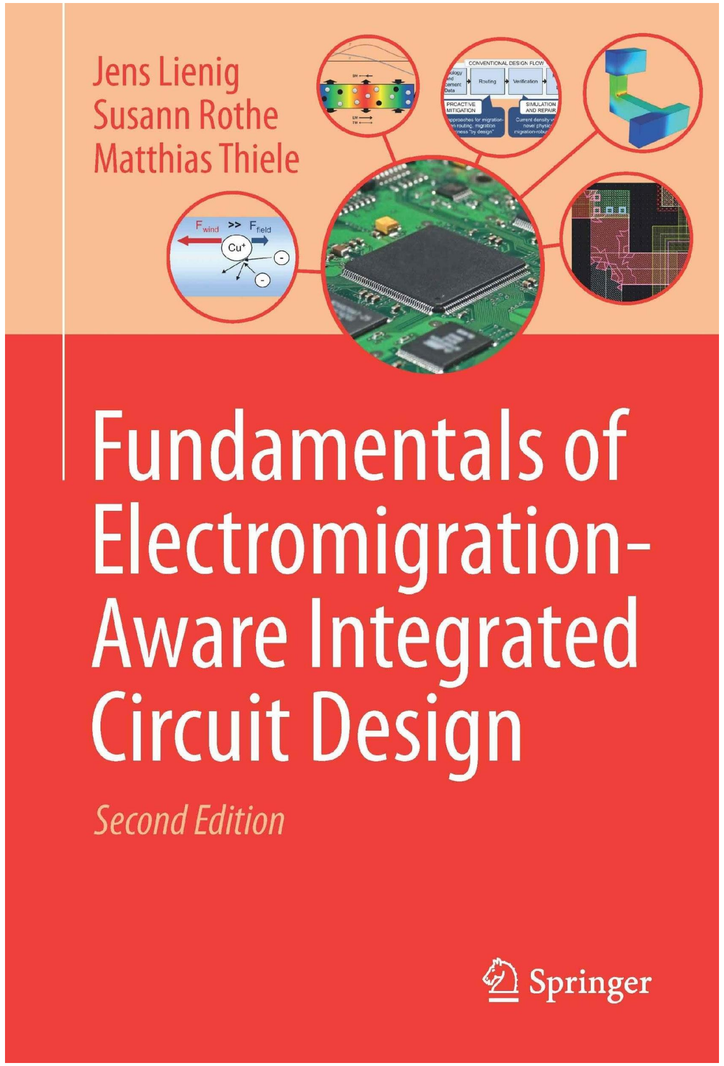

Fundamental treatise on migration effects their mitigation in IC-layout

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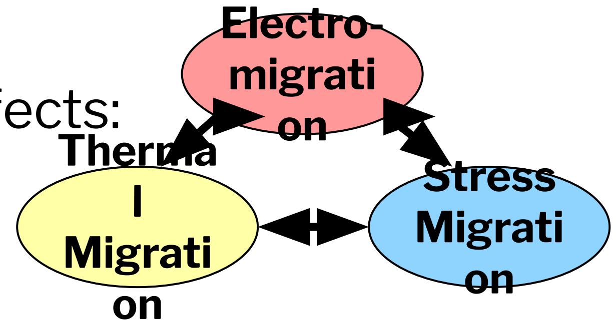

Electromigration-aware layout design

Special effects and dependencies

- Bamboo effect
- Critical length effect (Blech length)
- Frequence-depend effects
- Dependency of via positions
- The role of reservoirs
- New materials

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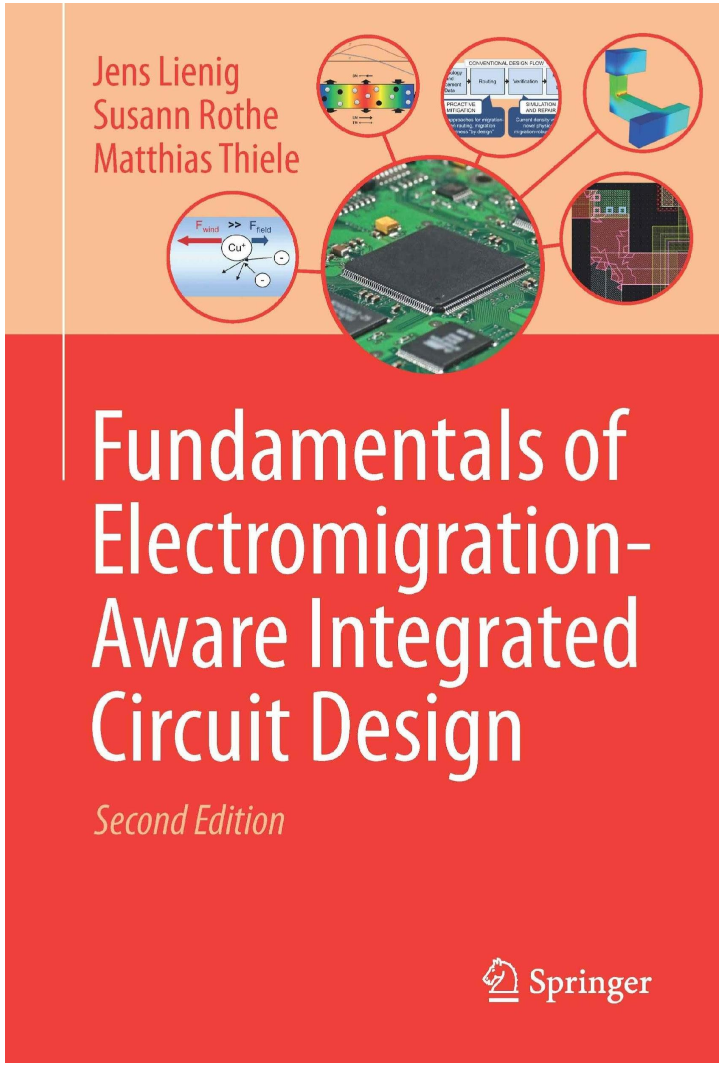

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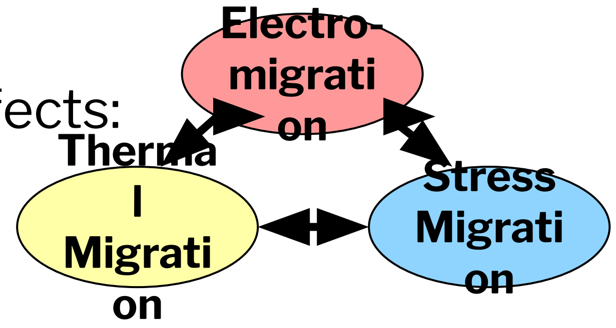

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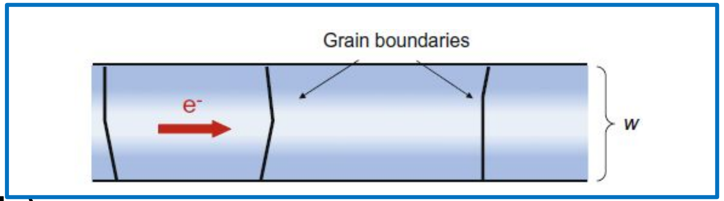

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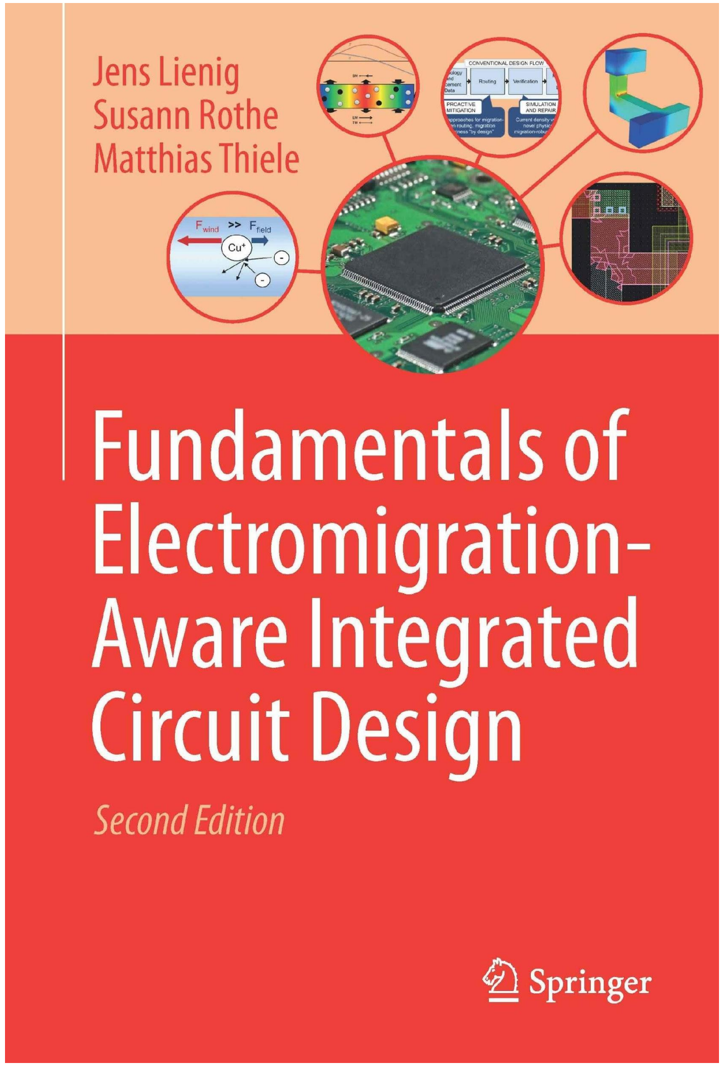

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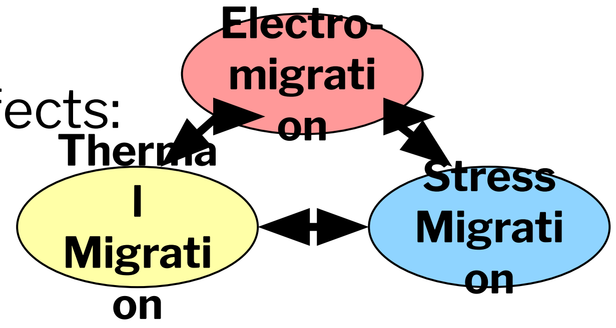

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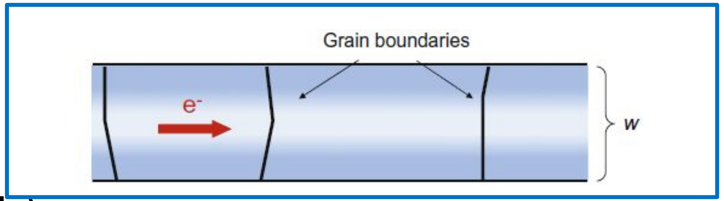
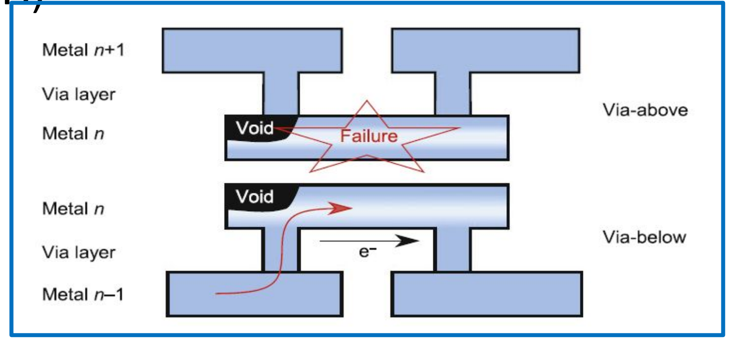
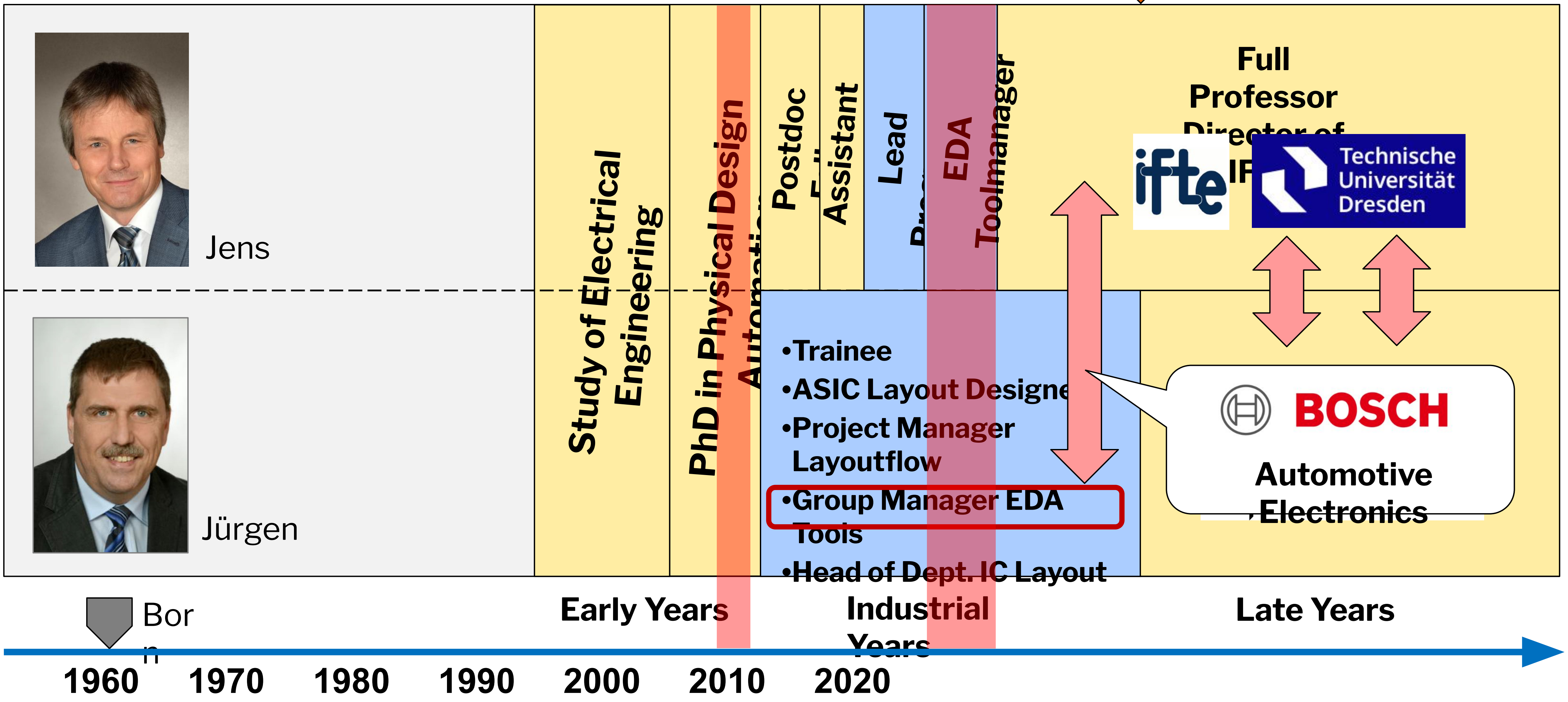
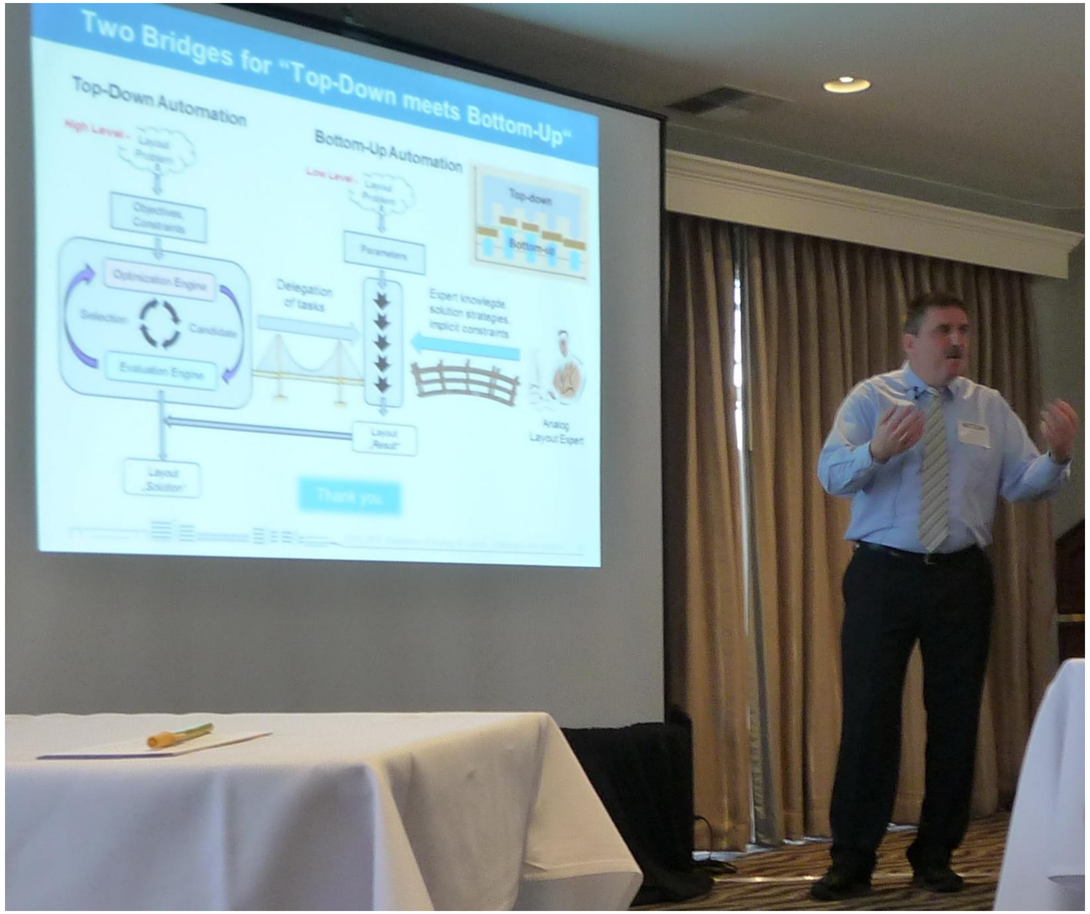




Two German Engineers



ISPD 2015, Monterey



Paper „Automation of Analog IC Layout", ISPD'16

Automation of Analog IC Layout – Challenges and Solutions

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ABSTRACT

Physical analog IC design has not been automated to the same degree as digital IC design. This shortfall is primarily rooted in the analog IC design problem itself, which is considerably more complex even for small problem sizes. Significant progress has been made in analog automation in several R&D target areas in recent years. Constraint engineering and generator-based module approaches are among the innovations that have emerged. Our paper will first present a brief review of the state of the art of analog layout automation. We will then introduce active and open research areas and present two visions – a "continuous layout design flow" and a "bottom-up meets top-down design flow" – which could significantly push analog design automation towards its goal of analog synthesis.

Categories and Subject Descriptors
B7.2[**Integrated Circuits**]: Design Aids

General Terms
Algorithms, Design, Verification.

Keywords
Analog design; layout; constraint engineering; design methodology; physical design; analog layout automation

1. INTRODUCTION

While physical design automation of analog IC design has seen significant improvement over the past decade, it has not advanced at anything like the rate of its digital counterpart. This shortfall is primarily rooted in the analog IC design problem itself, which is very much more complicated even for small problem sizes: it deals with a large number of specific circuit classes; it requires a customized design approach for each circuit class; and analog circuits are very susceptible to noise and process variations. In particular, the work and costs involved in producing analog layout is a serious bottleneck in IC design, despite numerous attempts at automating the process. Furthermore, the analog design problem lacks a sufficiently comprehensive and exact descriptiveness in conventional CAD approaches [1-3].

Advances in analog layout automation have been made however in recent years in many R&D target areas, such as generator-based module approaches [8,9,11-13,16]; and we have witnessed the emergence of constraint engineering to support top-down design styles [2,6,10,18,19,24].

Unfortunately, achievements made thus far fall way short of meeting the needs of advanced analog layout automation. Active new research areas needed to bridge this deficiency gap include

- The next generation of constraint engineering approaches;
- Context-aware layout design;
- Advanced methods for assisted layout design;
- The development of top-down design approaches, tailored for analog circuits, and very powerful bottom-up design procedures, such as module-generator-based and template-based design.

The purpose of this paper is to give an up-to-date overview of analog design automation, highlighting physical design, its specific characteristics and its current research areas from both an industrial and an academic perspective. Specifically, we will first review the analog layout design problem itself and discuss various aspects of today's design flows. We then introduce active and open research areas and finally present two visions, a *continuous layout design flow* and a *bottom-up meets top-down design flow*. It is our hope that these new design paradigms will significantly enhance analog design automation and bring us one step closer to the long-awaited goal of analog synthesis.

2. THE LAYOUT OF ANALOG CIRCUITS

2.1 Sources of Complexity

The majority of today's ICs are mixed signal designs, i.e., they consist of analog and digital circuits (blocks, partitions). Both analog and digital designers claim their design tasks are "highly complex", and in fact both are right, but in a different sense.

Analog designs are characterized by a much richer and more complex set of design constraints that need to be considered simultaneously and which may span several domains (e.g., electrical, electro-thermal, electro-mechanical, technological, geometrical domain). Therefore, in typical mixed signal ICs, the effort needed to design the analog part often matches or even exceeds the effort for the digital part by far. This is true despite the fact that analog modules typically contain only a small number of devices compared to digital ones.

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http://dx.doi.org/10.1145/2717764.2717781

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Two Visions for analog mixed-signal integrated circuits

1. „***Continuous design flow***"
   A revolutionary new way of dealing with constraints in interactive layout

2. „***Bottom-up-meets-top-down design flow***"
   Conflating two different automation paradigms:
   - Bottom-up: *procedural* (i.e. knowledge-based) automation methods
   - Top-down: *optimization-based* automation methods

Very successful paper
- Nr. 3 among all ISPD papers (> 3.000 downloads)
- 105 citations (Google Scholar)
- Reported in EE Times article

This paper, initiated by Jens, has had a significant impact
- in the professional community and

Textbooks on Layout Design of Integrated Circuits

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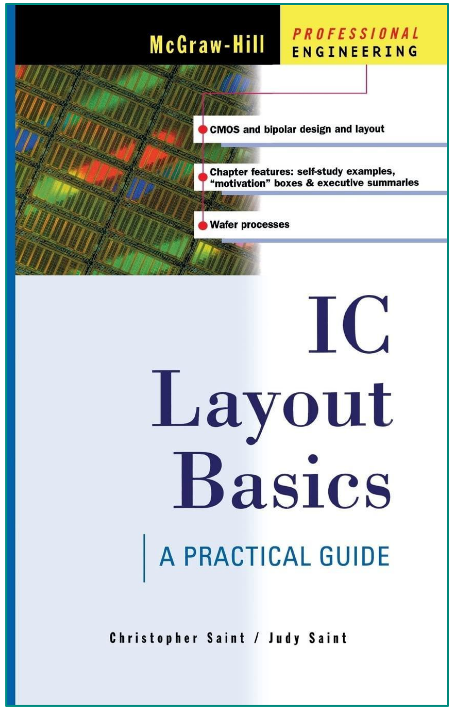

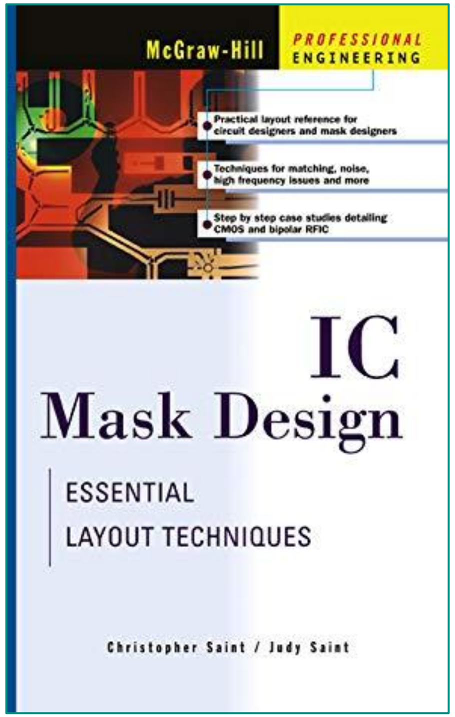

- „Plain-English“ guides for readers without an engineering background, no technical depth
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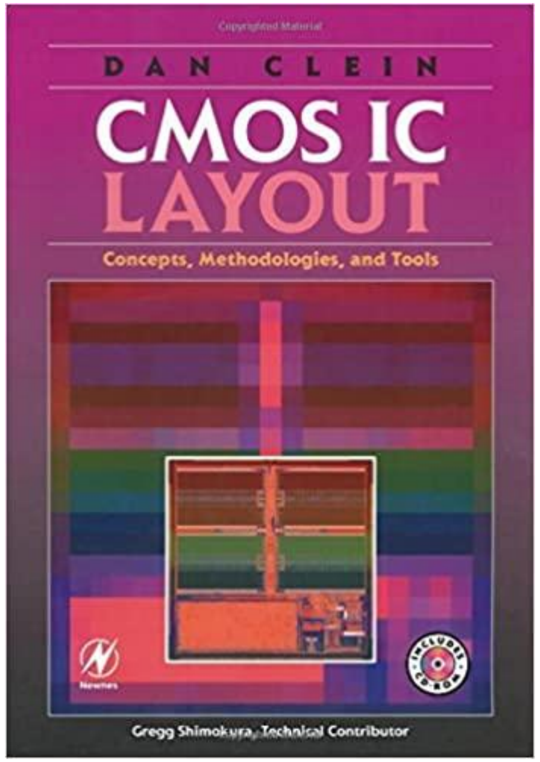
- Narrative form, anecdotes
- **Last edition: 2001 / 2002**



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- Strong flow perspective
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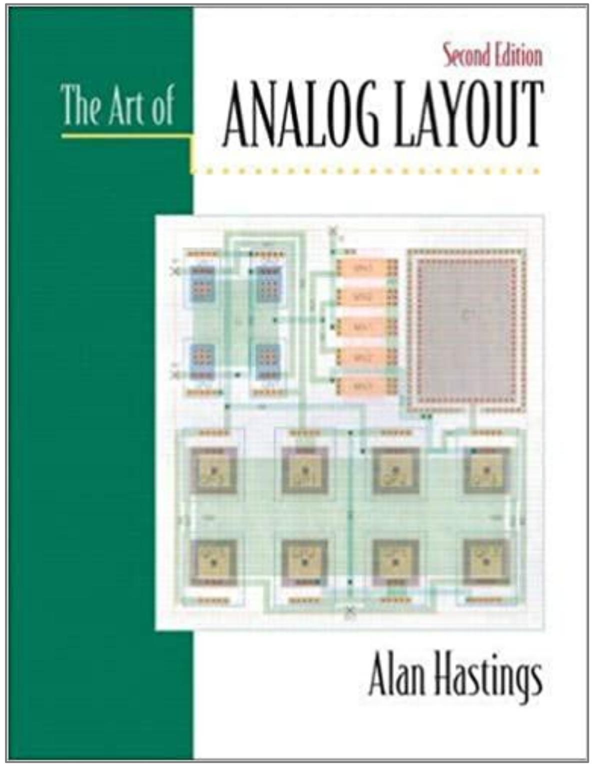

- Excellent reference book with technical depth
- Analog only, including fabrication
- No tool/flow perspective
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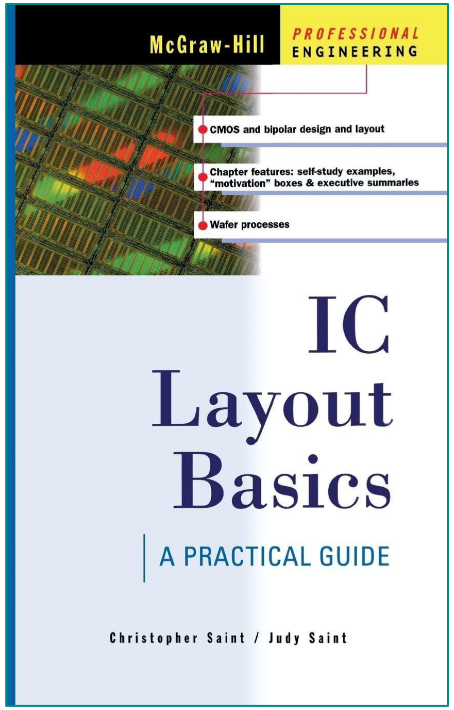

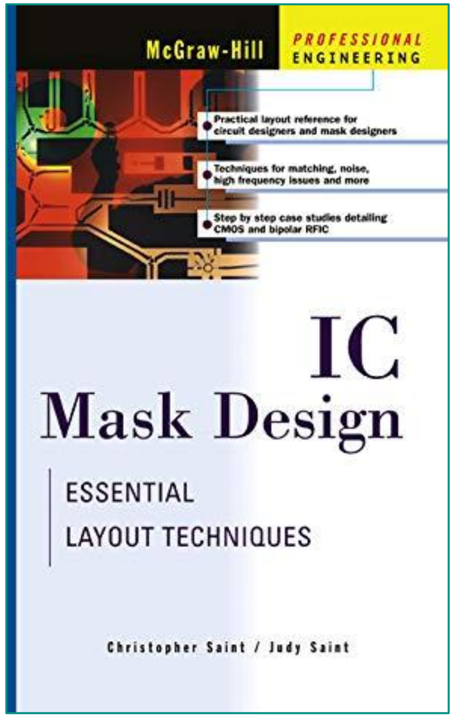

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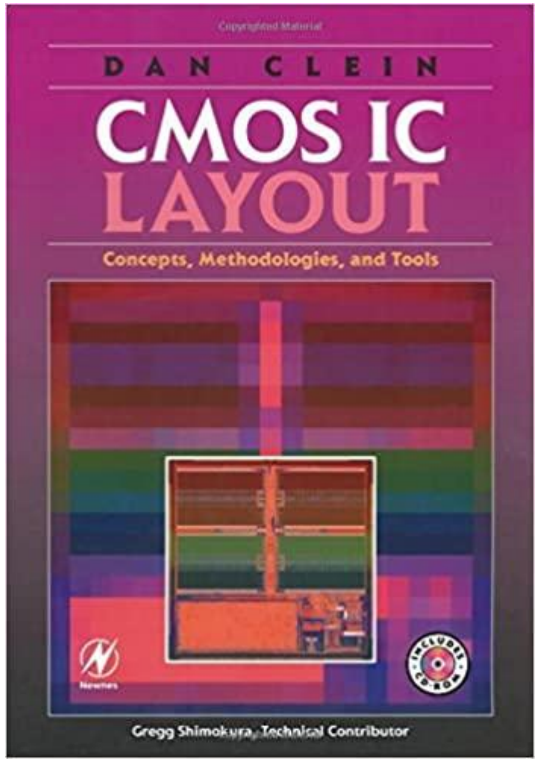

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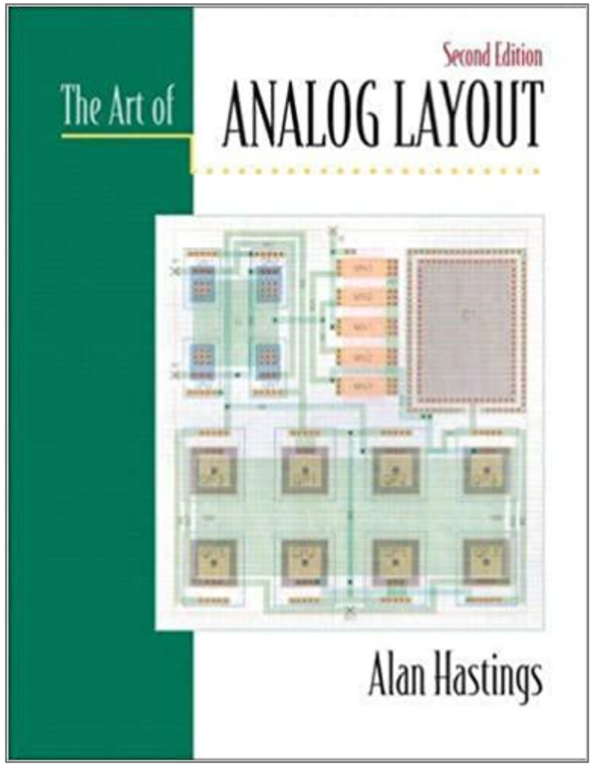

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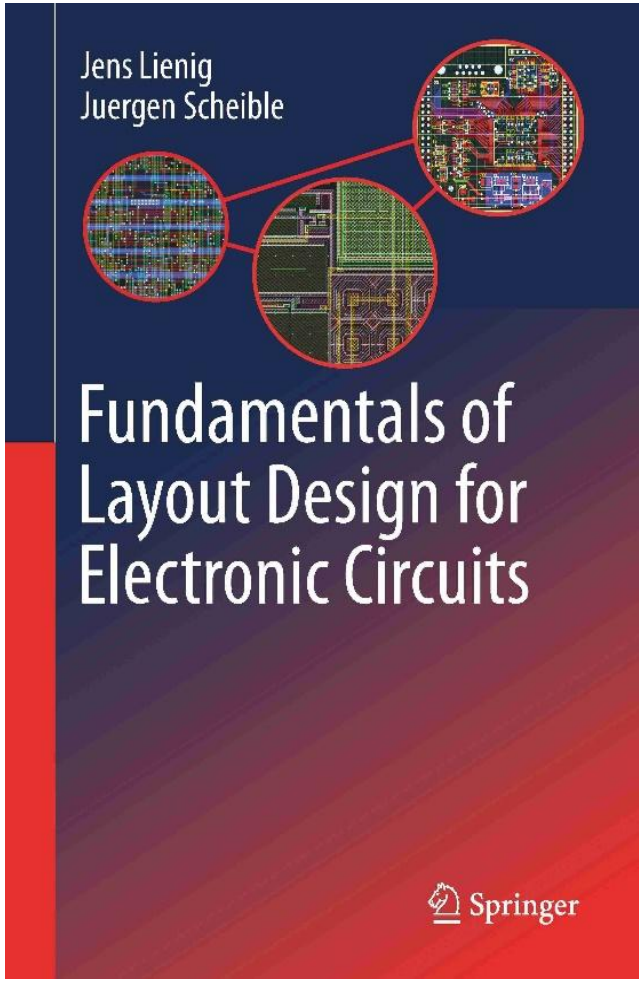

Published: 2020

<u>All aspects of layout design are covered</u>

- Technology knowhow
- Analog and digital
- IC and PCB
- Circuit data, layout data, post process
- Design rules and libraries
- Layout models, styles, tasks, flows
- Layout design steps
- Special techniques for analog IC layout
- Reliability measures in layout design

Published: 2023

Thank You!