Invited: Analog IC Design Automation -- More than a Technical Challenge

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Benjamin Prautsch, Uwe Eichler

The work presented was carried out in the framework of the APECS Pilot Line of the Chips Joint Undertaking, funded by Horizon Europe (ID: 101183307) and Digital Europe (ID: 101182906) Programmes and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain.
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»Analog circuit design is like chess—just because you *know* how *the pieces* move doesn't mean you *know how to play* the game.«

Patrick M. Lahey
(secondary source)

Picture: [https://pixabay.com/de/photos/schach-brettspiel-strategie-1080533/]

Agenda

Analog IC Design Automation – More than a Technical

- Relevance and Challenge of Analog IC Design
- Brief State of the Art in Analog IC Design Automation
- Generators in Analog Design
- Conclusion and Outlook

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Automation of Analog IC Design using Generators

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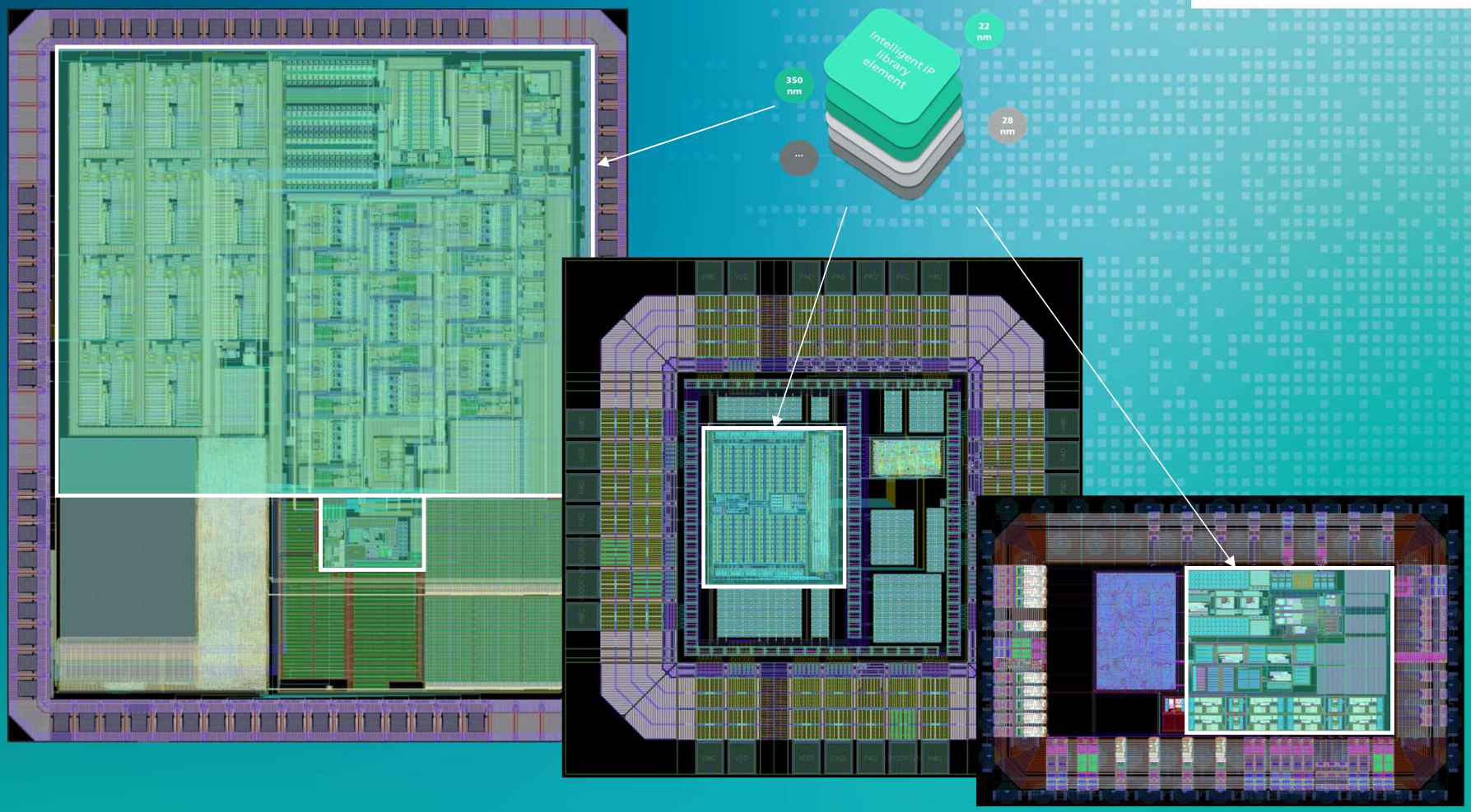
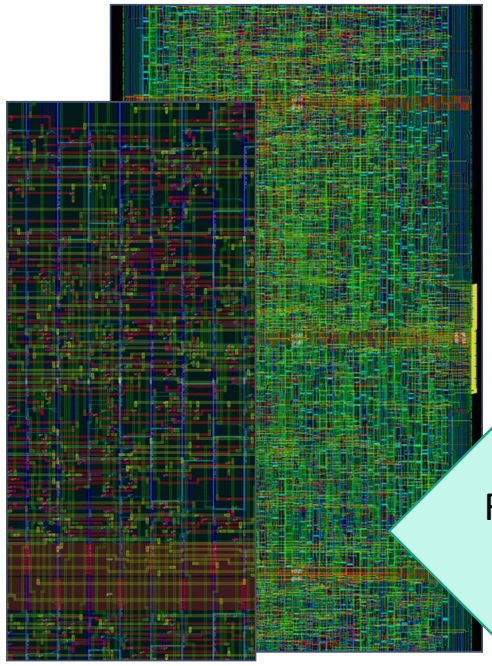


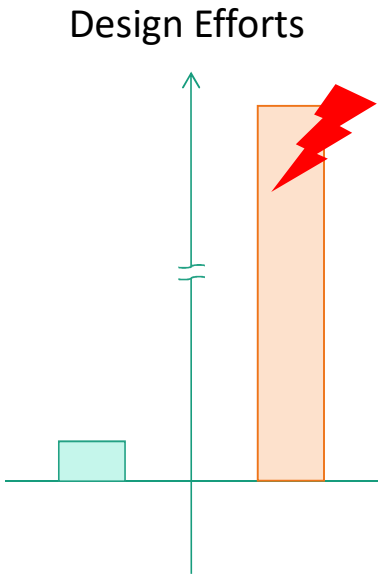
Relevance and Challenge of Analog IC Design

Analog vs. Digital – Design Efforts Layout

Digital:



Few 10s of minutes



Analog:

Weeks to months

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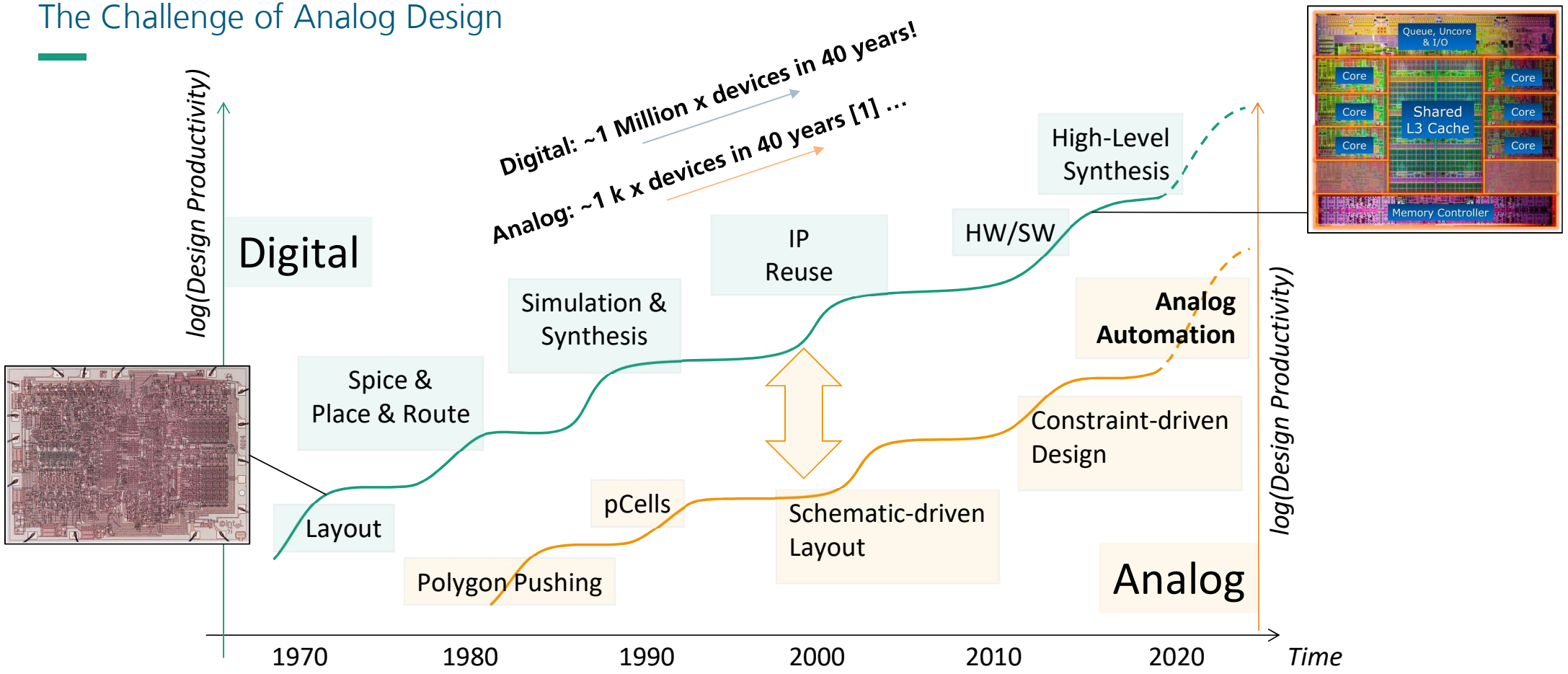
Relevance and Challenge of Analog IC Design

The Challenge of Analog Design



Plot based on ideas from: [eet-china.com], [http://www.eet-china.com/news/article/201606221630]

[1] J. Scheible. "Optimized is Not Always Optimal - The Dilemma of Analog Design Automation." In Proc. of ISPD '22, March 27-30, 2022, Virtual Event, Canada, ACM, New York, NY, USA, 8 pages https://doi.org/10.1145/3505170.3511042

Chip-photo 1971: [theregister.co.uk, https://www.theregister.co.uk/2011/11/15/the_first_forty_years_of_intel_microprocessors/]
Chip-photo 2012: [gamestar.de,http://www.gamestar.de/hardware/prozessoren/intel-core-i7-3960x/test/intel_core_i7_3960x_sandy_bridge_e,389,2562037.html]

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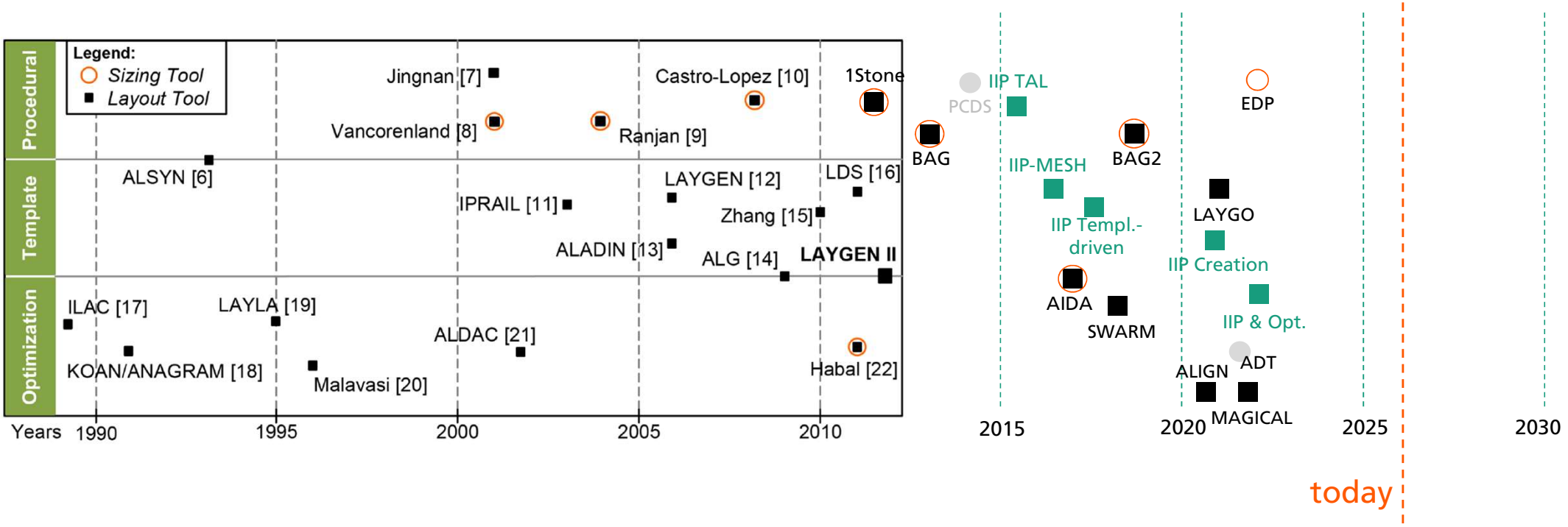
Brief State of the Art in Analog IC Design Automation

The underlying Methods – Overview of (some) former Work



[Ricardo Martins, Nuno Lourenc¸o, and Nuno Horta, „LAYGEN II—Automatic Layout Generation of Analog Integrated Circuits ,“IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 32, NO. 11, NOVEMBER 2013]

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Brief State of the Art in Analog IC Design Automation

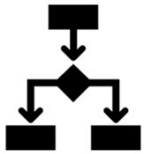
The underlying Methods – Overview and Challenges

Methodological Approaches

Optimization-based
- Utilizes constraints & objectives
- Searches a solution in the *unknown* solution space

Templates
- Is a special form of a constraint
- Pre-defines geometry

Generators
- Are procedural and executable programs
- A *known strategy* tackles a given problem



Related Challenges

Optimization-based
Who defines the constraints & objectives?
Is the solution found good enough?

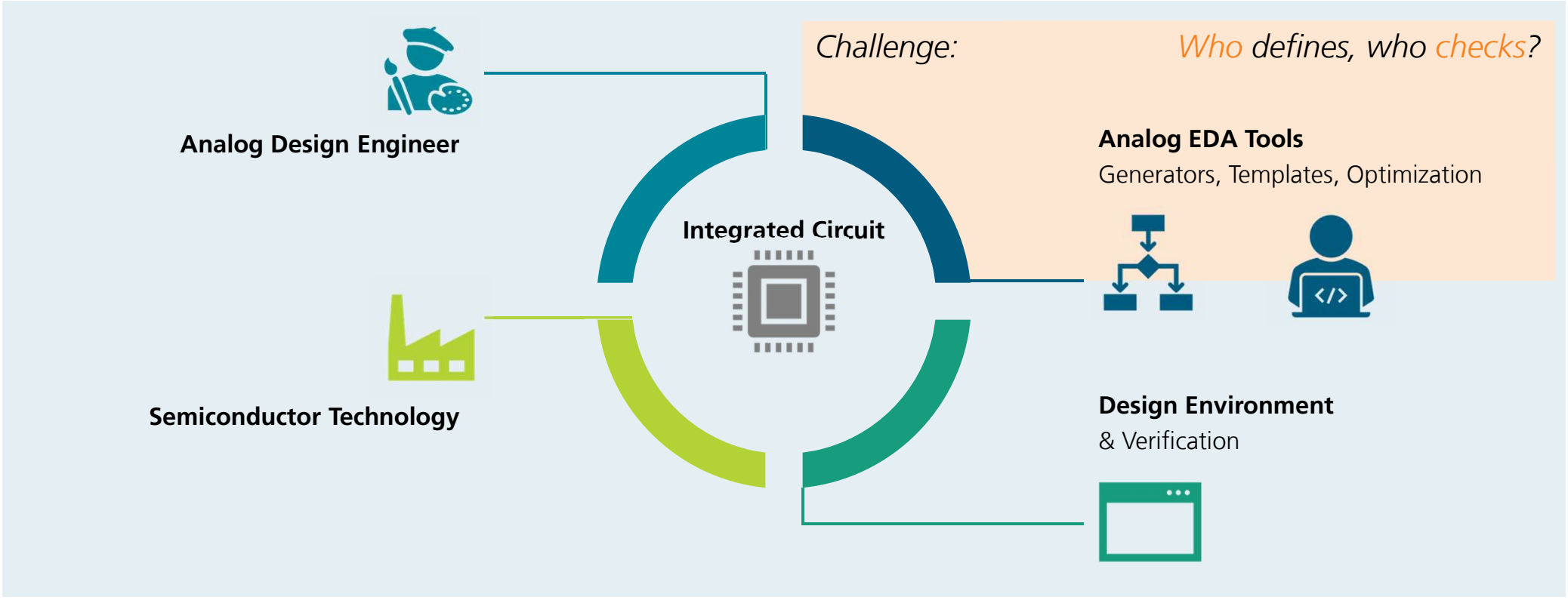
Templates
Who defines the templates?
Is the pre-defined geometry good enough

Generators
Who writes the generators?
Is the procedural strategy good enough?

How to integrate these methods into projects and design flows?

How to Integrate these Methods into Projects and Design Flows?

Who and what is involved?



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How to Integrate these Methods into Projects and Design Flows?

The underlying Methods – Overview and Challenges

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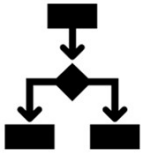

Setup

Optimization
Design Expert
(EDA Expert)

Template
EDA Expert
(Design Expert)

Generators
EDA Expert

Usage

Design Expert

Design Expert

Design Expert

How to treat this communication barrier?

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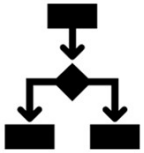

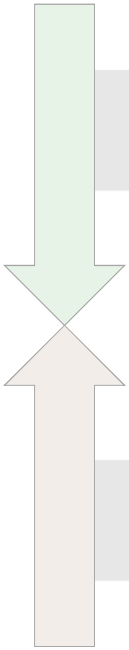

Enable flexible variant **search**

Combination of the approaches is promising: **„Meet in the Middle“**

Reuse of Design Expert knowledge

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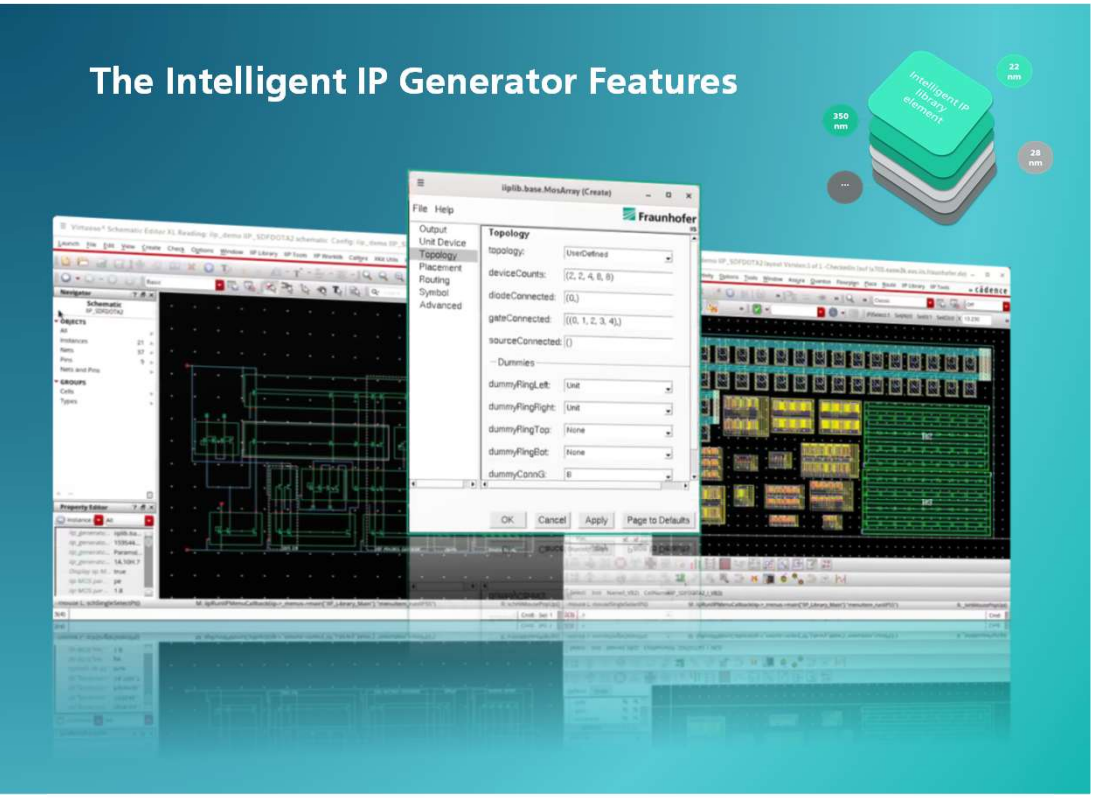
Generators in Analog Design

Core Features of Intelligent IP for Analog IC Design Automation



User-Driven

- Designers have full control, like in pCell handling
- From parameter to whole layout blocks in a matter of seconds
- Custom generators can be created from your design by a klick – or from us as a service

PDK-Agnostic & Full PDK Support

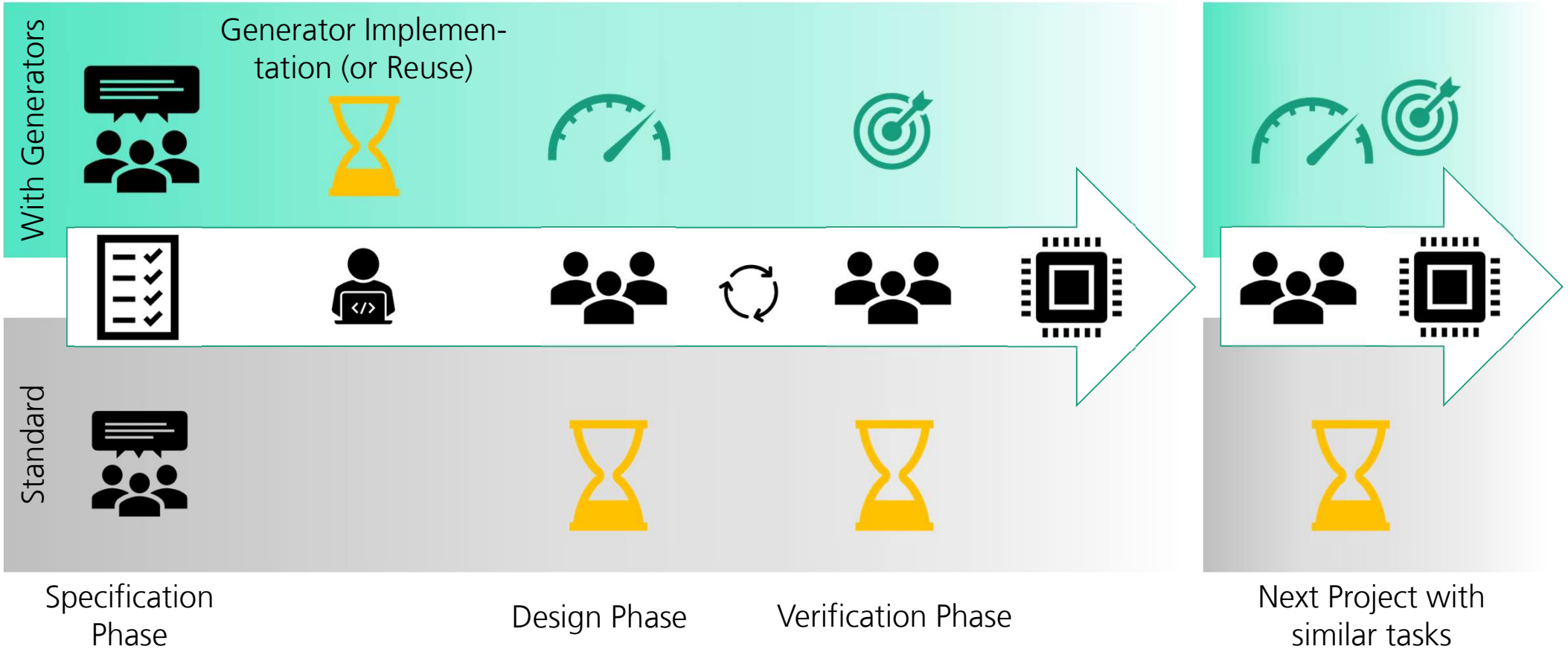
- Support of various foundries, also on-site
- Nodes supported from 350 … 22 nm with PoC <=16nm
- PDK pCells are always used same as designers would do

Fully Flow-Compatible & Full Design Data

- IIP is embedded into the design environment for full control for the designers
- IIP generates schematic, symbol & layout cells into library
  - Generated cells are accessible also without IIP tool
  - Generated cells can be fully edited by designers

Generators in Analog Design

Standard Design vs. Custom Generators for Repetitive Layouts



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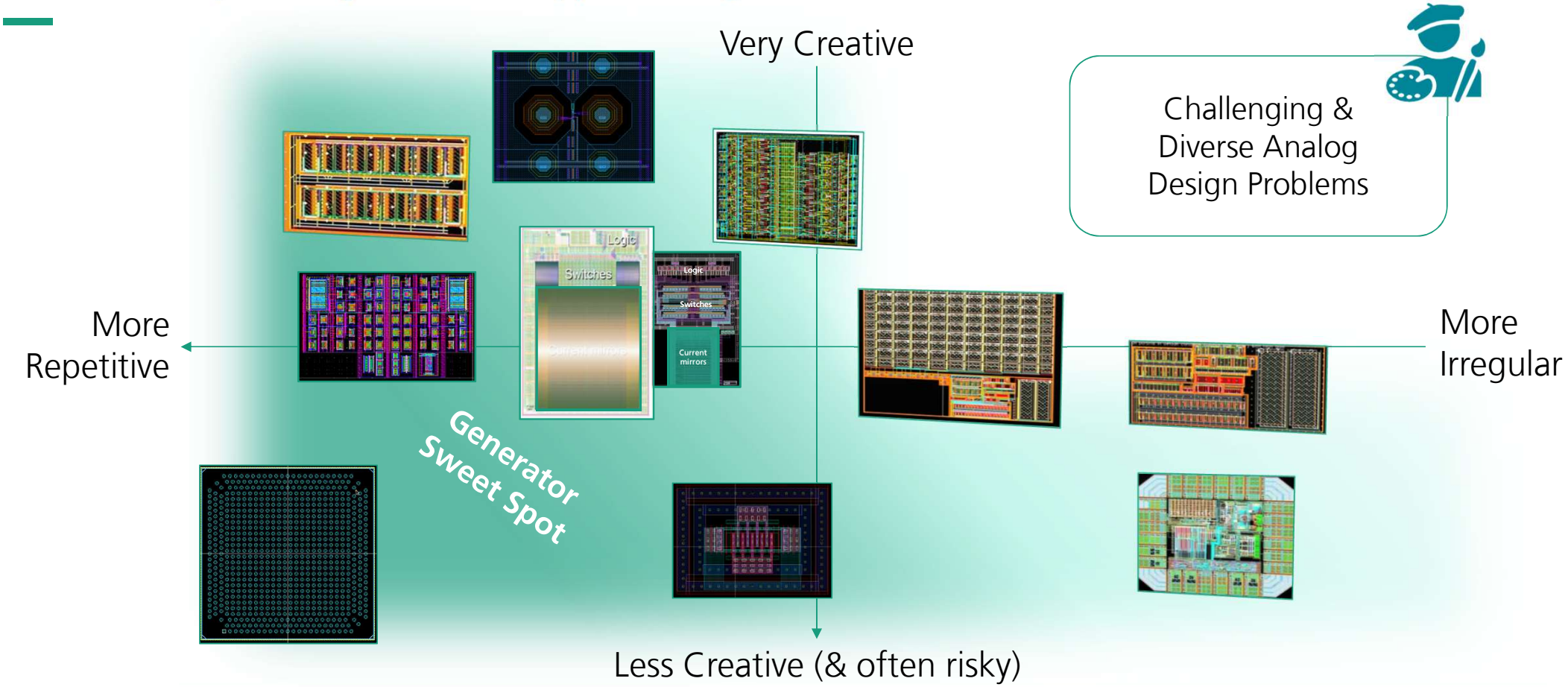
Generators in Analog Design

More Efficiency in Design: How IIP Supports Designers



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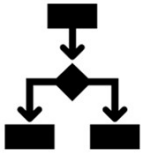

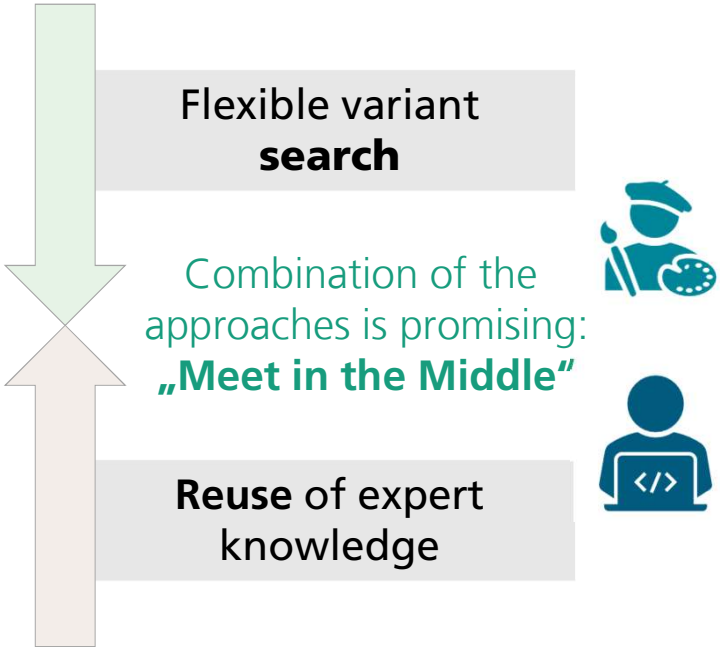

Community and Exchange will be Key!

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Conclusion and Outlook

Conclusion

Analog IC design is *complex and challenging*

Good communication **between both Design Experts and EDA Experts is Key**

There is probably *no one-size-fits-all solution* in analog EDA

Combining methods **should be considered in both analog design and EDA**

Both **design experts and EDA experts should closely align with each other!**

Conclusion and Outlook

Outlook

Good communication

- We should find ways for exchange among both design experts and EDA experts (Conferences, Education, ….)
- What we think is hard-to-realize might not be for the other expert – and vice versa!

Combining methods

- Sweet spot: The methods used must serve problem solving (but identifying it might be hard – communication!)
- Specifically, generators that utilize templates might be the missing link to combine knowledge-based methods and optimization

Usability is key – Analog EDA should be thought from the designer’s perspective

Thank You for Your Attention

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