Substrate Netlist Extraction in Analog Design

With PNAware and PNAwareRC

Klaus Heinrich

March 2026

Setting the benchmark in **Design Support**

Through our **comprehensive design and prototyping support**, we enable first-time-right designs not only for digital, but also for **analog mixed-signal designs**.

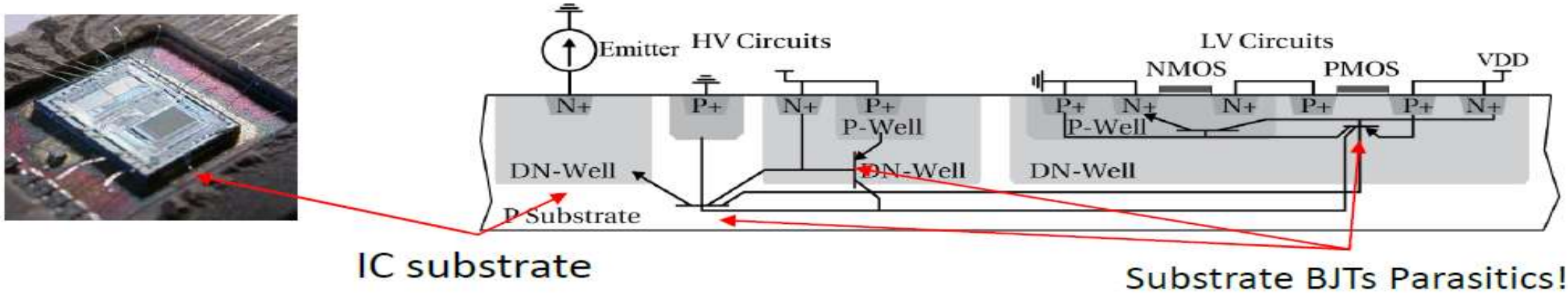
- **Feature-rich, proven design kits**: The solid basis for your designs with full access to all process features
- **Unique X-FAB tools** to solve design challenges, accelerate the design process and enable first-time-right design
- **Support for multiple EDA vendors**: Choose the flow which fits best to your needs
- **Expert support** when needed, from idea to design, tape-out, prototyping and production
- **Largest foundry IP offering**: Reduce design risk and improve time-to-market

PNAware XSUB

parasitic substrate netlist extraction tool for HV-CMOS

Motivation:
Re-designs due to substrate coupling

- A Re-design root cause in Smart Power ICs, like motor drivers
  - some customers are affected by Re-designs due to unwanted substrate coupling
  - today these problems are handled by hand, Trial & Error by very experienced designers after measured silicon: time consuming!
  - Substrate coupling is an active and distributed large signal problem
  - not locally concentrated
  - AC simplifications do not work



Motivation:
Re-designs due to substrate coupling (2)

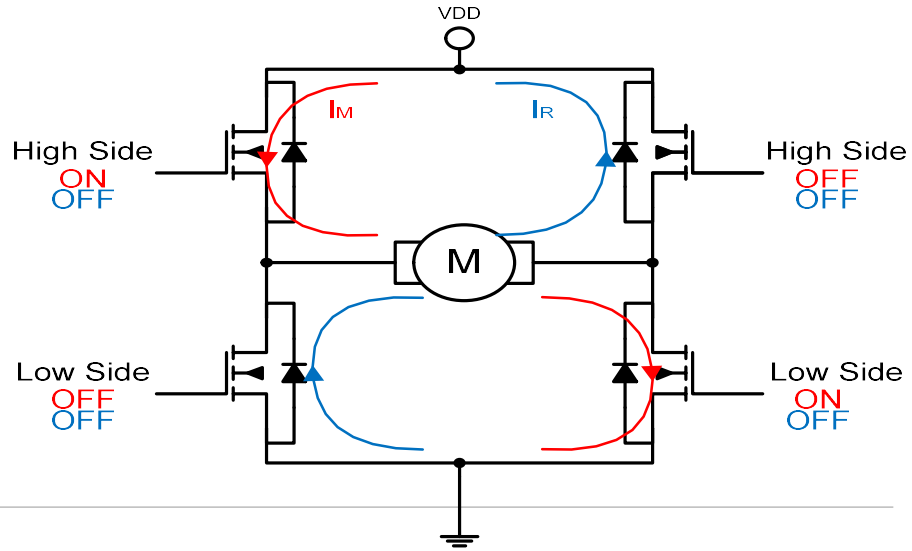
- EMC, e.g. DPI Tests (=Direct Power Injection, P<=36dBm=4W)
  - significant portion of DPI problems is accounted to substrate coupling in HV-CMOS

- Motor driver guardring concept insufficient
  - Most critical situation: Drain below ground (after LS transistor switched off)
  - Minority carriers (Electrons) can travel several mm in the substrate to any N-type Well
  - Severe disturbance of sensitive circuits

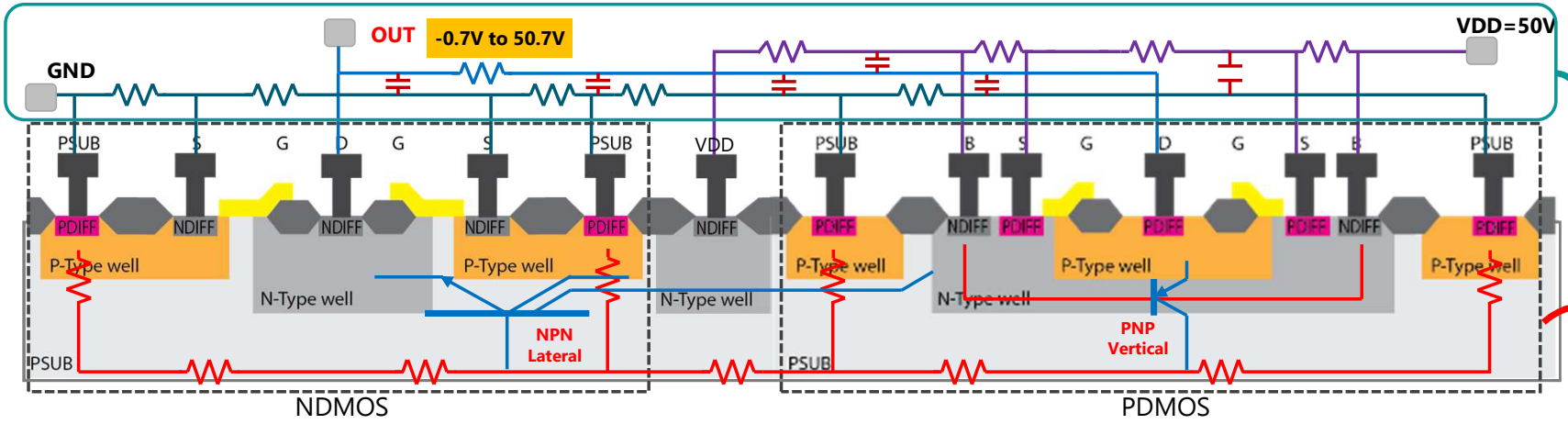
    like Bandgaps, ADCs, Pre-drivers…

- Such Re-designs are expensive

  full mask re-designs



Parasitic Elements in HV-CMOS processes

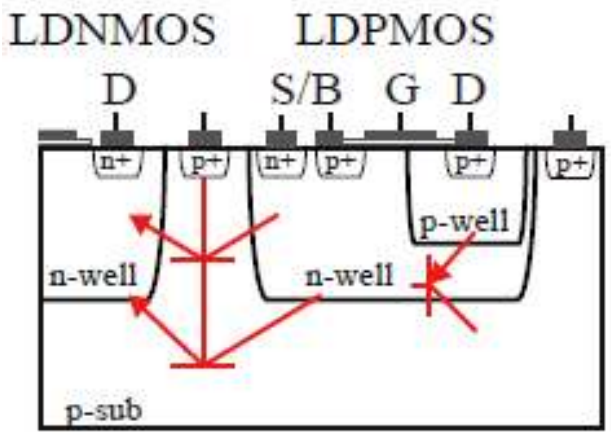


- Metal interconnect and substrate diodes extraction for noise coupling simulations
- Lateral NPN and vertical PNP bipolar transistors. If activated, they generate substrate currents!
- Challenges in control, design and causes failures!

A solution exists

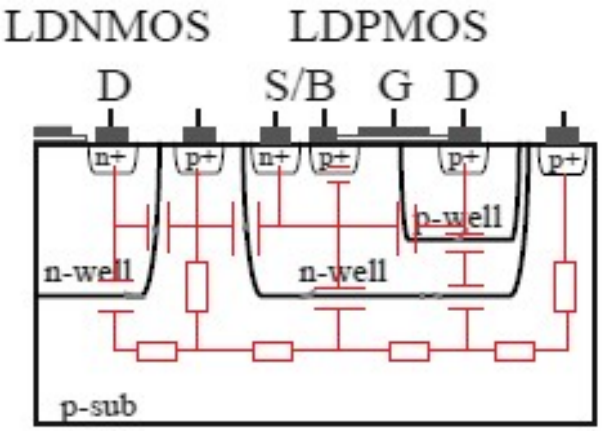
PNAware

Extraction of **substrate lateral bipolar transistors** in with junction-isolated technologies

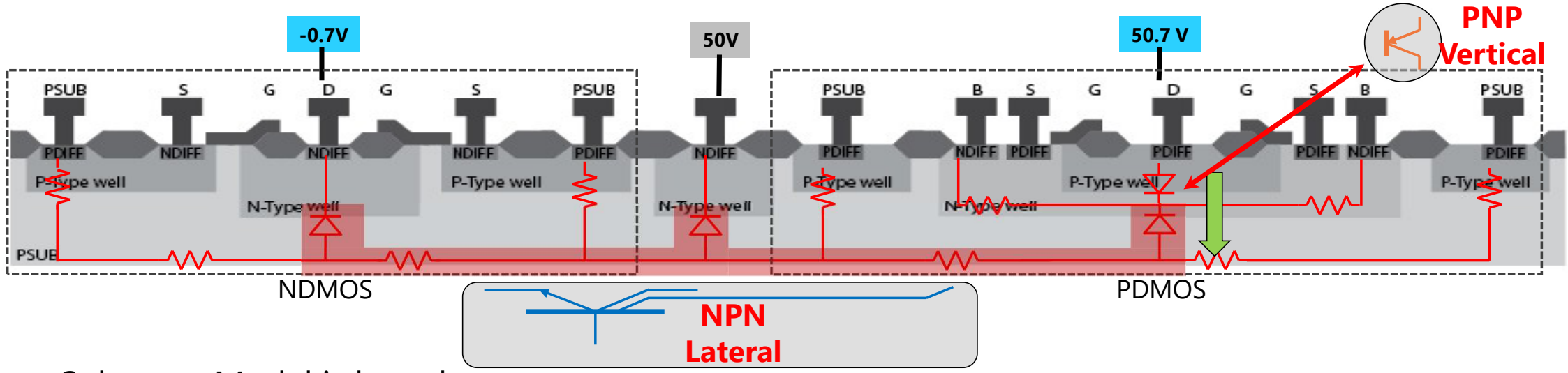


PNAwareRC

Extraction of **substrate passive RC** network



PNAware - Substrate Model Approach



Substrate Model is based on:

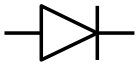
a) Detection of parasitic pn-junctions in substrate

b) Description of parasitic current propagation in the substrate

c) Description of doping discontinuities at p-p+ or n-n+ substrate contacts

Parasitic bipolar transistors are **automatically** detected from layout

PN Diode



PN Resistor

PN Homo-Junction

PNAware - 3D Substrate Model

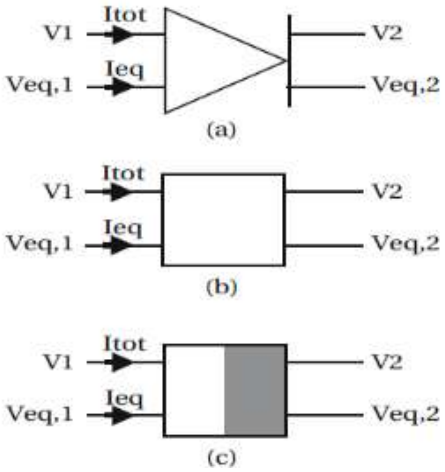
Introduction of three devices with four terminals:

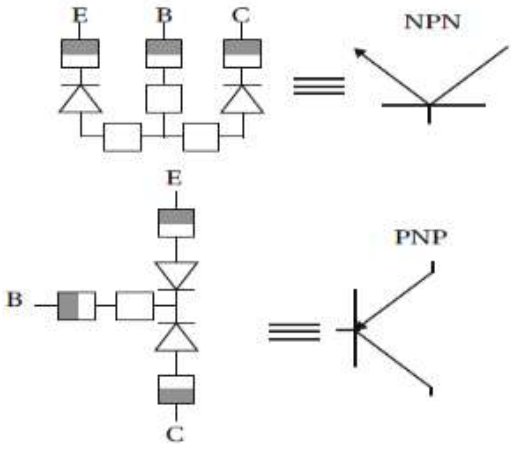
- top terminals carry substrate voltages and currents
- bottom terminals carry equivalent voltages and currents which are proportional to excess minority carrier concentration and their gradient.

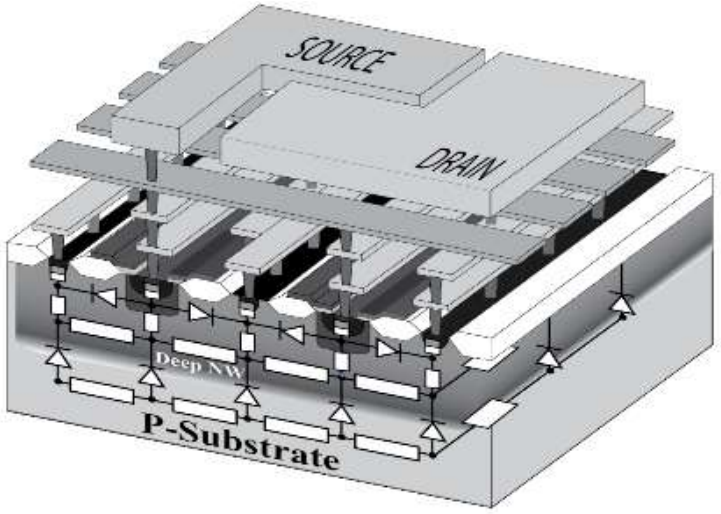
PN Diode

PN Resistor

PN Homo-Junction

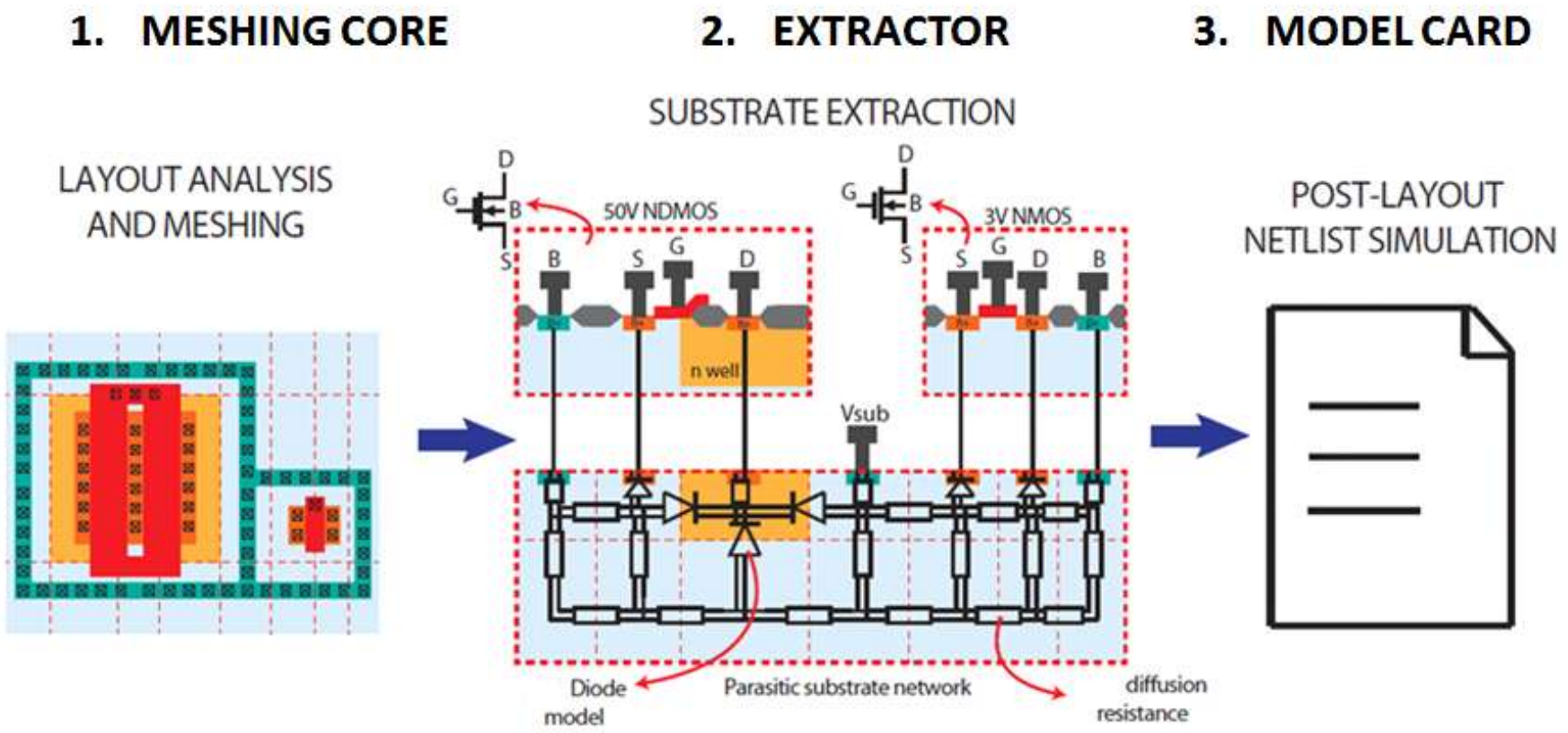






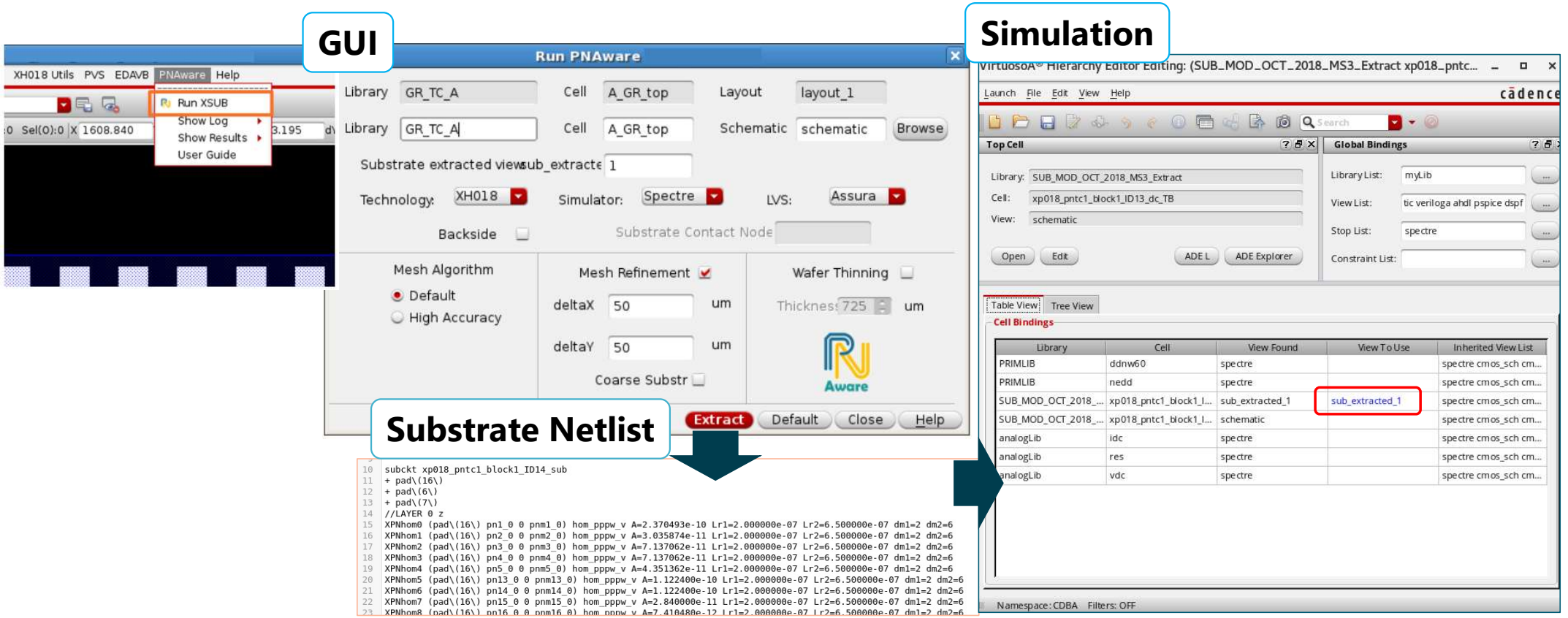
C. Stefanucci, P. Buccella, M. Kayal, J.M. Sallese, Spice-compatible modeling of high injection and propagation of minority carriers in the substrate of Smart Power ICs, Solid-State Electronics *105*, 2015.

PNAware Operation
Core + Extractor + Model



PNAware XSUB: How to use it?

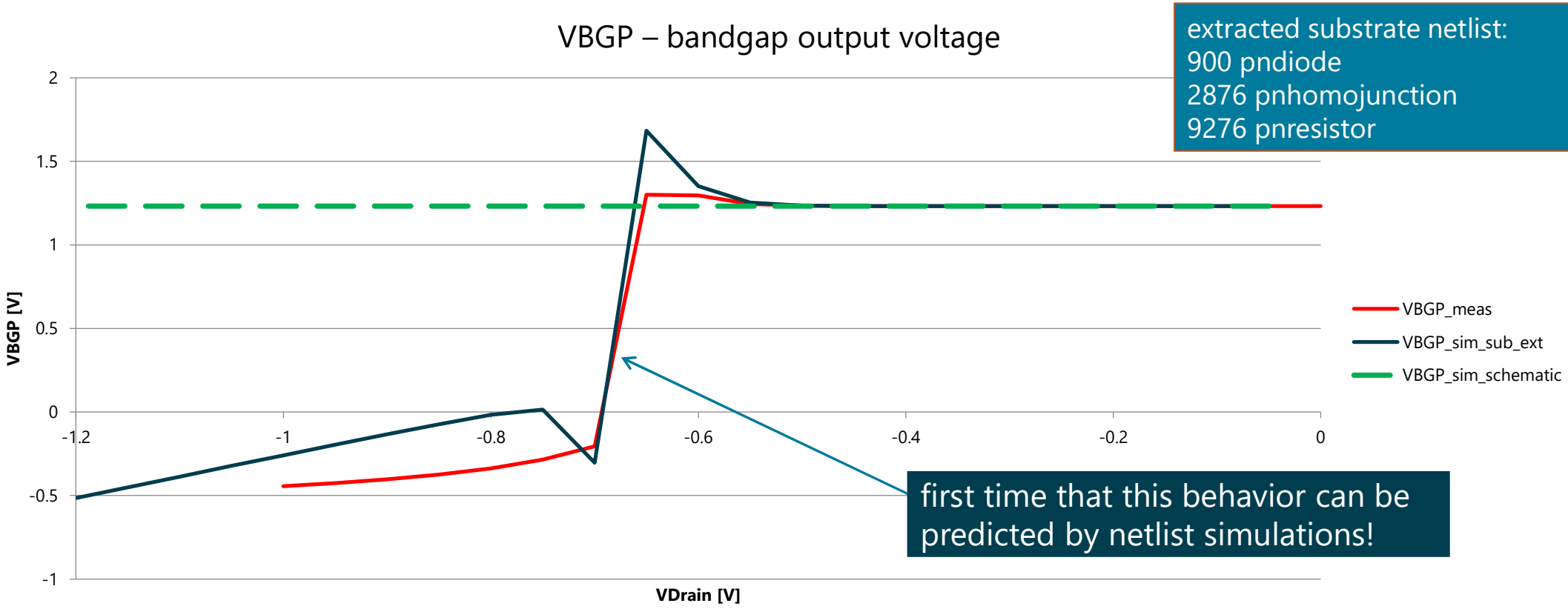
- To run PNAware: 1. LVS clean design. 2. Add recognition layer SUBEXT in layout over regions of interest



Electron Injection test with LDMOS transistor + Bandgap

Drain of NDMOS is pulled below substrate potential and injects electrons
-> no N-type-Well guardring around the LDMOS
-> electrons collected in Bandgap at all NWell connections (pmos, resistors, bipolars)

extracted substrate netlist:
900 pndiode
2876 pnhomojunction
9276 pnresistor



first time that this behavior can be predicted by netlist simulations!

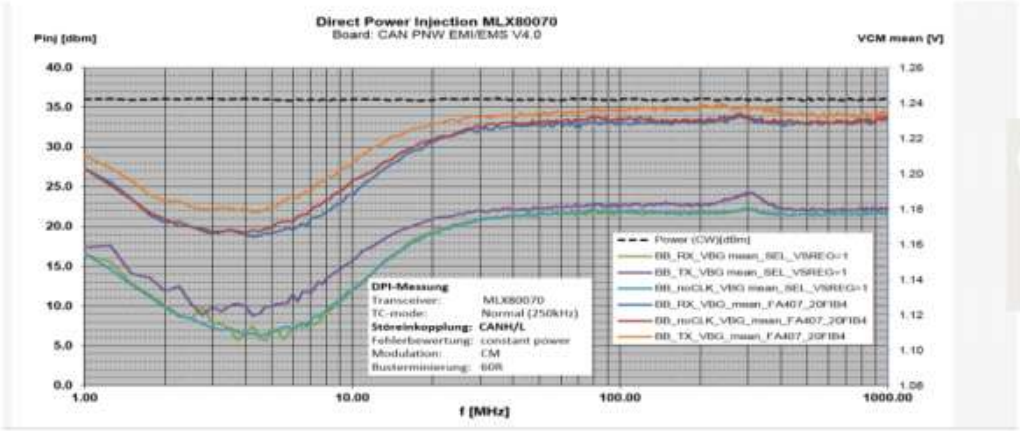
PNAware RC

parasitic substrate netlist extraction tool for SOI

motivation:
Re-designs due to substrate coupling

- Re-design root cause in automotive ICs , like CAN-FD-TRX: parasitic Substrate Couplings
  - Even very experienced customers are affected by Re-designs due to unwanted substrate coupling
  - today these problems are handled by hand, Trial & Error by very experienced designers after measured silicon: time consuming!
  - Substrate coupling in Bulk-CMOS is in most cases a distributed multi-collector lateral bipolar problem
  - Substrate coupling in SOI is in most cases a passive RC coupling problem

Measurement results under DPI stress on CANL/H



Dip of the bandgap voltage (VBG and VBG_TC) at low frequencies in between 1 .. 20MHz

PNAwareXSUB for substrate netlist extraction in HV-Bulk CMOS

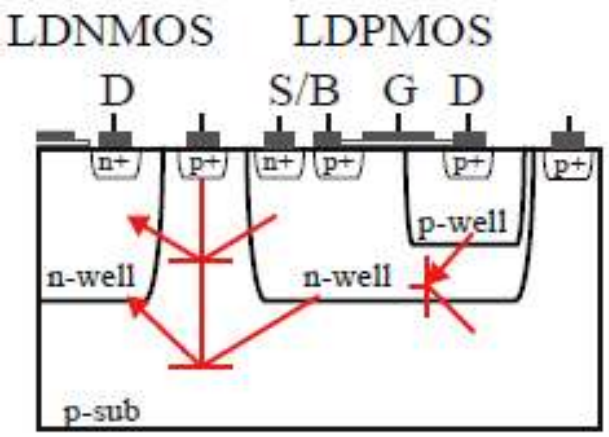
PNAwareRC for substrate netlist extraction in SOI.

Picture taken from Technology Conference 2022, Dirk Nuernbergk

A solution exists

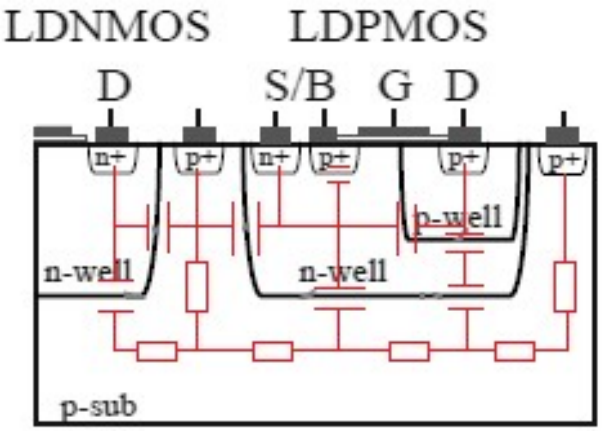
PNAware

Extraction of **substrate lateral bipolar transistors** in with junction-isolated technologies



PNAwareRC

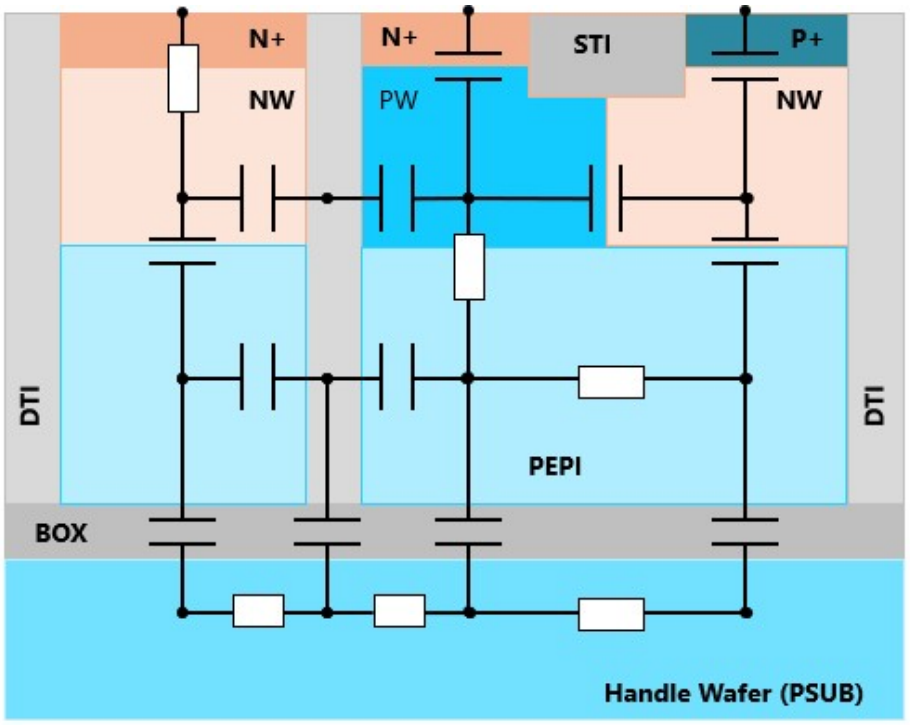
Extraction of **substrate passive RC** network



PNAwareRC: SOI process

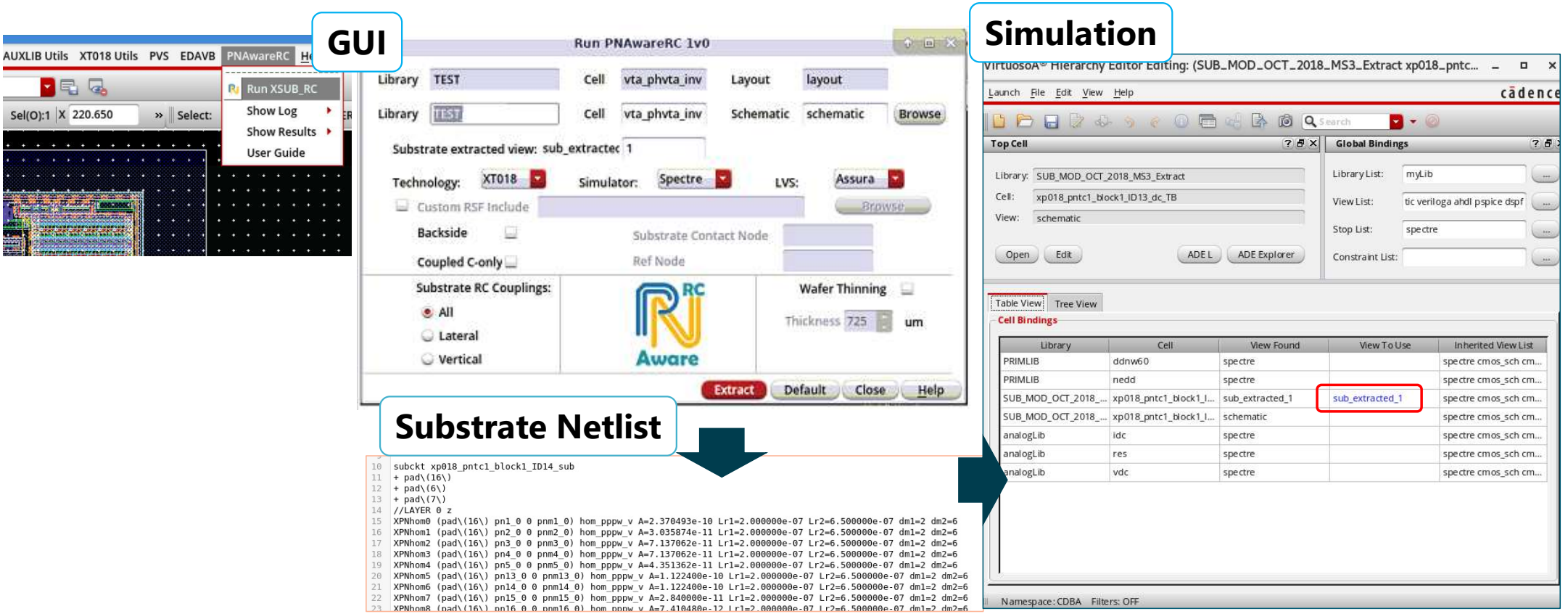
- Even in SOI technologies, the isolation is not perfect, as passive R and C couplings are still present

- In SOI, PNAwareRC extracts a passive RC network including lateral and vertical coupling paths resulting from DTI and BOX isolations



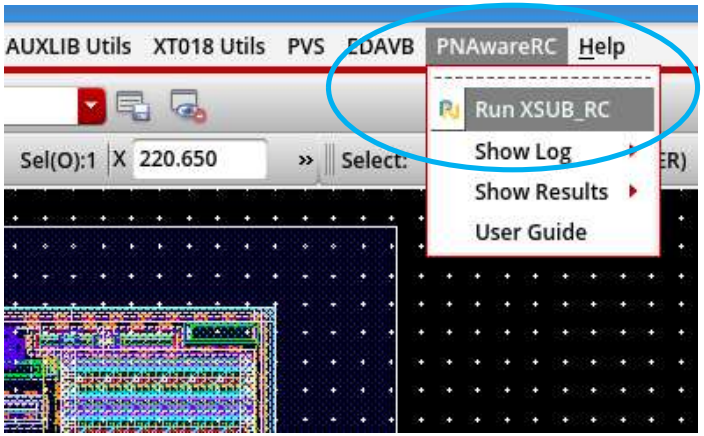
PNAware RC: How to use it?

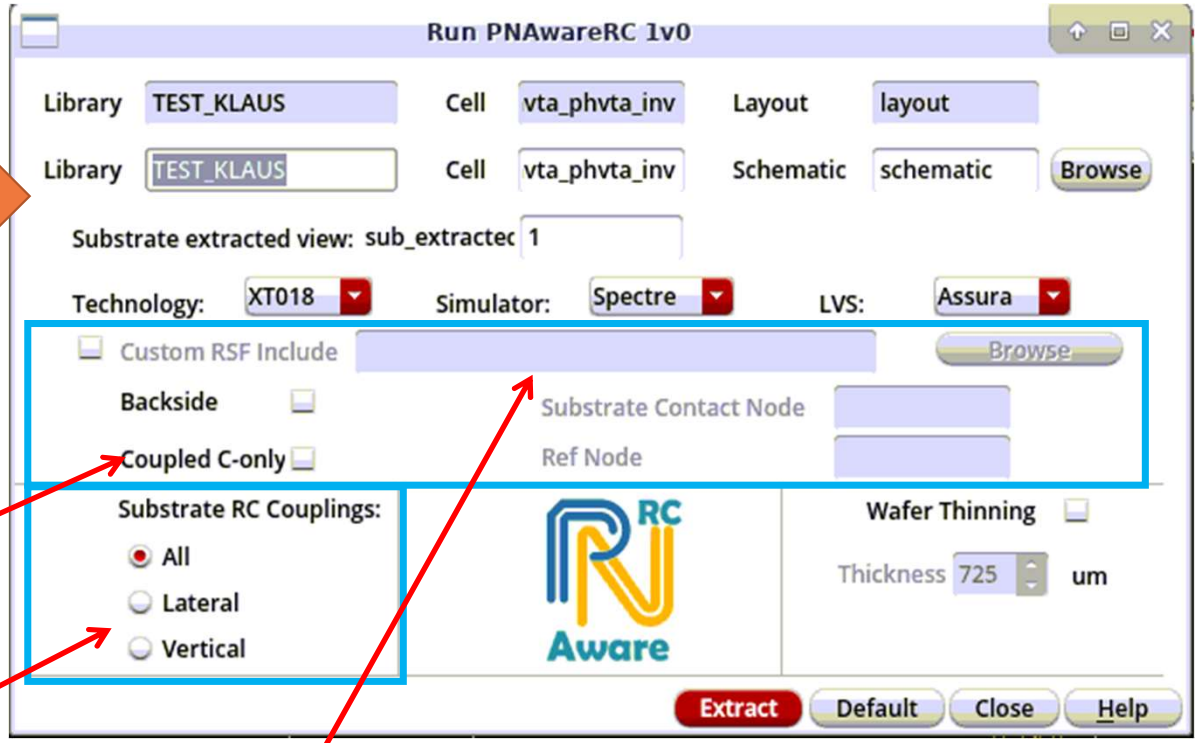
- To run PNAwareRC: 1. LVS clean design. 2. Add recognition layer SUBEXT in layout over regions of interest



PNAwareRC: useful extraction options

- Launch PNAwareRC -> Run XSUB_RC





- Backside contact
- Wafer thinning
- **include parasitic metal caps (Coupled C-only)**
- **RC Coupling modes**
- **Customer specific RSF include file (if LVS switches are needed to get a clean LVS)**

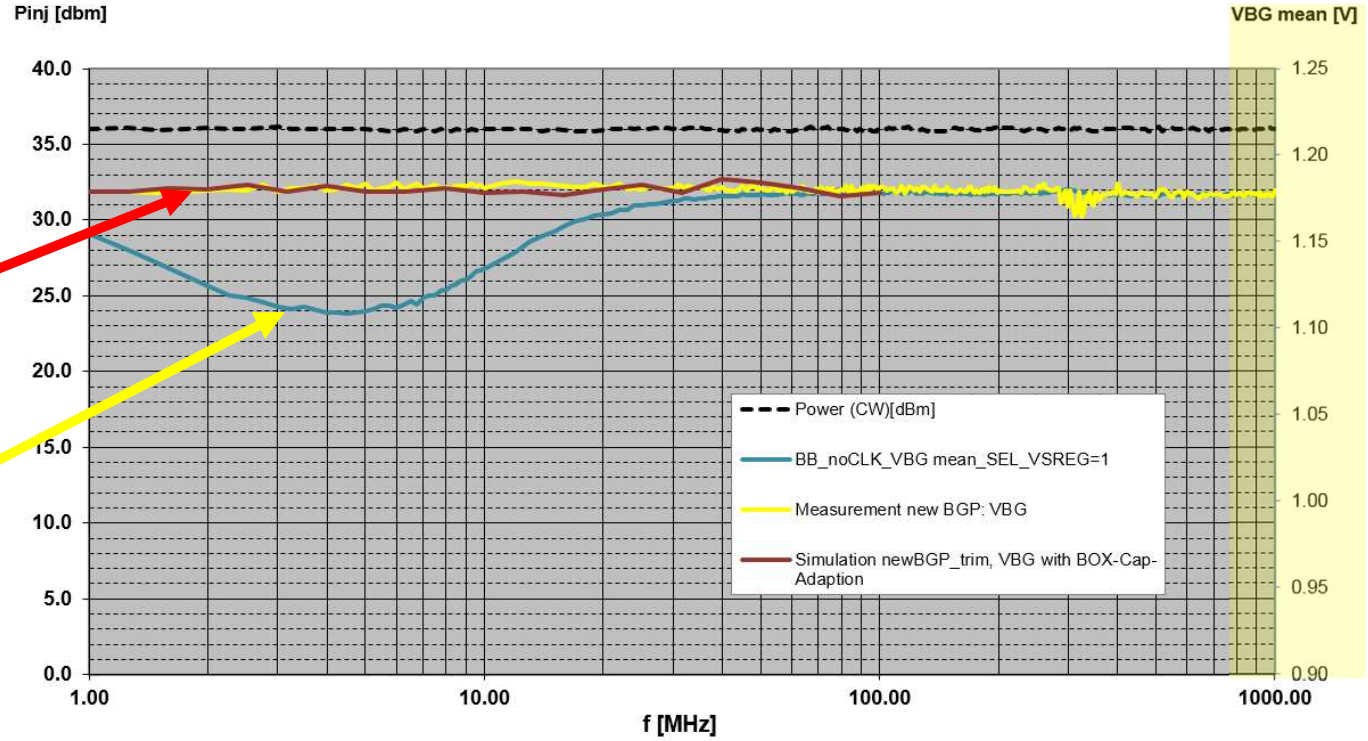
Simulation results vs. measurement (bandgap voltage) –new BGP

- Re-design: Shielding of Diff-Pair by GND connection of substrate and other topology changes

- Good fit of measurement and simulation

Measurement new BGP

Measurement old BGP



Picture taken from X-FAB Technology Conference 2022, Dirk Nuernbergk

Summary

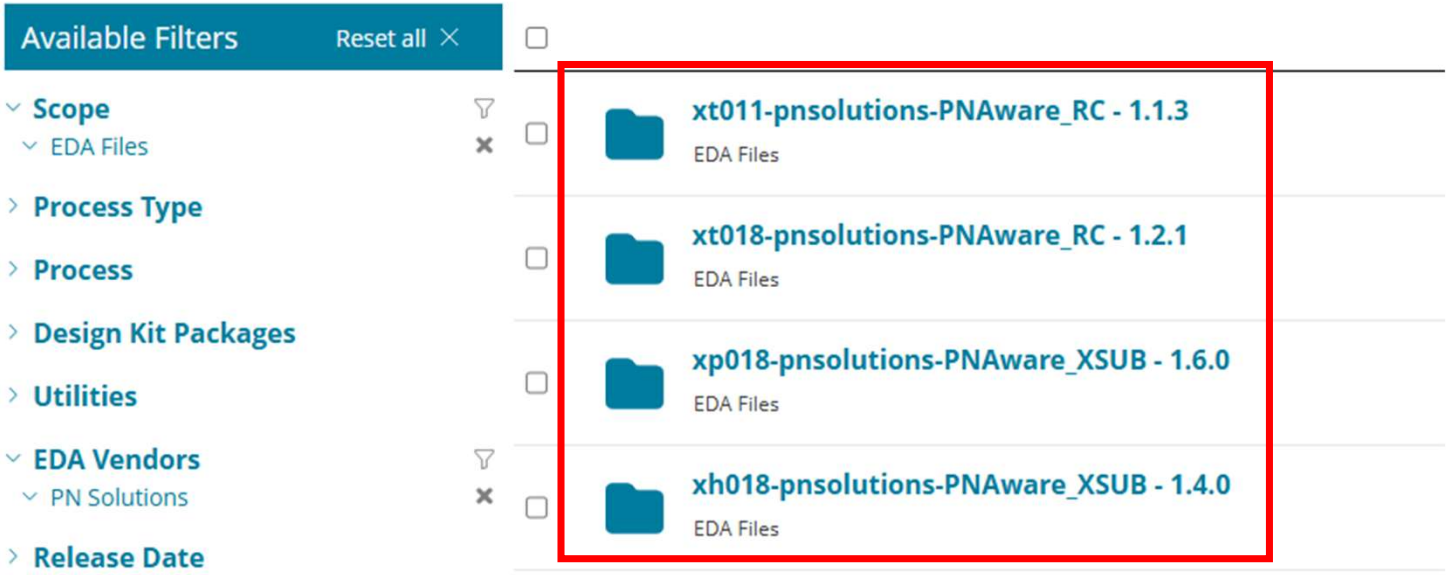
✓ PNAware - PNAwareRC: reduce the risk of re-designs

- ✓ Post-layout parasitic extraction Tools → post-layout substrate netlist including all relevant active and passive elements in the substrate
- ✓ Enable designers
  - to evaluate substrate problems by means of circuit simulation
  - to assess potential substrate coupling problems before the 1st Tape-Out
  - to evaluate circuit and guarding concepts with better immunity to substrate coupling

PNAware XSUB and PNAware RC: Integration in XFAB PDKs

- PNAware XSUB available for HV-CMOS:
  - XH018 Cadence PDK
  - XP018 Cadence PDK

- PNAware RC available for SOI:
  - XT018 Cadence PDK
  - XT011 Cadence PDK




Everything
you need
to achieve
first-time-
right


xfab
Thank you