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Addressing Electromigration Challenges in 3D Integrated Circuit (3DIC) Wafer-On-Wafer Technology

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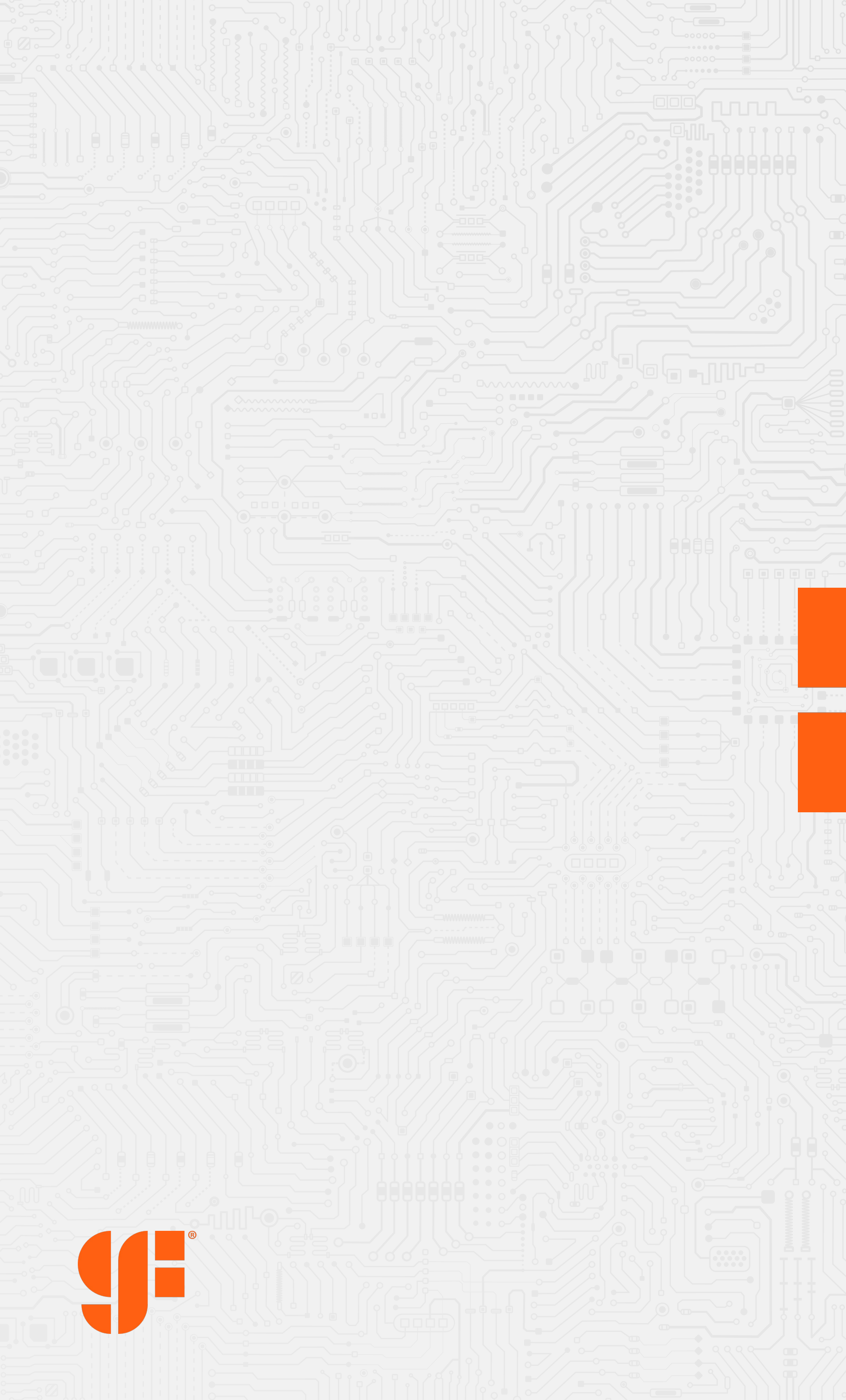
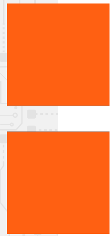
Agenda

- Modelling Electromigration – Heat dependency
- Electro-Thermal Co-Simulation in 3DIC Design
- EDA Flow for Electromigration Analysis with Self-Heating
  - Parasitic Extraction (PEX) and Multi-Wafer Simulation Challenges
  - Modelling Self-Heating and Thermal Coupling for EM in Multi-Wafer 3DIC
- Summary

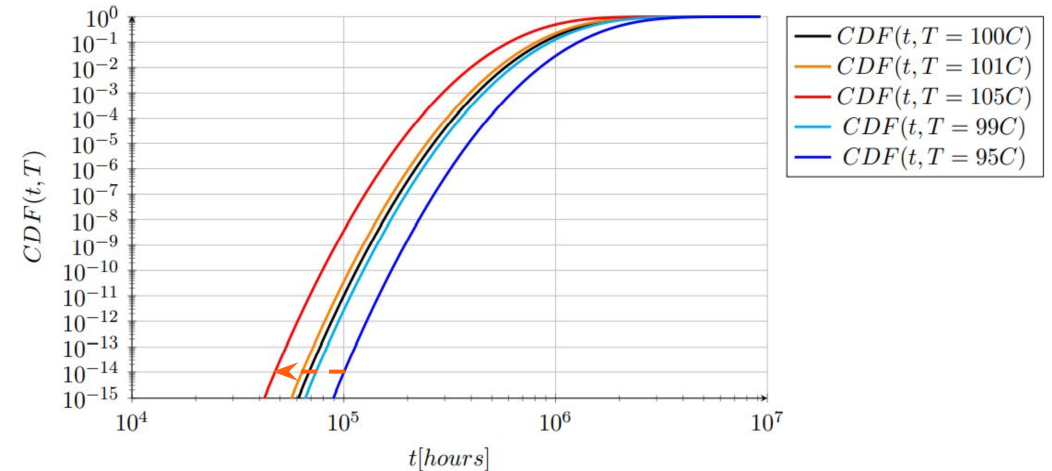
Modelling Electromigration – Heat dependency

Electromigration (EM) and temperature

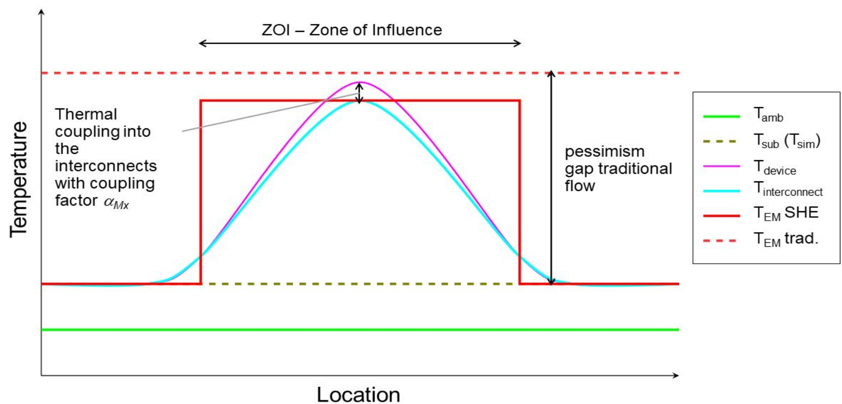
- Temperature has exponential impact on EM, cmp. Black's law

$$MTTF = Aj^{-n}\exp\left\{{E_a}/{k_B T}\right\}$$

- Mean Time To Failure (MTTF) is roughly halved with increased ΔT=10K
- Traditional approach: choose highest temperature in design => leads to overdesign



Cumulative Distribution function for different temperatures, σ=0.4, Ea = 0.9eV, A/j^n=1.025E-6h

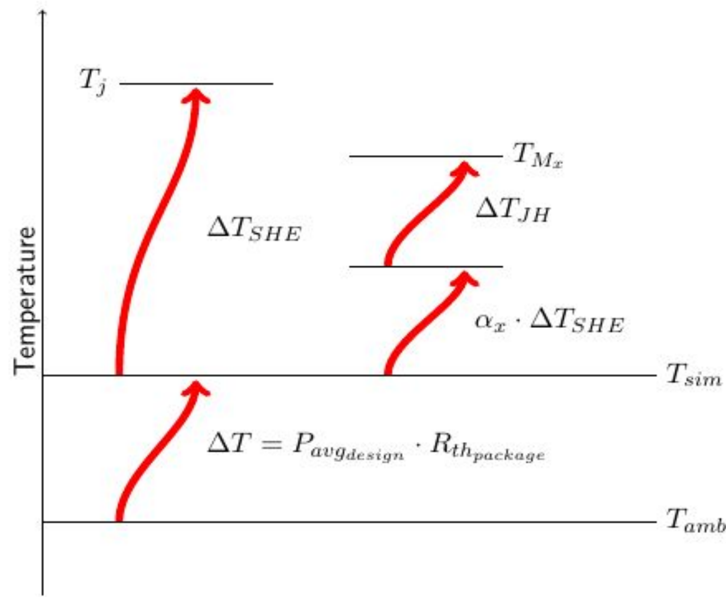


Contributors of Local temperature in a metal segment and different modelling approaches: Traditional vs. SHE

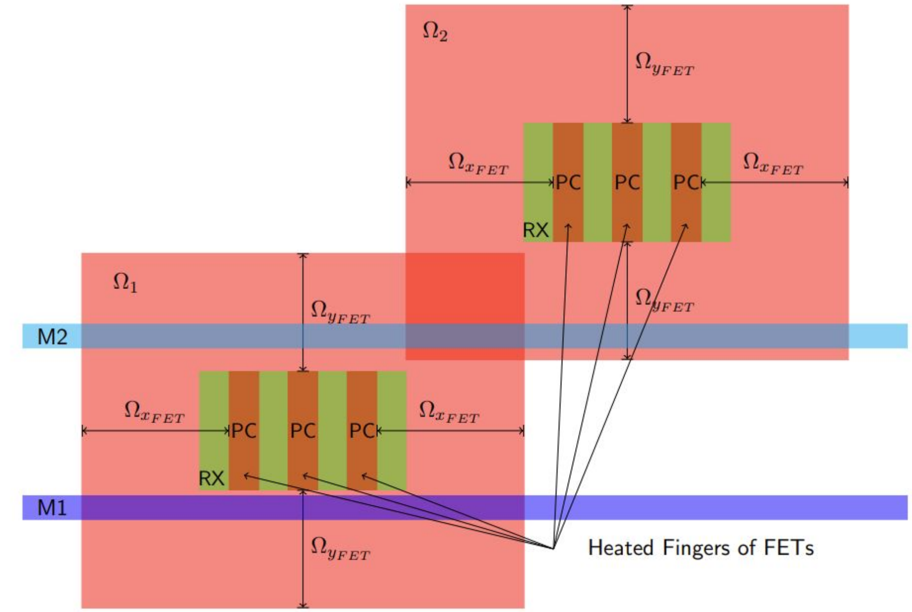
- Self-Heating enabled (SHE) approach takes local device heat ΔT_{SHE} into account and applies it to Back-End-Of-Line (BEOL)
- Allows a more realistic margining, i.e. sizing of BEOL wires

EM SHE: How is it modelled

- Local device temperature T_j (junction-T) spread to Zone-Of-Influence (ZOI) to model spherical heat propagation
- Overlapping ZOI: take maximum T_j

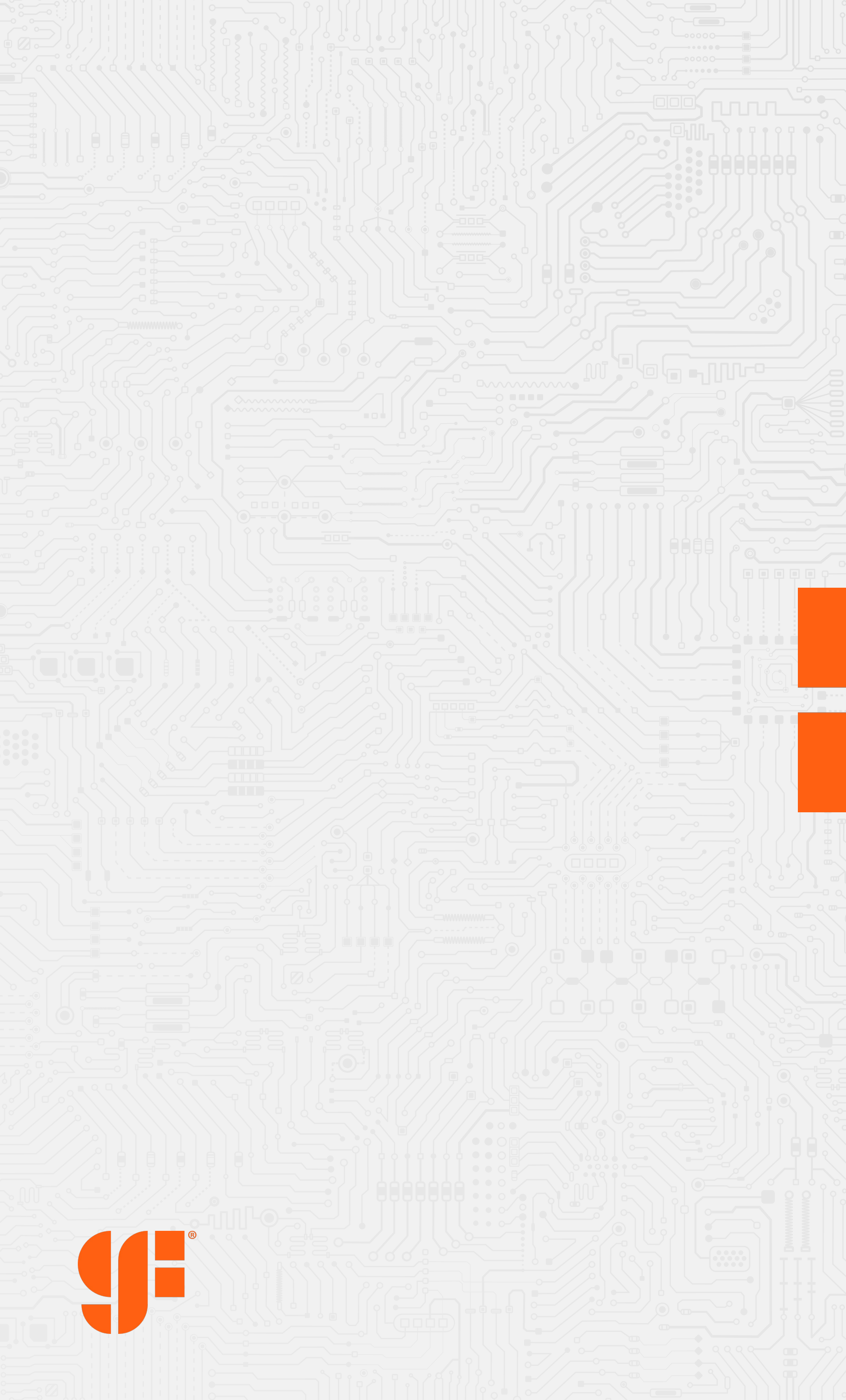
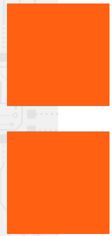


Definition of temperatures in design



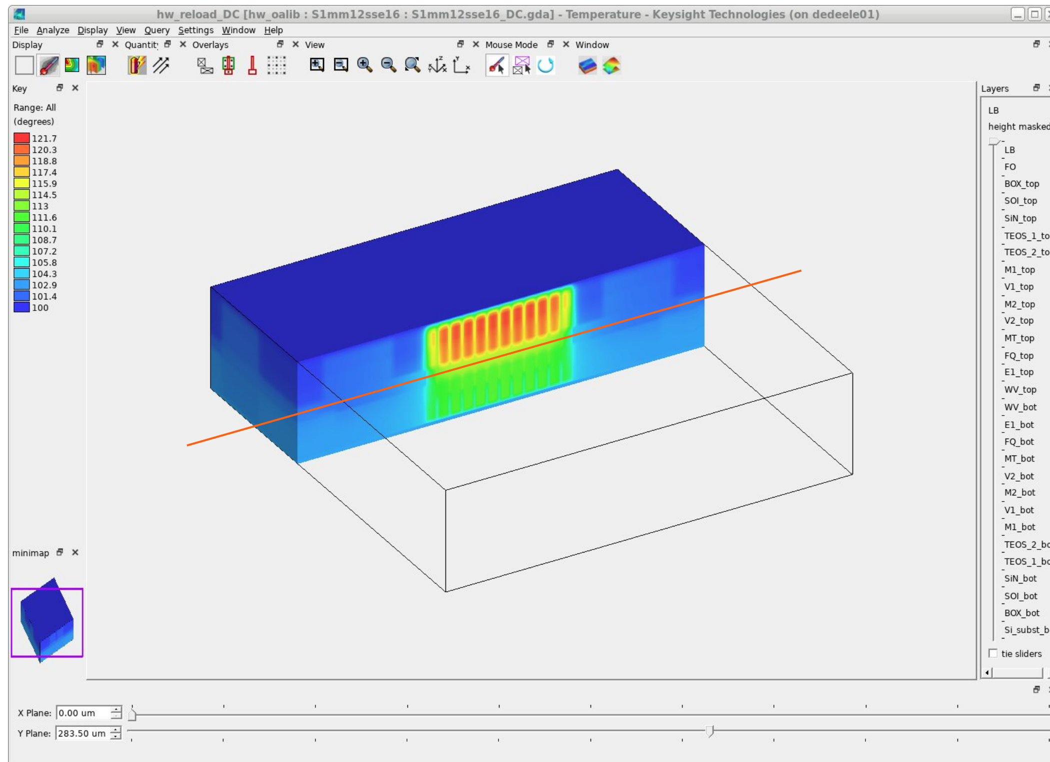
Construction of Zone-Of-Influence (ZOI) around FET

- BEOL is exposed to α_x*ΔT_{SHE} (α_x... thermal coupling factor per layer)
- Final temperature T_{Mx} comprises ΔT_{JH} by Joule heating (self-heating of metal due to rms current) and coupled α_x*ΔT_{SHE} plus T_{sim}

Electro-Thermal Co-Simulation in 3DIC Design

Advantages and thermal challenges of 3DIC circuits



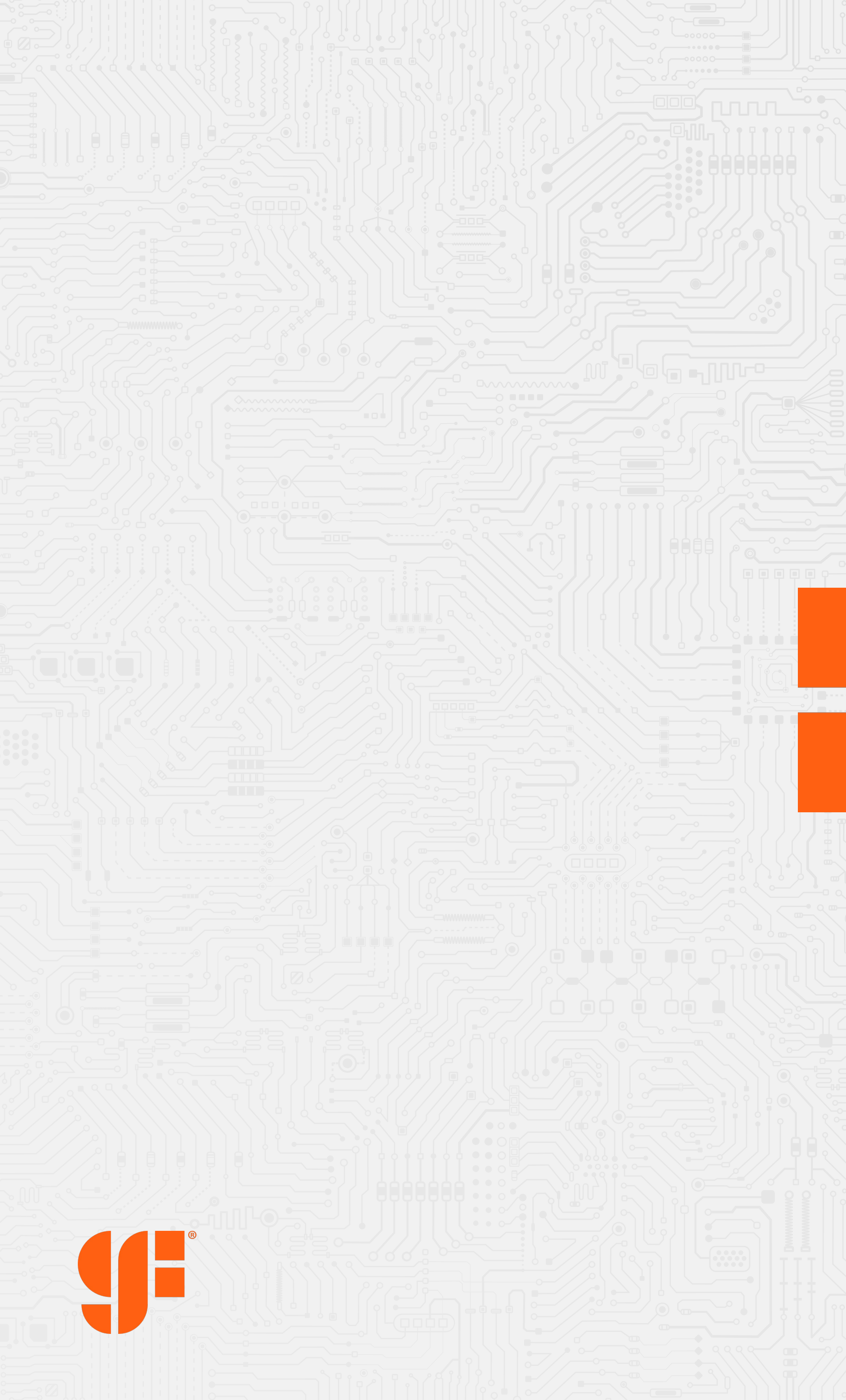
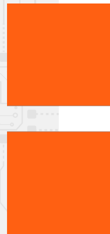
3DIC WoW RF switch Electro-Thermal simulation using Keysight Heatwave, added orange line: split of TOP and BOT wafers, z axis not proportional

- **Advantages of 3DIC stacking**
  Vertical stacking shortens signal paths, enhancing ***RF performance*** in 3DIC circuit designs.
  Stacking multiple dies vertically significantly boosts ***integration density*** in 3DICs.

- **Thermal Management Challenges**
  Proximity of heat sources in stacked dies exacerbates ***thermal issues*** in 3DIC designs that can result in performance and reliability issues

- **Electro-Thermal Co-Simulation (ETCosim)**
  Combining electrical SPICE simulation with FEM thermal solving enables precise temperature effect analysis. Package boundary conditions are considered. EM+SHE coupling coefficients and ZOI extensions are determined from ETCosim.

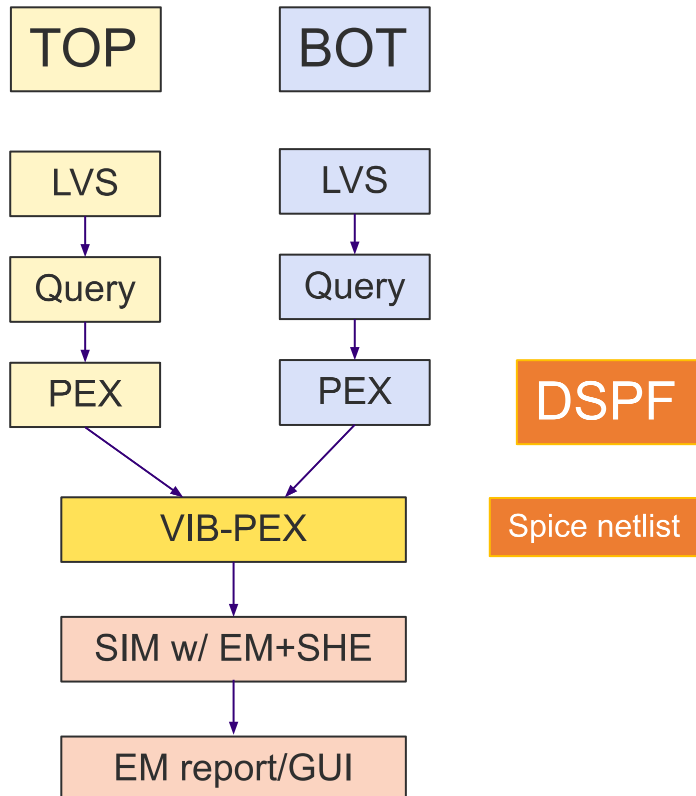
ETCosim serves as an input for Self-Heating enabled Electro-Migration analysis

EDA Flow for Electromigration Analysis with Self-Heating

EMIR flow for 3DIC

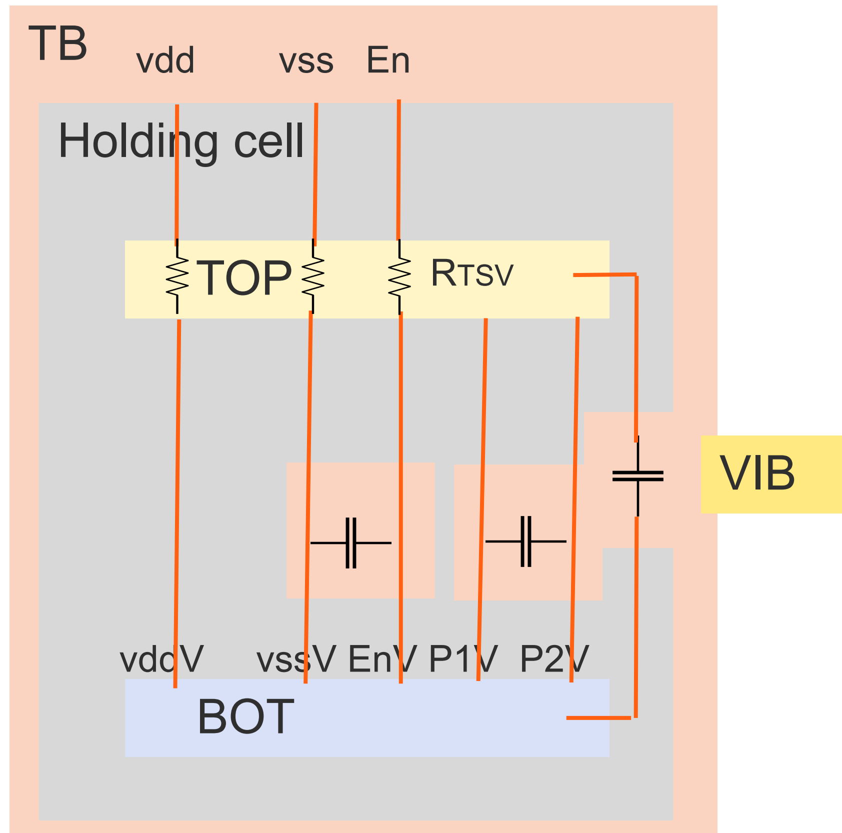
Example two wafers



- Separate run of LVS and PEX for TOP and BOT wafers
- Results in two DSPFs, dspf_top and dspf_bot
- VIB-PEX generates a spice netlist containing cross couplings between wafers
- During SIM (simulation), original circuits will be replaced with DSPFs from TOP and BOT
- Additionally, VIB is plugged in by „include“ statement
- SIM can be performed as MTS (Multi-technology simulation) if models or corners differ for TOP and BOT
- EM needs to be run separately with current EDA tool support

Legend: TOP top wafer, VIB virtual interface block, BOT bottom wafer

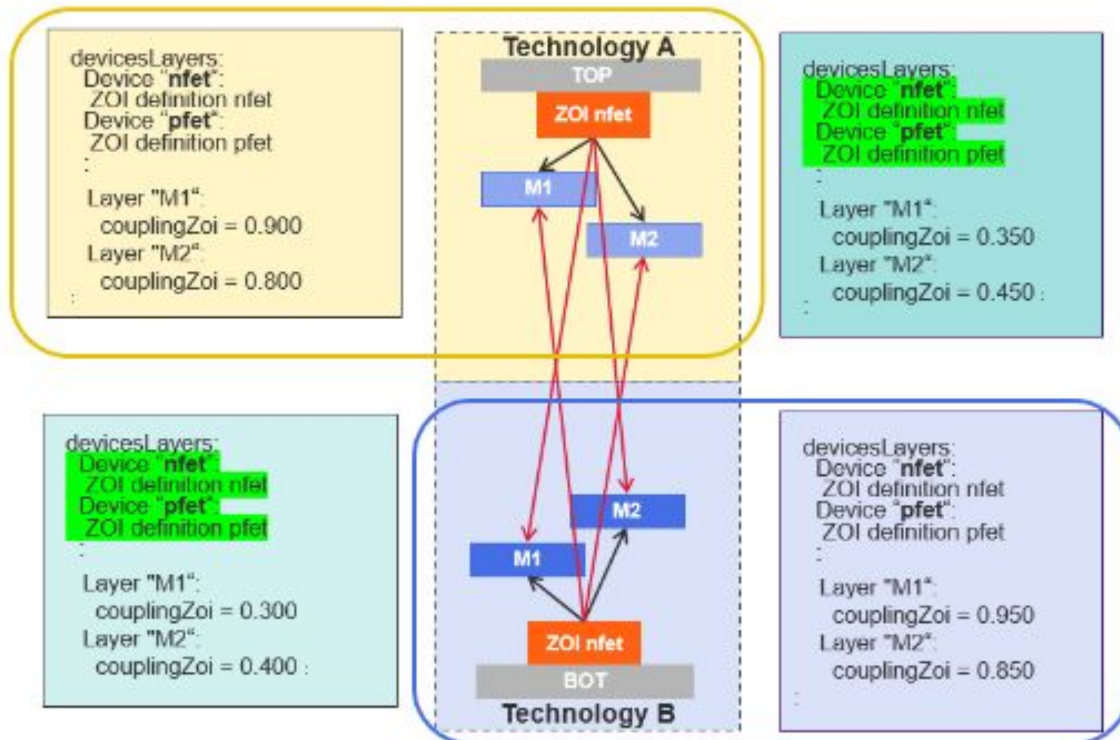
Parasitic Extraction (PEX) for 3DIC, VIB



- LVS/PEX is done for each wafer one-by-one
- Between two touching wafers a so-called Virtual Interface Block (**VIB**) is extracted that contains coupling capacitances of near metals of the opposite wafer
- VIB does not introduce a new hierarchy, additional C's are instantiated at test bench (**TB**) level
- EDA tools must handle VIB extraction
- Extensible to any number of wafers

=> PEX effects can be added modularly

3DIC EMIR+SHE Thermal coupling model

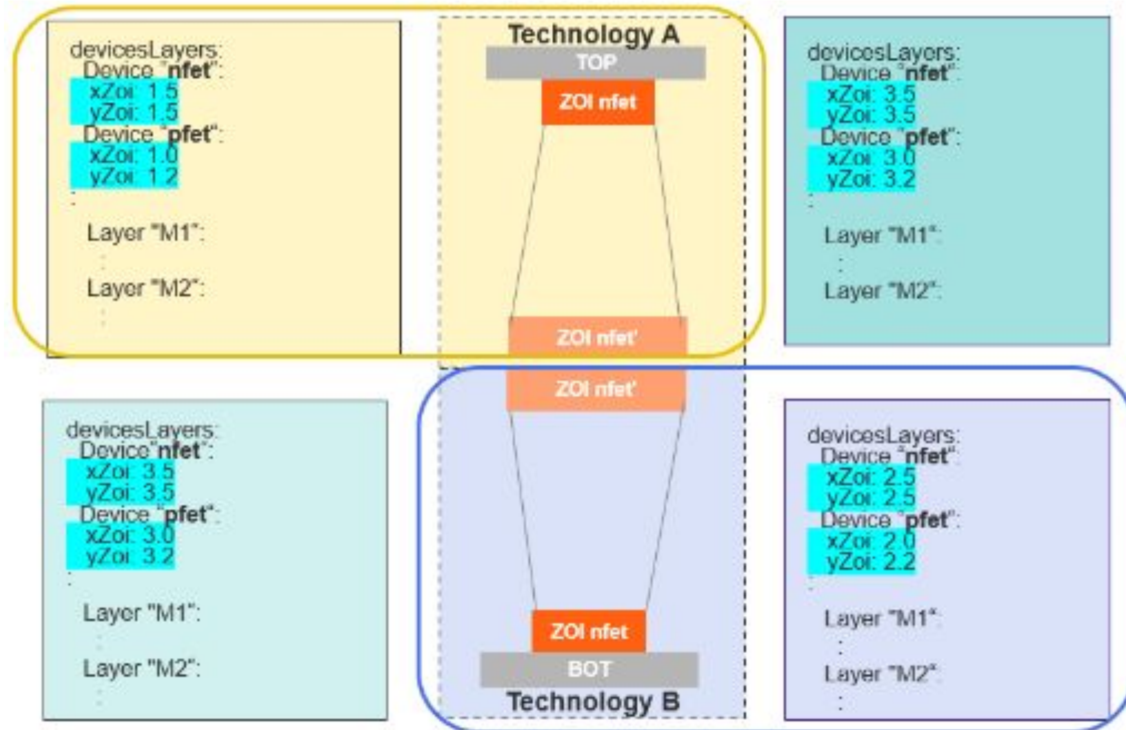


Thermal couplings in wafer-on-wafer back-end-of-line structures

- **Single-Wafer-Coupling**
  Yellow and blue boxes denote self-coupling parameters for each individual wafer in the thermal model. (gray arrows)
- **Cross-Wafer-Coupling**
  Cyan colored boxes represent cross-coupling effects between different wafers in the schematic. (red arrows)
- Each arrow represents a coupling factor.

Coupled temperatures from ZOI_TOP and ZOI_BOT are superposed, i.e. added

3DIC EMIR+SHE - ZOI



- **Zone of Influence Concept**
  Zone of Influence (ZOI) idea applied to the border region of the wafer: ZOI nfet => ZOI nfet'. That represents lateral heat spread.

- **Combinable technologies**
  ZOI and couplings are kept modular
  - One file for each technology (e.g. technology A, technology B)
  - One file for each crossing (e.g. technology A => B)
  - One file for each back crossing (e.g. technology B => A)

Example for two technologies A and B, can be extended to any number of wafers/technologies.

Conclusion: Addressing Electromigration and Thermal Challenges for Robust 3DIC Designs

Electromigration Fundamentals in Electrothermal simulations

Understanding electromigration is crucial for preventing failure in 3DIC wafer-on-wafer technology by improving circuit reliability. Modelling temperature (EMIR+SHE) will help in EM budgeting to avoid over- or underdesign.

Tackling 3DIC Simulation challenges

Parasitic extraction and Self-heating enabled EM analysis were enhanced to 3DIC. An EMIR+SHE model was introduced that shows a full flow for any number of wafers.

EDA Tool support

PEX and single-wafer EMIR+SHE is currently supported by EDA vendors, whereas 3DIC support is still under development. The t-Node approach by GF is ready for extensions, e.g. inter-device coupling.*)

***)See: Markus Herklotz, Ingo Kühn, Oscar Restrepo, Shanthi Siemes, Seungman Choi, Hendrik Mau, 2024, "EDA method to address interconnect reliability and reduce overdesign in custom analog designs", IEEE International Reliability Physics Symposium (IRPS)**

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