



Electromigration verification strategies

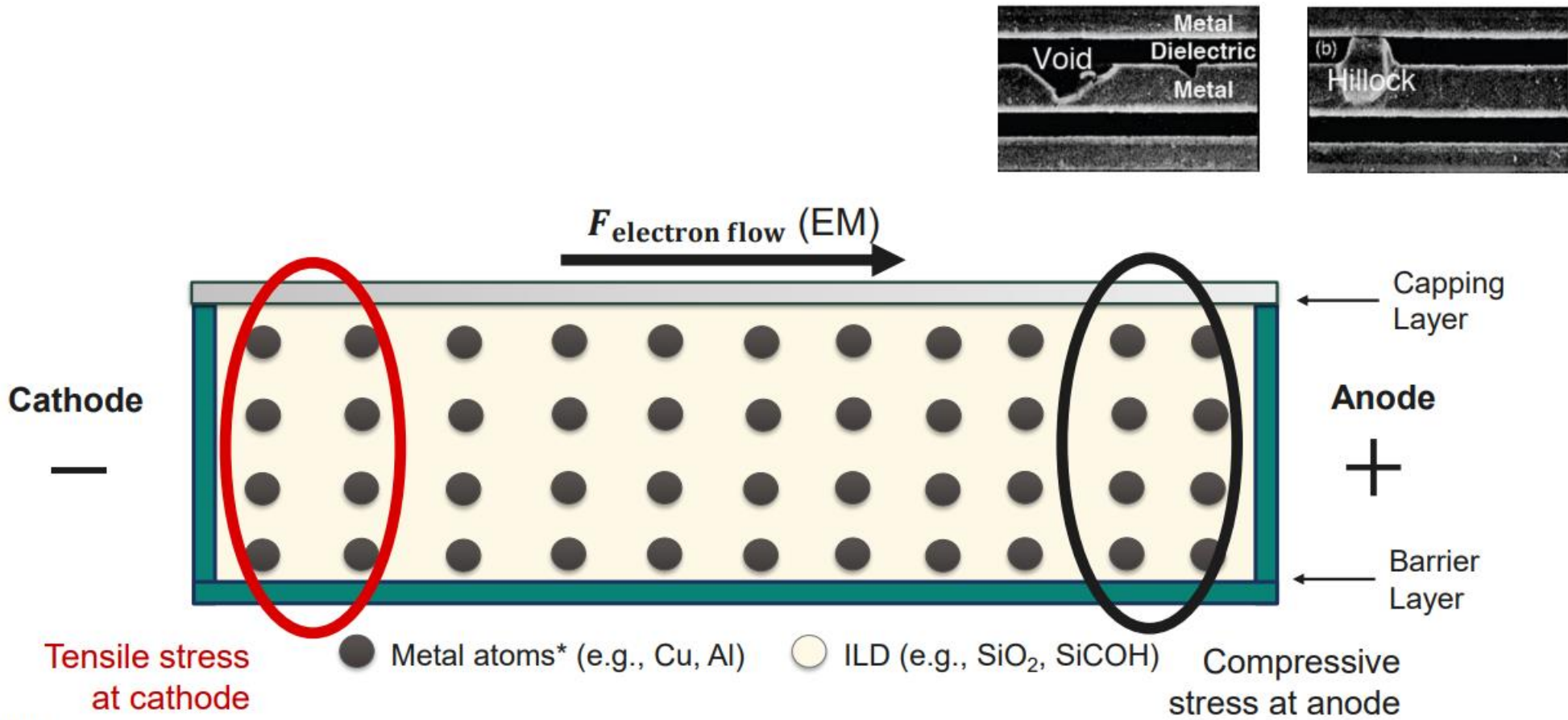
Shanthi Siemes, Principal EM Verification Methodology, Infineon Dresden



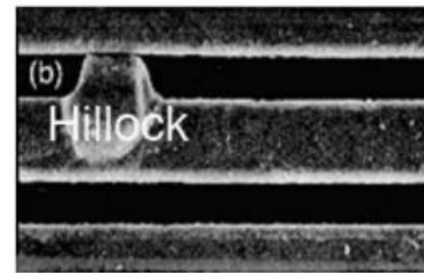
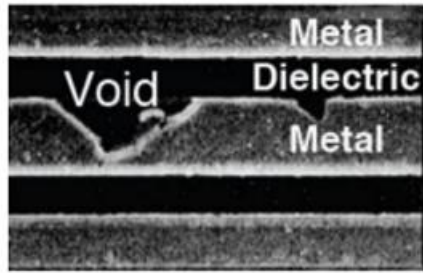
Agenda

- Introduction
- Transition Layers
- Power CMOS
- Hierarchical Flow
- Summary

Electromigration



Electromigration



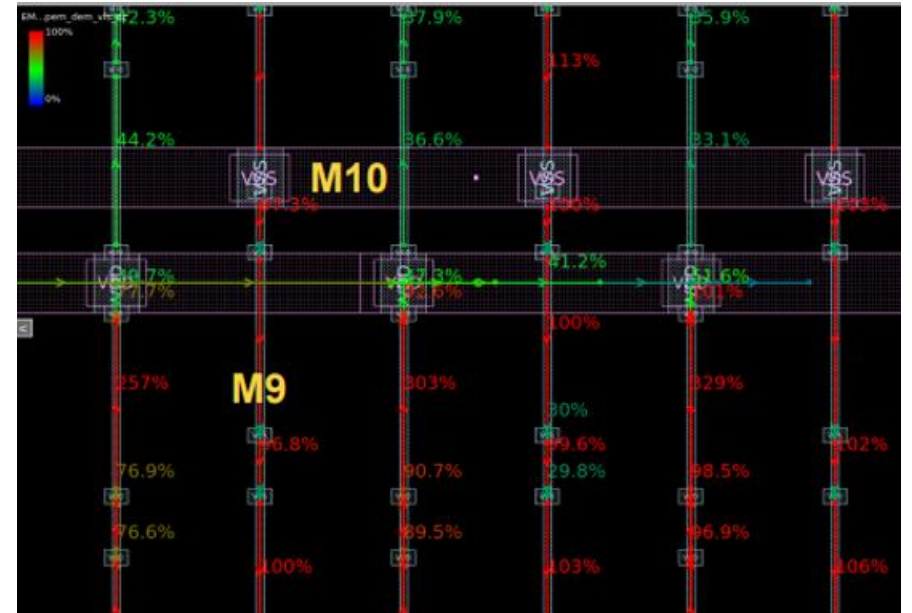
- Gradual displacement of ions in the metal lines
 - Causing open and short circuits
- Occurs when the current density is sufficiently high to cause the drift of metal ions in the direction of electron flow.

- 3 types of electromigration checks
- **Peak:** Prevent immediate melting of wires/vias due to high current density
 - Independent of junction temperature.
 - Thresholds defined in foundry technology file.
- **RMS:** Check for Joule heating effects (ΔT) on the wires/vias
 - Acceptable ΔT is set to 5C
- **DC or Average:** Check for Lifetime/MTTF effects, based on Black's equation
 - Depends on Junction temperature

Transition Layers

Transition layers

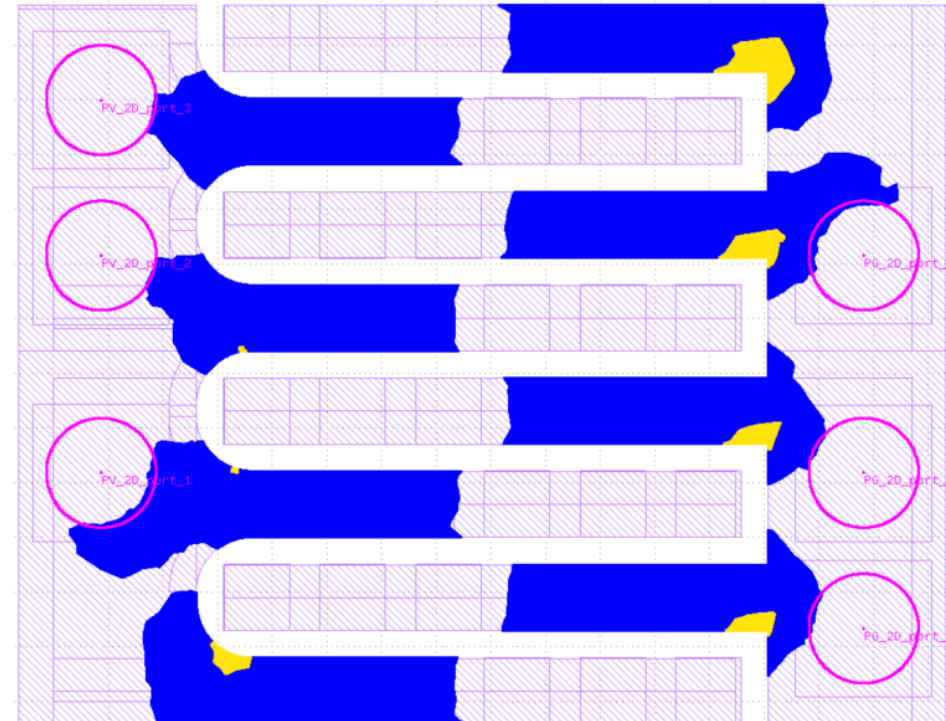
- Transition metal layers and transition vias in designs pose challenges to electromigration sign off. These layers have to be carefully routed and analyzed for electromigration.
- Depending on application, the currents can be horizontal or even vertical.
- Depending on the current flow direction, one can use short line rules to reduce EM.



Power CMOS

Power CMOS flow

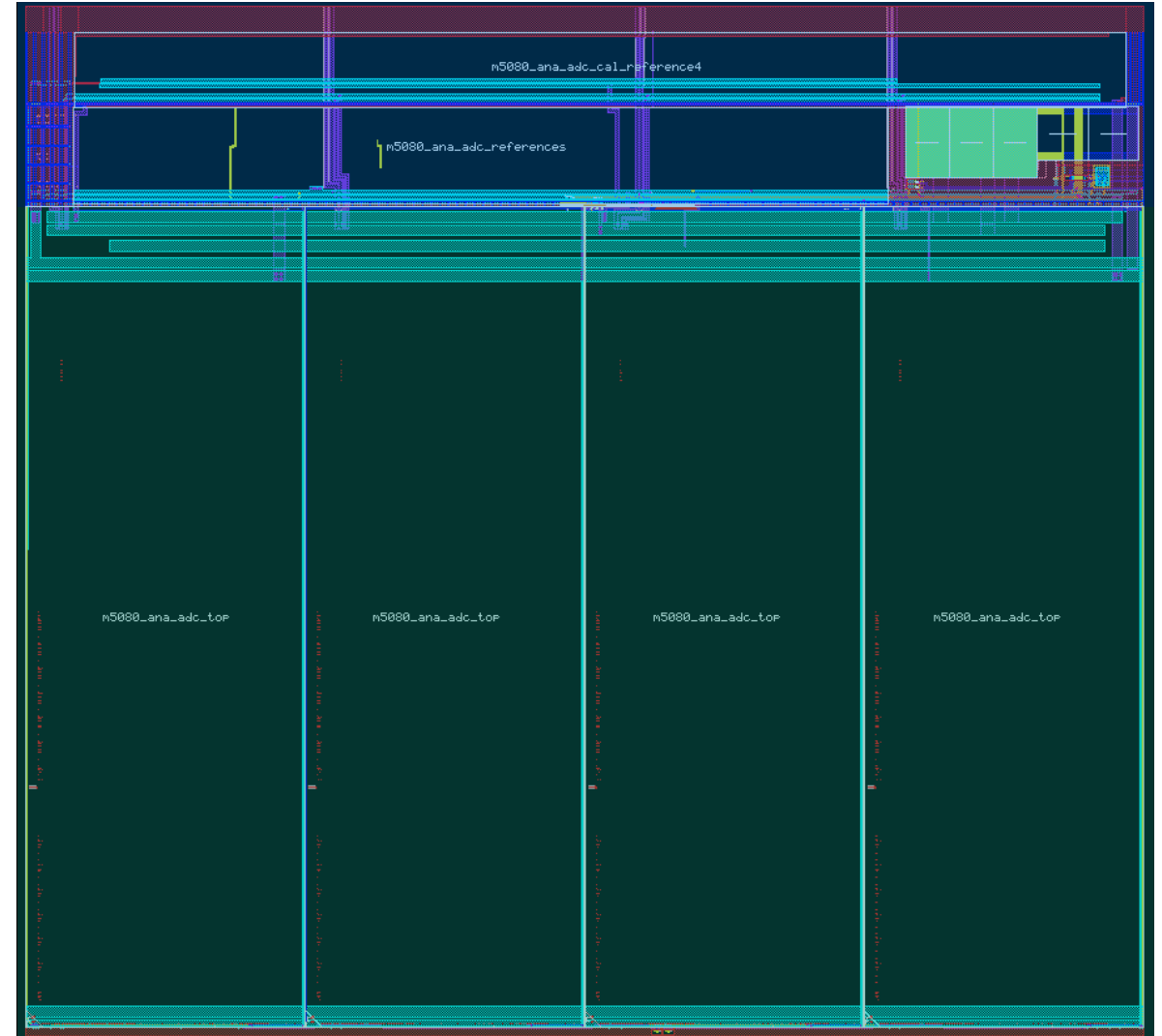
- Classical EDA tools have issues to check currents on 2D structures like metal plates and rounded shapes.
- Tools with powerful 2D meshing can be used to accurately check the currents.



Hierarchical Flow

Hierarchical flow

- Large complex designs cannot be simply run with flat approach due to large run time and memory requirement.
- Hierarchical flow is needed in these cases.
- Example shows IP with 4 ADCs
- One ADC is run and the generated macro model is then used at the top level.



Summary

Summary

- Understanding current density rules, Blech or short length rules, technology understanding of where the voids occurs the most is a must to avoid EM.
- Transition metal layers and transition vias in designs pose challenges to electromigration sign off. These layers have to be carefully routed and analyzed for electromigration.
- Power CMOS needs 2D meshing algorithms to check currents on large plates and rounded shapes.
- Hierarchical flow is a must to close large designs as the design complexity increases with advanced technology nodes.

