Reinforcement Learning or Simulated Annealing for Analog Placement? A Study based on Bounded-Sliceline Grids

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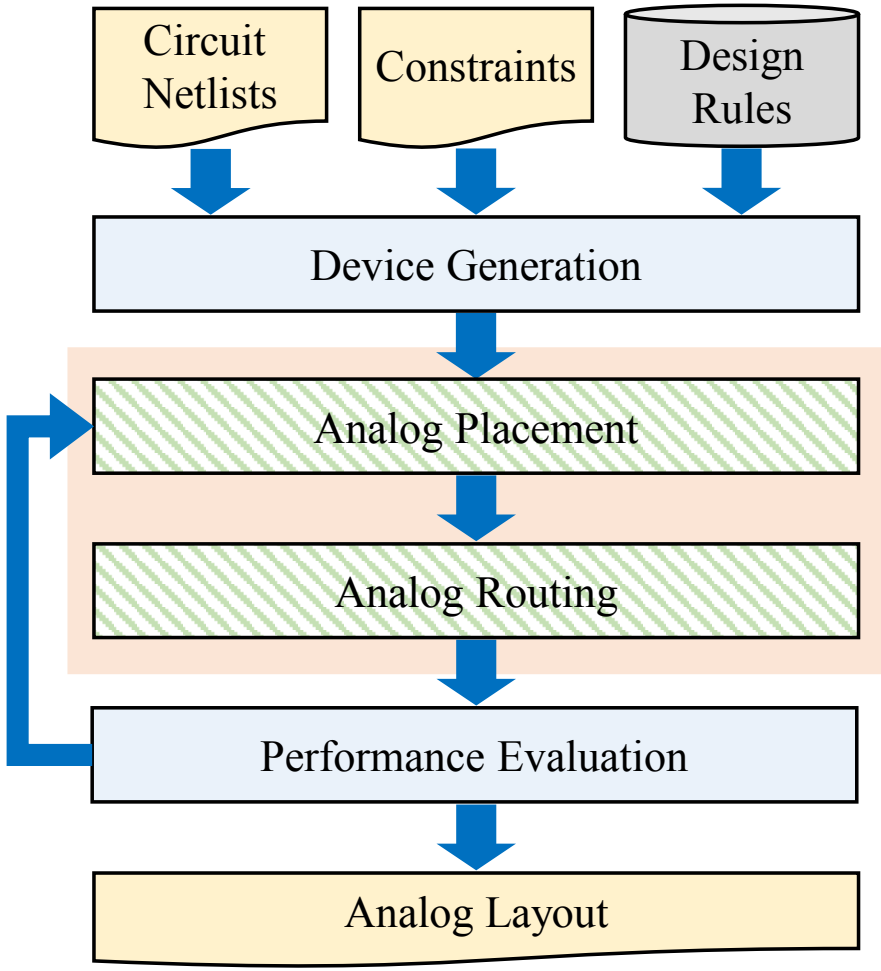
Outline

- **Introduction**
  - Analog layout synthesis flow
  - Analog placement methods, essential constraints, and representations
  - The bounded-sliceline grid (BSG) structure
- **RL-based analog placement**
- **Experimental results**
- **Conclusions**

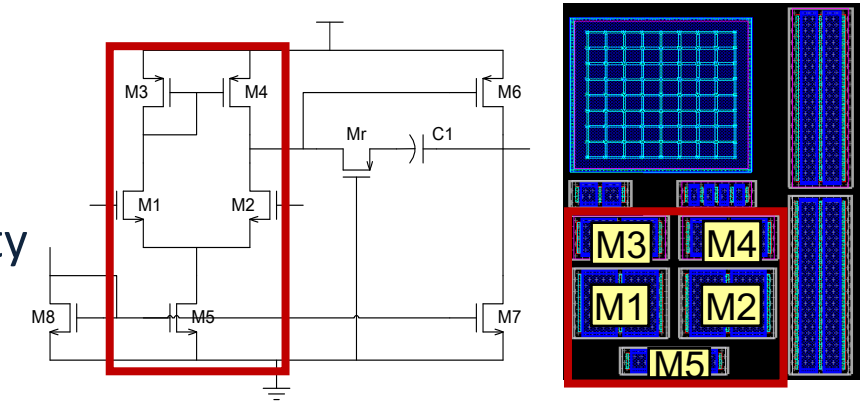
Analog Layout Synthesis Flow

- **Device/Building block generation**
  - Create physical layouts of each device or device groups with different variants, including some internal routing
- **Analog placement**
  - Determine physical positions of devices according to the given layout area or aspect ratio, and placement constraints while minimizing the layout area and estimated wirelength
- **Analog routing**
  - Finalize the interconnections according to the routing constraints while minimizing the interconnecting wirelength



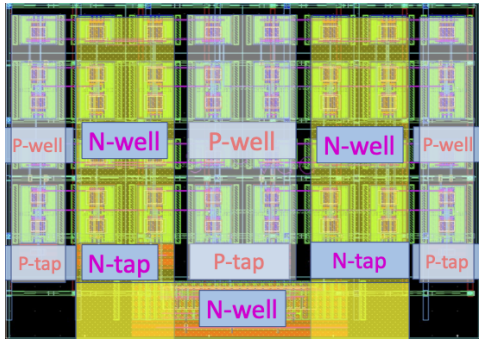
Essential Analog Placement Constraints

- **Symmetry / Symmetry-Island [Lin et al., DAC07]**
  - Improve matching quality between device components
  - Confines symmetric devices to be placed in the closest proximity for reducing the sensitivities due to process variations
  - Enhance overall circuit performance



[Lin et al., TCAD09]

- **Proximity / Well-Island [Ramprasath et al., ISPD22]**
  - Restrict devices within common well/substrate regions
  - Reduce layout area with common well taps for latch-up prevention
  - Avoid performance degradation due to substrate noise and interference



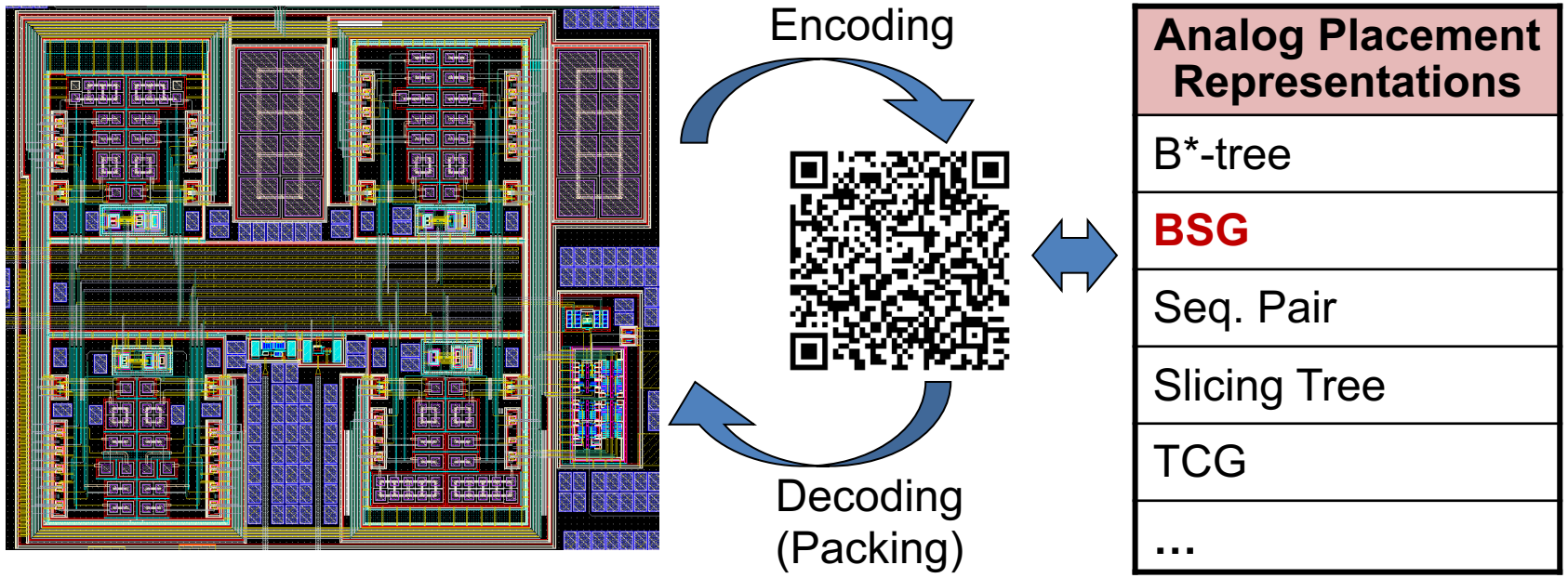
[Ramprasath et al., ISPD22]

[Lin et al., DAC07 & TCAD'09] *Analog Placement Based on Novel Symmetry-Island Formulation. DAC 2007: 465-470*

[Ramprasath et al., ISPD22] *Analog/Mixed-Signal Layout Optimization using Optimal Well Taps. ISPD 2022: 159-166*

Analog Placement in a nutshell

- Map placement solutions to some kind of **representations**
- Embed various placement constraints in the **representation**
- Find out the best configurations in the **representation** in terms of placement area and interconnecting wirelength



Analog Placement Representation

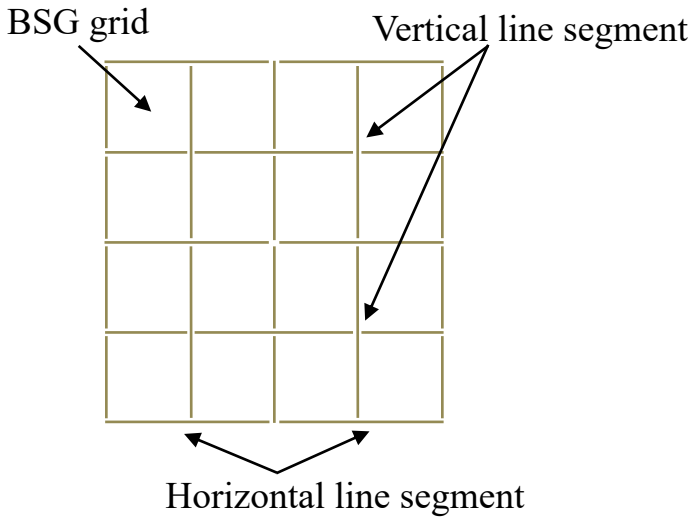
- **Absolute representation**
  - Each device/block is associated with an absolute coordinate on a gridless plane.
  - No packing is needed, but overlapping may happen.
  - A postprocessing step is required to eliminate overlapping.
- **Topological representations**
  - Topological relationships are defined in the representation without absolute coordinates.
  - A packing procedure is required to convert the representation into absolute coordinates, which guarantee non-overlapping.
  - Examples: Slicing tree, B*-tree, Sequence Pair (SP), Bounded Sliceline Grid (BSG), …

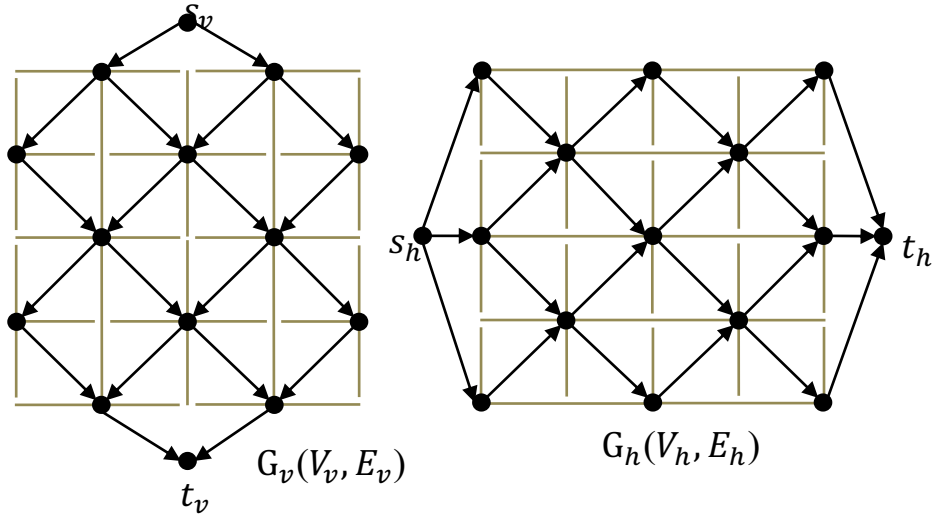
Common Analog Placement Method

- **Deterministic/Procedural method**
  - Follow existing layout template, or mimic analog layout designers' knowledge
- **Mathematical programming**
  - Composed of an objective function and a set of placement constraints
  - Optimize the objective through some analytical techniques
- **Simulated annealing (SA)**
  - Treat the placement configurations as states in a search space
  - Explores the space by accepting both uphill moves (worse solutions) and downhill moves (better solutions) based on a probability distribution that changes over time
  - SA is about the most popular approach in the literature due to its effectiveness and efficiency in leveraging various topological representations, such as B*-tree, sequence-pair, … etc.
- **Reinforcement learning (RL)**
  - Learns a policy to place components in a way that maximizes a reward function
  - Different from supervised learning, RL does not rely on labeled datasets, which is promising for applications without much existing data, such as analog placement.

Bounded-Sliceline Grid (BSG) Structure

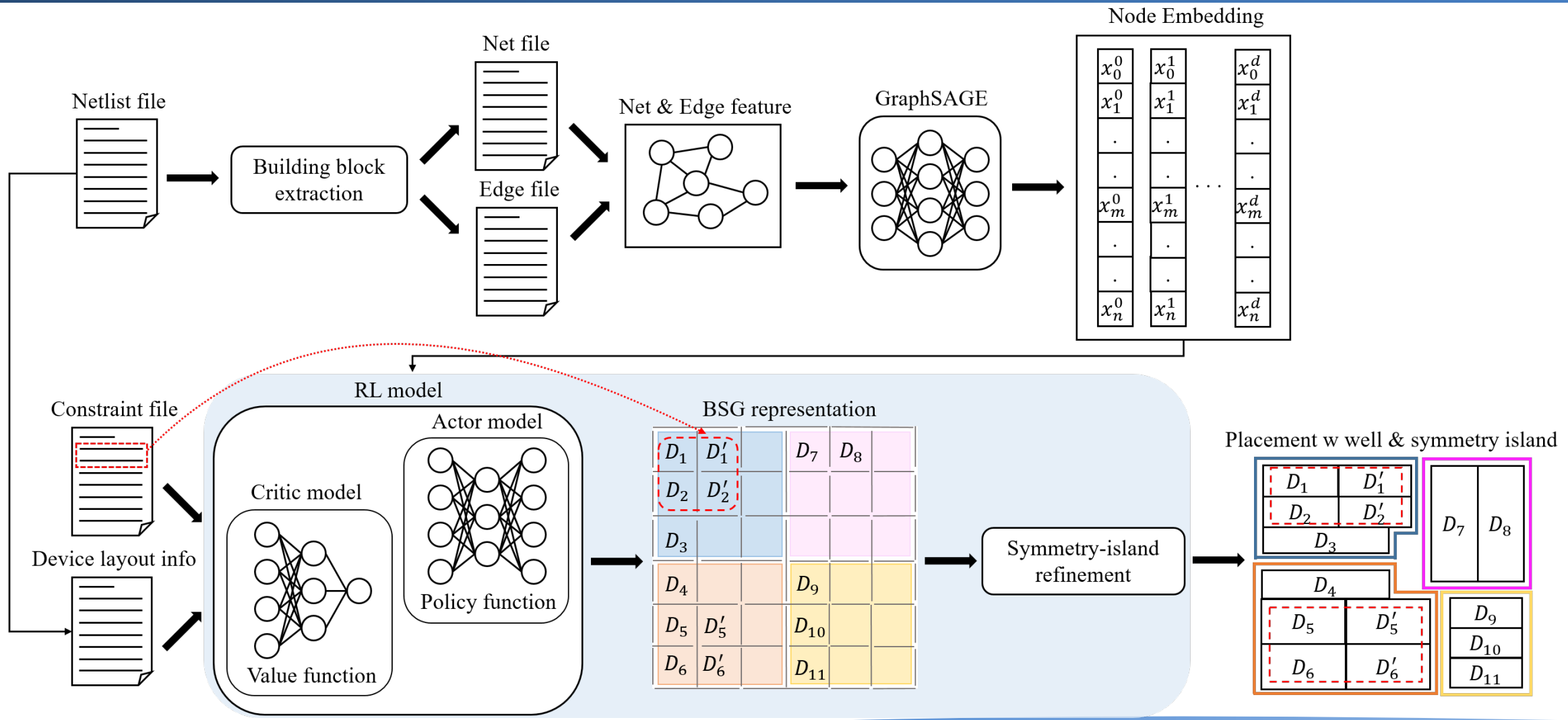
- Constructed by creating a vertical and a horizontal line segment with two unit length
- Shift the vertical (horizontal) line segment by one unit length and repeating them column by column (row by row)
- Area compression can be achieved by looking for the longest path on $G_v(V_v, E_v)$ and $G_h(V_h, E_h)$, meanwhile ensuring that there is no overlap.





[Nakatake et al., TCAD98] *Module packing based on the BSG-structure and IC layout applications. IEEE TCAD.17(6): 519-530 (1998)*

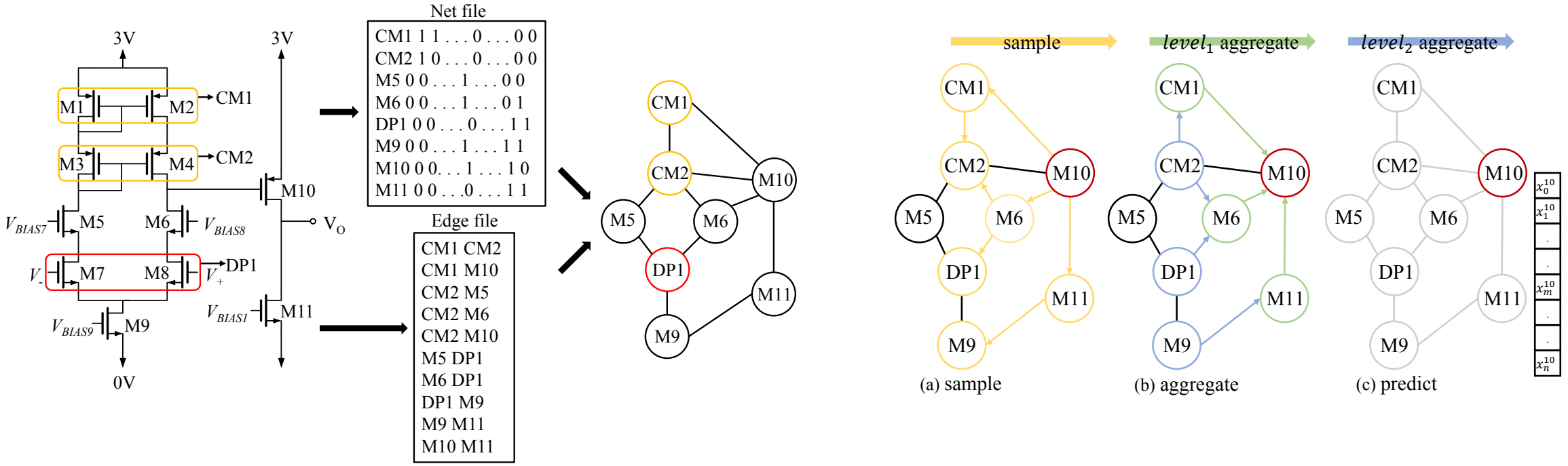
Proposed RL-based Placement on BSG Structure



Node Embeddings for Circuit Graph with GraphSAGE

❖ GraphSAGE: Inductive Representation Learning on Large Graphs

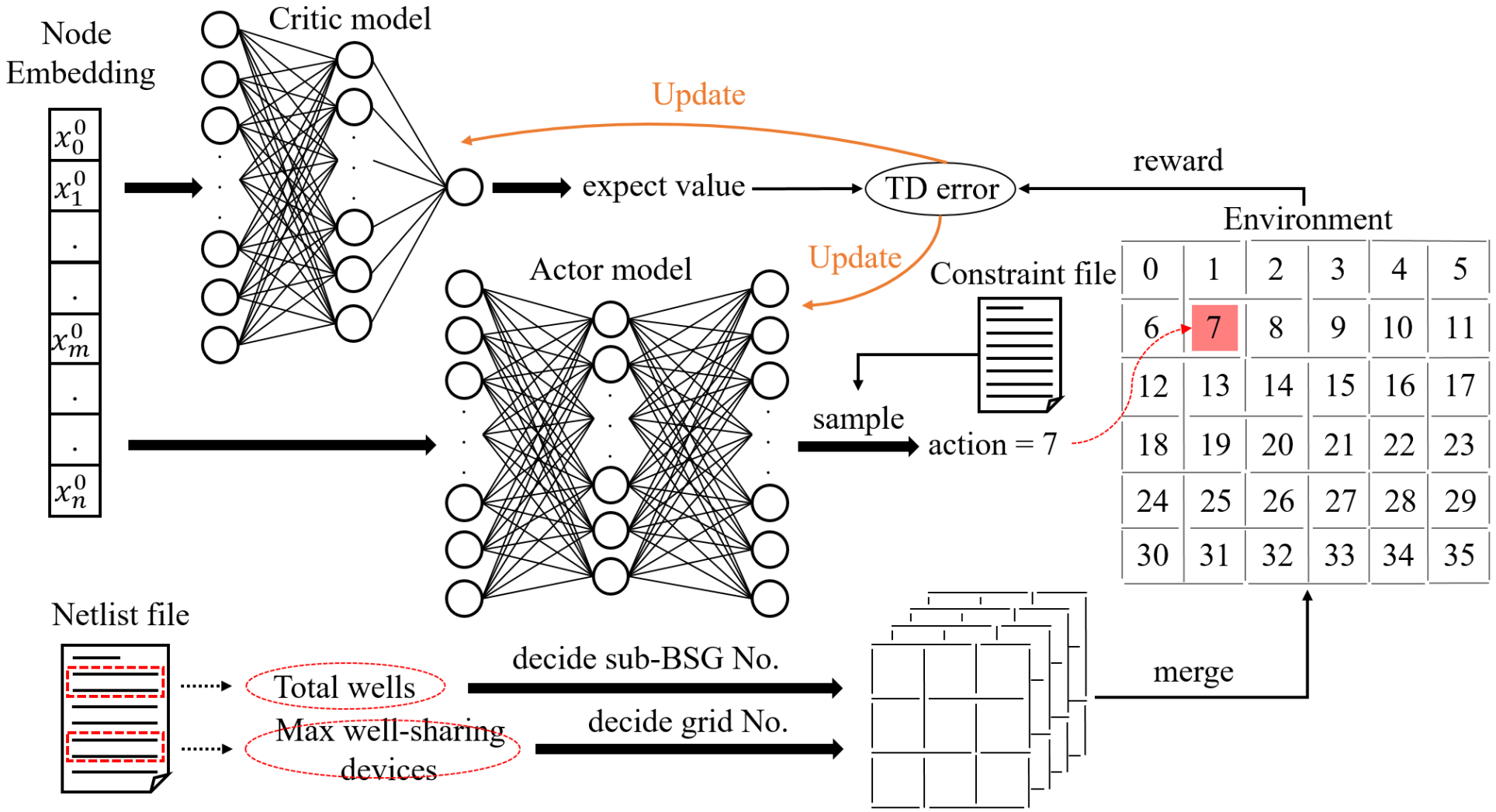
- Generate the node embeddings by sampling and aggregating neighboring node information from the circuit graph



Hamilton,et al., “Inductive representation learning on large graphs,” Advances in neural information processing systems, vol. 30, 2017.

The RL Environment on BSG

- **State**
  - Certain placement assignment on BSG
- **Action**
  - Move a device model to a different grid
- **Reward**
  - Calculate reward in terms of area and wirelength



Experimental Setup

- **Environment**
  - CPU: Intel i9-9900KF at 3.60GHz with 64GB memory
  - GPU: RTX-3090 with 24GB memory
  - Programming language: Python
- **Compared approaches**
  - For each benchmark, both RL and SA approaches are compared based on the BSG structure.
- **Benchmarks**

Table 3: Test circuit information

Test case	Device No.	Well-island No.	Proximity group	Symmetry group
Bandgap	15	2	2	2
Opamp	30	2	0	2
Cascode	38	2	3	3

Experimental Results

- The proposed RL approach is more effective than the SA approach in terms of the objective function, including area and wirelength.

Table 5: Comparisons of Manual, SA and Ours based on Bandgap.

Approach	Area	HPWL	Utility	Gain (dB)	PM (degree)	UGF (MHz)	Power (μW)	GBW (dB*GHz)
Manual	2160	617	84.4%	26.25	66.93	18.31	0.45	0.48
SA	2280	633	81.2%	26.55	67.08	19.46	**0.42**	0.52
Ours	**2024**	**613**	**90%**	**26.88**	**67.77**	19.53	0.45	**0.53**

Table 6: Comparisons of Manual, SA and Ours based on Opamp.

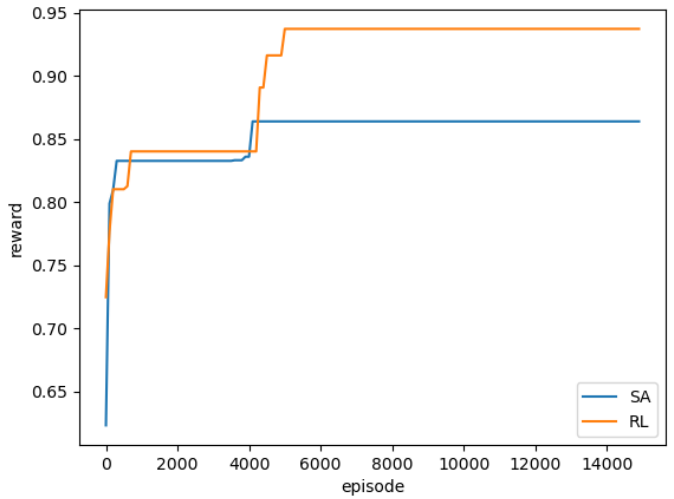
Approach	Area	HPWL	Utility	Gain (dB)	PM (degree)	UGF (MHz)	Power (μW)	GBW (dB*GHz)
Manual	5412	898	70.2%	68.24	141.74	52.24	**93.9**	3.56
SA	5520	922	70.4%	70.24	137.77	56.47	94.23	3.97
Ours	**4883**	**813**	**77.8%**	**74.07**	138.6	**58.48**	94.96	**4.33**

Table 7: Comparisons of Manual, SA and Ours based on Cascode.

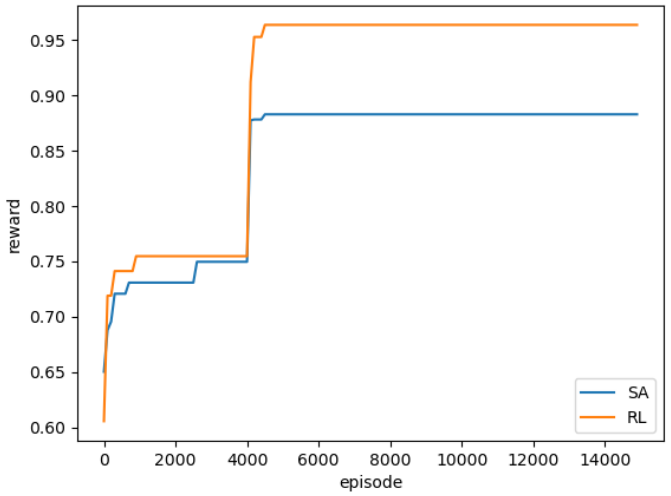
Approach	Area	HPWL	Utility	Gain (dB)	PM (degree)	UGF (MHz)	Power (μW)	GBW (dB*GHz)
Manual	3268	**1238**	88%	**60.56**	35.57	**317.8**	0.42	**19.25**
SA	3312	1366	85.8%	40.07	**41.79**	274.9	**0.39**	11.02
Ours	**3154**	1297	**90%**	60.33	36.34	316	0.42	19.06

Experimental Results

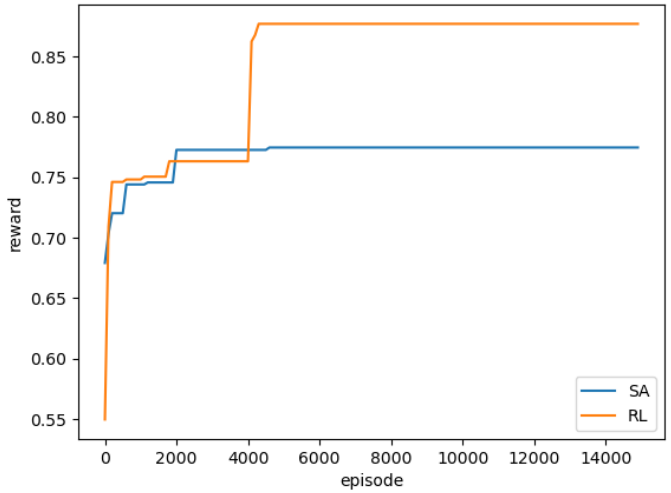
- The convergence of the RL approach consistently outperforms that of the SA approach across all test circuits.



(a)



(b)



(c)

Figure 9: The reward v.s. episode based on SA and RL, respectively. (a) Bandgap. (b) Opamp. (c) Cascode.

Experimental Results

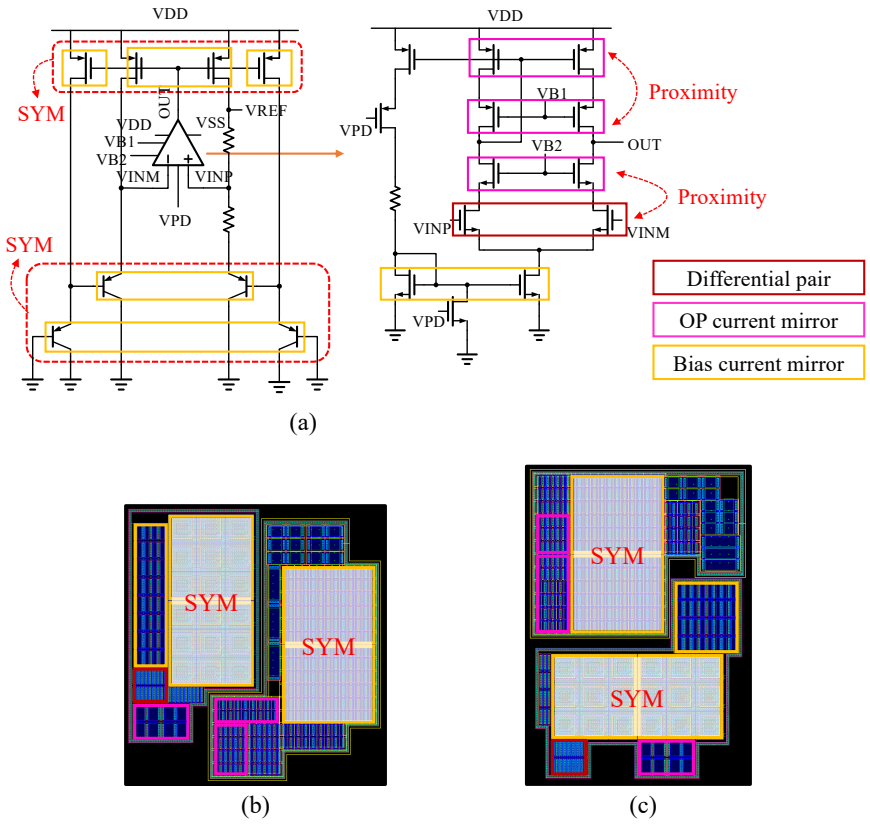


Figure 10: Bandgap circuit. (a) Schematic. (b) Resulting placement based on RL. (c) Resulting placement based on SA.

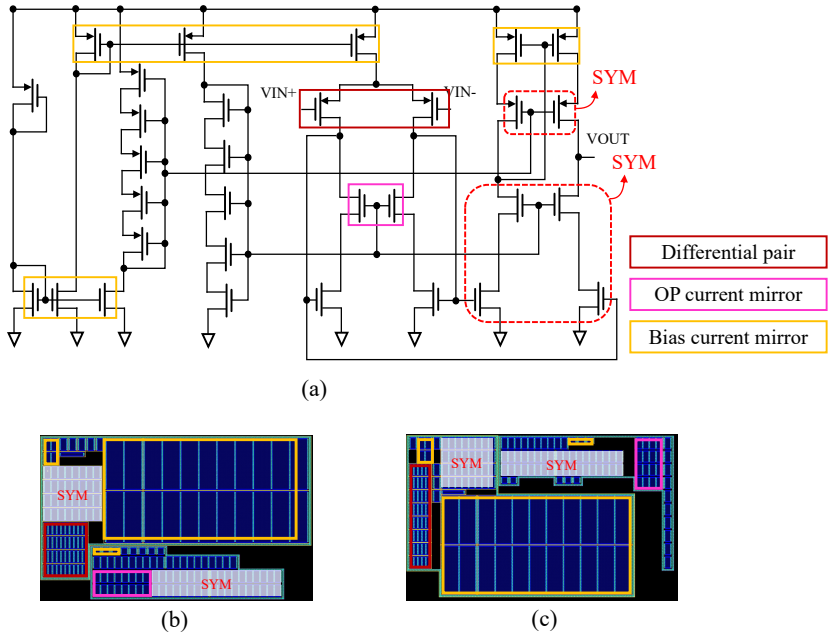


Figure 11: Opamp circuit. (a) Schematic. (b) Resulting placement based on RL. (c) Resulting placement based on SA.

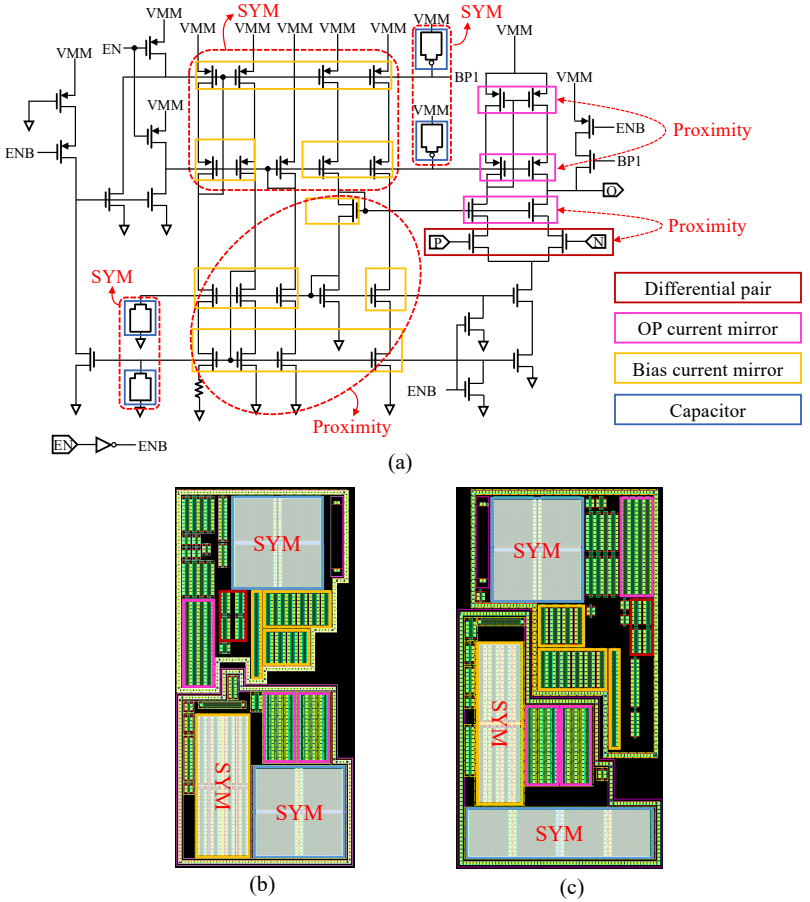


Figure 12: Casecode circuit. (a) Schematic. (b) Resulting placement based on RL. (c) Resulting placement based on SA.

Conclusions

- We employed the RL model and utilized the BSG structure for analog placement considering essential analog placement constraints.
- Through self-learning via the RL model, the agent acquires knowledge of diverse states and receives rewards from the environment, updating model parameters based on these rewards to enhance placement results.
- Compared with the conventional SA approach, the proposed RL approach can obtain superior analog placement quality and better convergence rate.

Thanks for your attention!