# Physical Design Challenges in Modern Heterogeneous Integration

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March 14, 2024

# Acknowledgements

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I.-J. Lin

B.-Q. Lin

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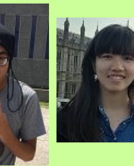
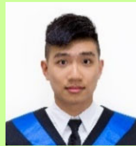
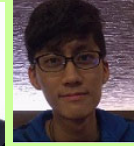

T.-C. Lin

C.-H. Chiang

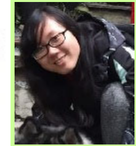
Y.-S. Lu

## Students


F.-Y. Chuang


Y.-C. Cai

H.-T. Wen


Z.-R. Nei

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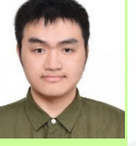
Y.-T. Chen

H.-Y. Chang

M.-H. Chuang


C.-C. Lee

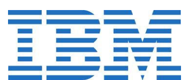
Y.-J. Chen

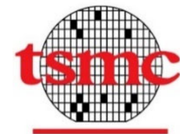
## Friends

C. Shen

Prof. J. Chen

## Sponsors



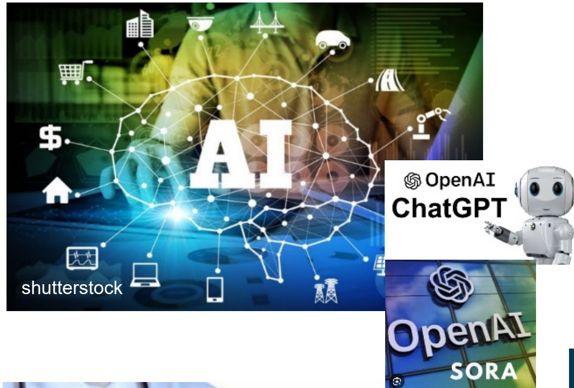


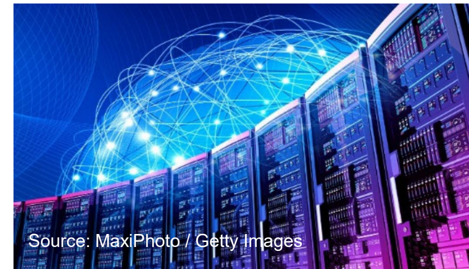
# Outline

Concluding Remarks

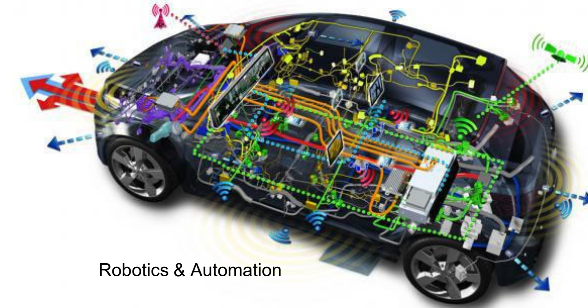
# Technology Drivers

## Artificial intelligence



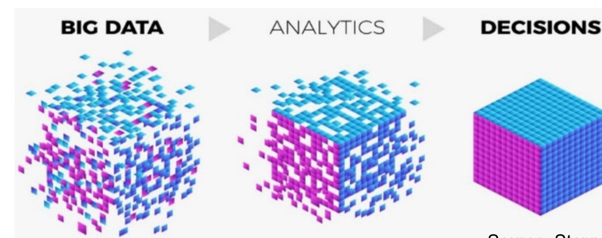

## High-performance computing




## Automotive electronics

## Intelligent medicine

## Big data analytics



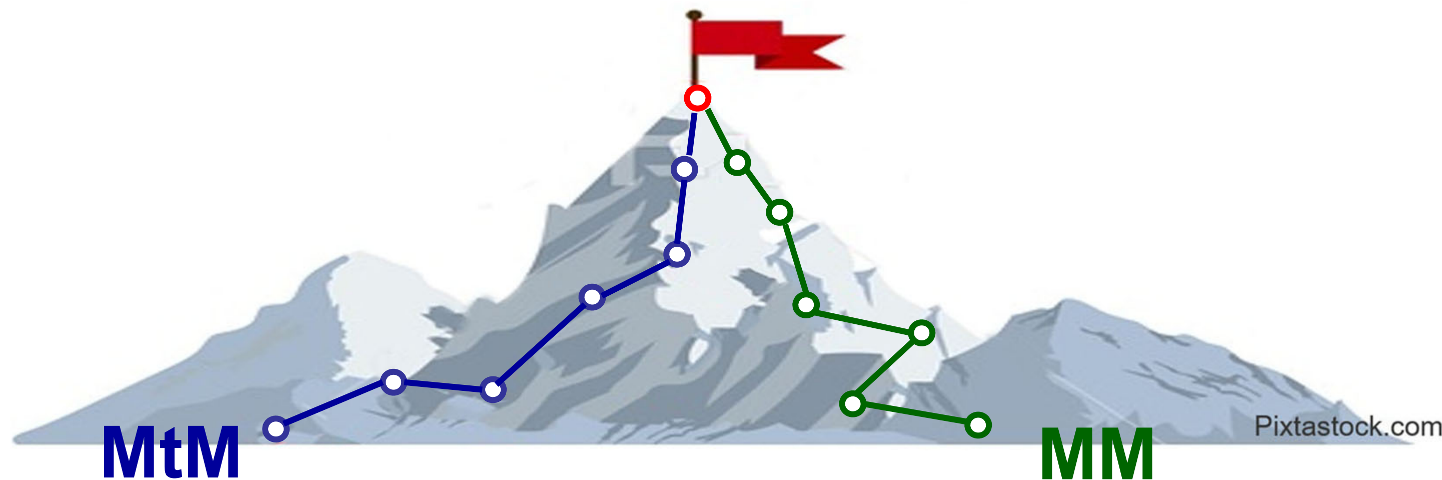

Source: Stargazr

## 5/6G+IoT+Cloud

shutterstock

# Technology Options for Achieving PPA Target

Higher Performance
Lower Power
Smaller Area

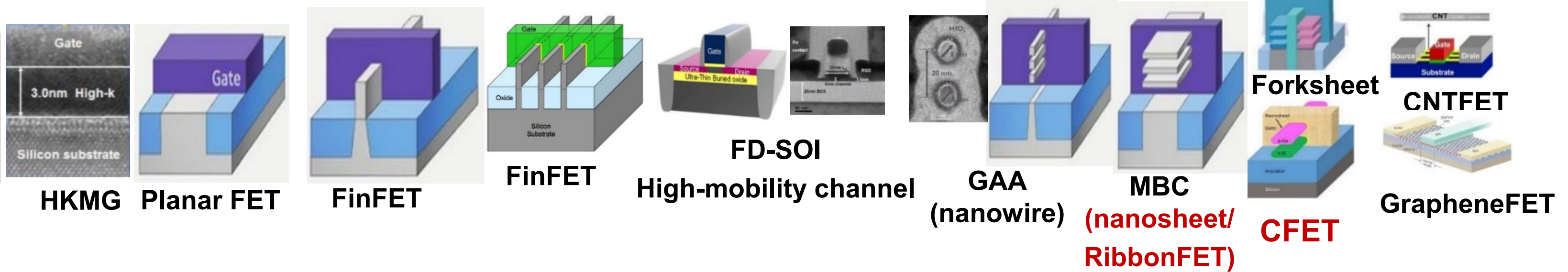



| More-than-Moore (MtM) | More Moore (MM) | Beyond CMOS |
|---|---|---|
| Heterogeneous Integration | Continued Scaling | New Devices |
| 2.5D/3D Packaging | FinFET/Nanosheet/CFET | GaAs/SiC/GaN |
| RF/MEMS/sensor/analog | Multiple patterning/EUV/DSA | Ferroelectric (FeFET) |
| Optical component | Backside power delivery | Graphene (GFET) |
| | | Carbon nanotube (CNTFET) |

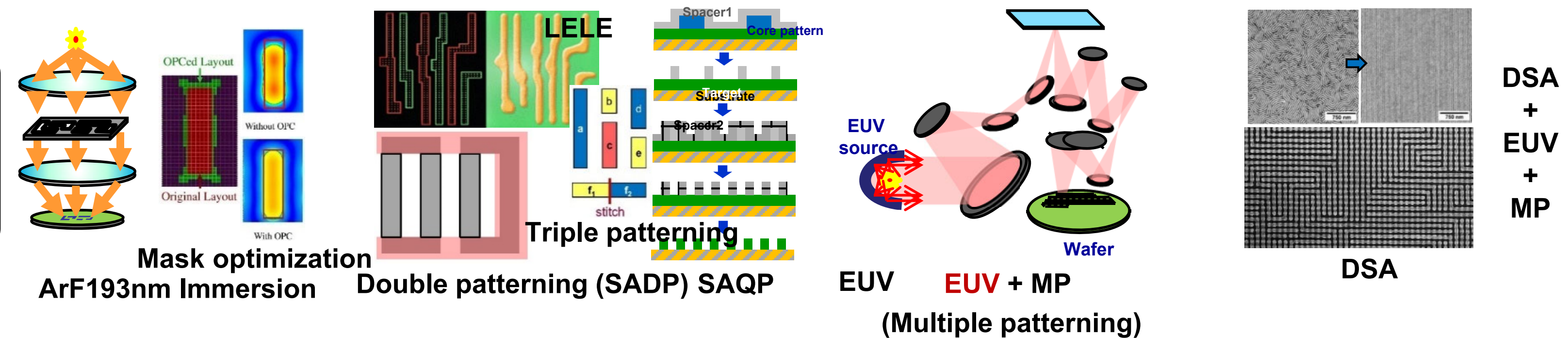
# More Moore Technology Landscape

| 45/40nm | 32/28nm | 22/20nm | 16/14nm | 10nm | 7nm | 5nm | 3nm | 2nm & beyond |
|---|---|---|---|---|---|---|---|---|

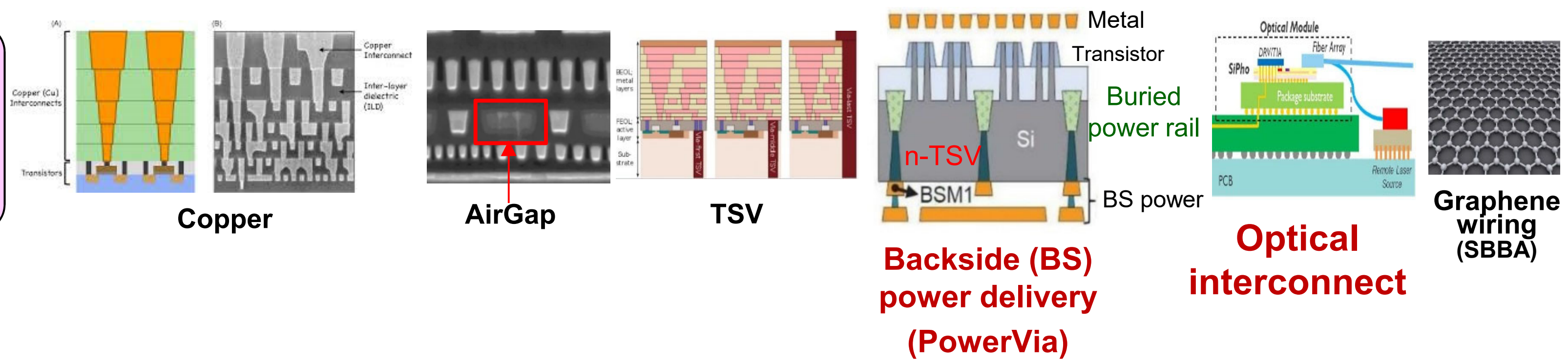
Transistor




Patterning




Interconnect



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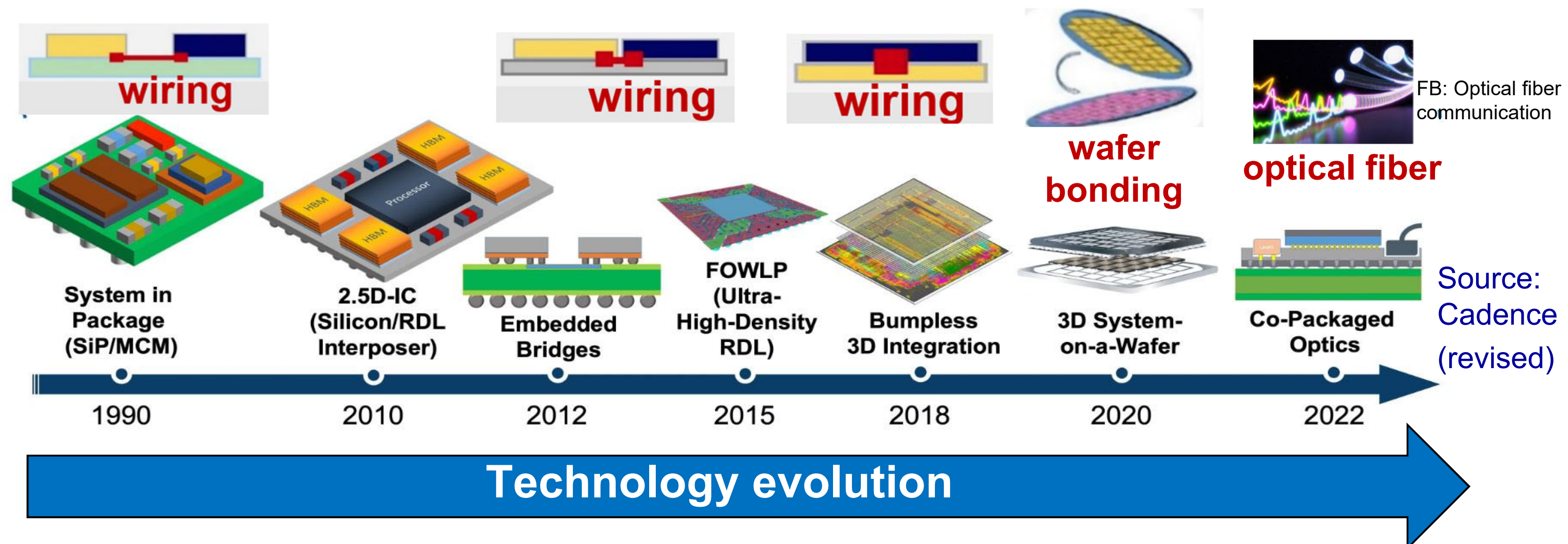
# More-than-Moore Heterogeneous Integration

- Economic advantages of More-Moore scaling are getting smaller (high manufacturing costs with advanced transistors, EUV, etc.), making the More-than-Moore trends more obvious.
- Heterogeneous integration with 3D stacking is promising with better system PPA, form factor, functionality, etc.
- Issues: complexity, yield, heat, interconnect cost, mechanical stress, testing, standardization, etc.







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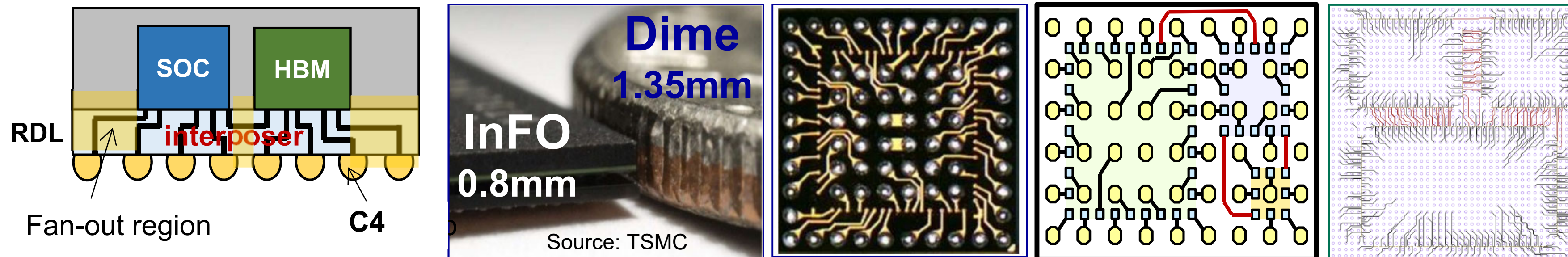
# Advanced Packaging for TSMC's Success

- **Dr. Morris Chang (2016): InFO is key for TSMC to beat Samsung for Apple's A10 chip orders**

商周

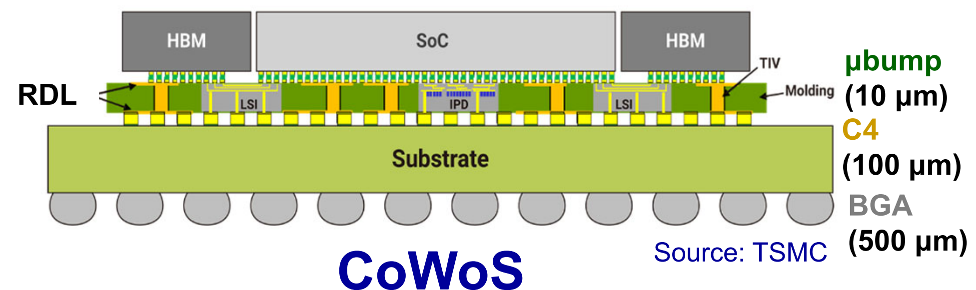
BARRON'S Dec 01, 2015, **TSMC Will Regain Apple In A10, InFO**




**First published InFO package router** [Lin et al., ICCAD'16], **US Patent 9,928,334, 2018 (with AnaGlobe)**

TechInsights 2023

**NVIDIA H100 Hopper TSMC CoWoS-S Flip Chip Ball Grid Array**

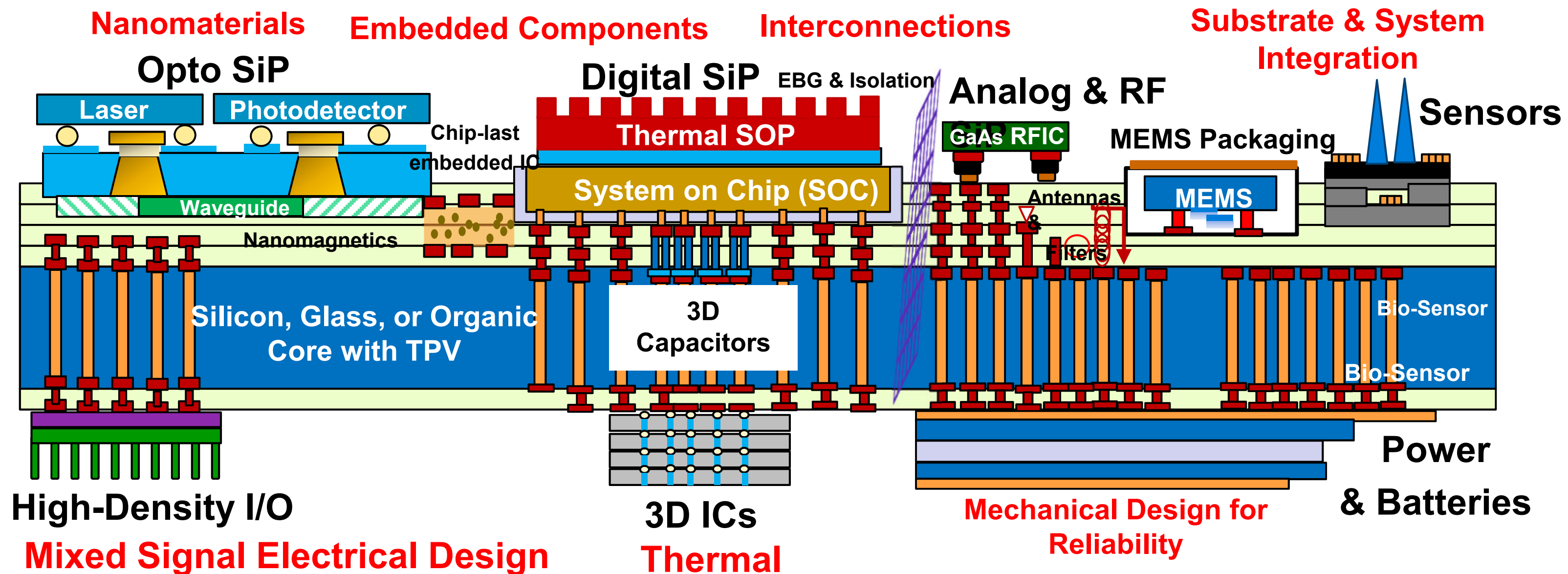



**CoWoS**

Source: TSMC

# Heterogeneous Integration & Multi-Physics Domains

| Interconnect Scale: | Devices (nm) | Packages (um-nm) | Boards (mm-cm) | Systems (cm-m) |
|---|---|---|---|---|




Source: Georgia Tech PRC, http://www.prc.gatech.edu/

**System/Physical**
- System partitioning
- Architecture evaluation
- Placement & Routing
- Timing

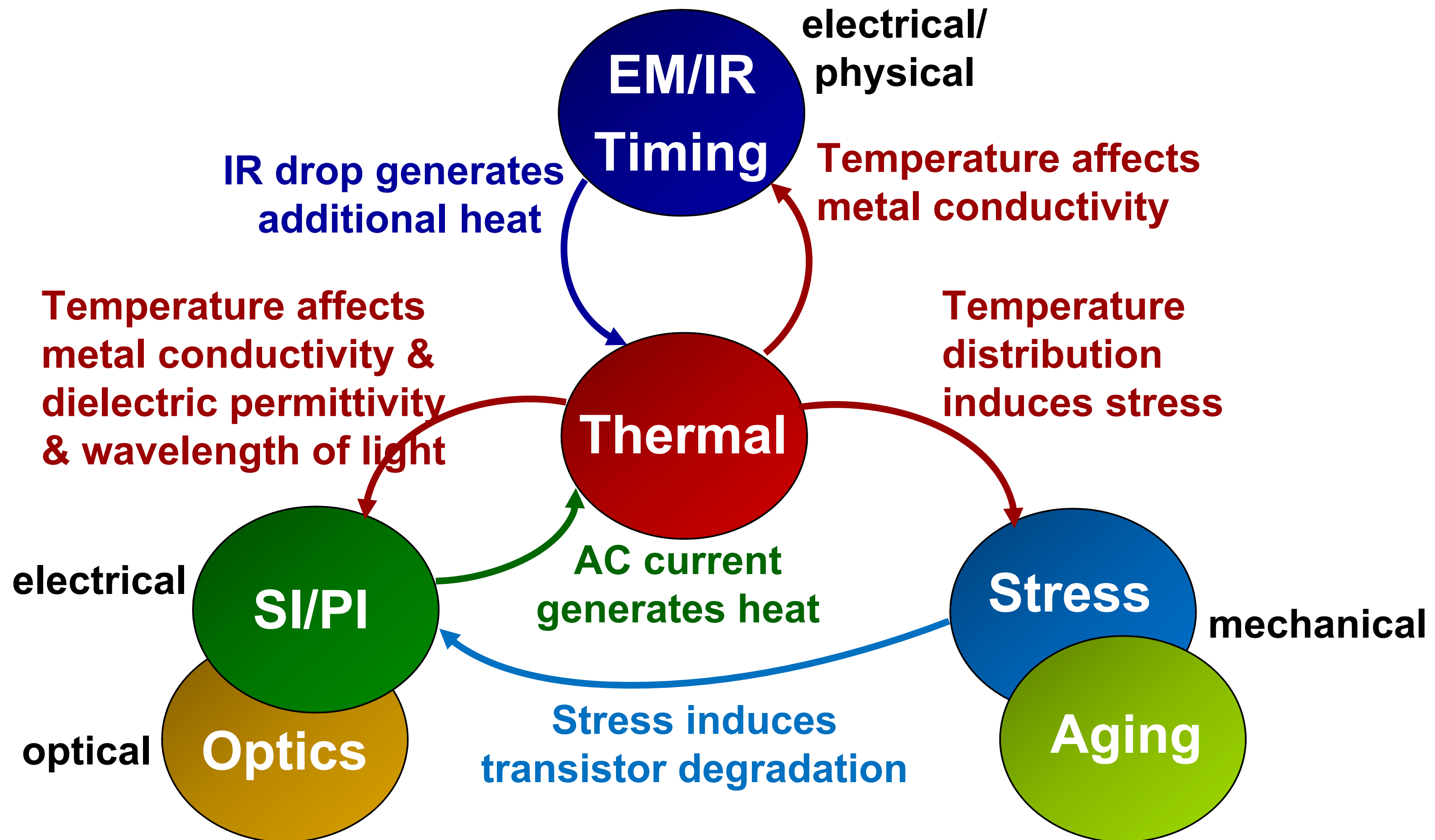
**Electrical**
- Power/signal integrity
- EMI
- Power maps
- Mobility shifts

**Thermal**
- Joule heating
- Hot spots
- Device cooling

**Mechanical**
- Warpage
- Metal migration
- Delamination
- Fatigue

**Optical**
- Laser power
- Routing
- Thermal effect

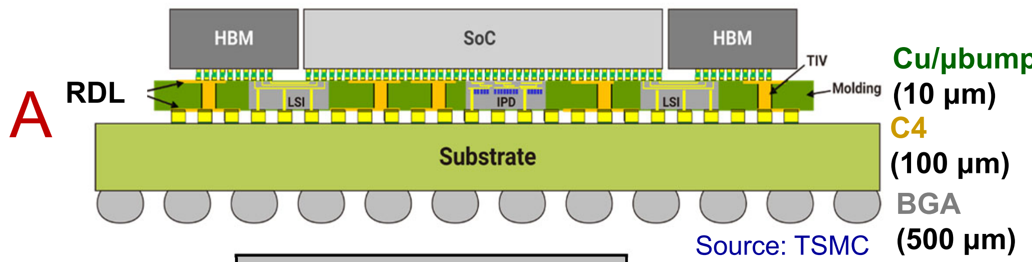
# Multi-Physics Interactions




Source: TSMC/Ansys (w. revision)

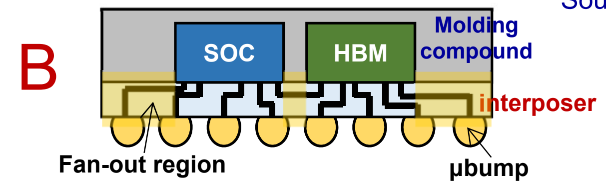
# Multiple Options for Heterogeneous Integration (HI)

A



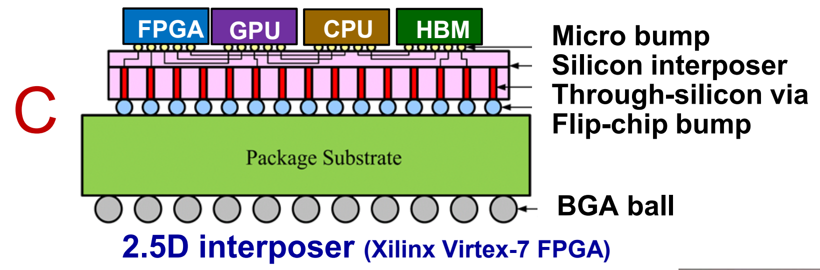

**CoWoS (Chip on Wafer on Substrate)**
**TSMC**

B




**Integrated fan-out (InFO)**
**TSMC, ASE, Amkor, etc.**

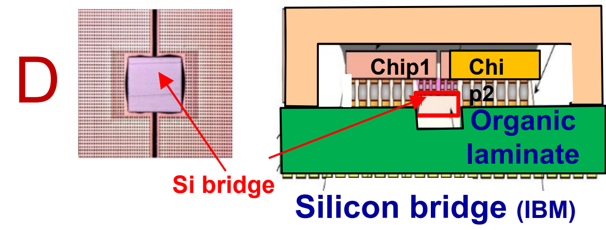
C



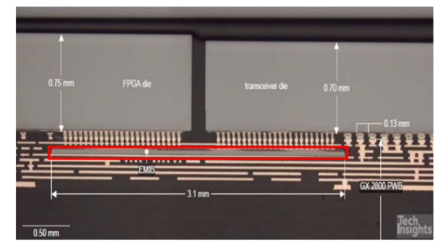

2.5D interposer (Xilinx Virtex-7 FPGA)

**Silicon interposer**
**TSMC/Xilinx (since 2012), Google, NVIDIA & AMD (GPU + HBM), etc.**

D



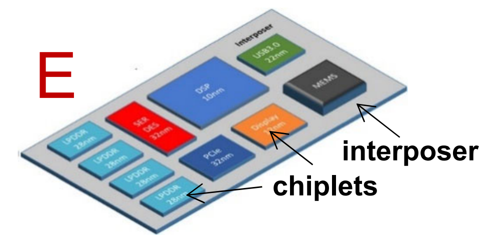

Silicon bridge (IBM)



Silicon bridge (Intel)

**Silicon bridge die**
**Intel, IBM, SPIL, etc.**

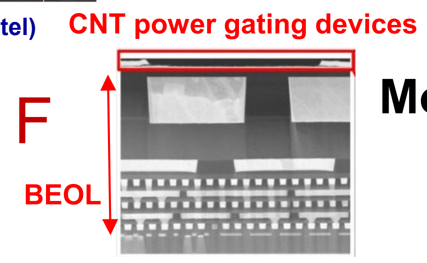
E




**Chiplet**
**AMD, etc.**

F

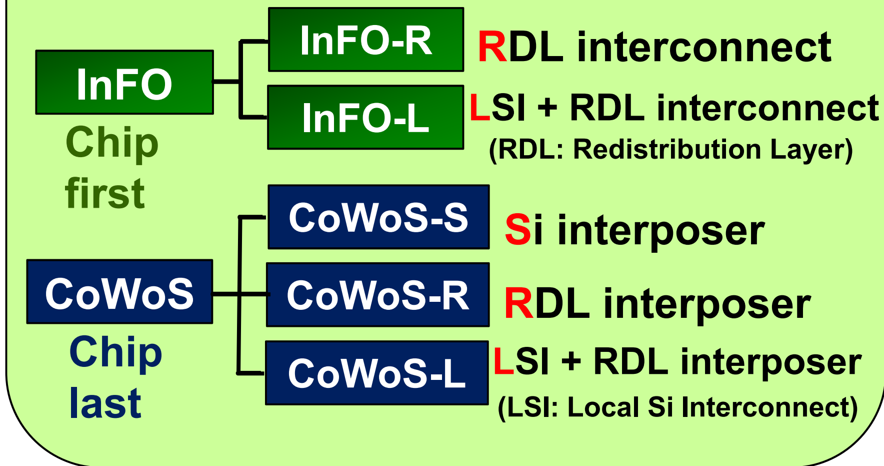
CNT power gating devices

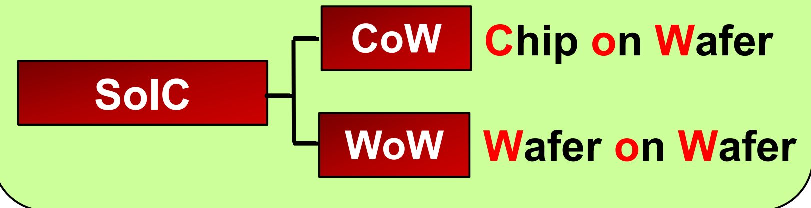


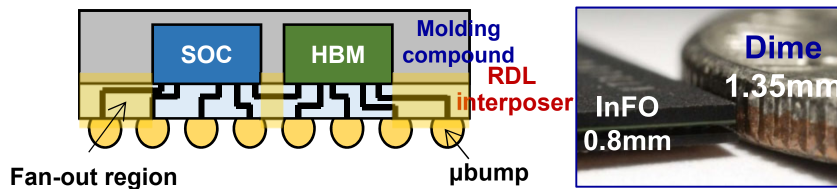

**Monolithic 3D IC**
**IMEC**

# TSMC 3D Fabric™ (since August 2020)

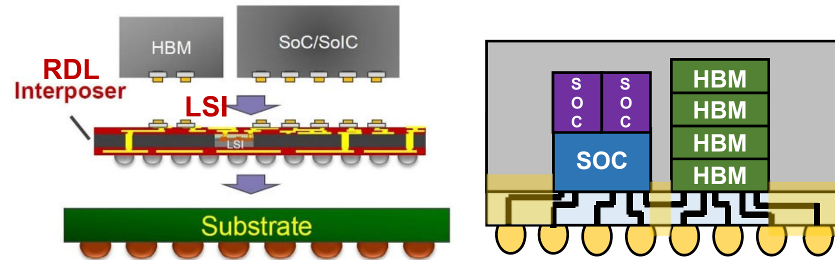
**King of Advanced Packaging??**



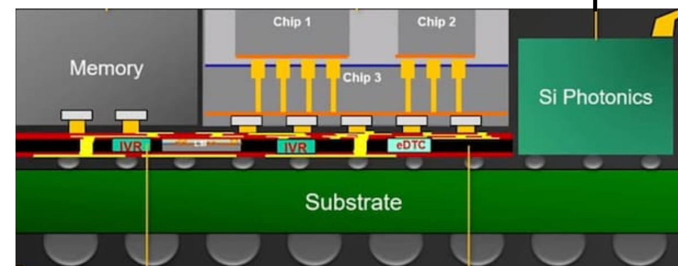

**Integrated Fan-Out (InFO)**
**cheaper, wider/thicker wires**




**CoWoS**
**Chip on Wafer on Substrate**
**silicon process, denser wires**

**SoIC**
**System on Integrated Chips**

**Co-packaged Optics**

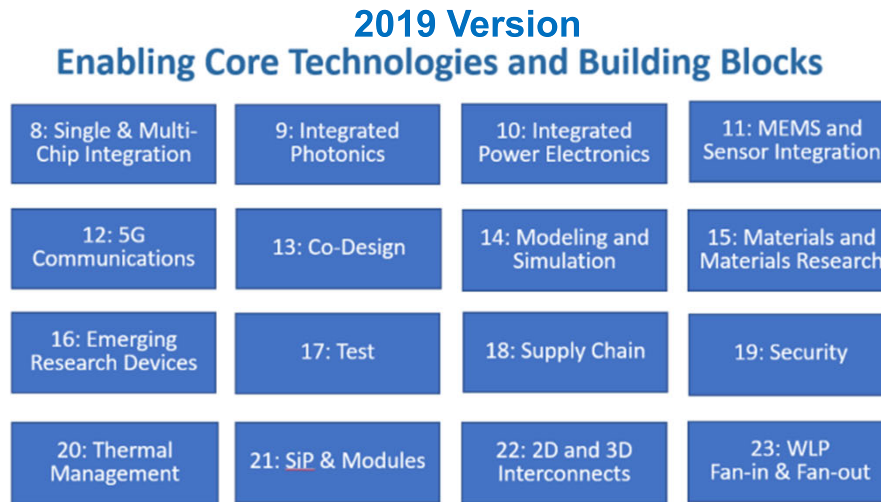



**Future package with optics (2025)**

Source: TSMC

# Heterogeneous Integration (HI) Roadmap

- **HI Roadmap since 2015** vs. ITRS & IRDS Roadmaps




**Applications**

- Chapter 1 Introduction
- #2: HPC
- 3: IoT
- 4: Medical, Health, Wearables
- 5: Automotive
- 6: Aerospace and Defense
- 7: Mobile

*Table 1: Flip chip interconnects*

| *Year of Production* | 2018 | 2019 | 2020 | 2021 | 2022 | 2025 | 2028 | 2031 | 2034 |
|---|---|---|---|---|---|---|---|---|---|
| **Flip Chip Pitch** | | | | | | | | | |
| Flip Chip- Large Body Solder >12mm Sq Die | 135 | 130 | 130 | 130 | 130 | 130 | 130 | 130 | 130 |
| Flip Chip- Small Body Solder <12mm Sq Die | 135 | 130 | 130 | 130 | 130 | 130 | 130 | 130 | 130 |
| Flip Chip - Cu Pillar Small Body <12mm Sq Die (Bond on Trace) | 45 | 30 | 30 | 30 | 30 | 20 | 20 | 20 | 20 |
| Flip Chip- Cu Pillar Large Body >12mm Sq Die | 110 | 100 | 100 | 100 | 90 | 90 | 90 | 90 | 90 |
| Flip Chip Solder - COW | 50 | 50 | 50 | 50 | 50 | 50 | 50 | 50 | 50 |
| | | | | | | | | | |
| Flip Chip Cu Pillar -COW (Chiplets) | 40 | 35 | 35 | 35 | 30 | 25 | 25 | 25 | 25 |
| Flip Chip Cu Nano Particles | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 30 | 30 |
| Wafer to Wafer Cu to Cu Interconnect | 5 | 5 | 5 | 2 | 2 | 2 | 1 | 1 | 1 |
| Embedded Die In Substrate Interconnect Pitch | 120 | 120 | 120 | 120 | 90 | 90 | 70 | 70 | 70 |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

**Flip-chip interconnect roadmap**

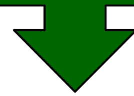
**Heterogeneous Integration Technical Working Groups (TWGs)**

**Source: HIR Roadmap, 2019 (latest: 2023)**

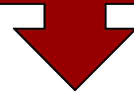
ITRS: International Technology Roadmap for Semiconductors (1998-2015)
IRDS: IEEE International Roadmap for Devices and Systems (2016-)

# Outline

Technology Background



Physical Design Challenges/Solutions



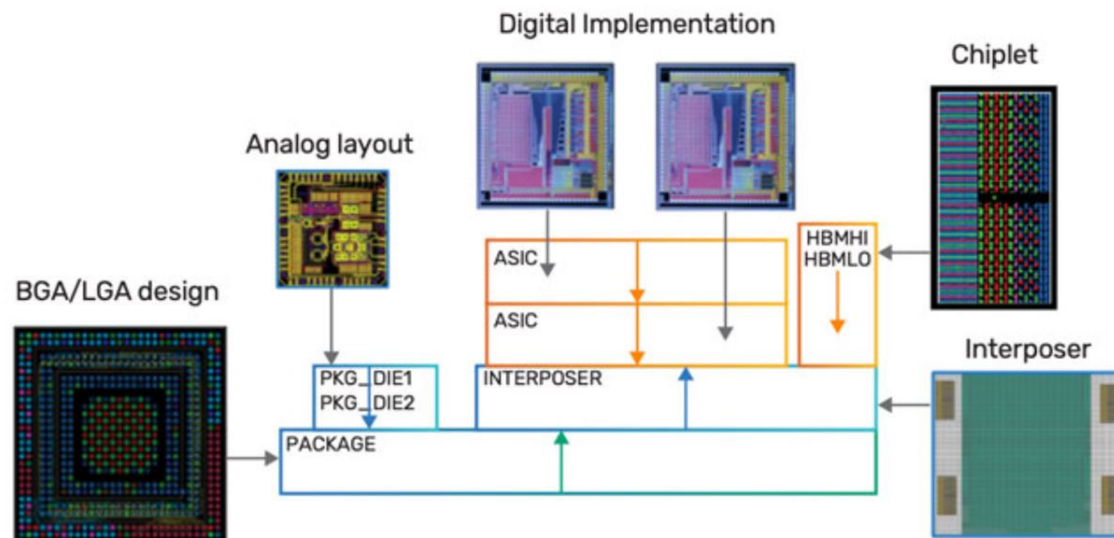
Concluding Remarks

# Multi-Domain Challenges & Opportunities

| | |
|---|---|
| **System** | • System-level HI modeling & simulation, heterogeneous device applications & computing<br>• Power/performance/thermal/cost analysis for heterogeneous platforms<br>• Architecture with HI components, cost evaluation & decision, hardware security & reliability |
| **Physical** | • 3D partitioning, floorplanning, placement, routing, post-layout optimization (RDL routing)<br>• Package-/board-level routing, chip-package-board co-design (bump-aware design)<br>• Cross-domain timing analysis/optimization, chip/board/system & 3D IC test, DFT connectivity |
| **Electrical** | • 3D power/signal integrity & EMI prevention (PTH), buried power rail, stacking P/G network<br>• Stacking STA (cross dies) & electrostatic discharge (ESD), inter-die coupling, substrate RLC |
| **Thermal** | • Stacking interconnect/full-system thermal analysis & electromigration reliability<br>• Joule heating, hotspot detection & handling, device cooling |
| **Mechanical** | • Warpage/delamination/stress-aware optimization<br>• Metal migration simulation and optimization, fatigue reliability |
| **Optical** | • Optical routing, thermal-aware power device placement, electrical & optical co-design<br>• System-based optical device analysis & optimization, laser power network, reliability |

# 3D System-level Partitioning

- **Partition mixed-logic and -memory into multiple dies with different technologies for PPA optimization**
  - Device sizes & design rules change with different die assignment, **NOT** just min-cut partitioning!
- **Must consider process technologies for multiple dies and corresponding interconnect/via/bump parameters for the overall cost optimization**

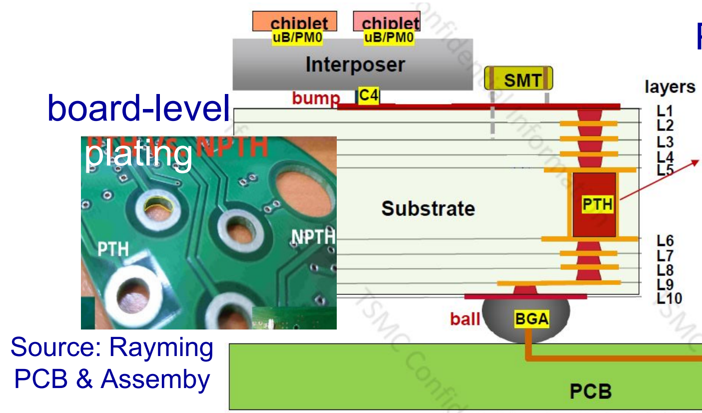



System-level partitioning, planning, aggregation, and optimization

Source: Cadence

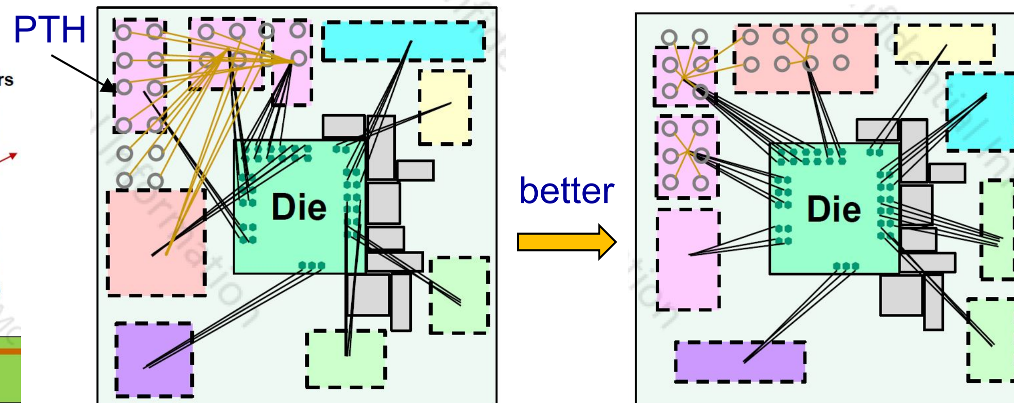
# Cross-physics-domain Floorplanning

- **Integrating dies into an advanced package may suffer from severe electrical, thermal, and mechanical effects, e.g., stress, warpage, substrate noise, Joule heating, and delamination.**
- **A PTH (plating through hole) connecting a bump to a ball may induce severe EMI (electromagnetic interference) problems**
  - Must meet constraints: larger pitch for EMI, constrained regions, etc.
- **Floorplan PTH rooms (locations, aspect ratios, etc.) of holes for better bump-PTH-ball routing**




**PTH (plating through hole)**

Source: TSMC

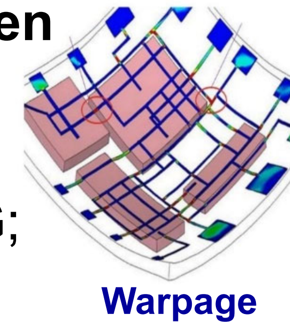



**Floorplan PTH rooms to optimize routing**

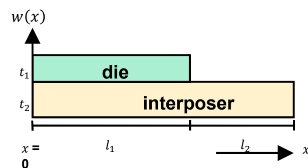
Source: TSMC

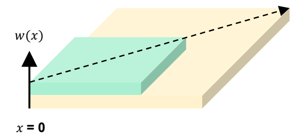
# Mechanical Issue: Warpage-aware Floorplanning

- Hsu, Chung, and Chang, "Transitive closure graph-based warpage-aware floorplanning for package designs," ICCAD'22
- **Mismatch in coefficients of thermal expansion between Si (die) & laminate substrate (interposer) causes thermo-mechanical stress and warpage**
- **Warpage modeling:** Suhir's theory; **floorplanning:** TCG; **simulation:** ANSYS & Moldex3D



Warpage




$$w(x) = \frac{t\Delta\alpha\Delta T}{2\lambda D}\left(\frac{1}{2}x^2 - \frac{\cosh kx - 1}{k^2 \cosh kl}\right)$$

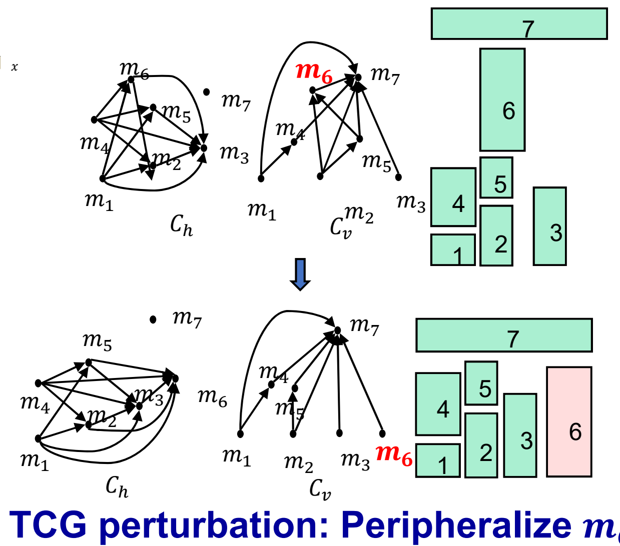
$$\cosh kx - 1 > 0$$

$t$: thickness

$k, D, \lambda$: material related coefficients

$\Delta T$: the temperature difference between initial temperature and final temperature

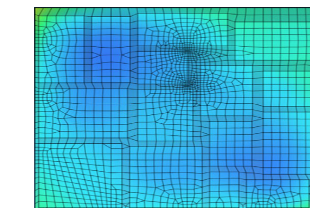
$\Delta\alpha$: difference of coefficient of thermal expansion




TCG perturbation: Peripheralize $m_6$

Traditional TCG-based floorplanning



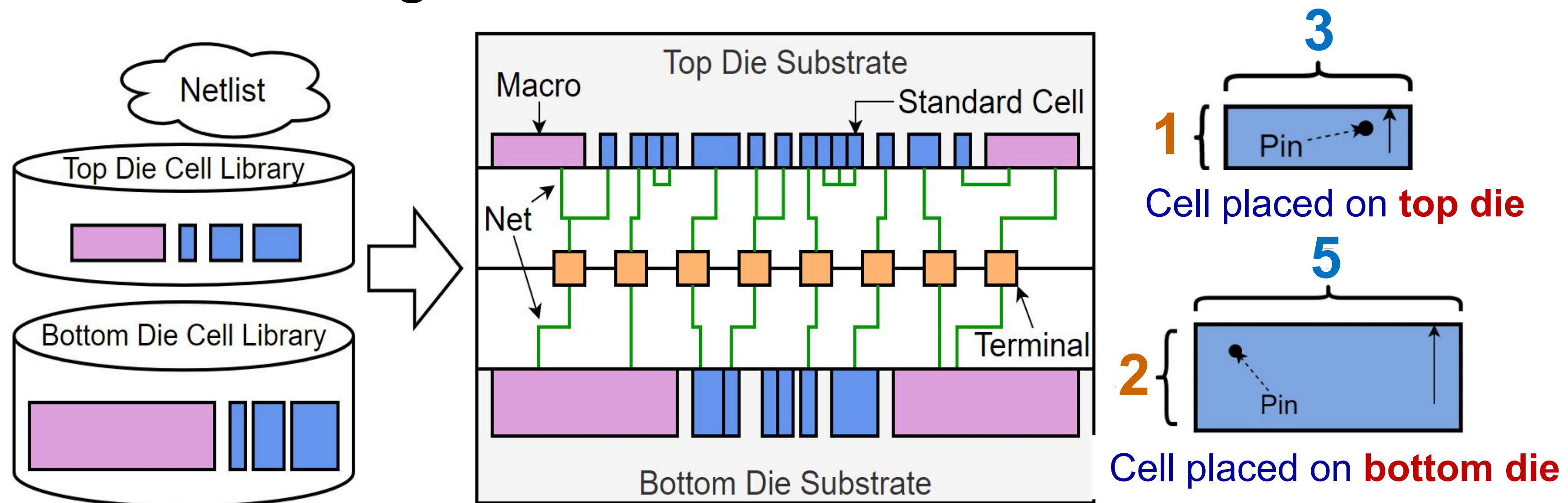


Warpage-aware TCG-based floorplanning

Suhir, "Interfacial stresses in bimetal thermostats," *J. Appl. Mech.*, 1989.

# Multi-die, Multi-technology Placement

- **Dies integrated into a package could be fabricated with different technology nodes, so block (standard cell or macro) sizes are changed "dynamically" with die assignments.**
  - Signals are connected by hybrid bonding terminals.
- **Chicken-and-egg challenge: Block dimensions change with die assignments.**



# 2023 ICCAD 3D F2F Placement Contest

SYNOPSYS

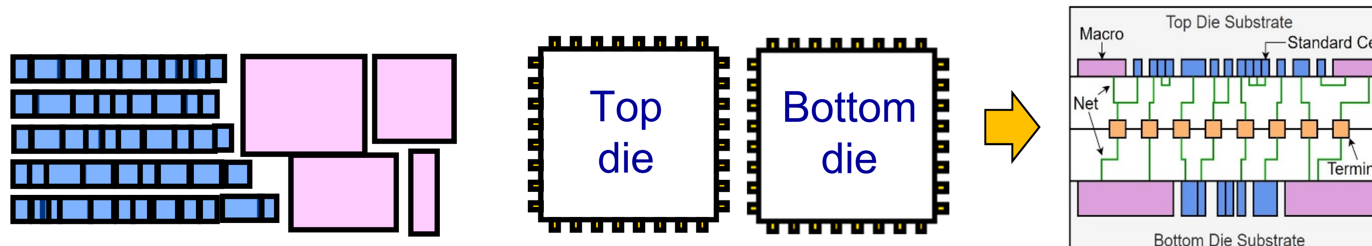
- **Input**
  - Netlist (including macros and standard cells)
  - Cell libraries
  - Terminal cost
- **Objective: minimize the scoring function**

$$HPWL_{top} + HPWL_{bottom} + N_{term}C_{term}$$

Total Wirelength — Terminal Cost

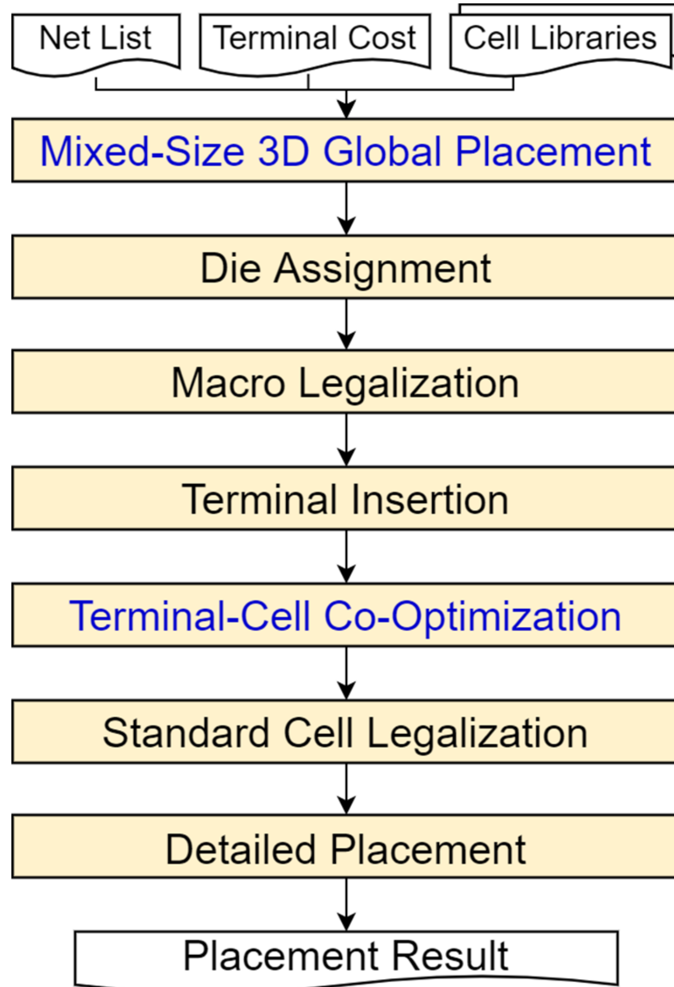
- **Constraints**
  - Non-overlapping blocks
  - Spacing between terminals
  - Maximum utilization rates on each die

2023 CAD Contest @ ICCAD
NTU: 1st Place



# Our Placement Framework

- Chen, et al., “Mixed-size 3D analytical placement with heterogeneous technology nodes,” DAC’24 **(1st Place at the 2023 ICCAD CAD Contest).**




**Find the desired positions for each macro & standard cell using 3D analytical placement.**

**Assign each component to its closest die, considering die utilization constraints.**

**Remove macro overlaps using constraint graphs and integer linear programming.**

**Insert terminals to current optimal positions.**

**Simultaneously optimize the standard-cell & terminal positions using analytical placement.**

**Legalize standard cells using Abacus & Tetris.**

**Refine cell and terminal position further.**

# 3D Analytical Placement

- **Formulate an unconstrained optimization problem**

$$\textbf{min} \quad W(x,y) + \alpha Z(z) + \boldsymbol{\lambda} N(x,y,z)$$

**Wirelength** **Terminal Cost** **Density**

- Use our **Weighted-Average** model [Hsu, Chang, Balabanov, DAC-11, TCAD-13; US Patent, 2014] for wirelength optimization

$$W(\mathbf{x},\mathbf{y}) = \sum_{e\in E}\left(\frac{\sum_{v_i\in e} x_i \exp(x_i/\gamma)}{\sum_{v_i\in e}\exp(x_i/\gamma)} + \frac{\sum_{v_i\in e} x_i \exp(-x_i/\gamma)}{\sum_{v_i\in e}\exp(-x_i/\gamma)} + \frac{\sum_{v_i\in e} y_i \exp(y_i/\gamma)}{\sum_{v_i\in e}\exp(y_i/\gamma)} + \frac{\sum_{v_i\in e} y_i \exp(-y_i/\gamma)}{\sum_{v_i\in e}\exp(-y_i/\gamma)}\right)$$

$$\alpha Z(\mathbf{z}) = \sum_{e\in E}(\alpha + w_e)\left(\frac{\sum_{v_i\in e} z_i \exp(z_i/\gamma)}{\sum_{v_i\in e}\exp(z_i/\gamma)} + \frac{\sum_{v_i\in e} z_i \exp(-z_i/\gamma)}{\sum_{v_i\in e}\exp(-z_i/\gamma)}\right)$$

$\alpha$: Via cost
$w_e$: Net weight

- Apply ePlace-3D for density control [Lu et al., ISPD-16]

$$N(\mathbf{x},\mathbf{y},\mathbf{z}) = \frac{1}{2}\sum_{v_i\in V} q_i \psi_i(\mathbf{x},\mathbf{y},\mathbf{z})$$

$$\xi(\mathbf{x},\mathbf{y},\mathbf{z}) = \left(-\frac{\partial\psi}{\partial x}, -\frac{\partial\psi}{\partial y}, -\frac{\partial\psi}{\partial z}\right)$$

$q_i$: Volume of cell $i$
$\psi$: Potential function
$\xi$: Electric field

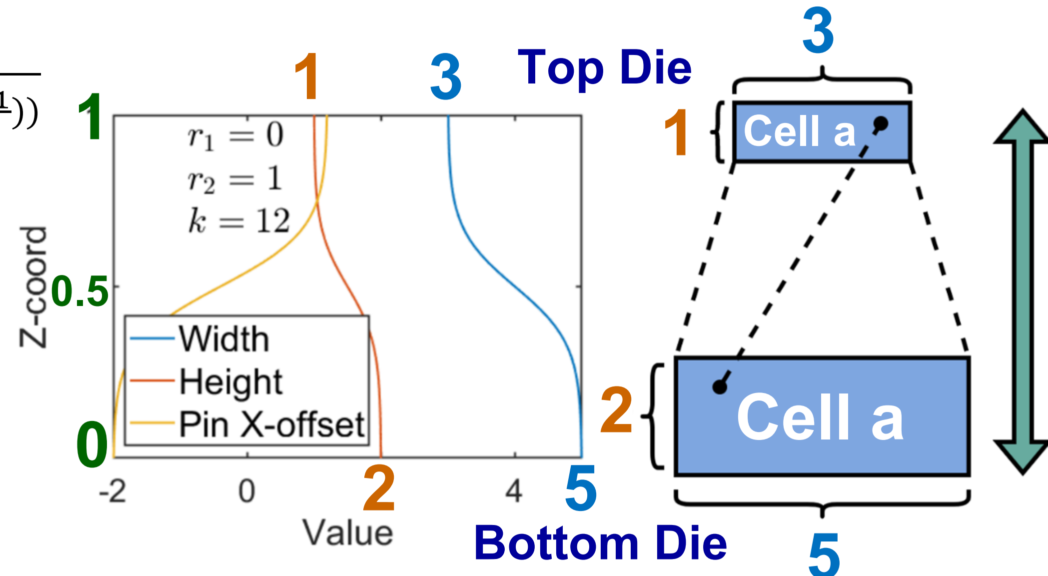
- **Optimize the objective function using gradient descent**
- **Increase $\lambda$ gradually to reduce the density to find the desired macros & standard cell positions $(x,y,z)$**

# Die Assignment

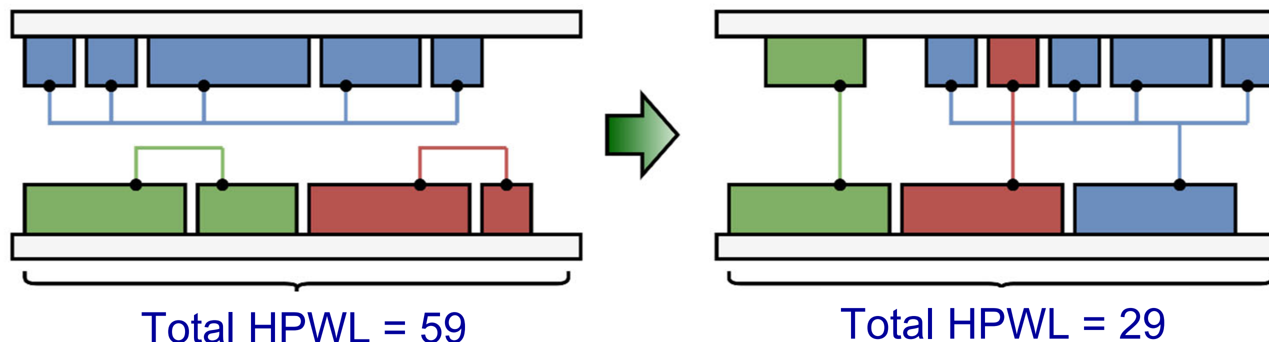
- **Relax the discrete assignment variable & use a sigmoid function to achieve smooth shape transition**

$$f(z) = s_1 + \frac{s_2 - s_1}{1 + \exp\left(\frac{-k}{r_2 - r_1}\left(z - \frac{r_2 + r_1}{2}\right)\right)}$$

  - $z$: Position on z-axis
  - $s_1$: Value at bottom die
  - $s_2$: Value at top die
  - $r_1$: Bottom die z-coordinate
  - $r_2$: Top die z-coordinate
  - $k$: User defined parameter

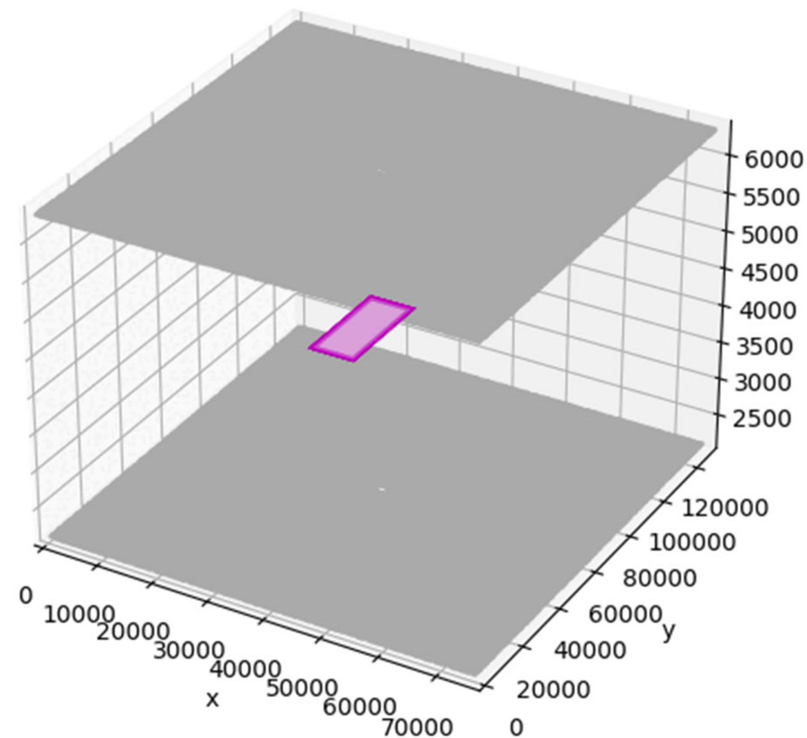



- **Partition the network using low-pin nets**



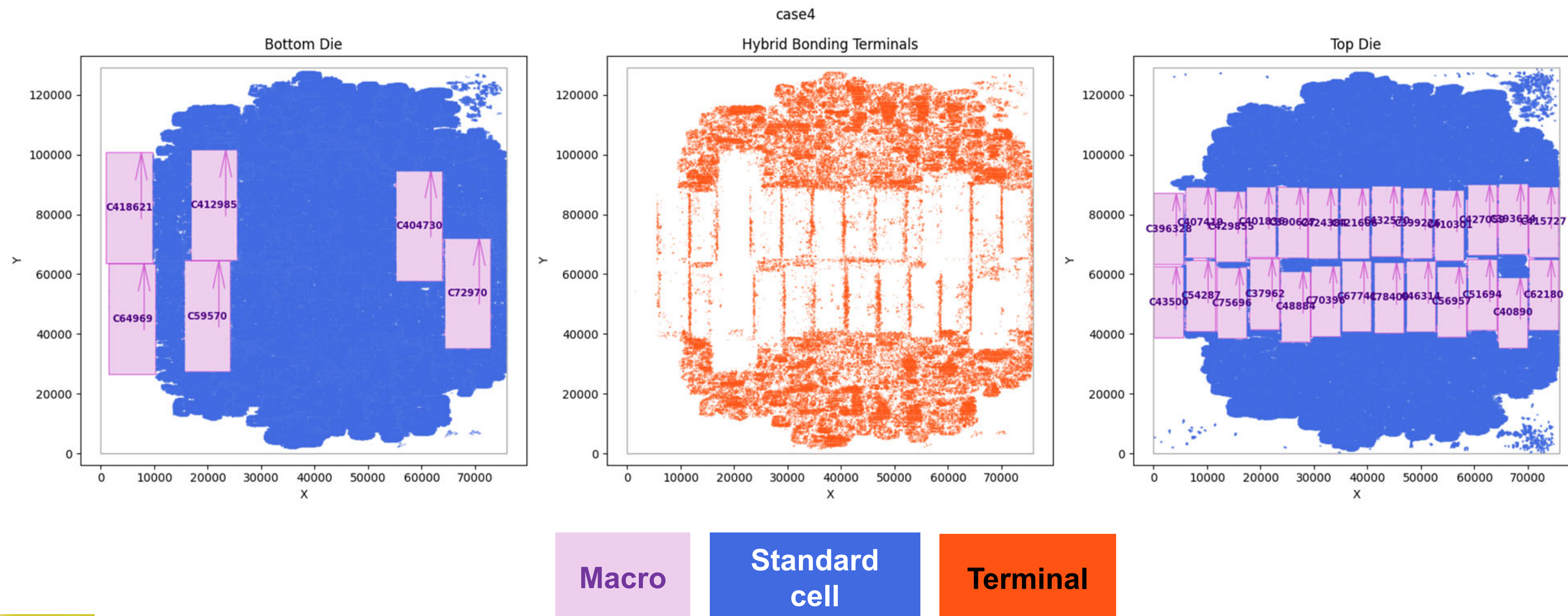
# Demo: 3D Mixed-Size Global Placement

- Benchmark: Case4
  - #macros: 32
  - #standard cells: 740,211
  - #nets: 758,860



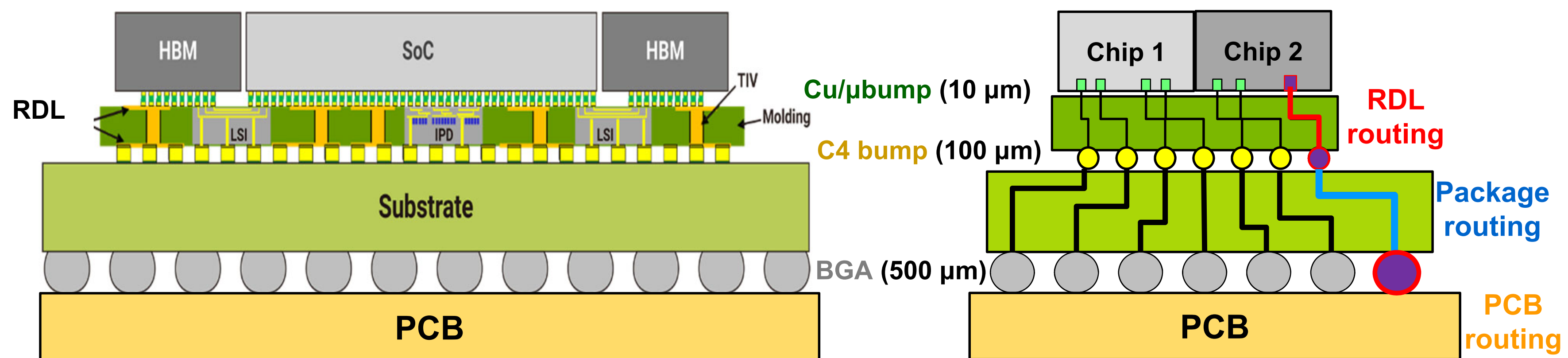
# Final Placement Result

- Benchmark: Case4
  - #macros: 32; #standard cells: 740,211; #nets: 758,860
- Results
  - Top-die wirelength: 864,717,801
  - Bottom-die wirelength: 181,388,384
  - Terminal cost: $160,993 \times 10 = 1,609,930$



# Package/PCB Routing

- **Modern packages require high-performance connections among chiplets through multi-layer redistribution layer (RDL) interposers or substrate** (e.g., CoWoS, InFO).
  - Use RDLs to connect I/O pads (chip) to bump pads (package) to achieve better quality (e.g., more areas for I/Os, higher performance interconnections, better signal integrity and robustness)
- **The rising complexity requires any-obtuse-angle routing to consider complex design rules**
  - Consider complex via stacking rules, irregular vias, inline/staggered bumps, max. metal density for reliability, differential pairs, shielding, etc.



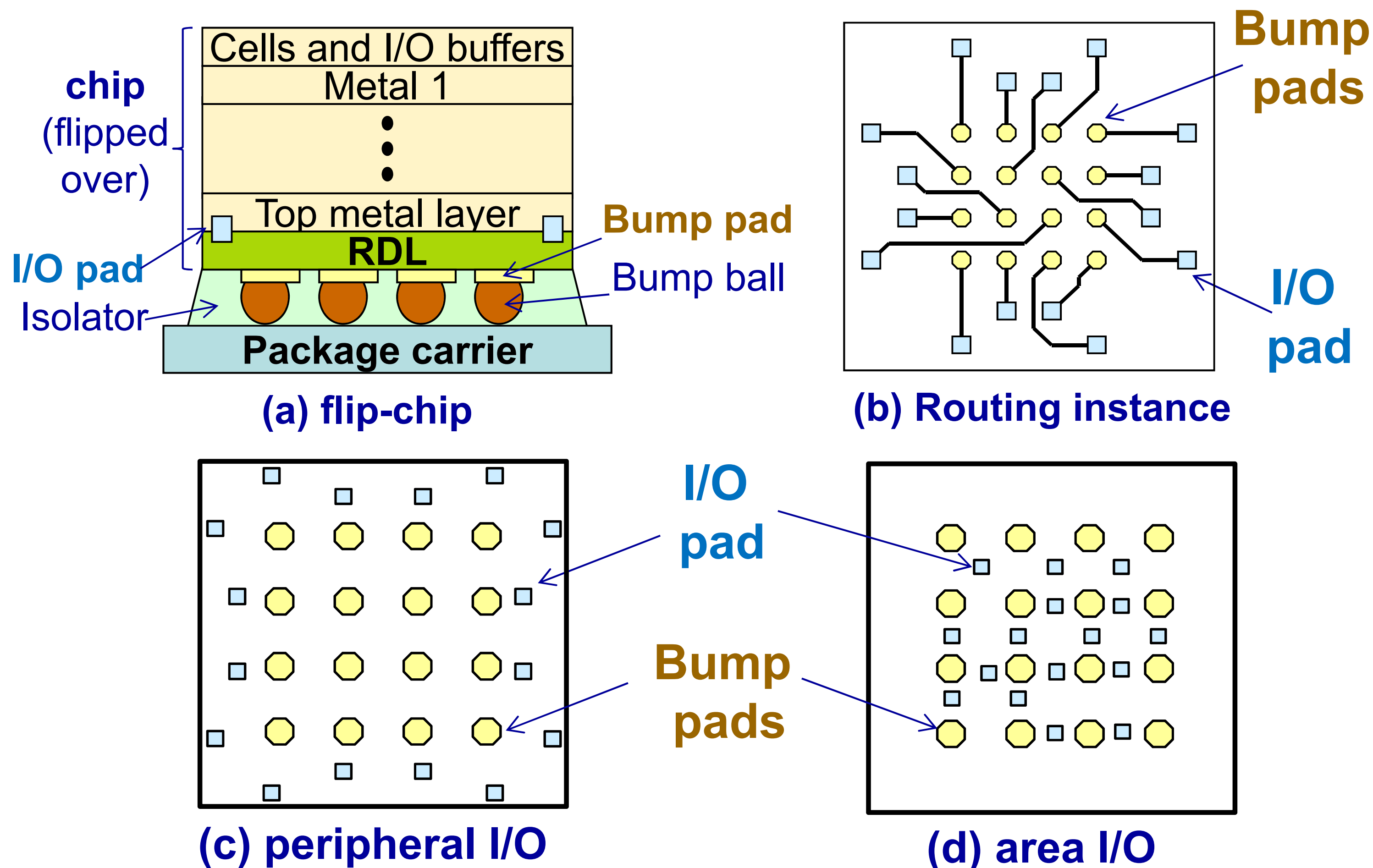

Source: TSMC (w. revision)



Y.-W. Chang

# Flip-Chip RDL Routing

- Flip-chip routing routes I/O pads to bump pads on RDL
- Two types of packages: (a) peripheral-I/O; (b) area-I/O




(a) flip-chip

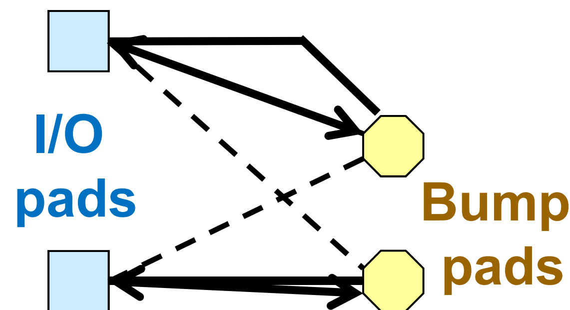
(b) Routing instance

(c) peripheral I/O

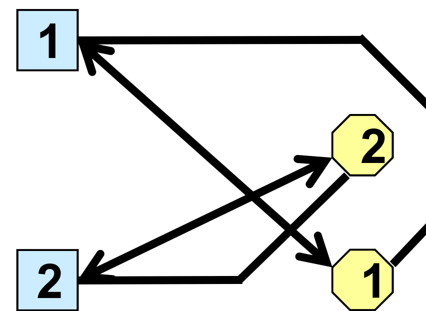
(d) area I/O

# Free- vs. Pre-assignment Routing

- **Free-assignment routing**
  - Each bump pad can be connected to any I/O pad
  - Router can assign each I/O pad to a bump pad
- **Pre-assignment routing**
  - Connections between I/O and bump pads are predefined
  - Router must connect a bump pad to its pre-assigned I/O pad




Free-assignment




Pre-assignment

# RDL Routing Classification & Techniques

**Peripheral I/O**

**Free-Assignment** ↔ **Pre-Assignment**

*Peripheral I/O, free-assignment*
**Fang et al., ICCAD'05 (TCAD'07): Flow**
Liu et al., DAC'10: VD+Flow
**more**

*Peripheral I/O, pre-assignment*
Fang et al., DAC'07 (TCAD'09): ILP
Lee et al., ICCAD'09 (TCAD'12): DP
**more**

*Peripheral-I/O, unified FA/PA*
Lin et al., ICCAD'16: DP+Flow

*Area I/O, free-assignment*
Fang & Chang, ICCAD'08 (TCAD'09): Flow
Yan & Chen, ASPDAC'09: VD
**more**

*Area I/O, pre-assignment*
Chang et al., ICCAD'19: VD

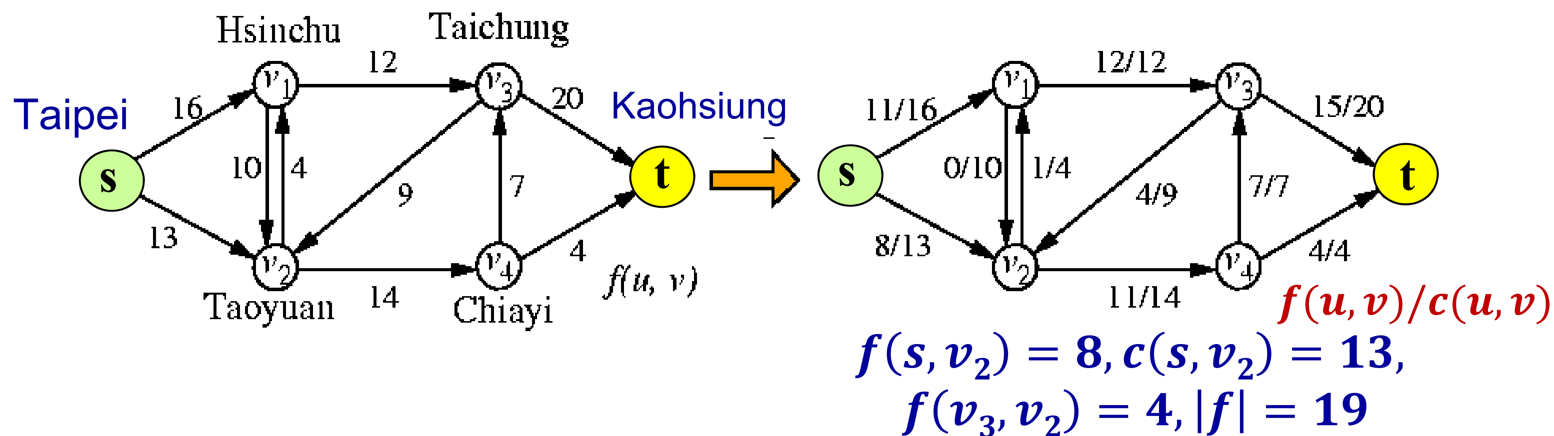
*Area-I/O, unified FA/PA*
Fang et al., DAC'09 (TCAD'10): VD+Flow
Wen et al., DAC'20: DP
Cai et al, DAC'21: VD

**Area I/O**

**Flow: Network-flow**
**VD: Voronoi Diagram**
**ILP: Integer linear programming**
**DP: Dynamic Programming**

# Network Flow Formulation

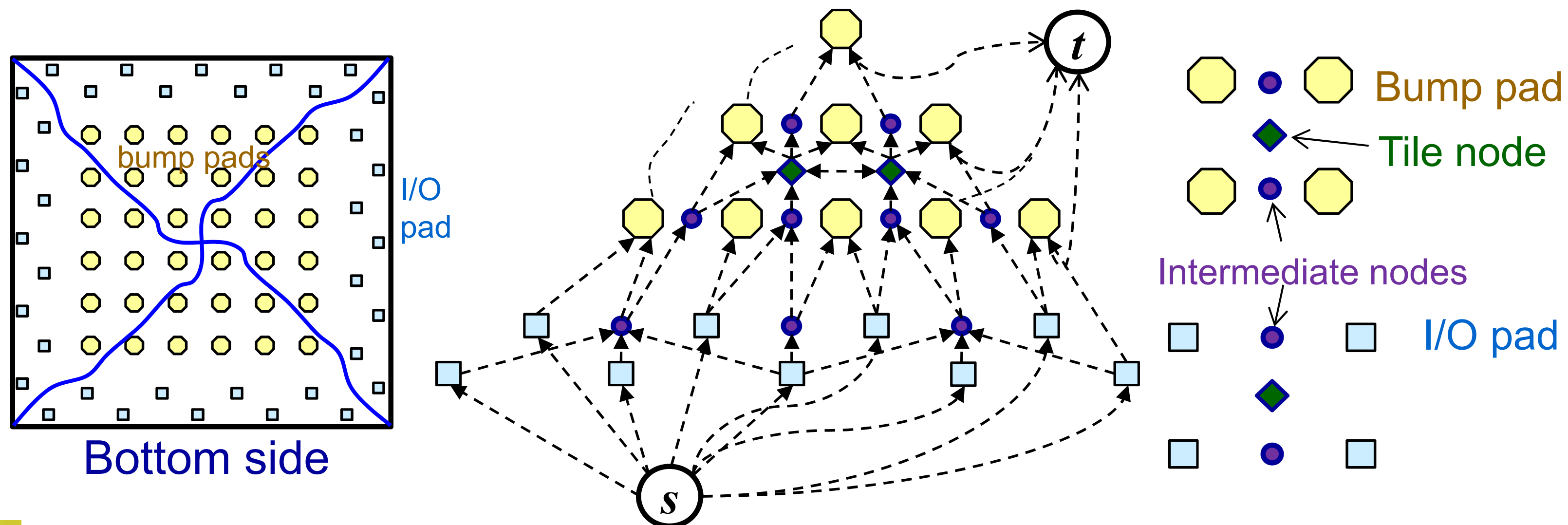
- **Network flow problem:** Given a flow network *G* with source *s* & sink *t*, find a maximum flow from *s* to *t*.
- Network flow formulation is useful for modeling **resource assignment (supply-demand) problems.**
- **Key limitation: Control only the total flow, but not the individual flow at a specific node/edge** (NP-complete multi-commodity flow problem)



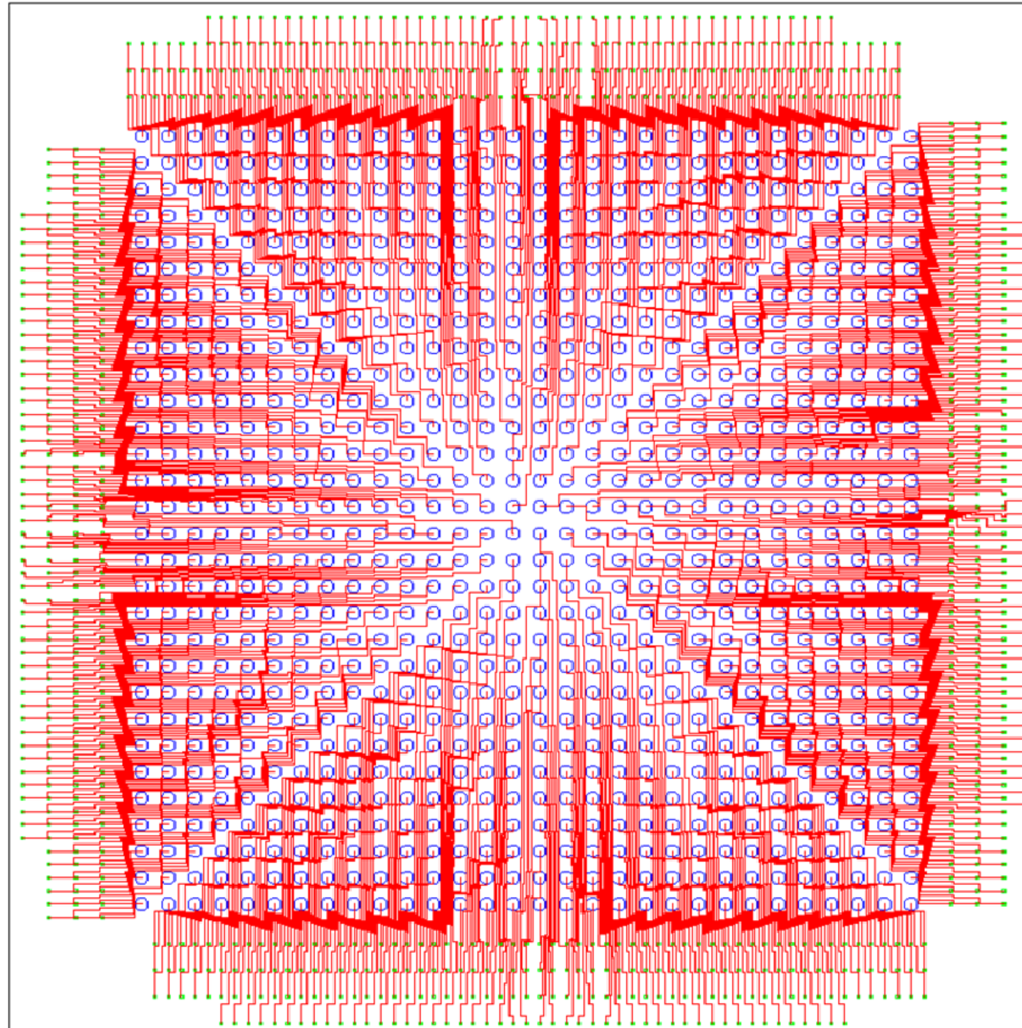

$f(s, v_2) = 8, c(s, v_2) = 13,$
$f(v_3, v_2) = 4, |f| = 19$

# Network Flow for Free-assignment Routing

- Most existing works are based on **Minimum-Cost Maximum-Flow (MCMF)** [Fang et al., ICCAD'05 & more]
- Divide a chip into four regions & route region by region
  - I/O pad ➔ source node
  - Bump pad ➔ sink node
  - Wire ➔ unit flow
  - Max-flow ➔ highest routability
  - Min-cost ➔ shortest wirelength



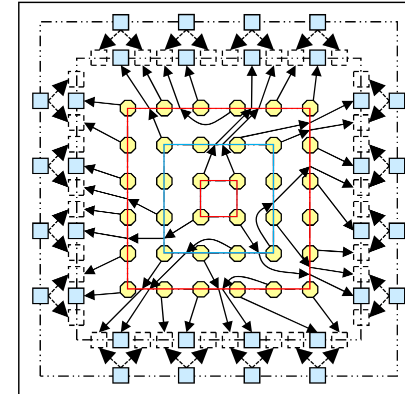
# Peripheral I/O, Free-assignment Routing Result



Circuit: fs900

# Dynamic Programming (DP) for Pre-assignment Routing

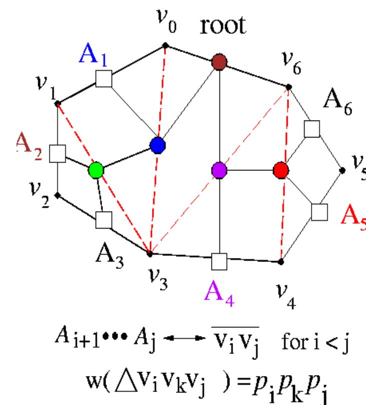
- **Utilize the regularity of the flip-chip structure to achieve better solutions**
  **[Lee et al., ICCAD’09, TCAD’12]**
- **DP works best on linearly ordered objects that cannot be rearranged!!**
  - Examples: Characters in a string, matrices in a chain, left-to-right order of leaves in a search tree, points on a line/polygon/circle boundary
- **Apply DP for pre-assignment routing**

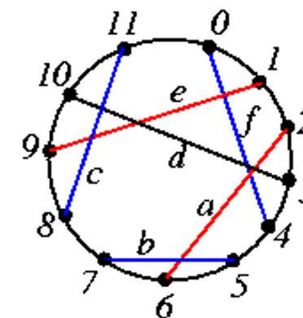


**String: NTUEE**

**Matrix chain**

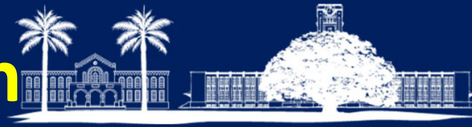
$((A_1\ (A_2\ A_3))((A_4\ A_5)\ A_6))$



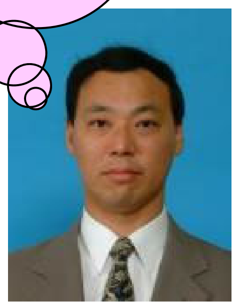

**Points on a line/polygon/circle boundary**

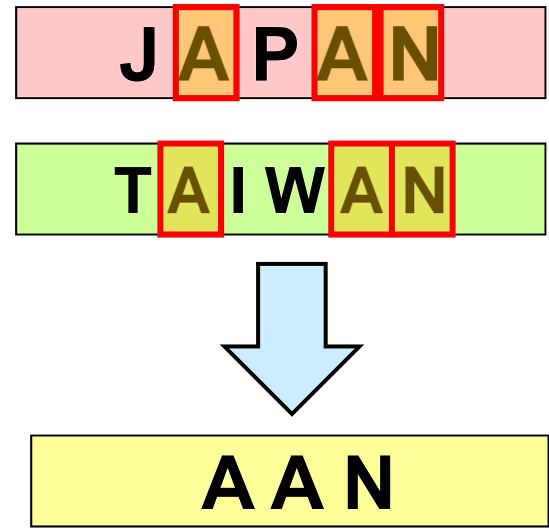
# "Da Vinci Code" between Japan and Taiwan



## 2010 Design Automation Conf. (DAC'10)

Why are Taiwanese so friendly to Japanese?






Reason #1…
#2…
…#100…

Dr. Kazutoshi Wakabayashi (NEC)

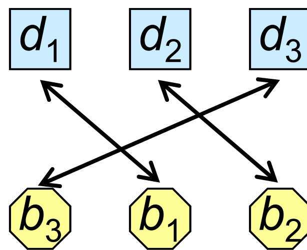
Yao-Wen Chang (NTU)

**Longest Common Subsequence**

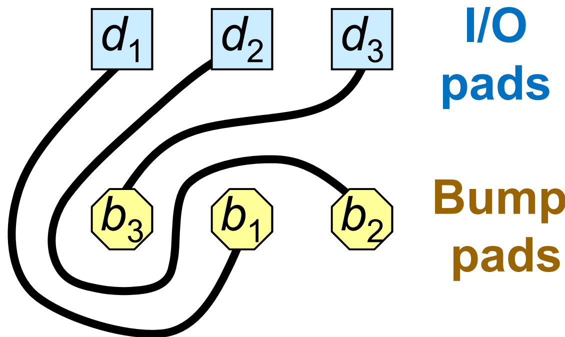
**Similarity: 50%+!!**

# Detours Minimization by DP

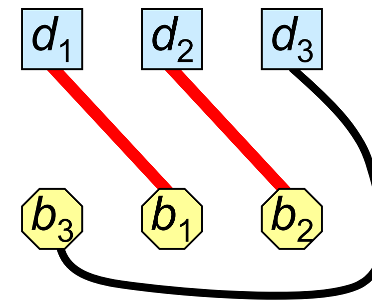
- **DP to minimize detours for pre-assignment routing**
- **Longest common subsequence (LCS) computation**




(a) seq.1=<1,2,3>
seq.2=<3,1,2>

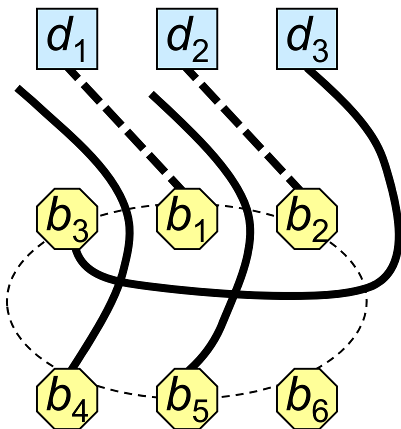



(b) Common subseq = <3>

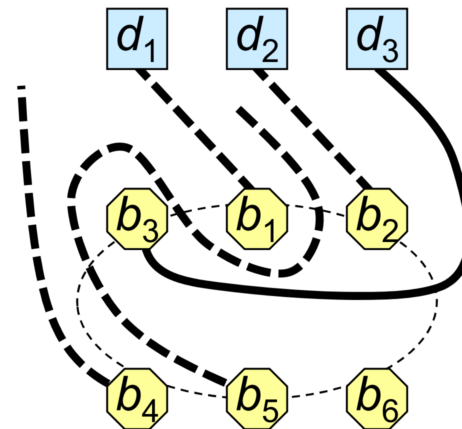



**(c) LCS= <1,2>**

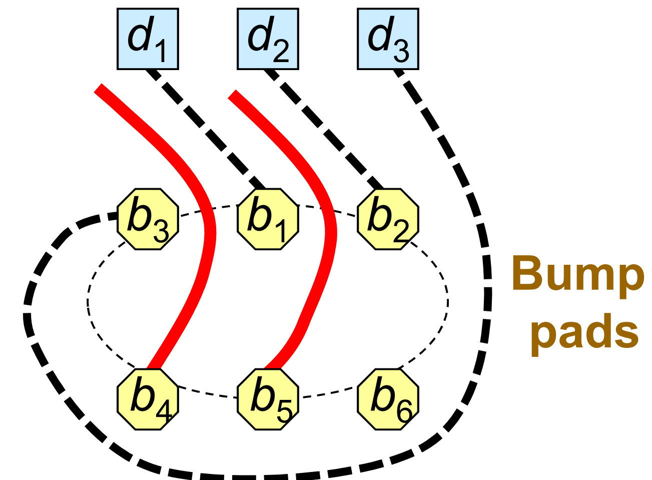
- **Maximum planar subset of chords (MPSC) computation**




(d) chord set: {3,4,5}




(e) subset:{3}

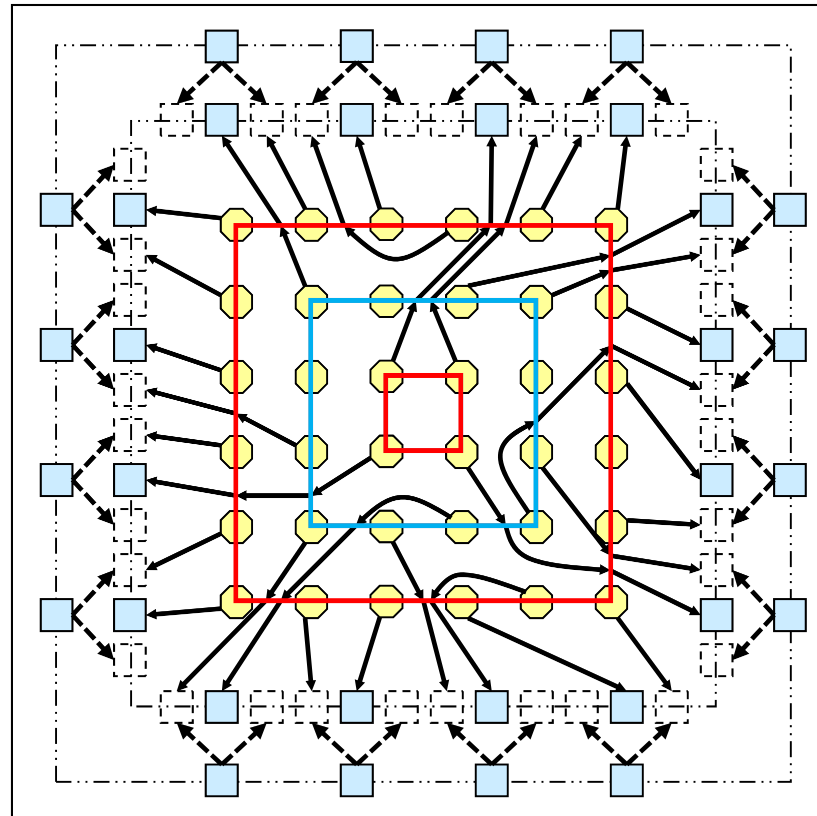



**(f) MPSC = {4,5}**

# Pre-assignment Ring-by-Ring Routing

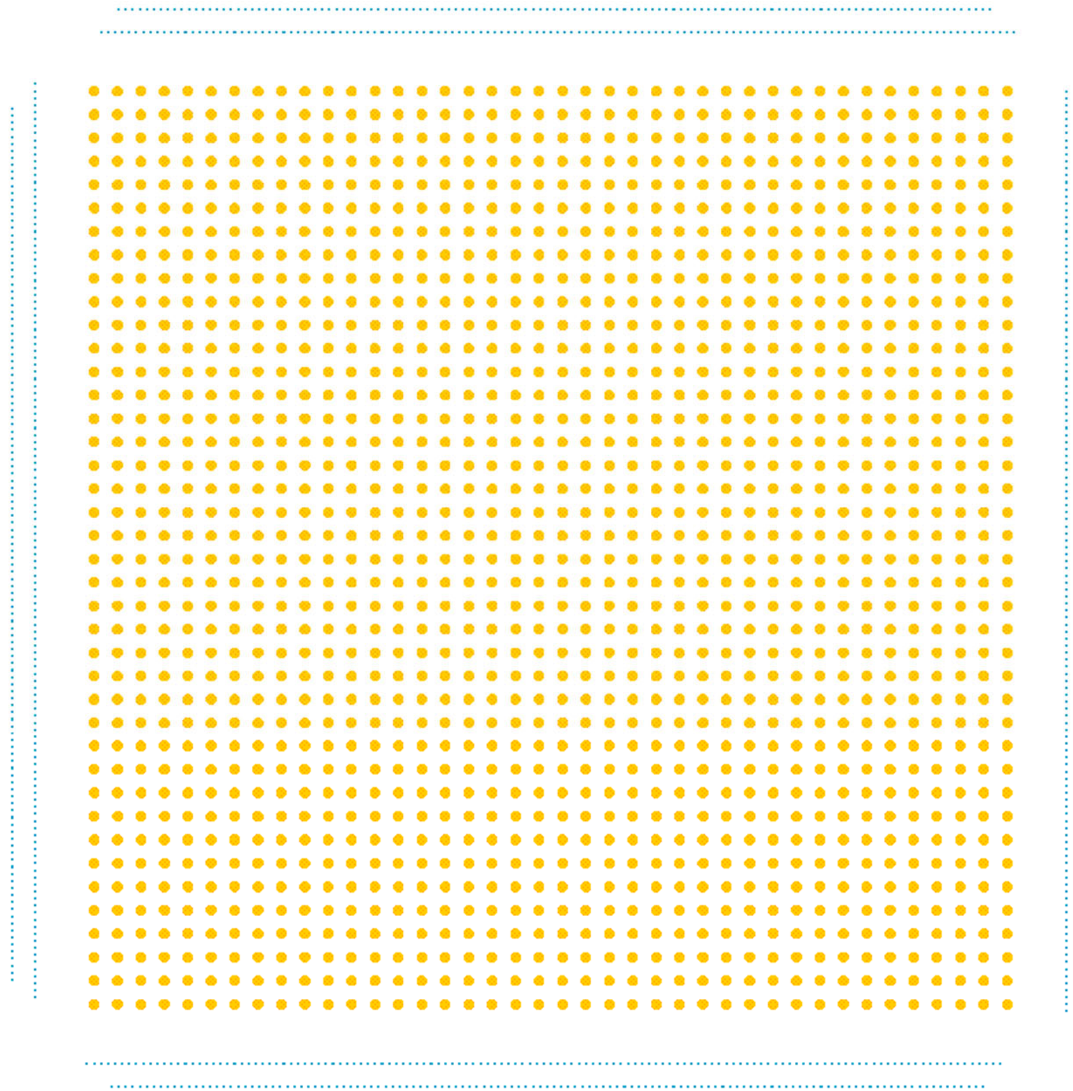
- Identify feasible sequences for I/O pads and apply LCS
- Decompose chip into rings of bump pads and route from inner rings to outer rings
- Keep applying MPSC between two adjacent rings (red ring & blue ring)

current ring
preceding ring



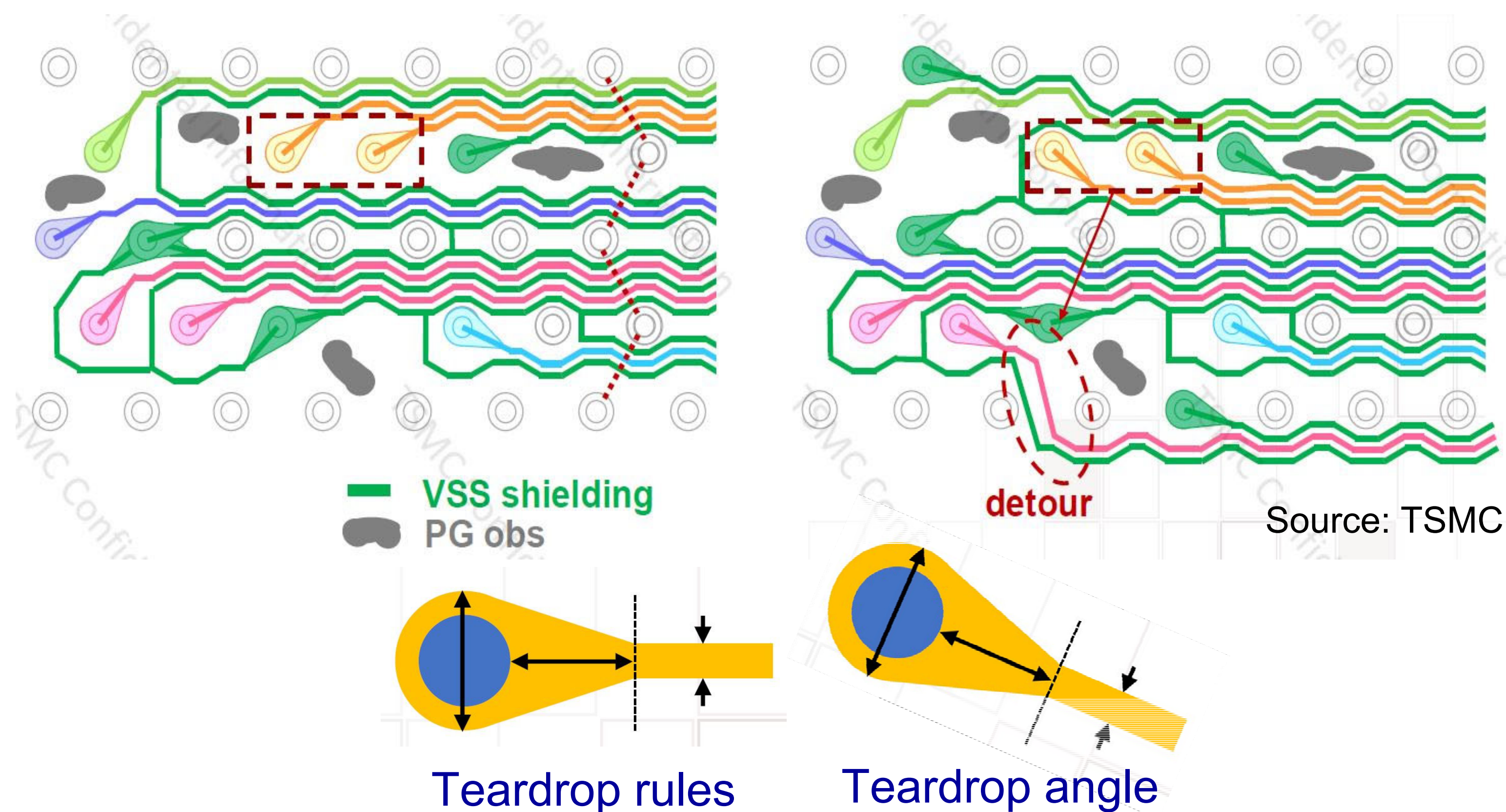
Achieve over 100X speedups than ILP with better quality!!

# Demo: Circuit fc2624



# Any-obtuse-angle Routing

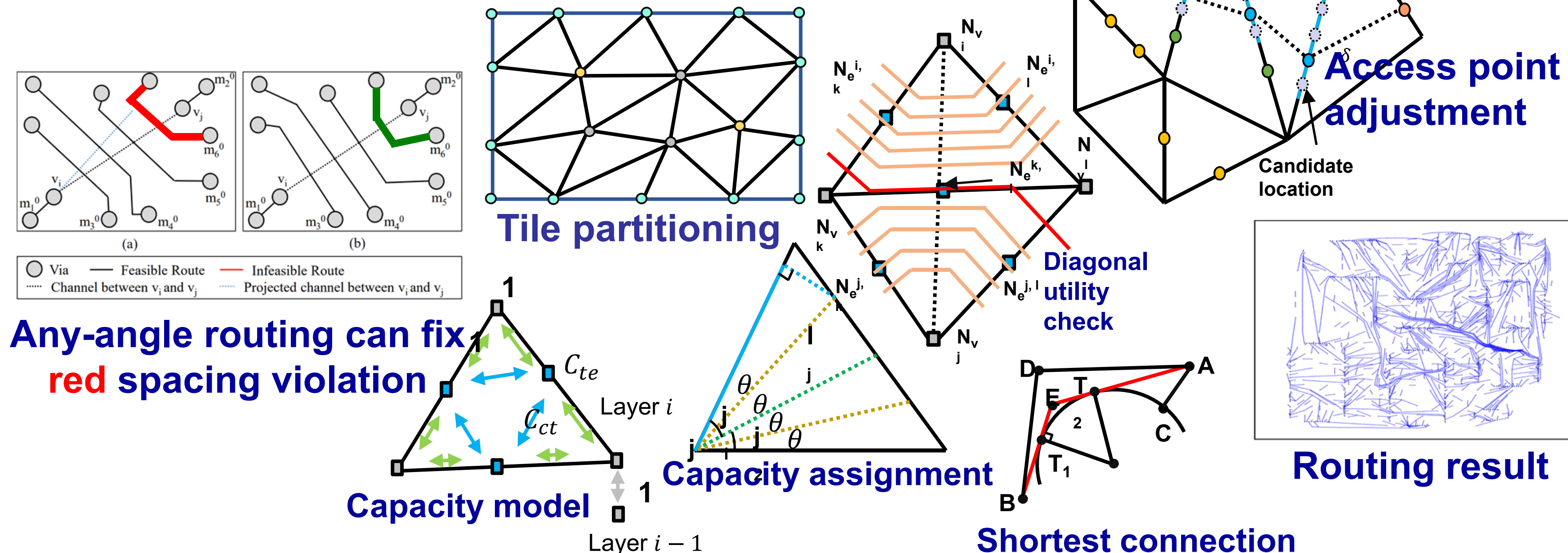
- **Need any-obtuse-angle routing to maximize flexibility**
- **Plan teardrop angles to maximize the routability**
  - Local teardrop angles could affect far-away connections




Teardrop rules    Teardrop angle

# Any-obtuse-angle Package Routing

- Chung et al., “Any-Angle Routing for Redistribution Layers in 2.5D IC Packages,” DAC’23
- **1st any-angle router with multiple RDLs**
- **Apply Delaunay triangulation for tile partitioning**
- **Model intra- and inter-tile capacity to generate routing guides**
- **Apply dynamic programming-based access point adjustment to route multiple nets simultaneously**
- **Achieve the best published routability**



Y.-W. Chang

# General Package Routing Considerations

- Differential pairs (for phase matching), plating-through-hole (PTH) placement with shielding, length matching for skew, matched escape orders for bus routing, constrained regions, inline/staggered bump structures, bump breakout, etc.
- More: irregular vias, max. metal density for reliability, etc.

Differential Pair

phase matching

Plating-through-hole PTH Placement

GND PTH

PTH

FMB and GND shielding

Match Group

Skew (length) matching

PG

SMT

Mutual-Escape Bus Routing

Matched escape orders

High-density Bump Breakout

Escape quality

Different Bump Structure

Inline, x/y stagger

Constraint Region

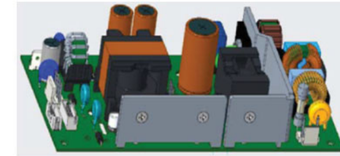
neck L/S

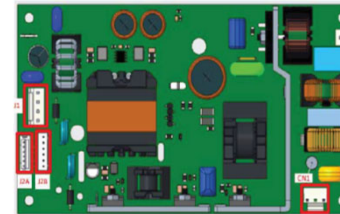
global L/S

Source: TSMC

# PCB Placement and Routing

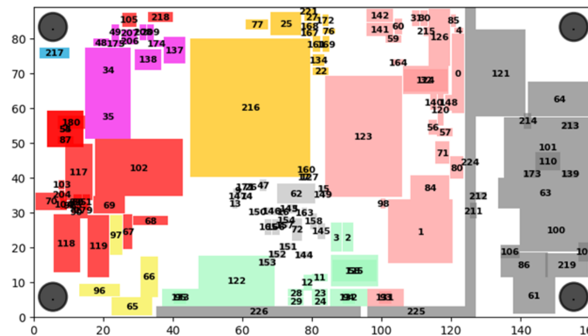
- Place irregular-shaped 3D components
- Route signal/PG wires of different widths
- Considerations: component orientations, diverse wire widths, dynamic spacing rules, power loop topologies, heat sink insertion, restricted areas, etc.

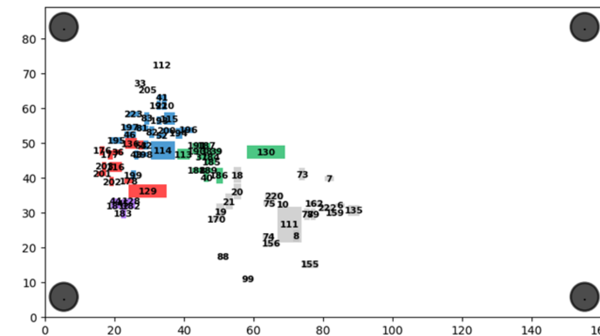




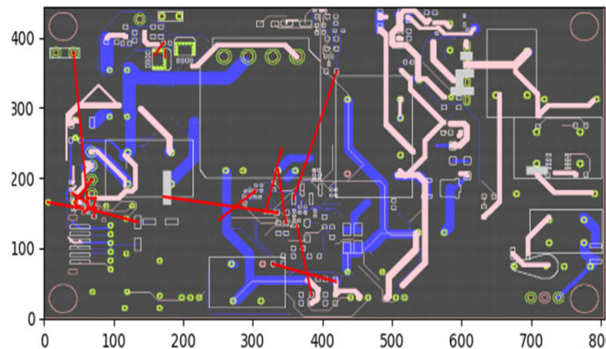
Irregular 3D components

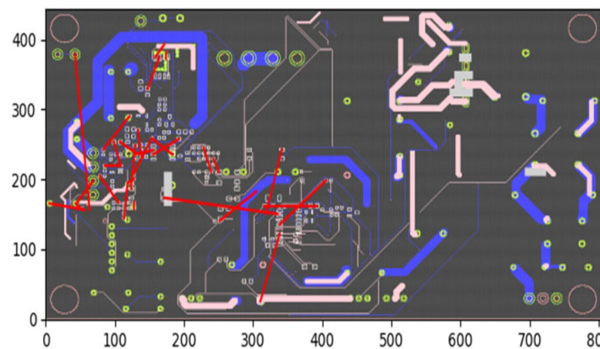
Placement



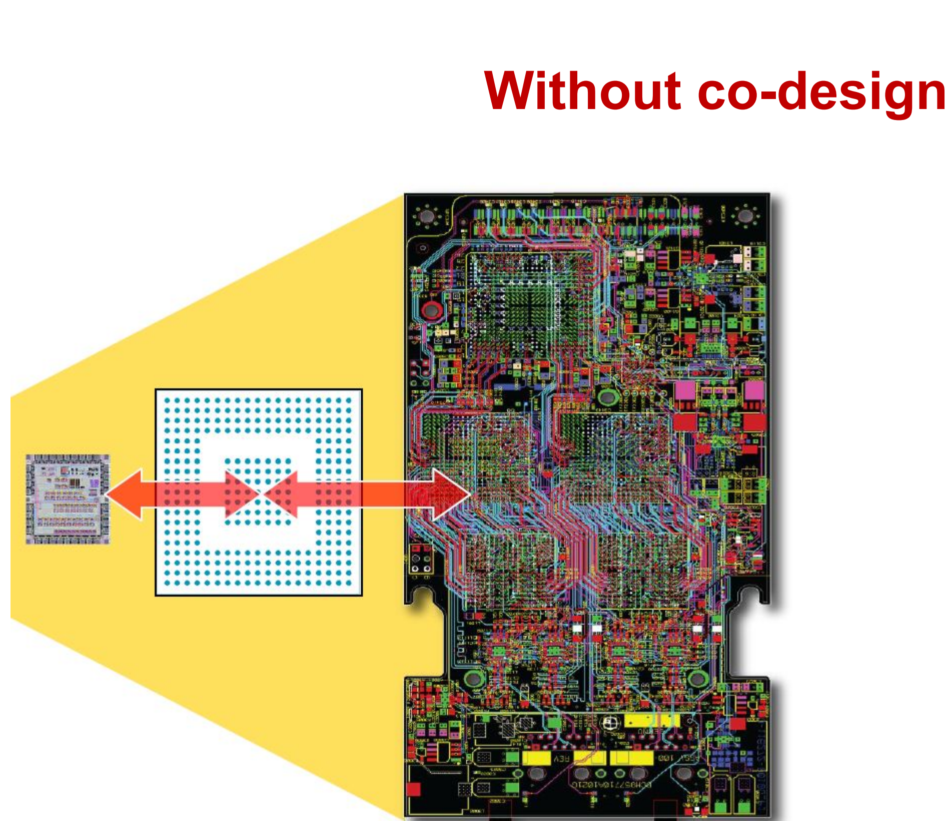

Routing



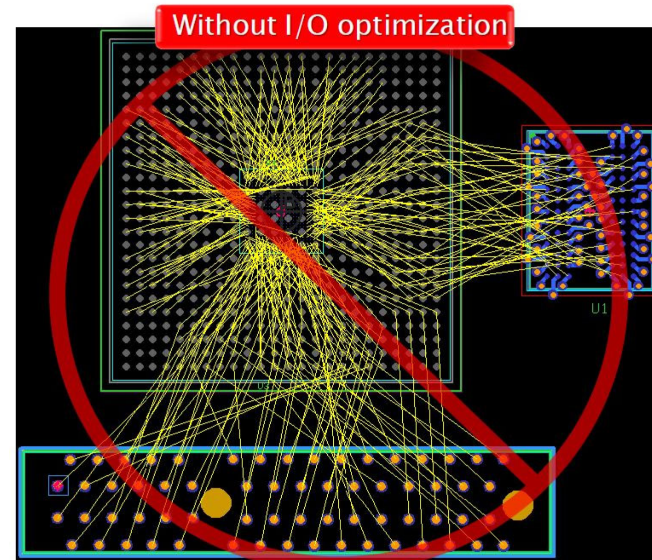



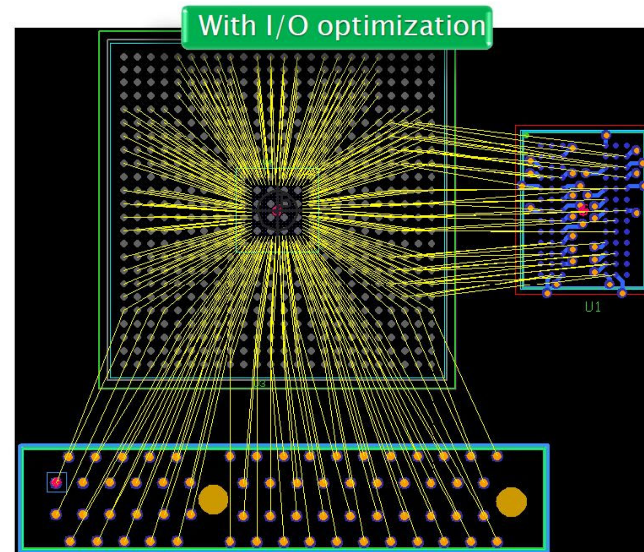
# Chip-Package-Board Co-Design

**Without co-design**



**John F. Park, ICCAD'10**

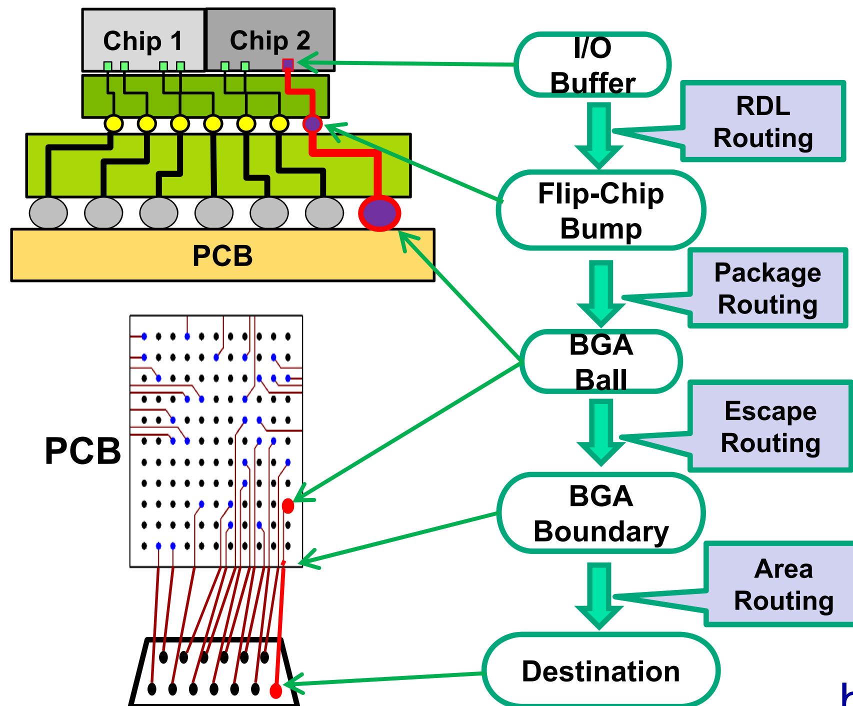


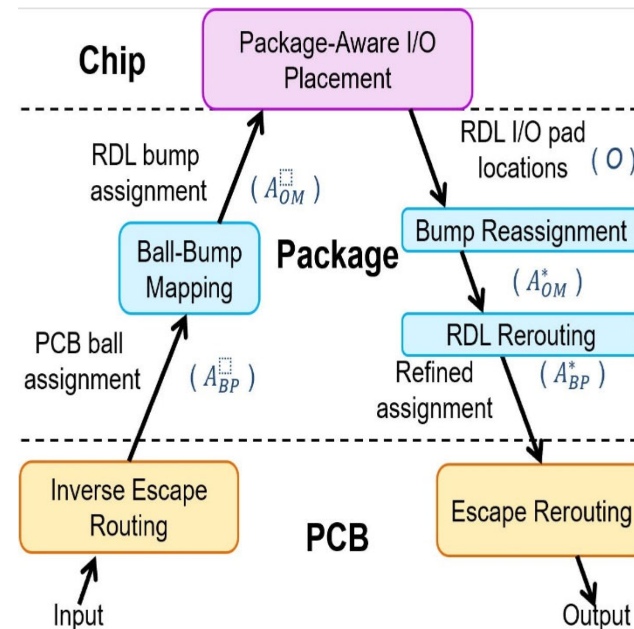




**With co-design**

# Chip-Package-Board Co-Design

- Lee and Chang, "A chip-package-board co-design methodology," DAC'12 (Fang, Ho, and Chang, ICCAD'08)
- Route a signal from an I/O buffer, to a flip-chip bump (RDL routing), and finally at a BGA ball (package routing), ready for PCB connection
- **Board-driven Λ-shaped codesign flow: Inverse escape routing (PCB), ball-bump mapping (package), package-aware I/O placement (chip), bump reassignment & RDL rerouting (package), escape rerouting (PCB)**




board-driven Λ-shaped codesign flow

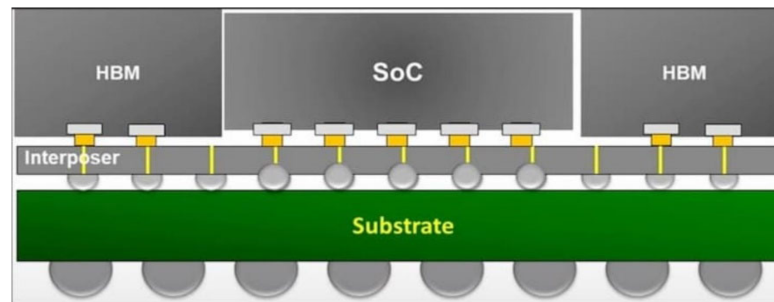
# Co-packaged Optics (CPO)

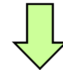
- **TSMC has announced to integrate silicon photonics components into its advanced package by 2025**

NIKKEI Asia

TSMC bets on silicon photonics to enable more powerful ChatGPT

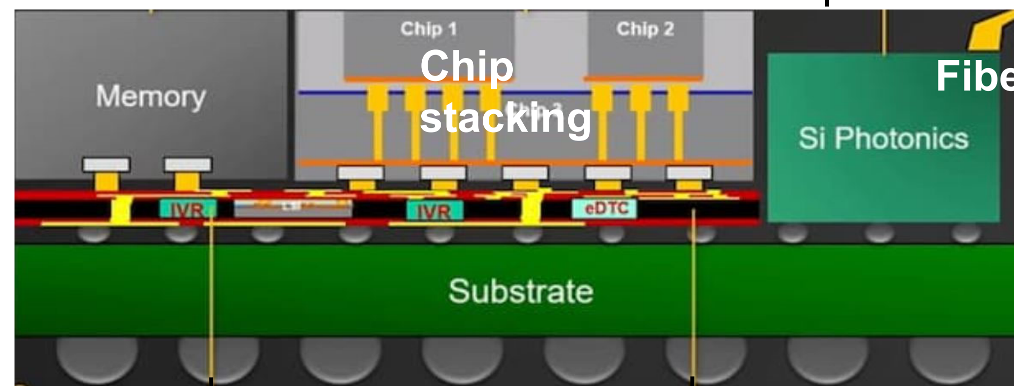
Emerging field becomes new battleground for major tech players




2400 W -> 850 W 

**Co-packaged Optics**

**RDL interposer + LSI + eDTC**
(embedded Deep Trench Capacitor)




Integrated voltage regulator

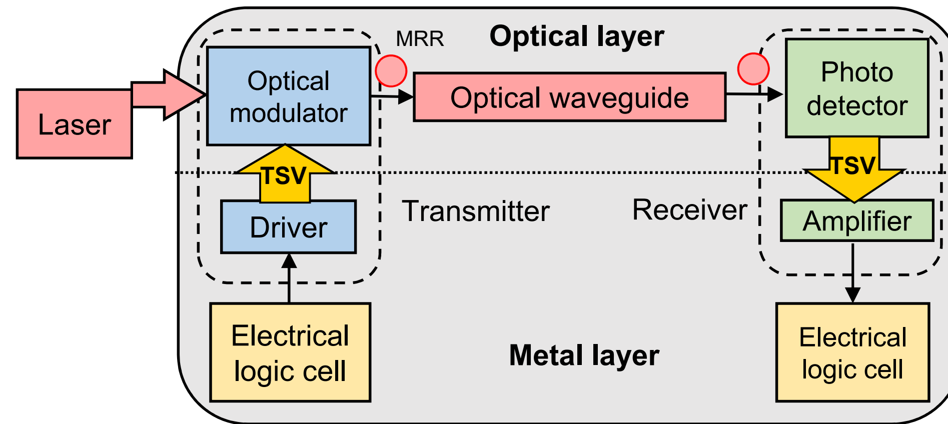
> 6X interposer

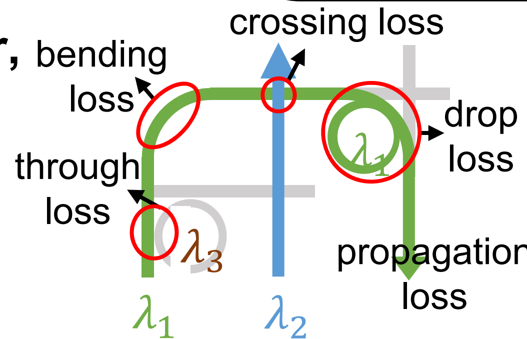
Source: TSMC (ISSCC'24)

# Optical Routing

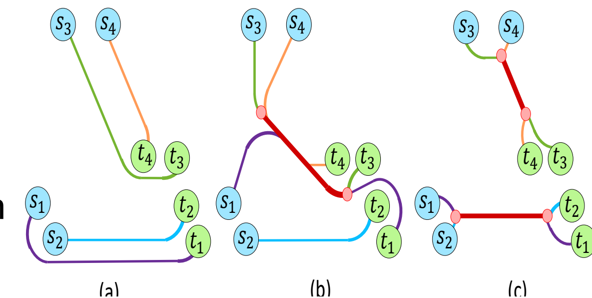
- Lu, Yu, Chang, "On-chip optical routing with provably good algorithms for path clustering and assignment," *TCAD*, 2022
- **Allows a connection in any direction & signal crossings w. higher bandwidth, lower power, and faster speed**
- **Transmit signals on shared waveguides**
  - Need signal clustering to better use WDM (Wavelength Division Multiplexing)
- **Minimize transmission loss & wavelength power**

**Electrical-optical architecture**

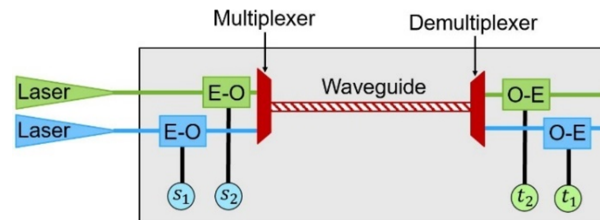



**Transmission loss**



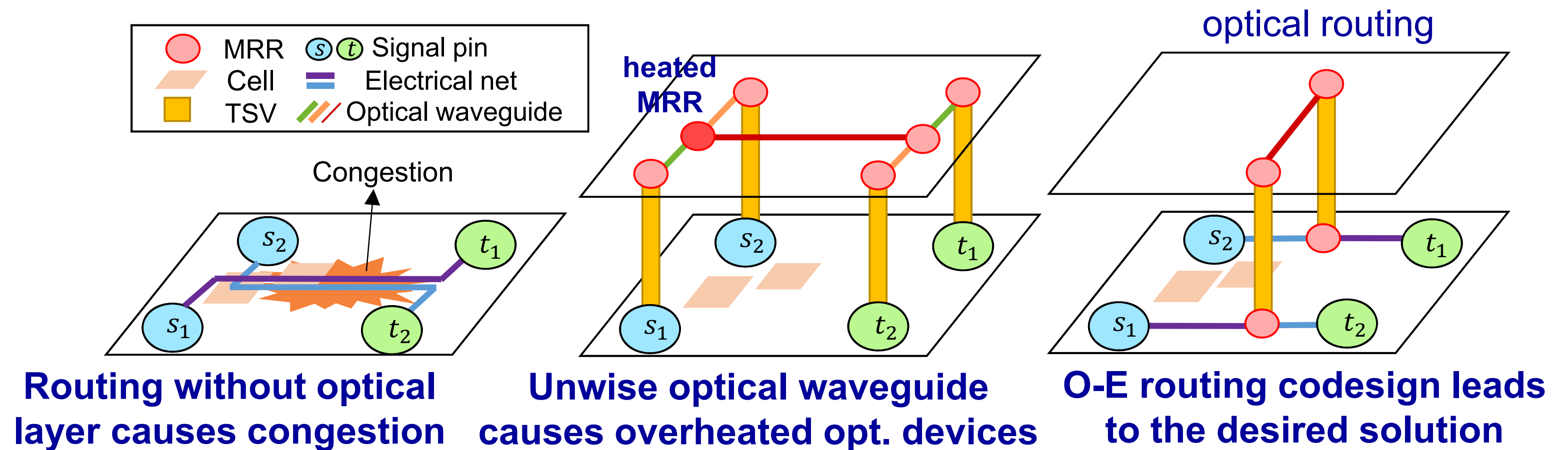

**Signal clustering** for WDM



Wavelength Division Multiplexing (WDM)

# Optical-electrical Codesign

- Lu, Chen, Hsu, and Chang, “Thermal-aware optical-electrical routing codesign for on-chip signal communications,” DAC’22
- **Generate global optical waveguides to optimize thermal impact, routing congestion, and wirelength**

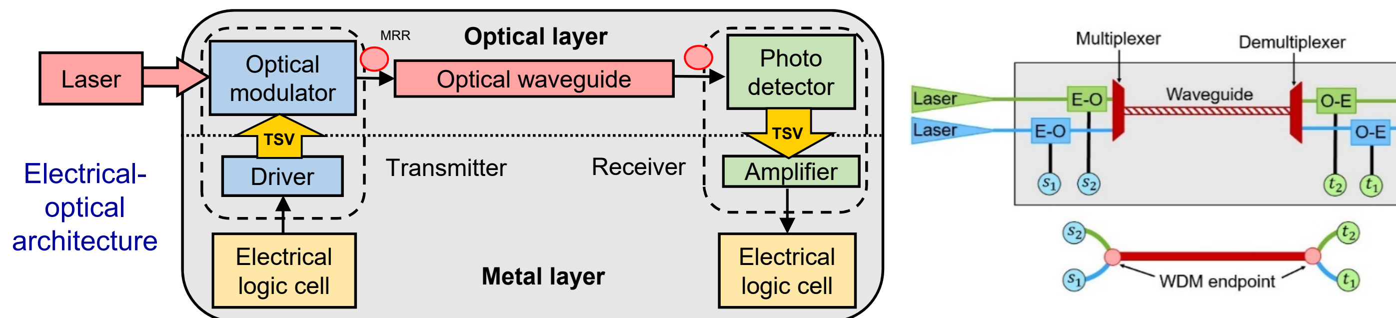



**Routing without optical layer causes congestion**

**Unwise optical waveguide causes overheated opt. devices**

**O-E routing codesign leads to the desired solution**

**Thermal-aware codesign for power, wirelength, congestion optimization!**



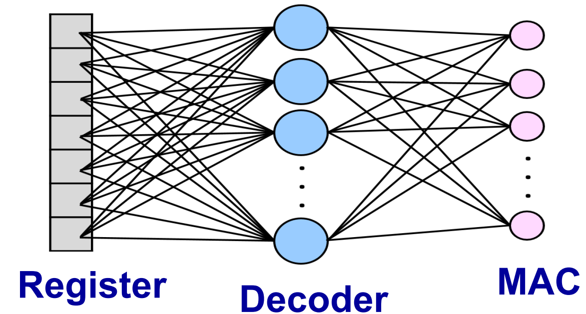
# AI for EDA & EDA for AI

EDA AI

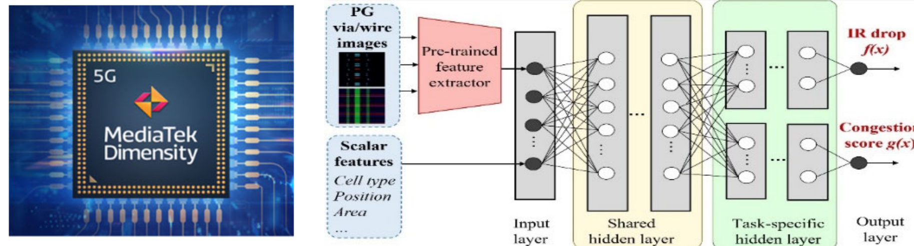
- **AI technologies reshape EDA**
  - Enhance EDA techniques with machine learning
- **EDA helps AI system designs**
  - Optimize the design of CNN kernel structure

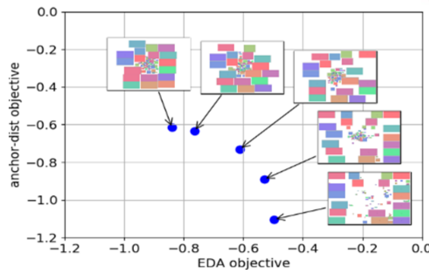
**EDA for AI** (chip design)

kernel structure of a CNN accelerator




**AI for EDA**

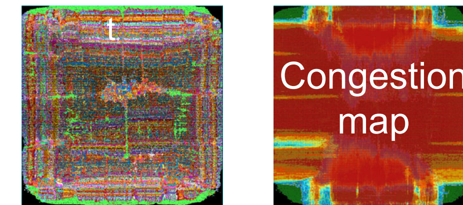


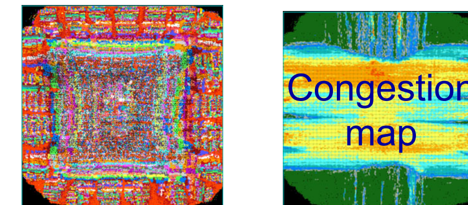
工商時報 謝易晏 2022.05.05

臺大攜手聯發科、至達科技產學研發 超越Google晶片擺置彈性

**DAC'22: Macro Placement by MTK/MAXEDA/NTU**




**Placement by "leading" industry tool**



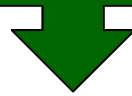

**Placement by NTU/MAXEDA tool**

**(acquired by Synopsys in 2023)**

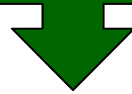
**DAC'21**

# Outline

**Technology Background**

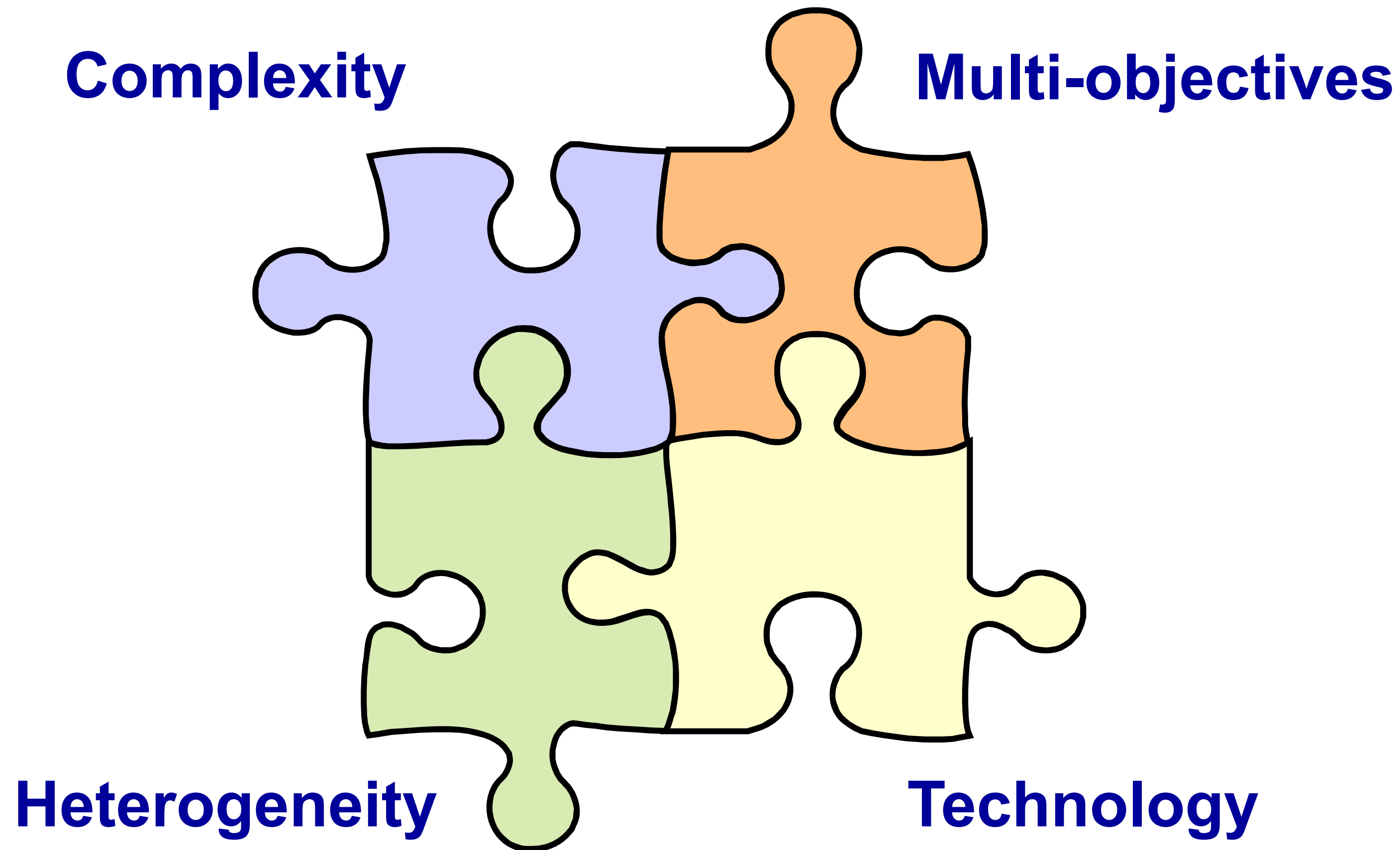


**Physical Design Challenges/Solutions**



**Concluding Remarks**

# Modern Design/EDA Challenges



# Example 3D Placement Challenges

- **High complexity**
  - 100M objects + nets

**Complexity**

- **Cross-physics constraints**
  - Multi-die technologies, warpage, thermal, etc.

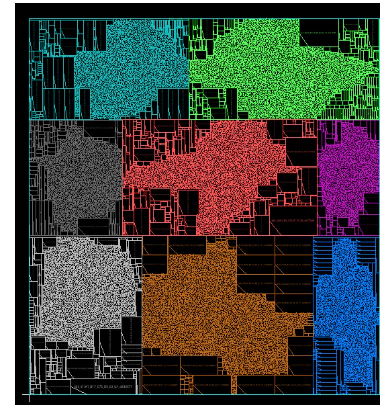
**Multi-objectives**

- **Mixed-cell-height, mixed-size placement**
  - 100K big macros with 100M small cells of multiple cell heights

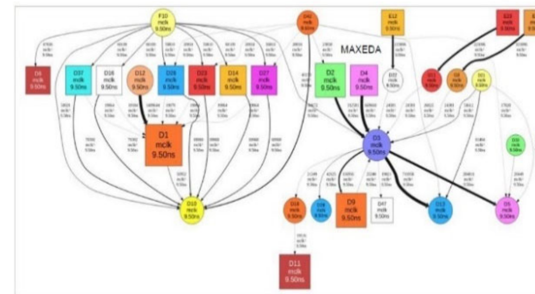
**Heterogeneity**

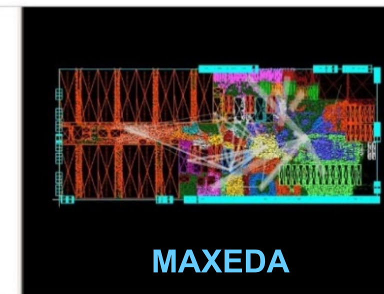
- **Emerging technologies**
  - AI, HI (bonding/integration TSV), etc.

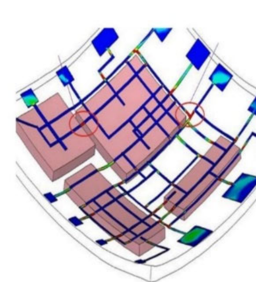
**Technology**



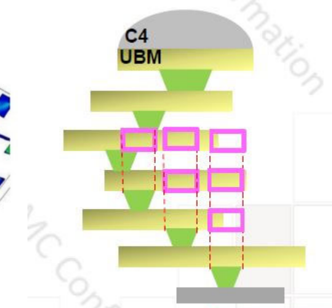
100M-cell + 100K-macro + 100M-net multi-die, multi-domain mixed-size design

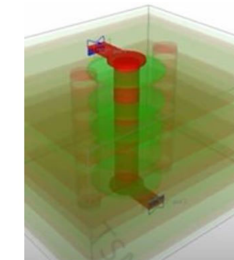


warpage



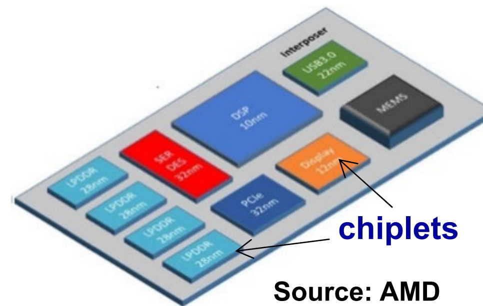
PTH placement (plating through hole)

Source: TSMC

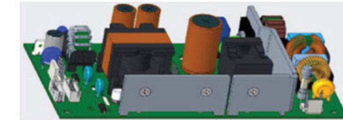
# Culture Clash vs. Collaborative Mindset

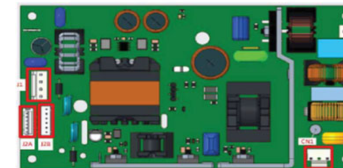
Source: MediaTek

Source: Apple




Source: AMD

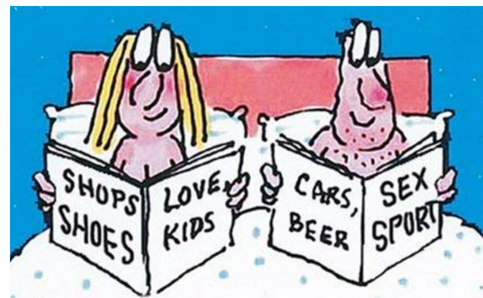




Source: Delta

## chip to package

Large-scale, regular, homogeneous components w. uniform design rules



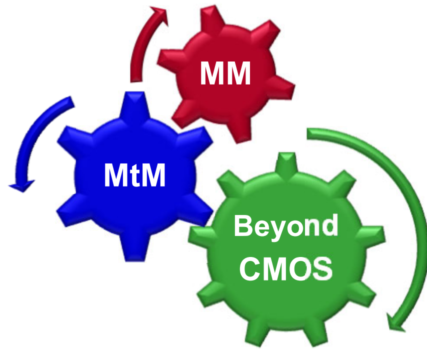

Source: Gray Jolliffe

## board to package

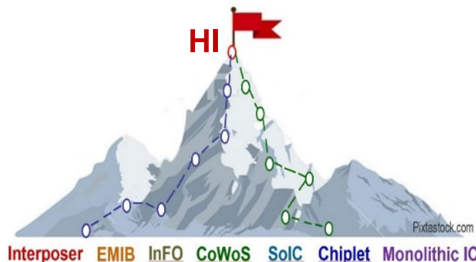
Small-scale, irregular, heterogeneous components w. complex design rules

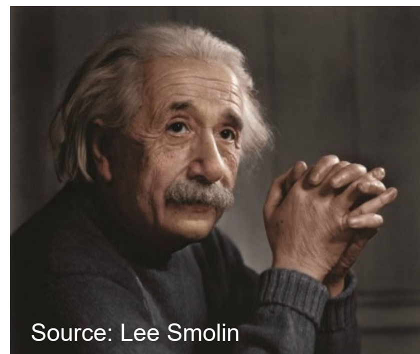
**Chip Designers (Men) Are from Mars, Board Designers (Women) Are from Venus…**

# Conclusions




- Multiple approaches to achieving the power/performance/area (PPA) holy grail
- Multiple complementary options to achieve the HI targets
- Need an ecosystem to achieve the ultimate PPA goal, where multi-physics domains need to be considered and EDA is essential
- Technology challenges will not limit our progress because imagination can bring us to the endless frontier!!





# Thank You!!

National Taiwan University