Physical Design Challenges in Modern Heterogeneous Integration

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Technology Drivers

Artificial intelligence

Intelligent medicine

High-performance computing

Automotive electronics

5G/6G+IoT+Cloud

Big data analytics
Technology Options for Achieving PPA Target

**Higher Performance**

**Lower Power**

**Smaller Area**

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**More-than-Moore (MtM)**
- Heterogeneous Integration
- 2.5D/3D Packaging
- RF/MEMS/sensor/analog
- Optical component

**More Moore (MM)**
- Continued Scaling
- FinFET/Nanosheet/CFET
- Multiple patterning/EUV/DSA
- Backside power delivery

**Beyond CMOS**
- New Devices
  - GaAs/SiC/GaN
  - Ferroelectric (FeFET)
  - Graphene (GFET)
  - Carbon nanotube (CNTFET)

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More Moore Technology Landscape

- **Transistor**
  - HKMG Planar FET
  - FinFET
  - FD-SOI High-mobility channel
  - GAA (nanowire)
  - MBC (nanosheet/RibbonFET)
  - CFET
  - GrapheneFET

- **Patterning**
  - Mask optimization
  - ArF 193nm Immersion
  - Double patterning (SADP) SAQP
  - Triple patterning
  - EUV
  - EUV + MP (Multiple patterning)
  - DSA + EUV + MP

- **Interconnect**
  - Copper
  - AirGap
  - TSV
  - n-TSV
  - Backside (BS) power delivery (PowerVia)
  - Optical interconnect
  - Graphene wiring (SBBA)

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Economic advantages of More-Moore scaling are getting smaller (high manufacturing costs with advanced transistors, EUV, etc.), making the More-than-Moore trends more obvious.

Heterogeneous integration with 3D stacking is promising with better system PPA, form factor, functionality, etc.

Issues: complexity, yield, heat, interconnect cost, mechanical stress, testing, standardization, etc.

More-than-Moore Heterogeneous Integration

Technology evolution

Source: Cadence (revised)
Advanced Packaging for TSMC’s Success

- Dr. Morris Chang (2016): InFO is key for TSMC to beat Samsung for Apple’s A10 chip orders

TSMC Will Regain Apple In A10, InFO

First published InFO package router [Lin et al., ICCAD’16], US Patent 9,928,334, 2018 (with AnaGlobe)

NVIDIA H100 Hopper TSMC CoWoS-S Flip Chip Ball Grid Array

source: TSMC

2023
Heterogeneous Integration & Multi-Physics Domains

Interconnect Scale:

- Devices (nm)
- Packages (um-nm)
- Boards (mm-cm)
- Systems (cm-m)

Nanomaterials
- Embedded Components
- Interconnections
- Substrate & System Integration
- Sensors
- Opto SiP
- Digital SiP
- Analog & RF
- MEMS Packaging
- Sensors
- Mixed Signal Electrical Design
- High-Density I/O
- 3D ICs
- System on Chip (SOC)
- Mechanical Design for Reliability
- Power & Batteries
- Thermal
- Laser
- Photodetector
- Chip-last embedded IC
- EBG & isolation
- GaAs RFIC
- Antennas
- MEMS
- Bio-Sensor
- Bio-Sensor
- 3D Capacitors
- Mechanical Design for Reliability
- Source: Georgia Tech PRC, http://www.prc.gatech.edu/

**System/Physical**
- System partitioning
- Architecture evaluation
- Placement & Routing
- Timing

**Electrical**
- Power/signal integrity
- EMI
- Power maps
- Mobility shifts

**Thermal**
- Joule heating
- Hot spots
- Device cooling

**Mechanical**
- Warpage
- Metal migration
- Delamination
- Fatigue

**Optical**
- Laser power
- Routing
- Thermal effect
Multi-Physics Interactions

- **Electrical/Physical (EM/IR)**
  - IR drop generates additional heat
  - Temperature affects metal conductivity
  - Temperature distribution induces stress

- **Thermal**
  - Temperature affects metal conductivity and dielectric permittivity, wavelength of light
  - Temperature affects metal conductivity
  - Temperature distribution induces stress
  - AC current generates heat

- **SI/PI (Electrical)**
  - Electrical

- **Optics (Optical)**
  - Optical

- **Stress (Mechanical)**
  - Mechanical
  - Stress induces transistor degradation

Source: TSMC/Ansys (w. revision)

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Multiple Options for Heterogeneous Integration (HI)

CoWoS
(Chip on Wafer on Substrate)
TSMC

Integrated fan-out (InFO)
TSMC, ASE, Amkor, etc.

Silicon interposer
TSMC/Xilinx (since 2012), Google, NVIDIA & AMD (GPU + HBM), etc.

Silicon bridge die
Intel, IBM, SPIL, etc.

Chiplet
AMD, etc.

Monolithic 3D IC
IMEC
**TSMC 3D Fabric™ (since August 2020)**

**King of Advanced Packaging??**

### Advanced Packaging (Backend 3D)
- **InFO**
  - Chip first
  - RDL interconnect
    - LSI + RDL interconnect
      - (RDL: Redistribution Layer)
- **CoWoS**
  - Chip last
  - Si interposer
    - RDL interposer
  - LSI + RDL interposer
    - (LSI: Local Si Interconnect)

### Chip Stacking (Frontend 3D)
- **CoW** Chip on Wafer
- **WoW** Wafer on Wafer
- **SoIC**
- **CoWoS**
  - Chip on Wafer on Substrate
  - silicon process, denser wires
  - **Dime** 1.35mm
  - **InFO** 0.8mm

**Integrated Fan-Out (InFO)** cheaper, wider/thicker wires

**Source:** TSMC

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**Future package with optics (2025)**

**Co-packaged Optics**

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Heterogeneous Integration (HI) Roadmap

- HI Roadmap since 2015 vs. ITRS & IRDS Roadmaps

2019 Version
Enabling Core Technologies and Building Blocks

8: Single & Multi-Chip Integration
9: Integrated Photonics
10: Integrated Power Electronics
11: MEMS and Sensor Integration
12: Communications
13: Co-Design
14: Modeling and Simulation
15: Materials and Materials Research
16: Emerging Research Devices
17: Test
18: Supply Chain
19: Security
20: Thermal Management
21: SiP & Modules
22: 2D and 3D Interconnects
23: WLP Fan-in & Fan-out

Applications

Chapter 1 Introduction

#2: HPC

3: IoT

4: Medical Health, Wearables

5: Automotive

6: Aerospace and Defense

7: Mobile

Heterogeneous Integration Technical Working Groups (TWGs)

Source: HIR Roadmap, 2019 (latest: 2023)

IRDS: IEEE International Roadmap for Devices and Systems (2016-)

Flip-chip interconnect roadmap
Outline

- Technology Background
- Physical Design Challenges/Solutions
- Concluding Remarks
## Multi-Domain Challenges & Opportunities

| System | • System-level HI modeling & simulation, heterogeneous device applications & computing  
• Power/performance/thermal/cost analysis for heterogeneous platforms  
• Architecture with HI components, cost evaluation & decision, hardware security & reliability |
|---|---|
| Physical | • 3D partitioning, floorplanning, placement, routing, post-layout optimization (RDL routing)  
• Package-/board-level routing, chip-package-board co-design (bump-aware design)  
• Cross-domain timing analysis/optimization, chip/board/system & 3D IC test, DFT connectivity |
| Electrical | • 3D power/signal integrity & EMI prevention (PTH), buried power rail, stacking P/G network  
• Stacking STA (cross dies) & electrostatic discharge (ESD), inter-die coupling, substrate RLC |
| Thermal | • Stacking interconnect/full-system thermal analysis & electromigration reliability  
• Joule heating, hotspot detection & handling, device cooling |
| Mechanical | • Warpage/delamination/stress-aware optimization  
• Metal migration simulation and optimization, fatigue reliability |
| Optical | • Optical routing, thermal-aware power device placement, electrical & optical co-design  
• System-based optical device analysis & optimization, laser power network, reliability |
3D System-level Partitioning

- Partition mixed-logic and memory into multiple dies with different technologies for PPA optimization
  - Device sizes & design rules change with different die assignment, **NOT** just min-cut partitioning!

- Must consider process technologies for multiple dies and corresponding interconnect/via/bump parameters for the overall cost optimization

System-level partitioning, planning, aggregation, and optimization

Source: Cadence

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Cross-physics-domain Floorplanning

- Integrating dies into an advanced package may suffer from severe electrical, thermal, and mechanical effects, e.g., stress, warpage, substrate noise, Joule heating, and delamination.
- A PTH (plating through hole) connecting a bump to a ball may induce severe EMI (electromagnetic interference) problems
  - Must meet constraints: larger pitch for EMI, constrained regions, etc.
- Floorplan PTH rooms (locations, aspect ratios, etc.) of holes for better bump-PTH-ball routing
Mechanical Issue: Warpage-aware Floorplanning

- Hsu, Chung, and Chang, “Transitive closure graph-based warpage-aware floorplanning for package designs,” ICCAD’22

- Mismatch in coefficients of thermal expansion between Si (die) & laminate substrate (interposer) causes thermo-mechanical stress and warpage

- Warpage modeling: Suhir’s theory; floorplanning: TCG; simulation: ANSYS & Moldex3D

\[
 w(x) = \frac{t \Delta \alpha \Delta T}{2\lambda D} \left( \frac{1}{2} x^2 - \frac{\cosh k x - 1}{k^2 \cosh k l} \right)
\]

- \( t \): thickness
- \( k, D, \lambda \): material related coefficients
- \( \Delta T \): the temperature difference between initial temperature and final temperature
- \( \Delta \alpha \): difference of coefficient of thermal expansion

Multi-die, Multi-technology Placement

- Dies integrated into a package could be fabricated with different technology nodes, so block (standard cell or macro) sizes are changed “dynamically” with die assignments.
  - Signals are connected by hybrid bonding terminals.
- Chicken-and-egg challenge: Block dimensions change with die assignments.
2023 ICCAD 3D F2F Placement Contest

- **Input**
  - Netlist (including macros and standard cells)
  - Cell libraries
  - Terminal cost

- **Objective:** minimize the scoring function
  \[ HPWL_{top} + HPWL_{bottom} + N_{term}C_{term} \]

  - Total Wirelength
  - Terminal Cost

- **Constraints**
  - Non-overlapping blocks
  - Spacing between terminals
  - Maximum utilization rates on each die

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2023 CAD Contest @ ICCAD
NTU: 1st Place

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Our Placement Framework

• Chen, et al., “Mixed-size 3D analytical placement with heterogeneous technology nodes,” DAC’24 (1st Place at the 2023 ICCAD CAD Contest).

Find the desired positions for each macro & standard cell using 3D analytical placement. Assign each component to its closest die, considering die utilization constraints. Remove macro overlaps using constraint graphs and integer linear programming. Insert terminals to current optimal positions. Simultaneously optimize the standard-cell & terminal positions using analytical placement. Legalize standard cells using Abacus & Tetris. Refine cell and terminal position further.
3D Analytical Placement

- Formulate an unconstrained optimization problem

\[
\min \ W(x, y) + \alpha Z(z) + \lambda N(x, y, z)
\]

Wirelength Terminal Cost Density

- Use our **Weighted-Average** model [Hsu, Chang, Balabanov, DAC-11, TCAD-13; US Patent, 2014] for wirelength optimization

\[
W(x, y) = \sum_{e \in E} \left( \frac{\sum_{v_i \in e} x_i \exp(x_i/\gamma)}{\sum_{v_i \in e} \exp(x_i/\gamma)} + \frac{\sum_{v_i \in e} x_i \exp(-x_i/\gamma)}{\sum_{v_i \in e} \exp(-x_i/\gamma)} \right) + \frac{\sum_{v_i \in e} y_i \exp(y_i/\gamma)}{\sum_{v_i \in e} \exp(y_i/\gamma)} + \frac{\sum_{v_i \in e} y_i \exp(-y_i/\gamma)}{\sum_{v_i \in e} \exp(-y_i/\gamma)}
\]

\[
\alpha Z(z) = \sum_{e \in E} (\alpha + w_e) \left( \frac{\sum_{v_i \in e} z_i \exp(z_i/\gamma)}{\sum_{v_i \in e} \exp(z_i/\gamma)} + \frac{\sum_{v_i \in e} z_i \exp(-z_i/\gamma)}{\sum_{v_i \in e} \exp(-z_i/\gamma)} \right)
\]

\[
\alpha: \text{Via cost} \quad w_e: \text{Net weight}
\]

- Apply ePlace-3D for density control [Lu et al., ISPD-16]

\[
N(x, y, z) = \frac{1}{2} \sum_{v_i \in V} q_i \psi_i(x, y, z)
\]

\[
\xi(x, y, z) = \left( -\frac{\partial \psi}{\partial x}, -\frac{\partial \psi}{\partial y}, -\frac{\partial \psi}{\partial z} \right)
\]

\[
q_i: \text{Volume of cell } i \quad \psi: \text{Potential function} \quad \xi: \text{Electric field}
\]

- Optimize the objective function using gradient descent
- Increase \(\lambda\) gradually to reduce the density to find the desired macros & standard cell positions \((x, y, z)\)
Die Assignment

- Relax the discrete assignment variable & use a sigmoid function to achieve smooth shape transition

\[ f(z) = s_1 + \frac{s_2 - s_1}{1 + \exp\left(\frac{-k}{r_2 - r_1}(z - \frac{r_2 + r_1}{2})\right)} \]

- \( z \): Position on z-axis
- \( s_1 \): Value at bottom die
- \( s_2 \): Value at top die
- \( r_1 \): Bottom die z-coordinate
- \( r_2 \): Top die z-coordinate
- \( k \): User defined parameter

- Partition the network using low-pin nets

Total HPWL = 59

Total HPWL = 29
Demo: 3D Mixed-Size Global Placement

- Benchmark: Case4
  - #macros: 32
  - #standard cells: 740,211
  - #nets: 758,860
Final Placement Result

- Benchmark: Case4
  - #macros: 32; #standard cells: 740,211; #nets: 758,860

- Results
  - Top-die wirelength: 864,717,801
  - Bottom-die wirelength: 181,388,384
  - Terminal cost: 160,993 × 10 = 1,609,930
Modern packages require high-performance connections among chiplets through multi-layer redistribution layer (RDL) interposers or substrate (e.g., CoWoS, InFO).

- Use RDLs to connect I/O pads (chip) to bump pads (package) to achieve better quality (e.g., more areas for I/Os, higher performance interconnections, better signal integrity and robustness)

The rising complexity requires any-obtuse-angle routing to consider complex design rules

- Consider complex via stacking rules, irregular vias, inline/staggered bumps, max. metal density for reliability, differential pairs, shielding, etc.

Source: TSMC (w. revision)
Flip-Chip RDL Routing

- Flip-chip routing routes I/O pads to bump pads on RDL
- Two types of packages: (a) peripheral-I/O; (b) area-I/O

![Diagram showing flip-chip and peripheral/area I/O packages with labels for various components like I/O pads, bump pads, and RDL.]
Free- vs. Pre-assignment Routing

• Free-assignment routing
  – Each bump pad can be connected to any I/O pad
  – Router can assign each I/O pad to a bump pad

• Pre-assignment routing
  – Connections between I/O and bump pads are predefined
  – Router must connect a bump pad to its pre-assigned I/O pad
RDL Routing Classification & Techniques

Peripheral I/O
- Peripheral I/O, free-assignment
  - Fang et al., ICCAD’05 (TCAD’07): Flow
  - Liu et al., DAC’10: VD+Flow
  - more
- Peripheral I/O, pre-assignment
  - Fang et al., DAC’07 (TCAD’09): ILP
  - Lee et al., ICCAD’09 (TCAD’12): DP
  - more
- Peripheral-I/O, unified FA/PA
  - Lin et al., ICCAD’16: DP+Flow

Area I/O
- Area I/O, free-assignment
  - Fang & Chang, ICCAD’08 (TCAD’09): Flow
  - Yan & Chen, ASPDAC’09: VD
  - more
- Area I/O, pre-assignment
  - Chang et al., ICCAD’19: VD
- Area-I/O, unified FA/PA
  - Fang et al., DAC’09 (TCAD’10): VD+Flow
  - Wen et al., DAC’20: DP
  - Cai et al, DAC’21: VD
  - more

Flow: Network-flow
VD: Voronoi Diagram
ILP: Integer linear programming
DP: Dynamic Programming

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Network Flow Formulation

- **Network flow problem**: Given a flow network $G$ with source $s$ & sink $t$, find a maximum flow from $s$ to $t$.
- Network flow formulation is useful for modeling resource assignment (supply-demand) problems.
- **Key limitation**: Control only the total flow, but not the individual flow at a specific node/edge (NP-complete multi-commodity flow problem)

$$f(s, v_2) = 8, c(s, v_2) = 13,$$
$$f(v_3, v_2) = 4, |f| = 19$$
Network Flow for Free-assignment Routing

- Most existing works are based on **Minimum-Cost Maximum-Flow (MCMF)** [Fang et al., ICCAD’05 & more]

- Divide a chip into four regions & route region by region
  - I/O pad ➞ source node
  - Bump pad ➞ sink node
  - Wire ➞ unit flow
  - Max-flow ➞ highest routability
  - Min-cost ➞ shortest wirelength
Peripheral I/O, Free-assignment Routing Result

Circuit: fs900
Dynamic Programming (DP) for Pre-assignment Routing

- Utilize the regularity of the flip-chip structure to achieve better solutions [Lee et al., ICCAD’09, TCAD’12]

- DP works best on linearly ordered objects that cannot be rearranged!!
  - Examples: Characters in a string, matrices in a chain, left-to-right order of leaves in a search tree, points on a line/polygon/circle boundary

- Apply DP for pre-assignment routing
Why are Taiwanese so friendly to Japanese?

Dr. Kazutoshi Wakabayashi (NEC)  Longest Common Subsequence Similarity: 50%+!!  Yao-Wen Chang (NTU)

"Da Vinci Code" between Japan and Taiwan
Detours Minimization by DP

- DP to minimize detours for pre-assignment routing
- Longest common subsequence (LCS) computation

(a) seq.1 = <1,2,3>
(b) seq.2 = <3,1,2>
(b) Common subseq = <3>
(c) LCS = <1,2>

- Maximum planar subset of chords (MPSC) computation

(d) chord set: {3,4,5}
(e) subset: {3}
(f) MPSC = {4,5}
Pre-assignment Ring-by-Ring Routing

• Identify feasible sequences for I/O pads and apply LCS
• Decompose chip into rings of bump pads and route from inner rings to outer rings
• Keep applying MPSC between two adjacent rings (red ring & blue ring)

Achieve over 100X speedups than ILP with better quality!!
Demo: Circuit fc2624
Any-obtuse-angle Routing

- Need any-obtuse-angle routing to maximize flexibility
- Plan teardrop angles to maximize the routability
  - Local teardrop angles could affect far-away connections
Any-obtuse-angle Package Routing

- Chung et al., “Any-Angle Routing for Redistribution Layers in 2.5D IC Packages,” DAC’23

- 1st any-angle router with multiple RDLs
- Apply Delaunay triangulation for tile partitioning
- Model intra- and inter-tile capacity to generate routing guides
- Apply dynamic programming-based access point adjustment to route multiple nets simultaneously
- Achieve the best published routability

Any-angle routing can fix red spacing violation
General Package Routing Considerations

- Differential pairs (for phase matching), plating-through-hole (PTH) placement with shielding, length matching for skew, matched escape orders for bus routing, constrained regions, inline/staggered bump structures, bump breakout, etc.
- More: irregular vias, max. metal density for reliability, etc.
PCB Placement and Routing

- Place irregular-shaped 3D components
- Route signal/PG wires of different widths
- Considerations: component orientations, diverse wire widths, *dynamic* spacing rules, power loop topologies, heat sink insertion, restricted areas, etc.
Chip-Package-Board Co-Design

Without co-design

With co-design

John F. Park, ICCAD’10

Without I/O optimization

With I/O optimization

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Chip-Package-Board Co-Design

- Lee and Chang, “A chip-package-board co-design methodology,” DAC’12 (Fang, Ho, and Chang, ICCAD’08)
- Route a signal from an I/O buffer, to a flip-chip bump (RDL routing), and finally at a BGA ball (package routing), ready for PCB connection
- **Board-driven Λ-shaped codesign flow:** Inverse escape routing (PCB), ball-bump mapping (package), package-aware I/O placement (chip), bump reassignment & RDL rerouting (package), escape rerouting (PCB)
Co-packaged Optics (CPO)

- TSMC has announced to integrate silicon photonics components into its advanced package by 2025

Source: TSMC (ISSCC’24)
Lu, Yu, Chang, “On-chip optical routing with provably good algorithms for path clustering and assignment,” TCAD, 2022

- Allows a connection in any direction & signal crossings w. higher bandwidth, lower power, and faster speed
- Transmit signals on shared waveguides
  - Need signal clustering to better use WDM (Wavelength Division Multiplexing)
- Minimize transmission loss & wavelength power
Optical-electrical Codesign

- Lu, Chen, Hsu, and Chang, “Thermal-aware optical-electrical routing codesign for on-chip signal communications,” DAC’22

- Generate global optical waveguides to optimize thermal impact, routing congestion, and wirelength

Thermal-aware codesign for power, wirelength, congestion optimization!
AI for EDA & EDA for AI

- AI technologies reshape EDA
  - Enhance EDA techniques with machine learning

- EDA helps AI system designs
  - Optimize the design of CNN kernel structure

EDA for AI (chip design)
kernel structure of a CNN accelerator

Placement by “leading” industry tool

Placement by NTU/MAXEDA tool
(acquired by Synopsys in 2023)

DAC’21

DAC’22: Macro Placement by MTK/MAXEDA/NTU

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Outline

Technology Background

Physical Design Challenges/Solutions

Concluding Remarks
Modern Design/EDA Challenges

- Complexity
- Multi-objectives
- Heterogeneity
- Technology
Example 3D Placement Challenges

- **High complexity**
  - 100M objects + nets

- **Cross-physics constraints**
  - Multi-die technologies, warpage, thermal, etc.

- **Mixed-cell-height, mixed-size placement**
  - 100K big macros with 100M small cells of multiple cell heights

- **Emerging technologies**
  - AI, HI (bonding/integration TSV), etc.

Complexity
Multi-objectives
Heterogeneity
Technology
Culture Clash vs. Collaborative Mindset

chip to package
Large-scale, regular, homogeneous components w. uniform design rules

board to package
Small-scale, irregular, heterogeneous components w. complex design rules

Chip Designers (Men) Are from Mars, Board Designers (Women) Are from Venus…
Conclusions

- Multiple approaches to achieving the power/performance/area (PPA) holy grail
- Multiple complementary options to achieve the HI targets
- Need an ecosystem to achieve the ultimate PPA goal, where multi-physics domains need to be considered and EDA is essential
- Technology challenges will not limit our progress because imagination can bring us to the endless frontier!!

The human spirit must prevail over technology.

Source: Lee Smolin

Albert Einstein
Thank You!!