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*Silicon to Software*<sup>™</sup>

# DSO.ai – A distributed system to optimize design flows

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# Industry Trends and Challenges

Design talent is on track to face a shortfall of 35% workers by 2030



**89,000**  
Demand for US-based design workers in 2030

Demand for workers is expected to rise by ~50% ...



**66,000**  
Supply of US-based design workers in 2030

... While supply will grow by less than 1% annually ...



Source: BCG analysis

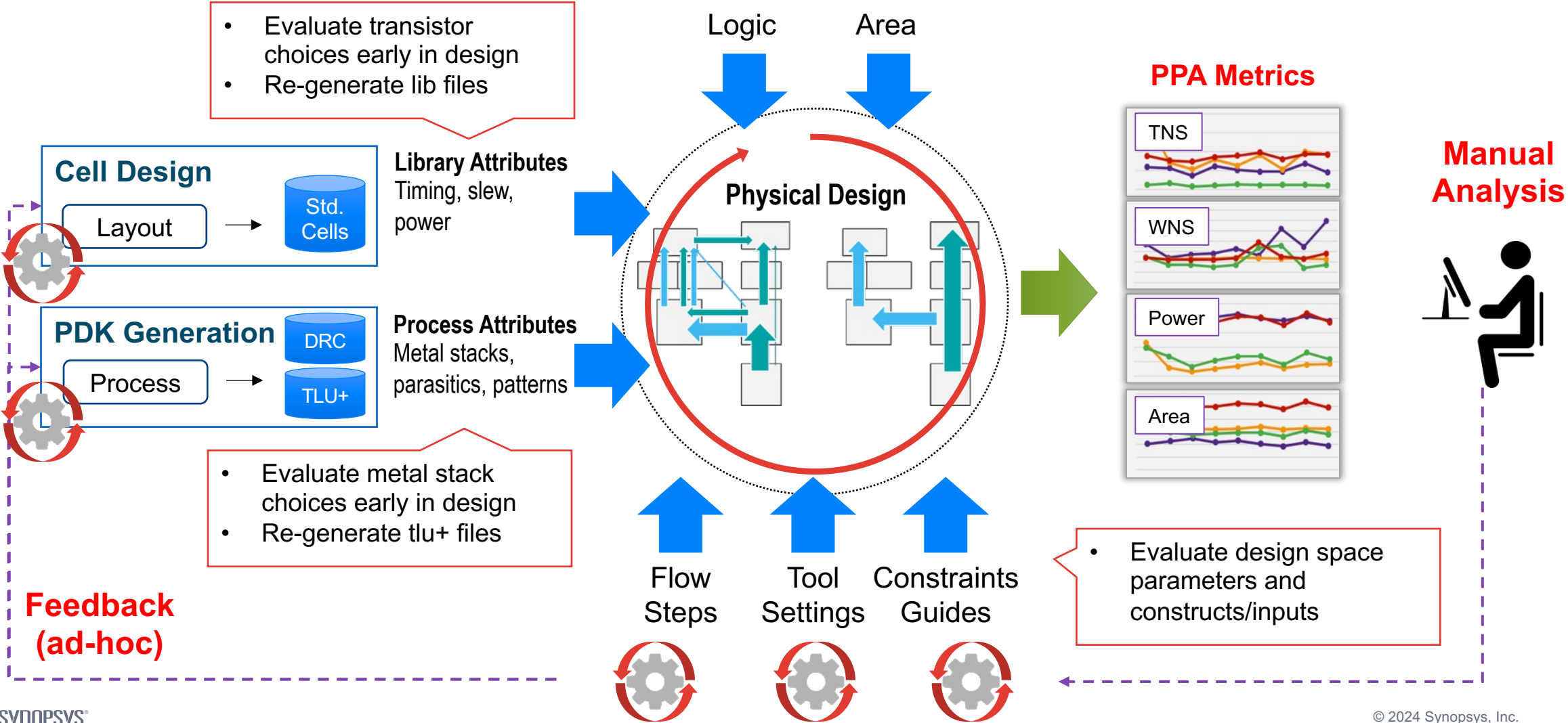
**23,000**  
Shortage of design workers in 2030, growing by 3,000 per year

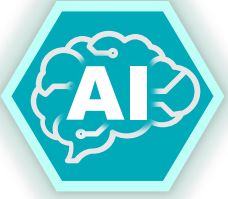
... Meaning that demand for design workers will **exceed supply** by nearly 35% in 2030

**Demands Significant Increase in Productivity**

# DSO.ai: Addressing the Broader Design-Technology Space

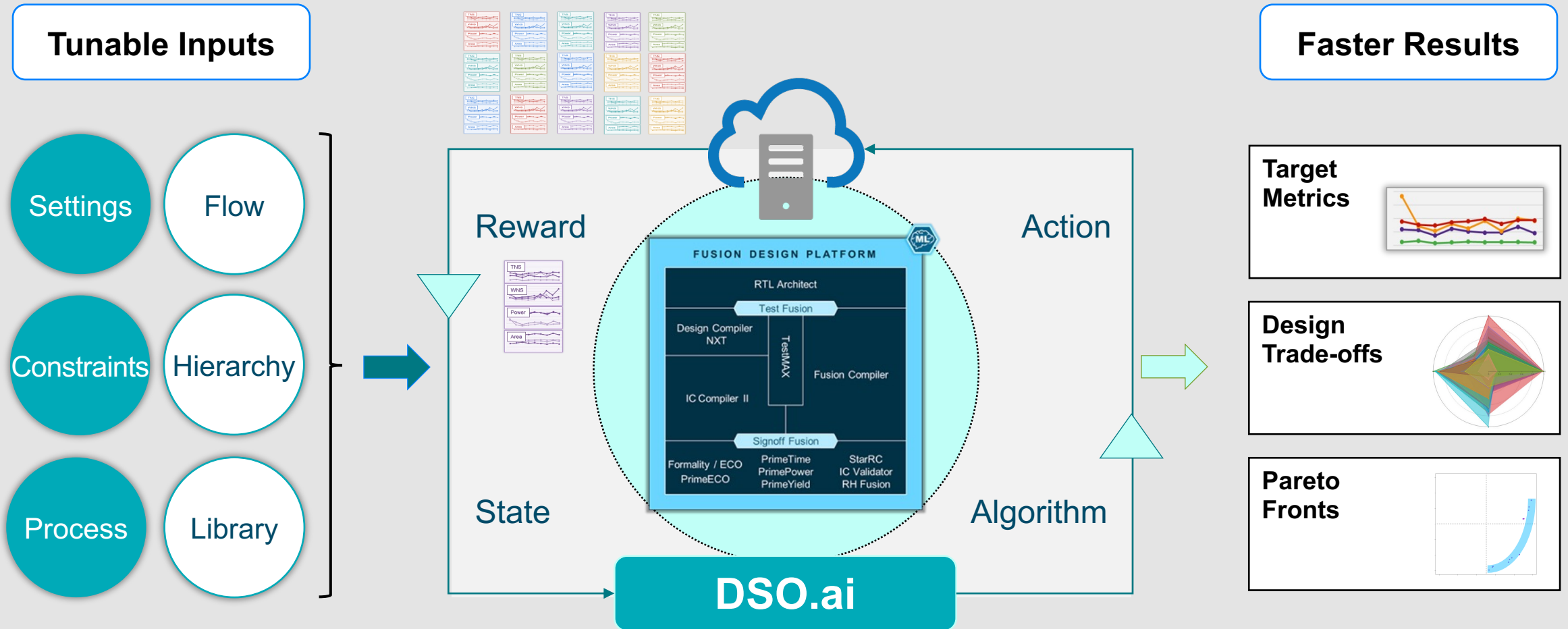
Separately optimized silos and complex heuristics





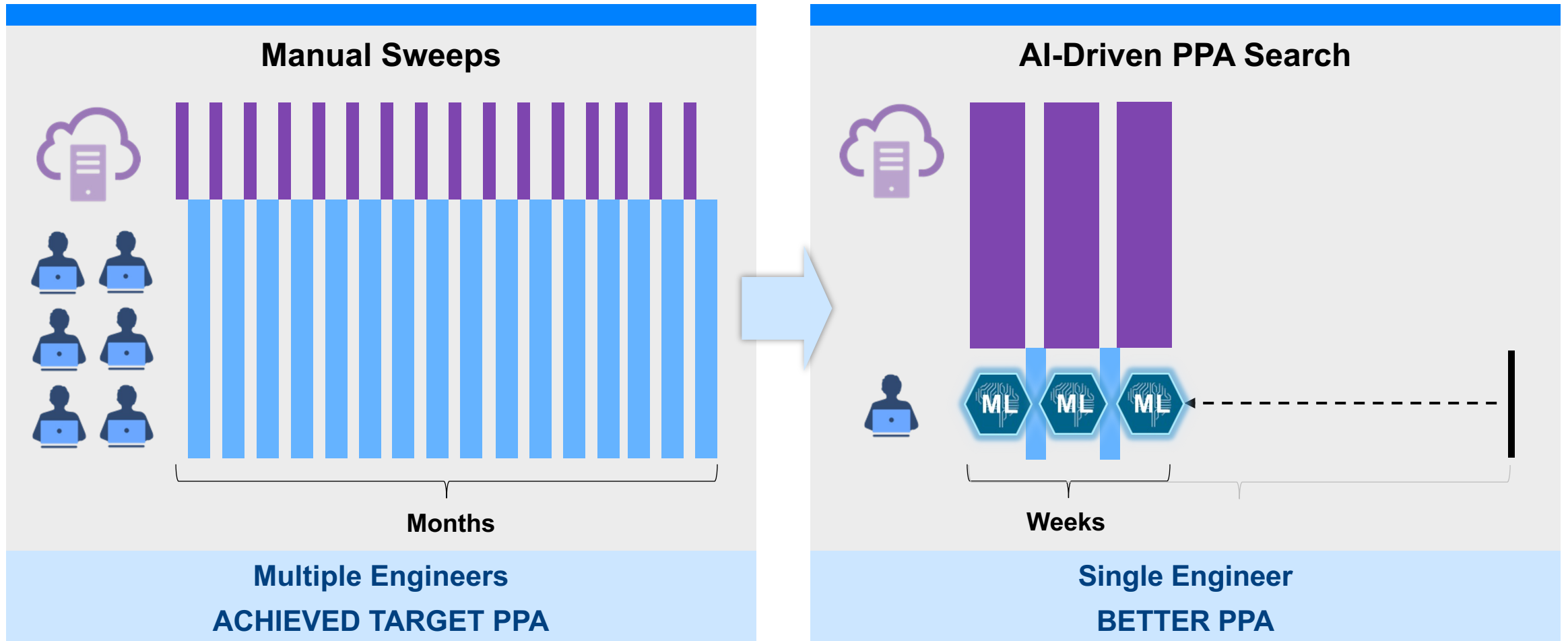
# DSO.ai – Design Space Optimization Loop

Uses reinforcement-learning to navigate the design-technology solution space



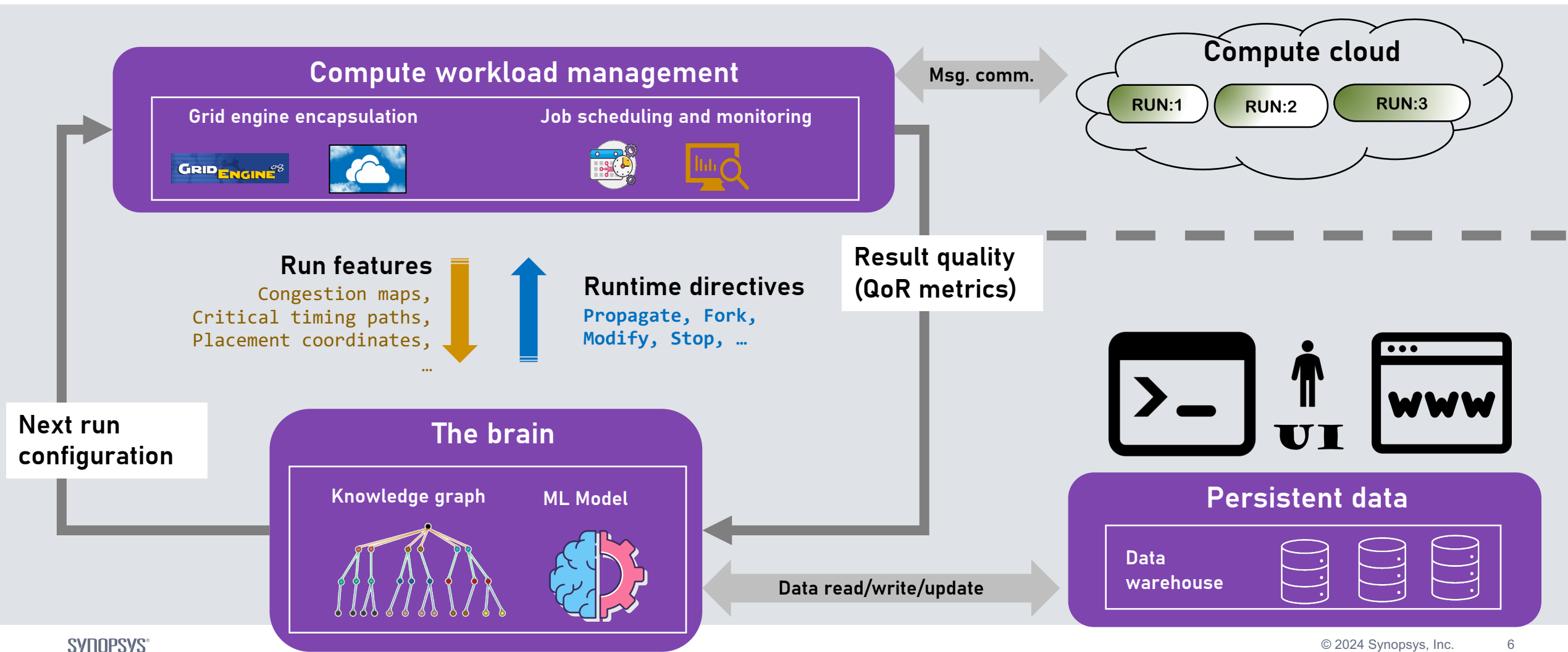
# AI-Driven Design Space Optimization (DSO)

10X productivity compared to traditional, manual exploration



# Architecture

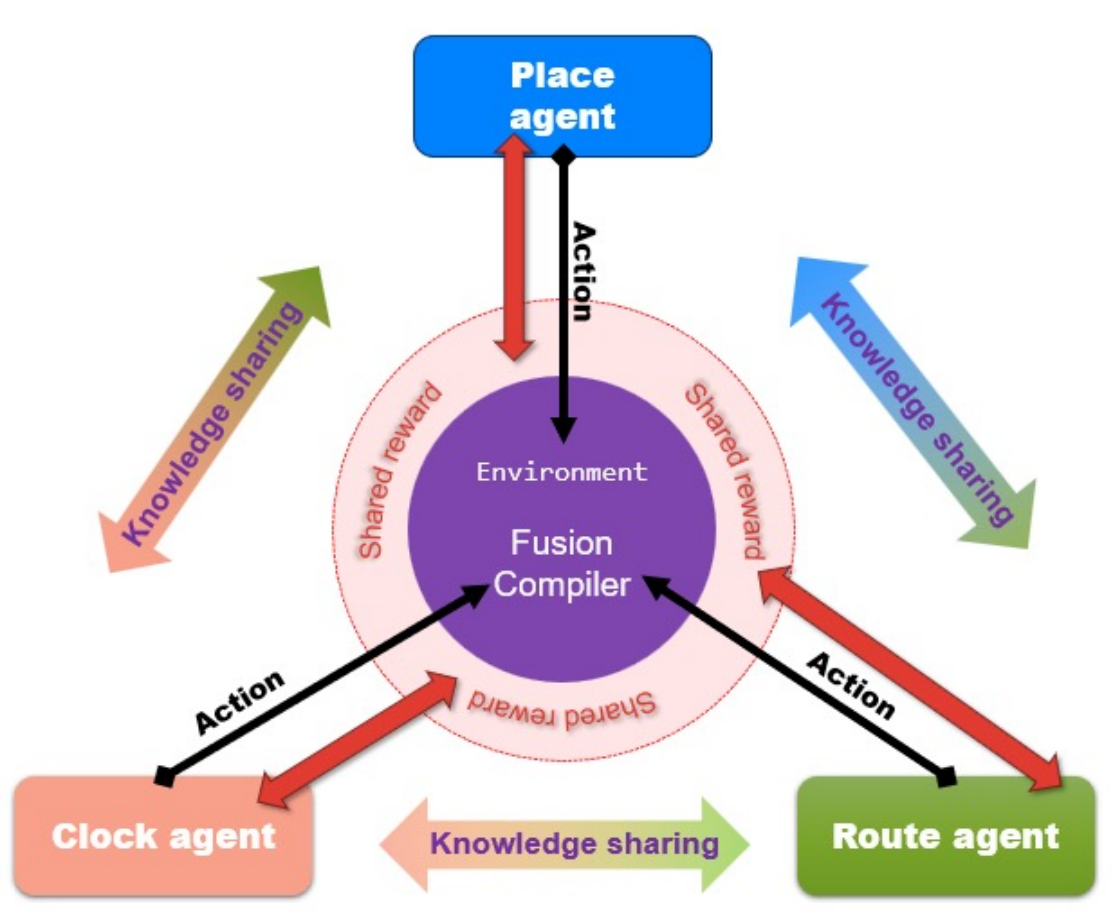
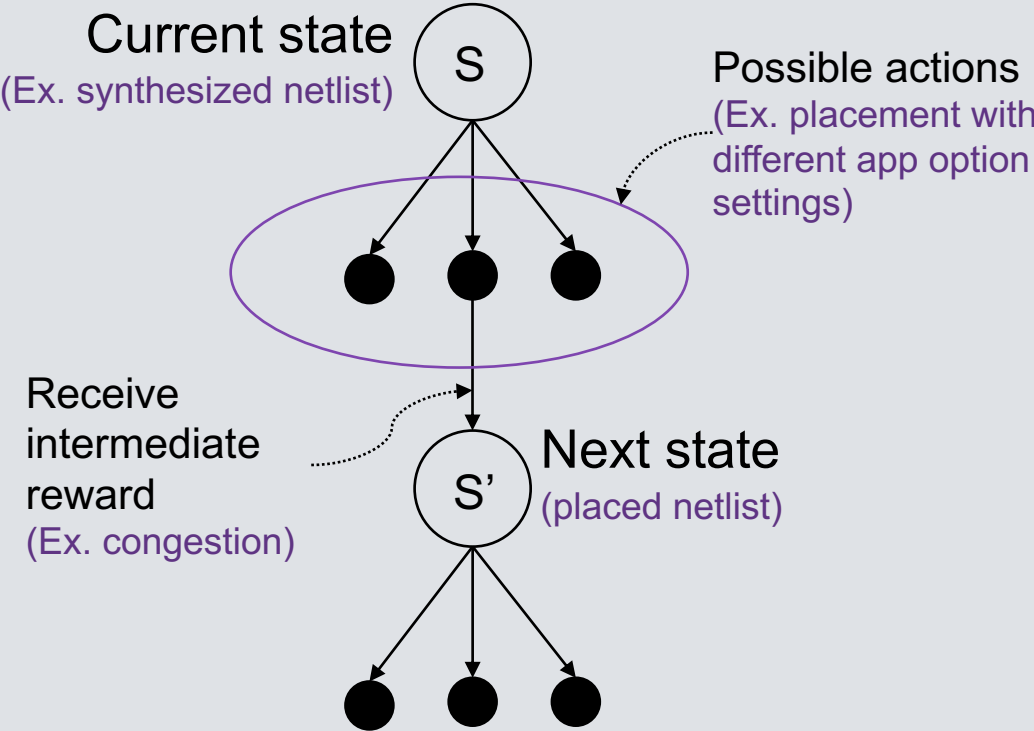
A scalable distributed system with continuous learning



# Reinforcement learning

Specialized RL agents operating at the flow level

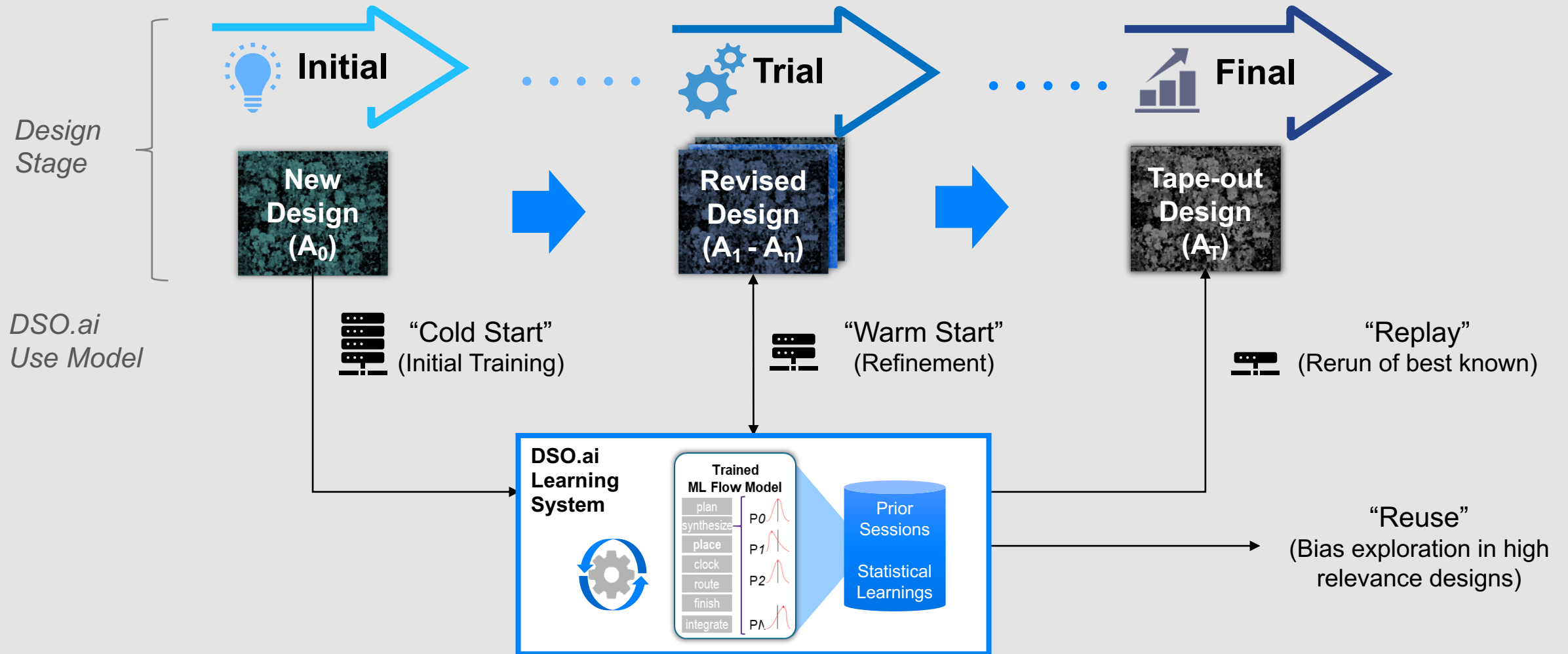
## Sequential decision making



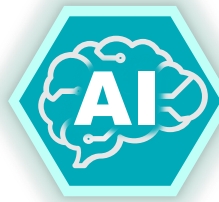


# Scaling through Systematic Learning and Reuse

ML models continuously train and accelerate convergence throughout the design cycle







# Customers Share Success with Production Deployment

Results from AI Track, SV SNUG 2023 Proceedings, customer engagements

**Power Opt.**  
5nm  
3% Total Power  
HPC

### DSO.ai at Microsoft – Power - Block 1

ADES_power	R2R_TNS	dso_metric_total_power	UTILIZATION	BLOCK_SAVE
0.75803	-1.2	0.97	0.98	ADES_power:0 dso_metric_total_power:0
0.76060	-1.3	0.97	0.98	ADES_power:1 dso_metric_total_power:1
0.76136	-0.97	0.98	0.99	ADES_power:2 dso_metric_total_power:2
0.77674	-0.8	0.98	1	R2R_TNS:0 dso_metric_leakage_power:0
0.99808	-1.10	1	1	R2R_TNS:2 dso_metric_leakage_power:0
1.00000	-1	1	1	R2R_TNS:1 dso_metric_leakage_power:1

Multiple choices with various tradeoffs

Composite Score (lower is better)

Non-DSO baseline (Designer database replayed in DSO)

- 3% better total power improvement with DSO power toolbox as measured in signoff power analysis
- Replayable for future iterations of the block via warm start

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**Power Opt.**  
Adv. FinFET  
5% Total Power  
XEON

### Results – DSO.ai vs PrimeTimeECO

Power Saving Strategy	P-Lkg	P-Dyn	P-Tot	Tot mW Saving
Baseline	-	-	-	-
Baseline + PT ECO	9%	0%	2%	2.9
Baseline + DSO	18%	0%	5%	6.4
Baseline + DSO + PT ECO	19%	0%	5%	6.7

\* All power measured at sign-off

Key Takeaway

- Run with DSO enabled shows 2x total power saving as compared to PT-ECO
- Concurrent timing and power optimization in early stage led to better optimized design
- DSO in compile stage allowed sequential cells to be down-sized and placed before they were fixed in clock stage

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**PPA Opt.**  
7nm  
3X productivity  
A510

### DSO.ai enabling PPA exploration

DSO/CLOUD Infrastructure

FC License up to 100

Search space  $10^{25}$

100% of PPA exploration performed with DSO.ai

180 Permuton number

2.7K FC runs

3x Productivity Gain

PPA exploration

\* SNPS/ST press release

Performance ✓ Reached targeted frequency

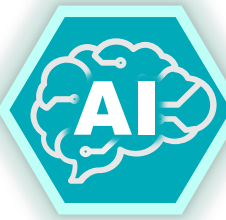
Power ✓ Best power compromise (Dynamic/Leakage)

Area ✓ Keep same floorplan shape dimension

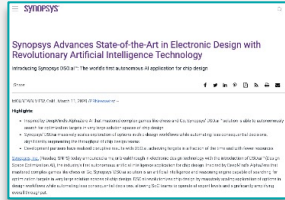
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<b>Automotive</b> <b>ANANKE CORE</b> FC+DSO.ai 14LPC Competitive Win <b>2x</b> Faster TAT <b>50%</b> Lesser Compute	<b>Automotive</b> <b>A78</b> FC+DSO.ai 5nm <b>9x</b> Less TNS <b>9x</b> Less DRC <b>7%</b> Lower Power	<b>Hunter-ELP</b> FC+DSO.ai <5nm <b>22%</b> Less TNS <b>3.3%</b> Higher Fmax
<b>Automotive</b> <b>HERCULES-AE CPU</b> FC+DSO.ai 5LPE <b>8%</b> Better Leakage <b>5%</b> Better Dynamic	<b>Foundry</b> <b>A72</b> FC+DSO.ai 4nm <b>HPC</b> Reference Enablement <b>6.5%</b> Higher Fmax	<b>Foundry</b> <b>A72-DS</b> FC+DSO.ai N3E <b>15%</b> Lower Leakage <b>13%</b> Higher Fmax

# Synopsys.ai – Leading Era of AI-driven Chip Design



2020



Synopsys introduces DSO.ai, world's first AI application for chip design

DSO.ai named **Innovative Product of the Year** by EETimes



2021

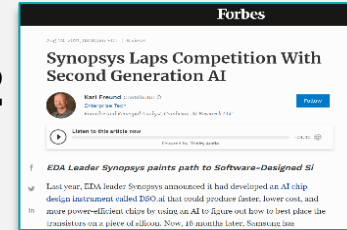


World productivity record: **10 blocks -9% total pwr ONE engineer**

Wired: World's first **AI-designed chip design**

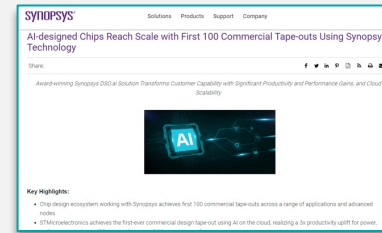


2022

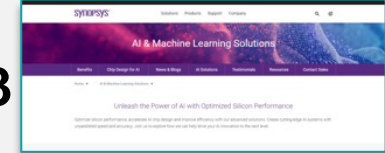


Record adoption: **9 of Semi Top-10 100% Better Results**

AI-designed Chips cross **400 Commercial Tape-outs** with DSO.ai

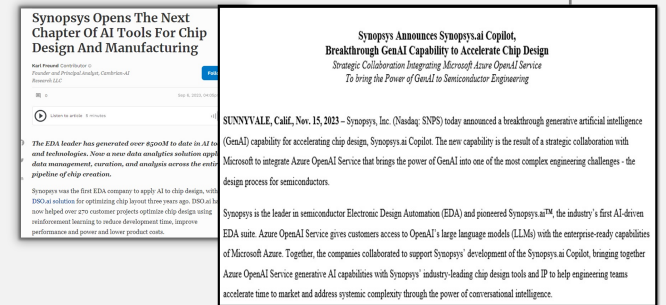


2023



Synopsys.ai **Industry's first AI driven EDA suite** – Design, test, verification, manufacturing

Synopsys.ai expansion to AI driven **Data Analytics & Generative AI** capabilities



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**THANK YOU**