

The background of the slide is a futuristic, dark blue and black digital environment. It features a perspective view of a hallway or data center aisle with glowing blue lines and patterns. A large, glowing 'AI' logo is positioned in the center-right, with circuit-like patterns extending from it. The overall aesthetic is high-tech and data-driven.

AI for EDA/Physical Design

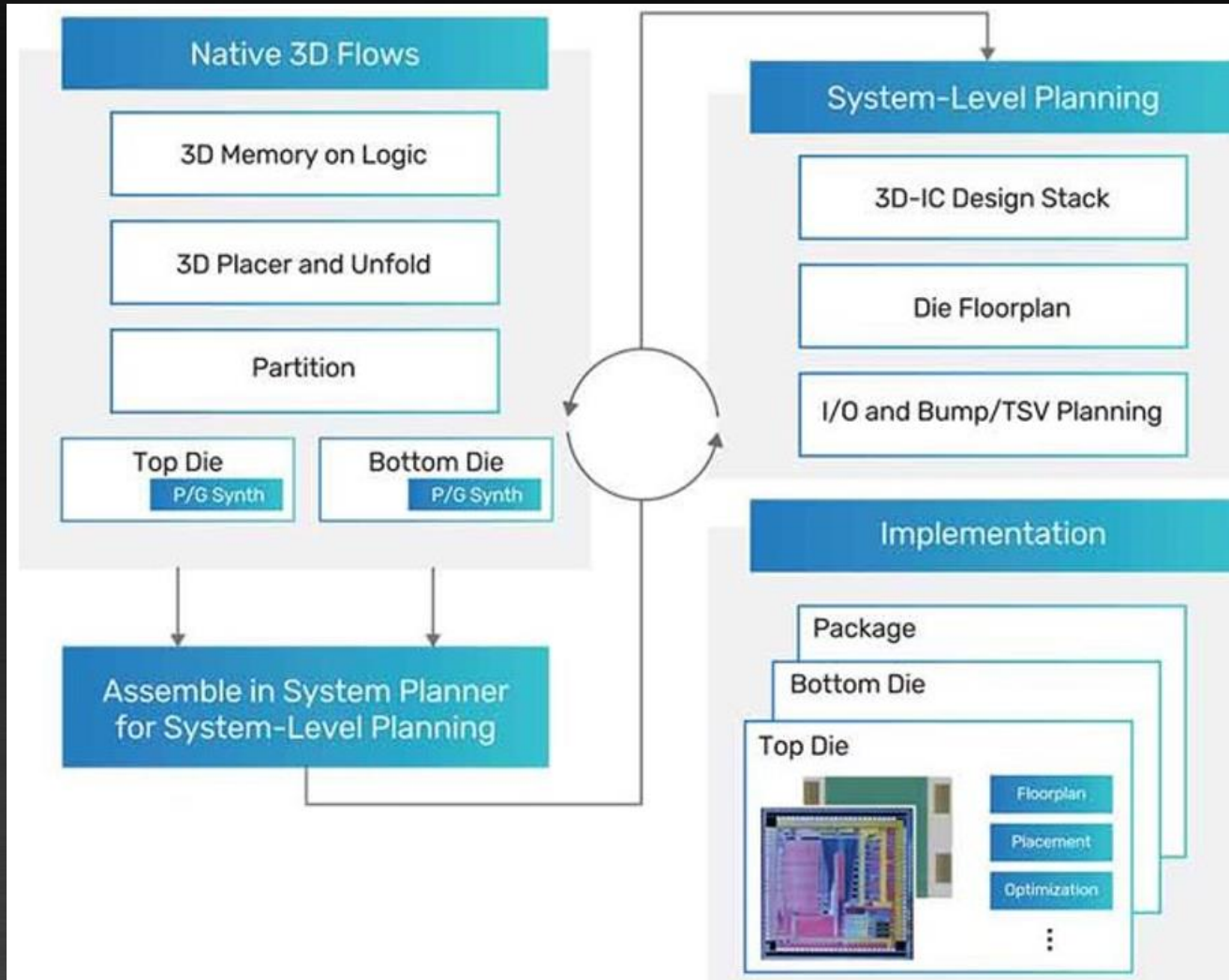
Driving the AI Revolution: The Crucial Role of 3D-IC

Erick Chao, Cadence Design Systems, Inc.

Mar/13/2024

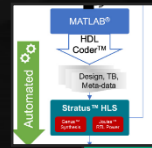
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AI-Driven 3D-IC Solution – Our Focus is to Eliminate the Iteration



3D-IC System Planning and Optimization

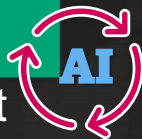
An AI Platform that can manage/connect all of stages



Architect In C

- Architect Optimization in C
- From system spec to RTL
- Architectural exploration and optimization
- AI-inspired technology, eliminates iterations

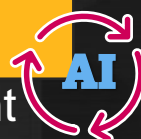
IP Development



2D Architect in RTL

- 2D Architect Optimization in RTL
- Automated flow to handle multiple RTL sources
- Explore RTL architect . restructuring, regrouping solution
- Early predict PPAC

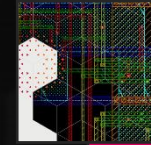
2D RTL Development



3D Architect in RTL

- 3D Architect Optimization in RTL
- Transform conceptual spec into 3D design
- Smart trade-off decision by AI
- Multi-objective to concurrently optimize bump, design partitioning, floorplanning with IR/Thermal driven

3D RTL Development



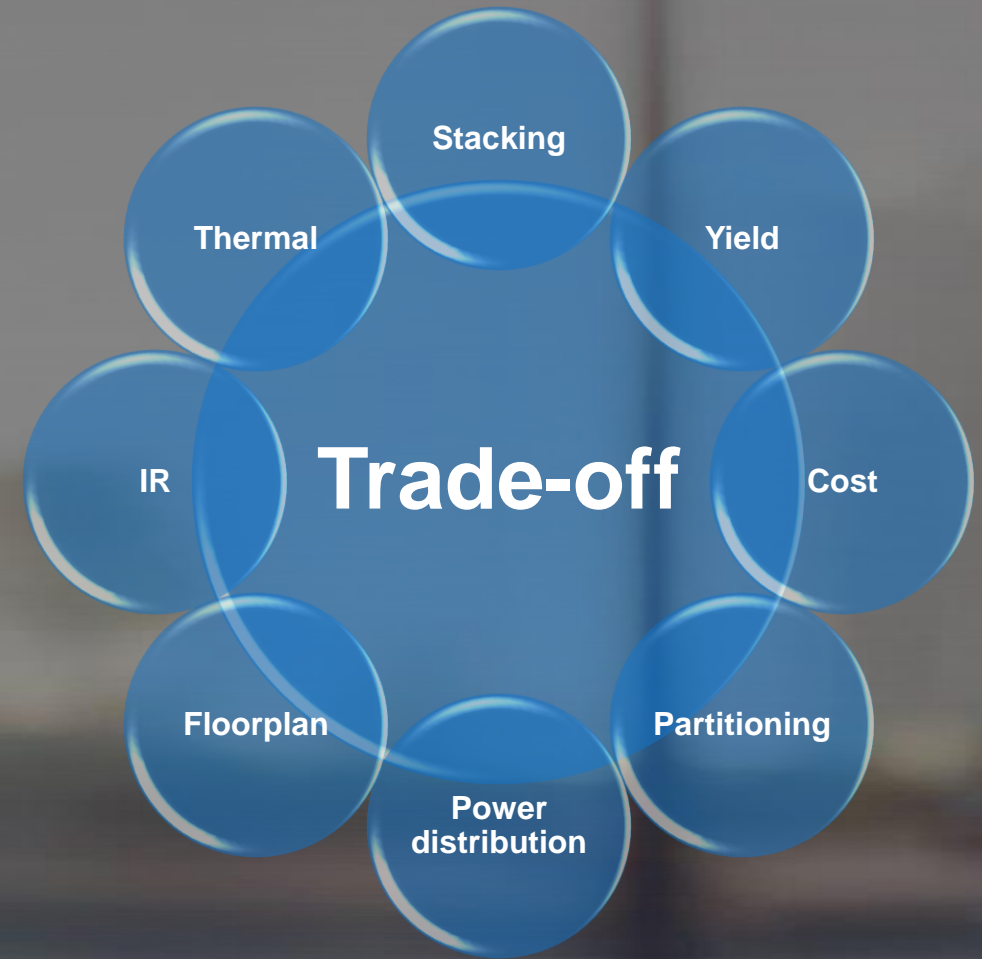
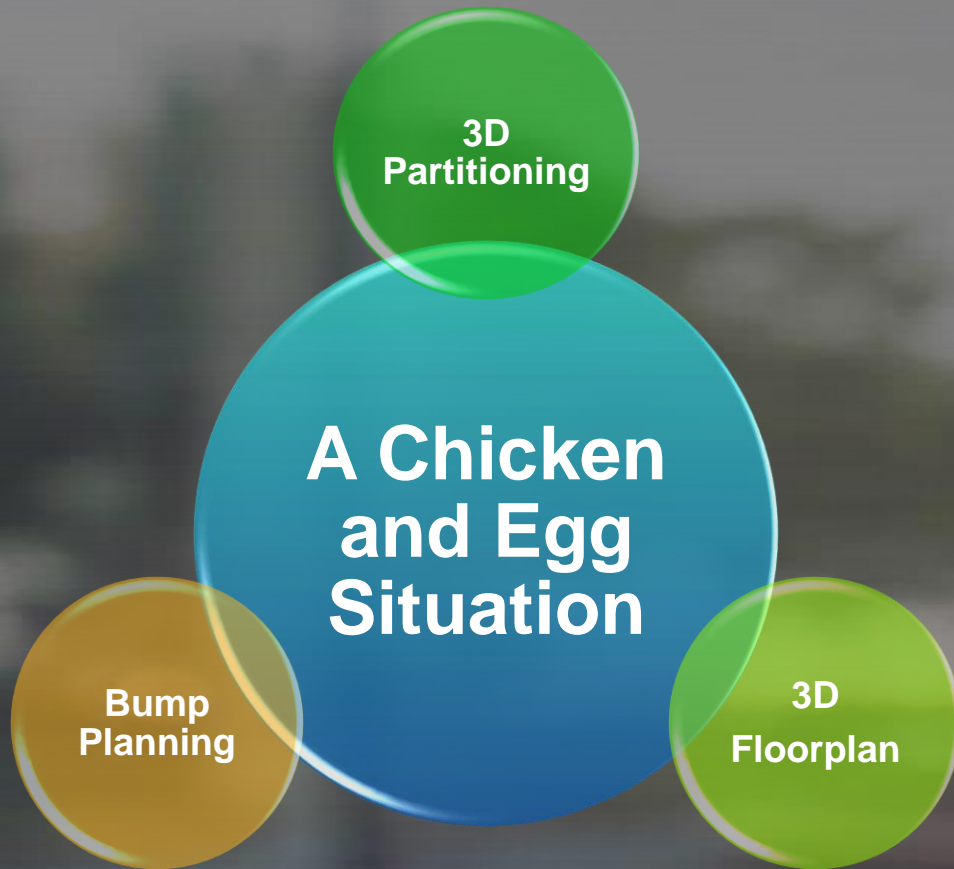
Chiplet implementation and Signoff

- AI-Inspired Hierarchy Flow
- AI-driven PPA optimization
- Generative-AI link with bigdata platform
- Cockpit for Multi-run visualization and dashboard

R2G Full Flow Development



Challenges of 3D-IC in Design and Flow Methodology



Parameters Need to Co-optimize in 3D Silicon Stacking

Stacking

Partitioning

Floorplan

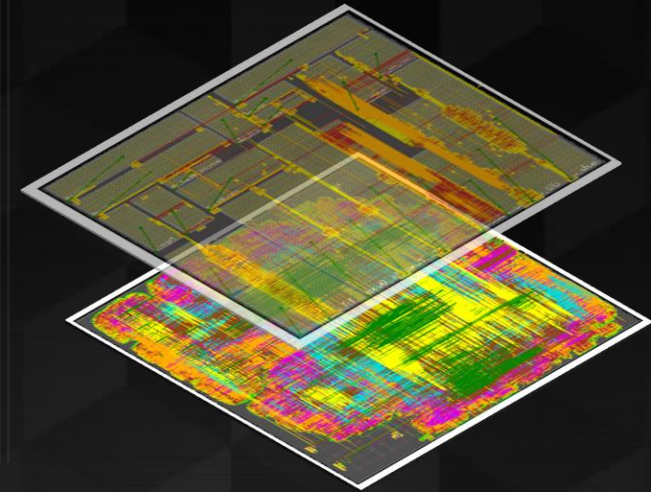
I/O, P/G Bump/TSV
Planning

Thermal

Power IR/EM



3D Silicon Stacking

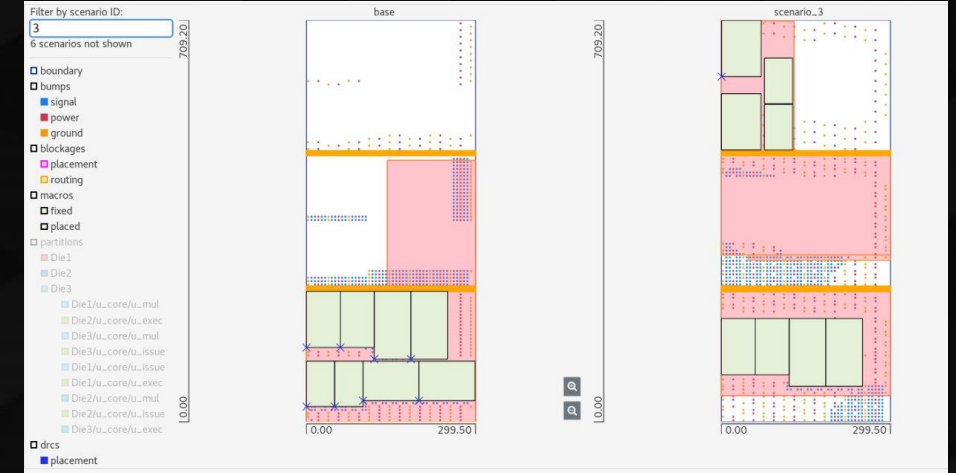


Example of Generated 3D-IC Architect Planning

3D-IC architect planning by AI



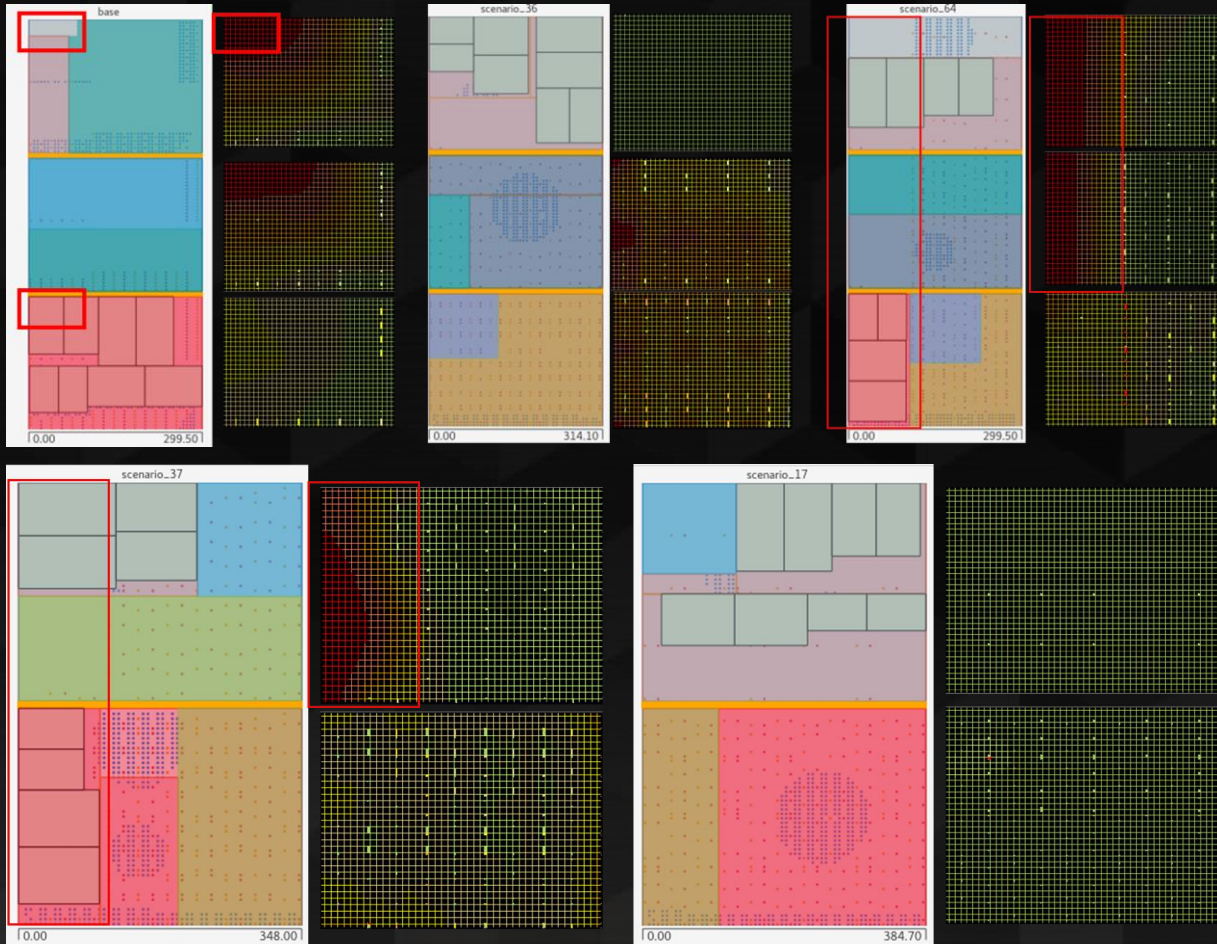
Bump planned and aware the macro placement



Multi-objective and trade-off decision by AI

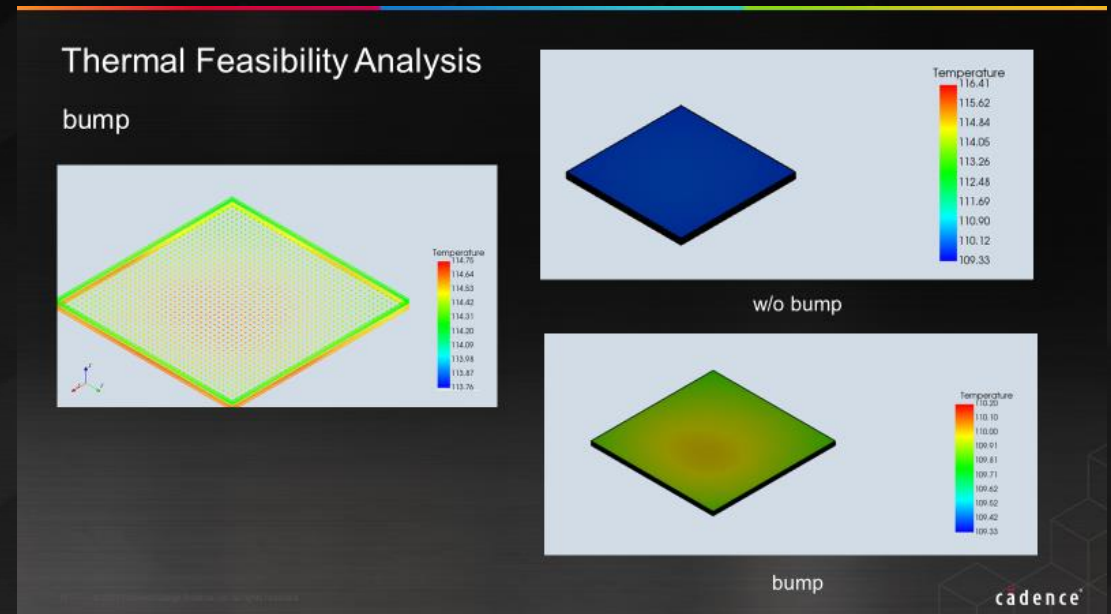
	2D wirelength	Z wirelength	Target density	Macro-on-Logic	TSV utilization	Bump floating	Bump violating
base	194820	7573.93	0.41	1.11	0.43	0.04	0.69
scenario_35	223636	7021.04	0.43	0	0.2	0	0.79
scenario_28	215772	5252.55	0.37	1.01	0.33	0.03	0.58
scenario_29	345552	5047.77	0.34	0.58	0.29	0.04	0.72

IR and Thermal Trade-Off Considering



- Bump connectivity impacts to thermal analysis
- Building the bump connectivity is important to successful early architect planning

Transform IR/Thermal into costing component to enable the learning of AI from the end-result



Summary

- Make design cycle collaboration efficiency and short TAT
- Early planning to reduce risk
- Comprehensive consideration to make immediate trade-off decision
- Enlarged productivity and performance optimization

The Cadence logo is centered on a dark background with a repeating pattern of light gray cubes. The word "cadence" is written in a white, lowercase, sans-serif font. A small red horizontal bar is positioned above the letter 'a'. A registered trademark symbol (®) is located to the upper right of the letter 'e'.

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