Enabling System Design in 3D Integration: Technologies and Methodologies

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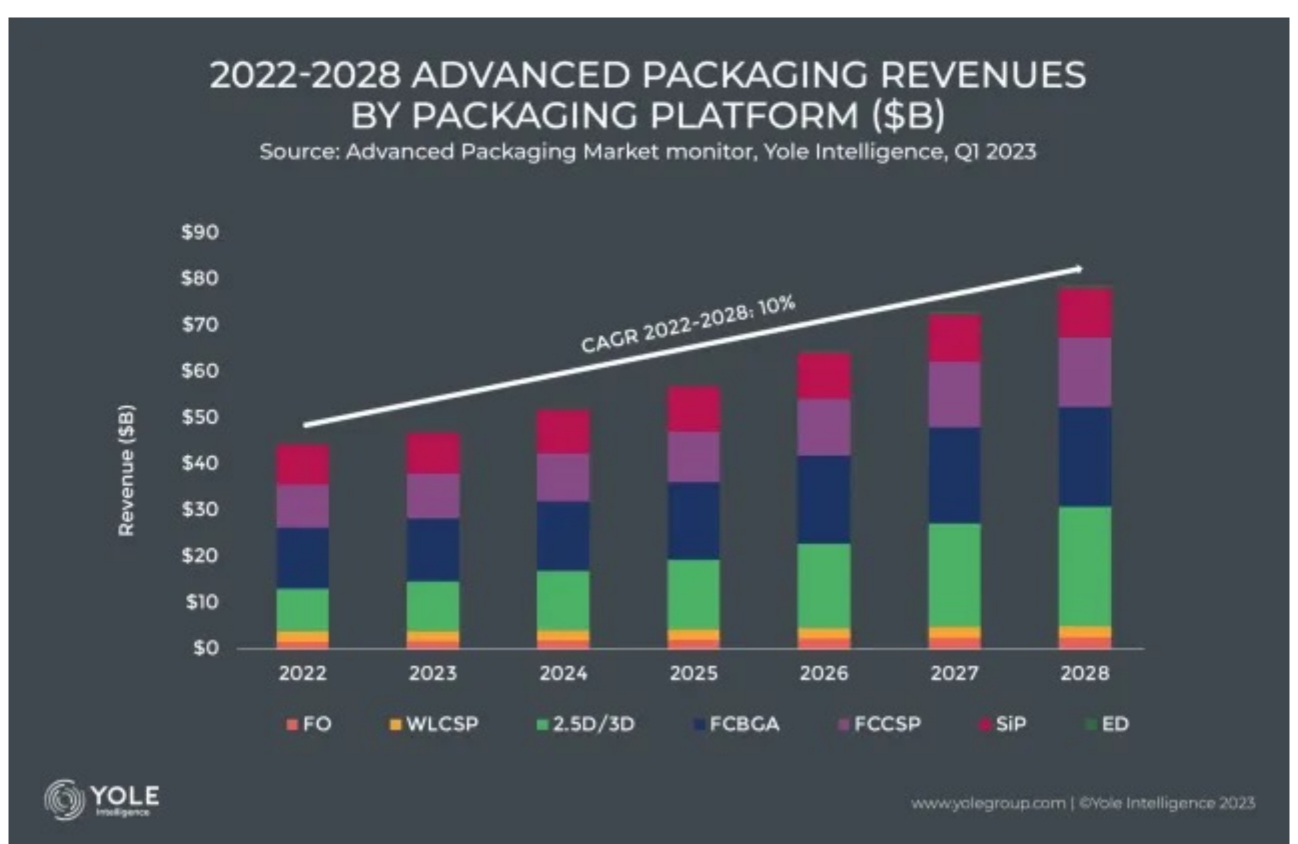
Advanced Packaging Trending



- Why advanced packaging?
  - M-chip production cost increase; disaggregating design rewarding; high-NA EUV

Source: Yole and EETimes: Understanding the Big Spend on Advanced Packaging Facilities

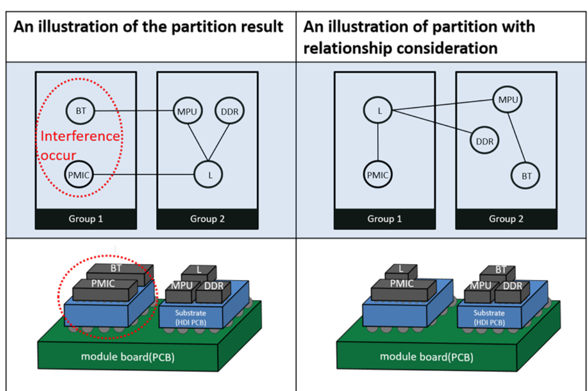
Outline

- Technology evolution in packaging manufacturing
- Methodologies in advanced packaging realization
- Chiplet the savior?
- Final remarks

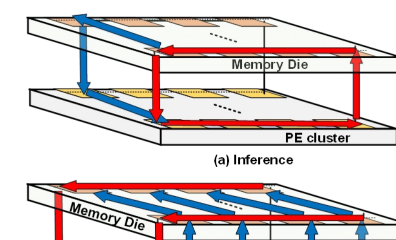
Previously on the Last Episode

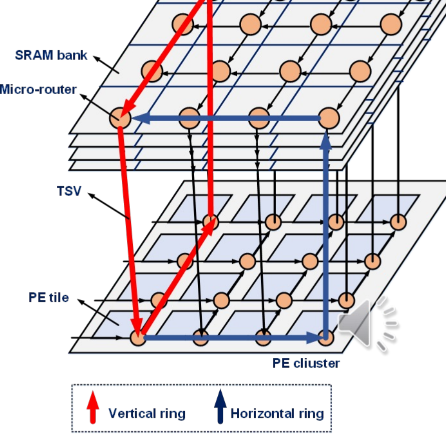
- Three conceptual observations to paving the way to easier 3D system prototyping and implementation

- IP becomes a critical issue when chipletizing the system: reuse or disaggregation/decomposition
  - Monolithic die can be decomposed into functional blocks or reorganized with other dies
- In the high-speed or frequency system, devices packed in a package or placed closely may cause degraded performance or dysfunction. Cut-only partition is not enough.



- 3D cross-ring interconnection architecture
  - Vertical rings (for IFM & Psm)
  - Horizontal rings (for weight & Psm)
- Efficient Dataflow for DNN
  - Inference
  - Training

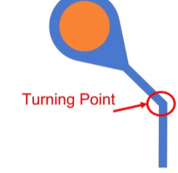




(a) The offset vias that occupy the same region in each layer.

(b) The offset vias that will not route back to the same region in prior layers.

Figure 6: Offset vias (stagger vias) are the vias in which any two adjacent layers will not overlap.

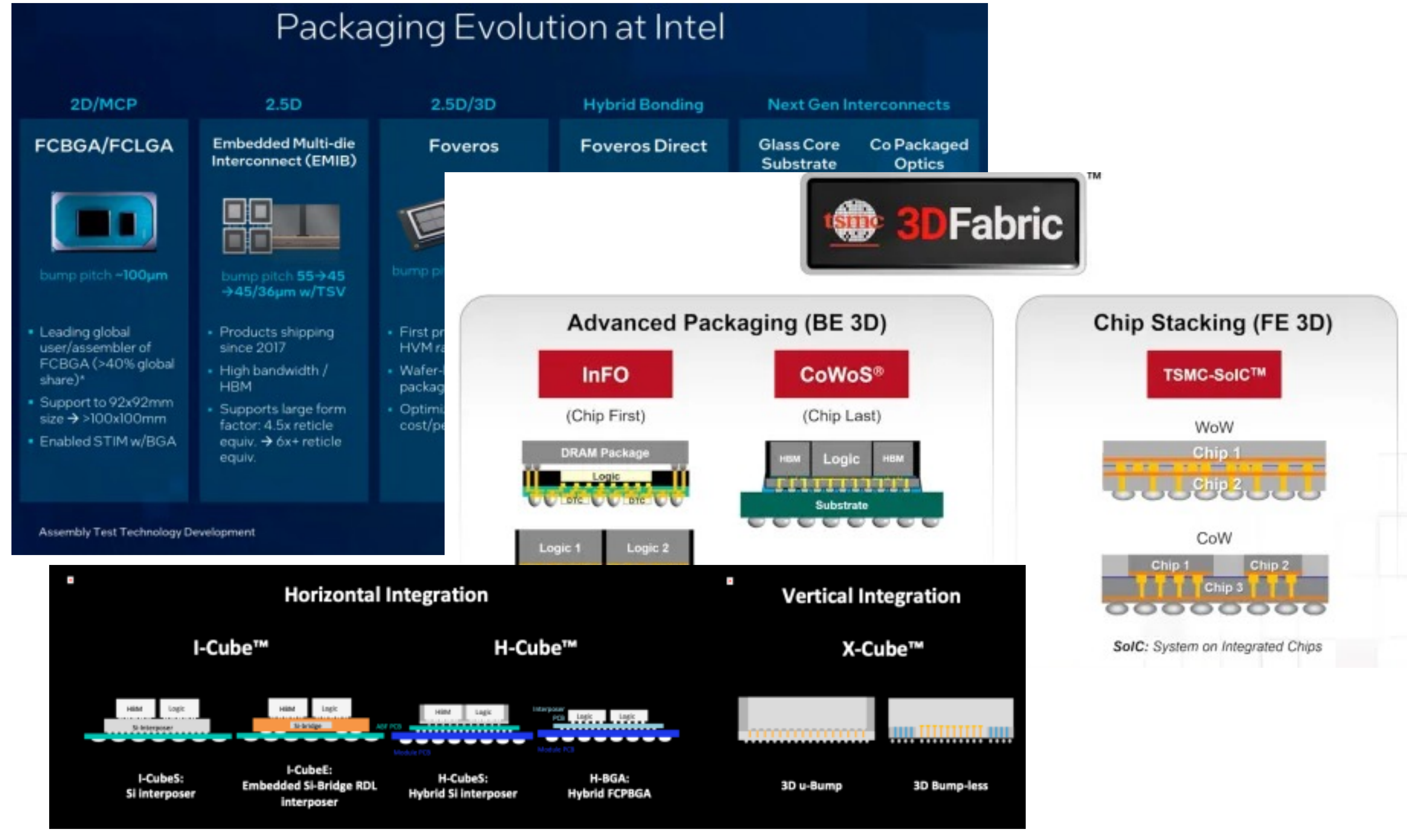


(b) Teardrop structure. A metal is shrunk from via to the wire. The turning point may suffer from stress problem.

Packaging Technology Evolution

- The conventional packaging usually happens after getting the bare dies from the wafer sawing. This covers PTH/DIP, QFP, BGA.
- The first single chip microprocessor (1971) has the density around 19000 transistors/cm^2. Ratio of IC to package level integration was roughly around 2000:1.
- Early 1990s, the transistor density is around 265000 transistors/cm^2, this translates to that ratio is around 5000:1.
- In 1998 Intel's Pentium III introduced the ratio of IC to package level integration grew to more than 0.5M:1, and BGA packages emerged.
  - Transition from computing to mobility
- Advancing to HPC and AI era

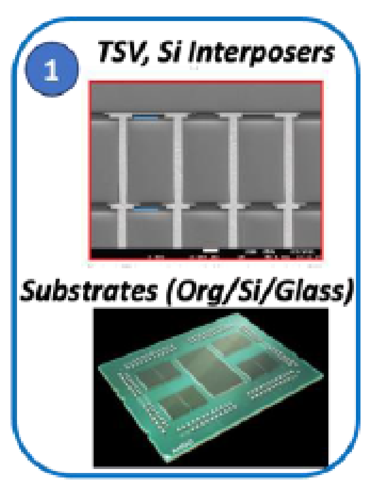
Advanced Packaging for HPC and AI

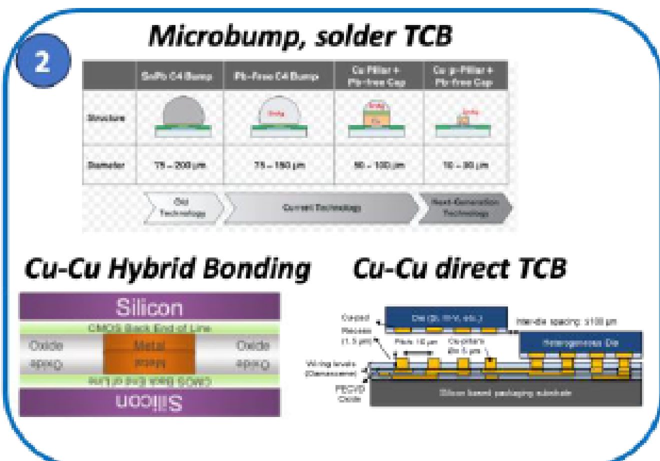


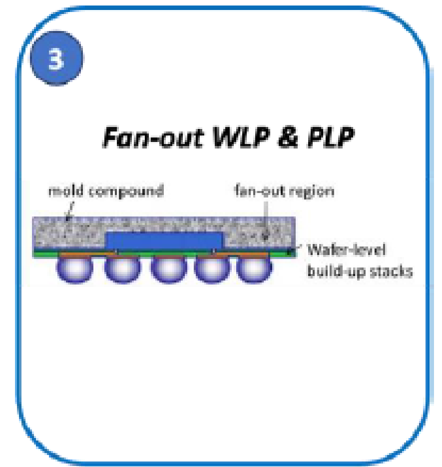
EETimes: Understanding the Big Spend on Advanced Packaging Facilities

From HIR Roadmap

Parameter	Unit	2025	2027	2029
Silicon Node	nm	3nm	2nm	1nm
I/O Bandwidth (Logic-HBM)	Gbps	1024 x 2.4	2048 x 3.6	4096 x 6.4
I/O per mm per layer (shoreline)	#	250	500	1000
I/O lines and spaces (and vias)	micron	2/2/2	1/1/1	0.5/0.5/0.5
Package to Board I/O BW	Gbps	64 per I/O	112 per I/O	256 per I/O
Package to Board Pin Count	#	9600	11200	12800
Power Density	W/mm^2	1	1.05	1.1
Package Dimension (Minimum)	mm	95	103	120



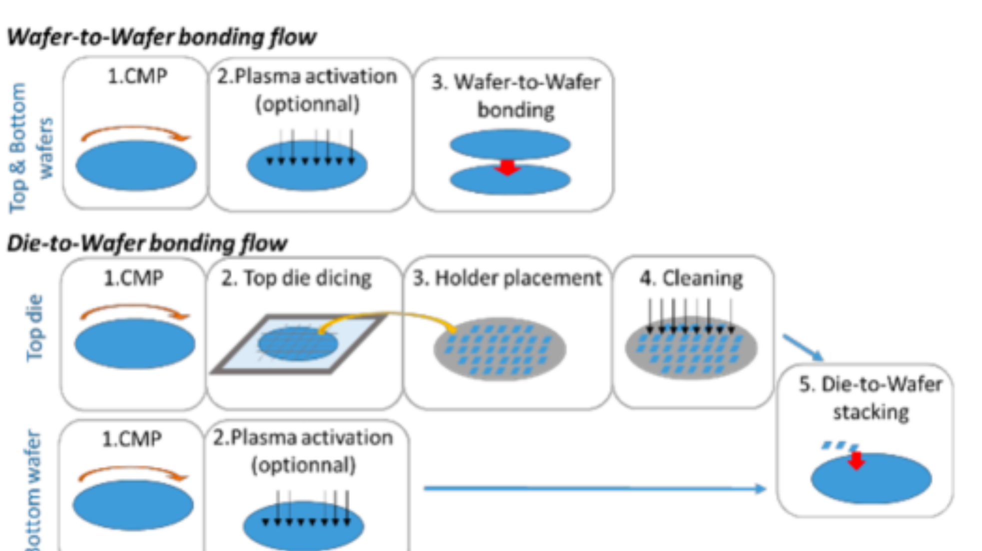




Source: MRHIEP Report

Technologies Snapshots

- Mainstream: Intel EMIB; TSMC SoIC; FOWLP
- Interposer (2.5D): costly, like PCB but more wires; secondary substrate
- Cu-to-Cu direct bonding (TCB) vs. Hybrid bonding
  - Two key differences: 40um and W2W/D2W



DTW process challenges :
Introduction of
- **Dicing & cleaning**
- **Die handling**
- **Die alignment**

with respect of :
surface cleanliness & nanotopography

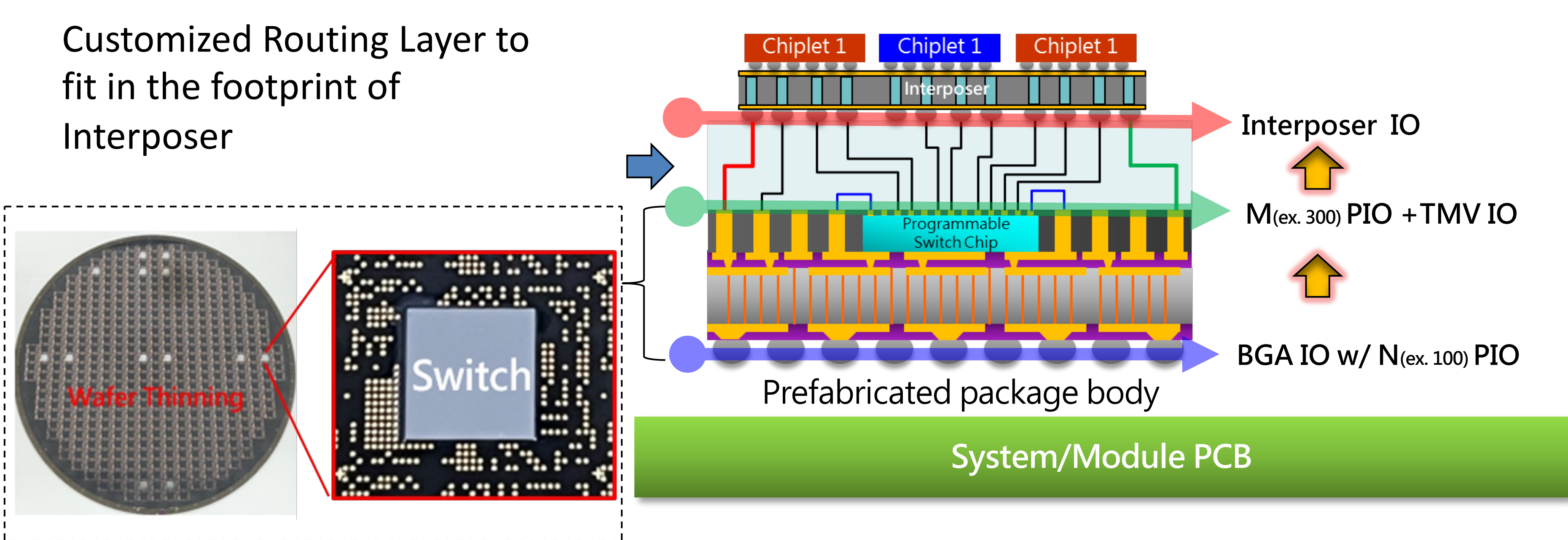
Source: EEtimes:Bumps vs. Hybrid Bonding For Advanced Packaging 2021

Technologies Snapshots

- Issues on the table
  - Reliability issues: homogeneous and heterogeneous integration, interposer material and warpage
  - Should have ability to integrate the right thermal features to define the physical envelope (i.e. form factor and number of die/die stacks that can be integrated on the package)
  - Bond pitch scaling for die-to-die, die-to-interposer and die-to-substrate (microbumping) interconnections
  - Possible to use standard packaging to achieve ap: scale down the pitch and solve crosstalk (for high performance)

Introducing Alternative Solution

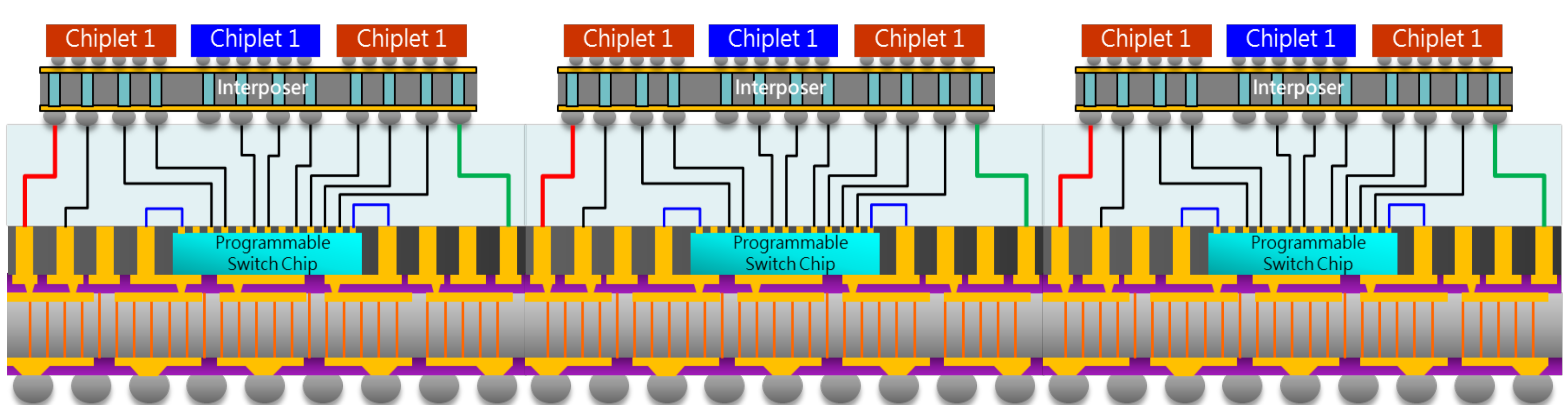
The package body is pre-designed and fabricated for 3D-IC rapid prototyping.



Taiwan ITRI's Prefabricated Package Service

Key features:

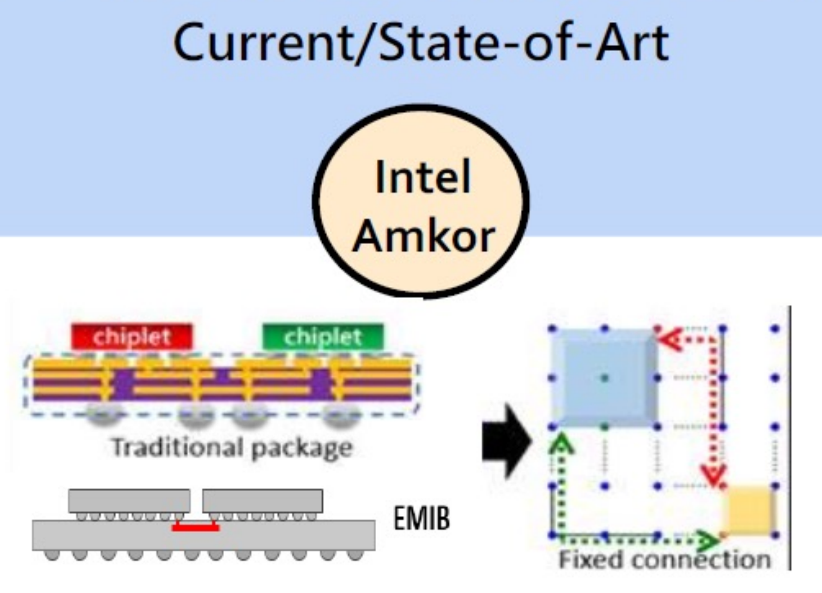
1. Rapid prototyping is achieved by employing a pre-designed and prefabricated package body with flexible, customized routing layers tailored to the net connection requirements of 3D-IC.
2. This serves as a rapid prototyping platform to accommodate high-density interconnection interposers or chiplets.
3. The PI/SI performance of the prefabricated package can be meticulously designed and verified
4. Furthermore, the scalability of the prefabricated package body can be implemented through cascading single units."



Programmable Packaging

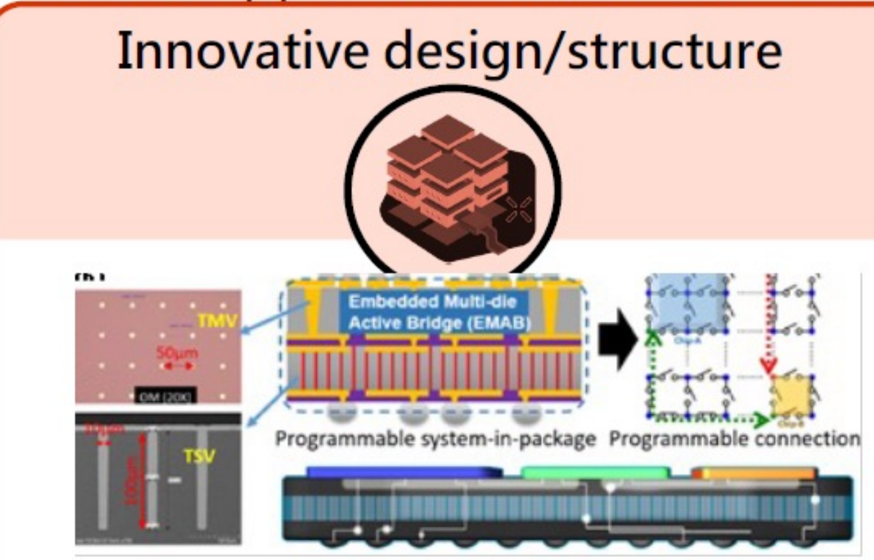
- Pre-fabricated substrate (size/function scalable)
- Patented embedded switching chips
- One-layer redistribution to meet different applications (infrastructure)

Current/State-of-Art



- regular design, fixed interconnect (w/o programmable) and MP
- less flexibility for same approach

Innovative design/structure



- Innovative achievement for AIoT
- 2022 IEEE Symposium on VLSI
- Prototyping and time-to-market

Source: HIR 2023 from ITRI

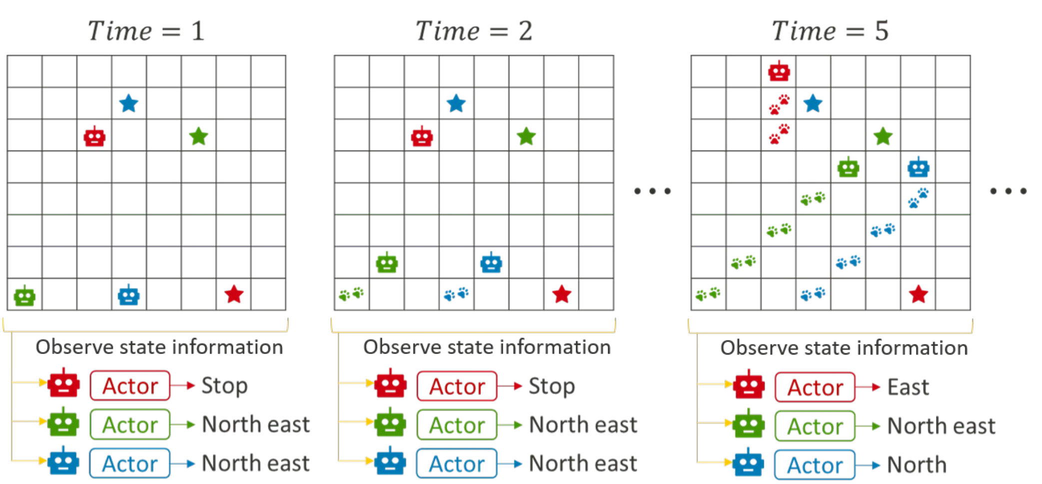
Methodologies/Tools Snapshots

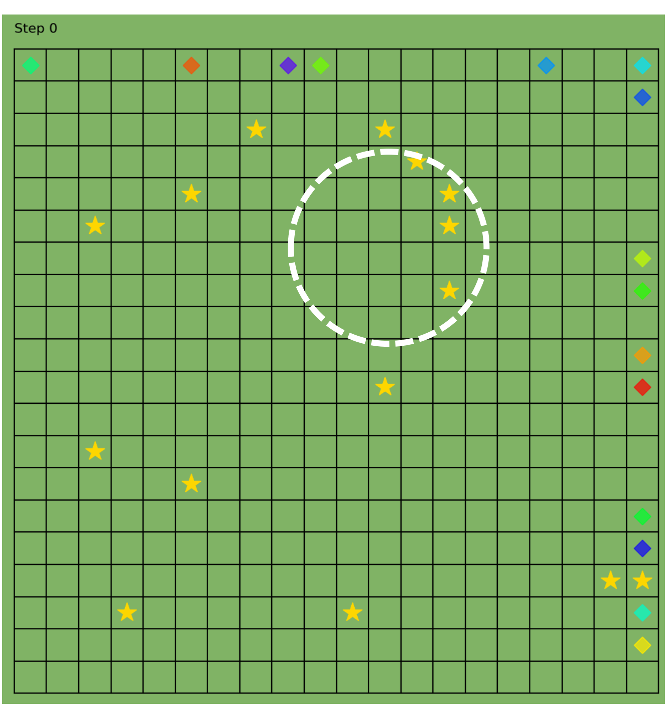
- Main focuses: RDL synthesis, chiplet placement, and thermal awareness physical design and simulation

- We are currently working on the following tasks
  - ML-based routing and SI-awareness on D2D and substrate
  - Programmable package layout design

Multi-Agent Package Router by Learning

- Multi-net concurrent routing
  - We built deep learning models to deal with net order problem on concurrent maze routing.
  - Observing features of environment, each agent performs an action at every time step that will maximize future rewards.

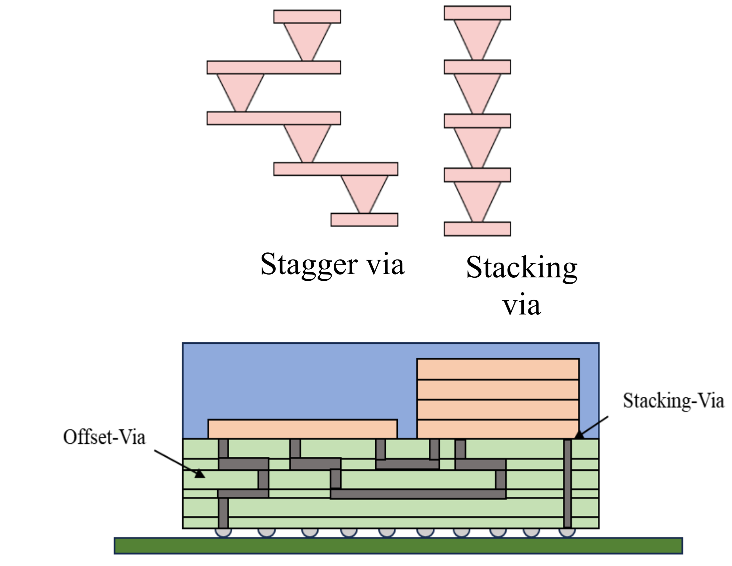




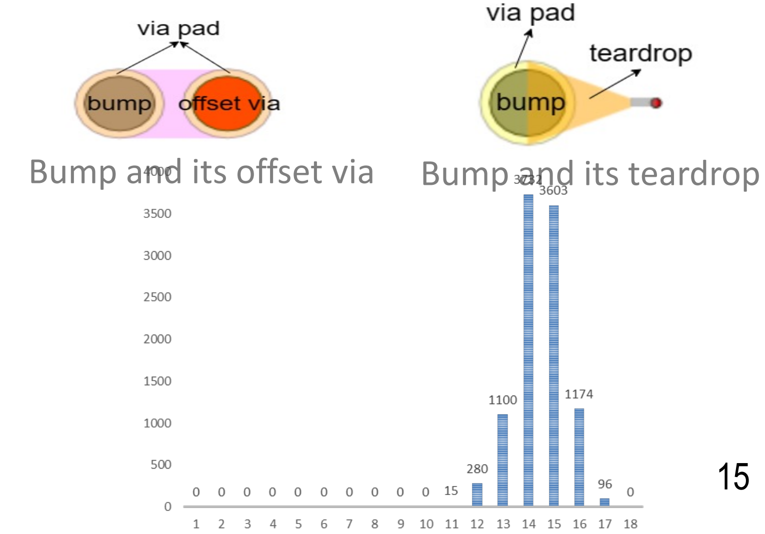
Source: Yeh et al ASPDAC 2023

SI-Aware Customized D2D Routing

- InFO constraints
  - Staggered via can reduce the line stress on via due to multi-layer RDLs
  - Improve the RDL integrity, and less prone to cracks compared to stacking via
  - Induces large area, routing resource decreases and routing difficulty increases
  - [6] shows that 4-tiers stacking via suffers 45% more line strain than stagger via
  - Due to the fine pitch line width for routing, teardrop can make the signal more smooth
  - Teardrop can reduce the crack between via and signal
- Preliminary results
  - Single layer and 2-layer interconnect shielding are studied and SI is improved by ML/DNN
  - Routing resource is upper bounded by our method, and new style will be proposed

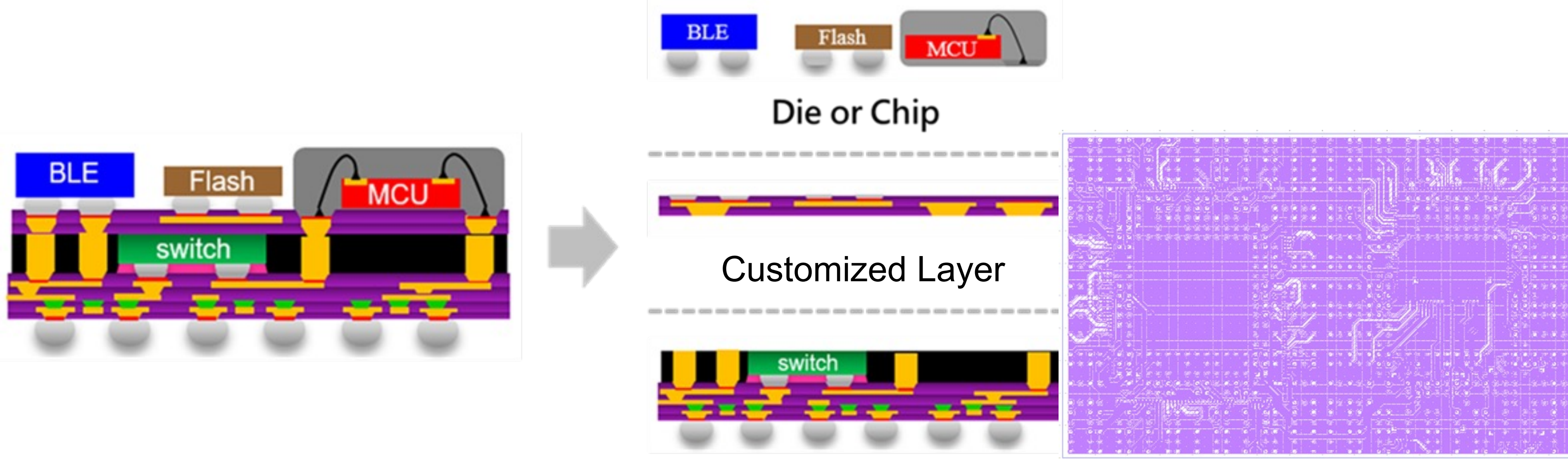


[6] Y. Chiang, S. Tai, W. Wu, J. Yeh, C. Wang, and C. Douglas, “Info_os (integrated fan-out on substrate) technology for advanced chiplet integration,” in 2021 IEEE 71st Electronic Components and Technology Conference (ECTC). IEEE, 2021, pp. 130–135.



Problems on Customized Layer Design

- Pin assignment between the programmable package and target chiplets
- Minimize the number of layers in the customized layer for cost reduction



Chiplets the Savior in System Implementation?

- Modular architecture/building block-based methods applicable?
- IP implementation becomes more difficult, many boundary conditions and technology-dependent issues (not good for fast migration)
  - When you don’t fully know the boundary conditions, you may have to over-design to make it reusable
- One needs to worry about chiplet/dielet warehousing. Chiplet mechanical and electrical standards are also essential.
- We need to generate physical, mechanical and thermal guardrails by developing modular packaging and chiplet designs based on modular domain-specific reference architectures.

Source: MRHIEP Report

Implementation Standards Efforts

- The use of standards can make it more feasible for multiple companies to create chiplet-based products.
- Current efforts on standards
  - D2D protocol (parallel): BoW, UCIe (for both laminate and advanced packaging technologies), SuperCHIPS, HBM (for DRAM)
  - Physical description
    - Chiplet-based design requires models of the physicals of chiplets to be available in an EDA tool flow for package design. These models need to capture the size, thermal information, power distribution, dynamic behavior (power model), power and signal integrity and other attributes relevant to package design.
    - Representatives: *TSMC 3Dblox*, CDXML
  - Test and verification: need more efforts

Source: MRHIEP Report

Standards for System Designs

- Standard will be good for testing, verification for chiplets will also become easy, but system verification becomes extremely difficult
- The industry is trying to reduce the burden at the system level by having standards, so that each designer or group can adhere to the standards, and then the assembly at the system level becomes much more convenient.
- Disaggregation has become necessary for some companies, either because of design size or for manufacturability issues. (also chiplet discovery)
- Within a scaled down assembled system, fine pitch interconnects make inter dielet communication simple using energy efficient protocols such as SuperCHIPS

Source: MRHIEP Report

Final Remarks

- HPC/AI systems suitable in advanced packaging: LLM, IMC
- System technology co-design (STCO) for lower cost and higher performance
  - How to realize the system under appropriate cost: system architect needed
  - IP/chiplet business and preparation are a must
- Predictive modeling for systems? Constraining upfront
  - Advanced packaging design cost-feasibility study