Warpage Study by Employing an Advanced Simulation Methodology for Assessing Chip Package Interaction Effects

Jun-Ho Choy[a], Stéphane Moreau[b], Catherine Brunet-Manquat[b] Valeriy Sukharev[a], Armen Kteyan[c] ,
[a] Siemens EDA, 46871 Bayside Parkway, Fremont, CA, USA.
[b] Univ. Grenoble Alpes, CEA, LETI, 38000 Grenoble, France.
[c] Siemens EDA, Yerevan, Armenia.

Junho.choy@siemens.com

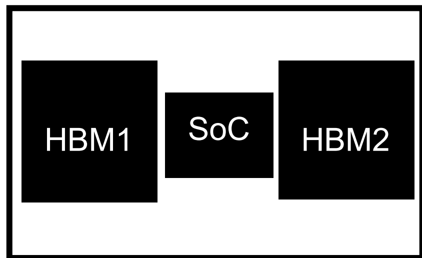
ISPD, March 2024

leti
ceatech
TECHNOLOGY RESEARCH INSTITUTE

SIEMENS

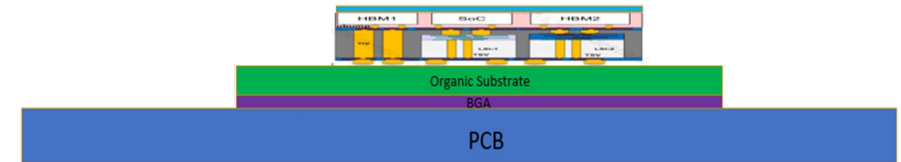
Chip-Package Interaction (CPI): the problem

Design – Signoff clean ☺



Circuit Performance after chip production ☺

Circuit Performance after chip packaging/soldering ☹



Impact of CPI on chip performance and reliability:
- **mechanical deformations/stresses**
- temperature increase during the operation
- electrical issues

Simulation capabilities are required to prevent IC failure after the packaging

SIEMENS

CPI stress induced challenges

Electrical impact - eCPI

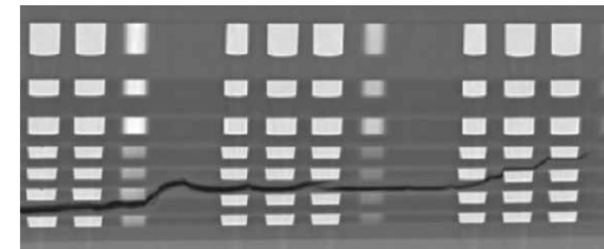
Stress impact on band structure of Si → variations in mobility changes may change circuits performance

Piezoresistence approximation:

$$\Delta U/U0 = -(\pi_l \sigma_l + \pi_t \sigma_t + \pi_z \sigma_z)$$

Mechanical impact - mCPI

Interconnect fracture –
cracking of ULK/ ELK dielectrics, delamination; bump fatigue and cracking



Crack propagation in a multilevel interconnect.

X. F. Zhang, et al., Advanced Metallization Conf., 2008.

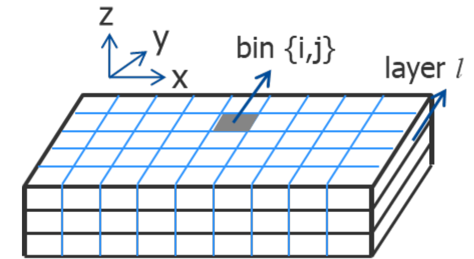
SIEMENS

EDA analysis flow for CPI induced problems

SIEMENS

Anisotropic Effective Material Properties (EMP) for Resolving Effects of Layout Nonuniformities

- **Effect of the layout-feature-scale variations in mechanical properties (responsible for essential variation in stress components) is accounted by introducing the Effective Anisotropic Properties of composite materials.**
- Composite layers are partitioned into rectangular bins. Different granularities are used for package-scale and IP-scale analysis.
- Metal density and routing direction in each bin are extracted by **layout extraction tools** and used for calculation of components of average Young's modulus, Poisson's ratio, and CTE in directions parallel and normal to the routing direction.



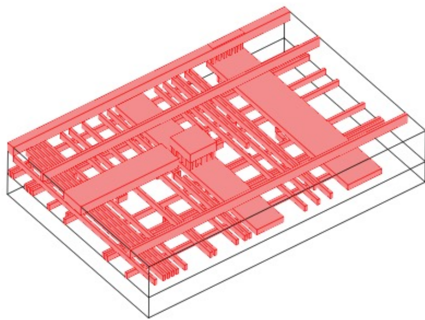
$$E_{\parallel} = E_M\rho_M + E_D(1-\rho_M),$$

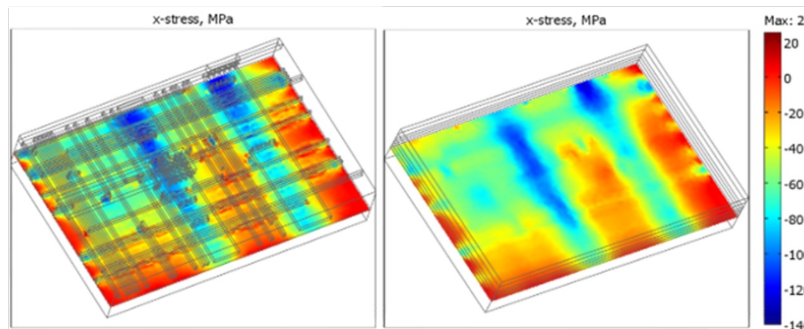
$$E_{\perp} = E_M E_D / \left(E_D\rho_M + E_M(1-\rho_M)\right)$$

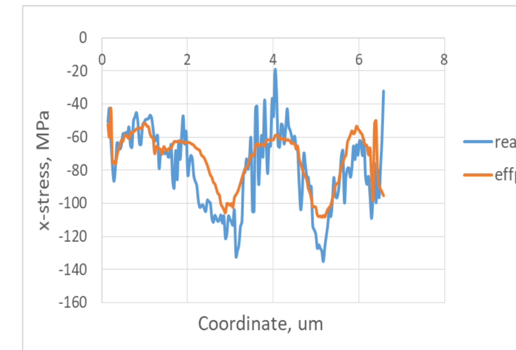
$$\alpha_{\parallel} = \frac{\alpha_M E_M \rho_M + \alpha_D E_D (1-\rho_M)}{E_M\rho_M + E_D(1-\rho_M)}$$

$$\alpha_{\perp} = \alpha_M\rho_M + \alpha_D(1-\rho_M)$$

$$\nu = \nu_M\rho_M + \nu_D(1-\rho_M)$$







SIEMENS

CPI stress: from package analysis to EDA flow

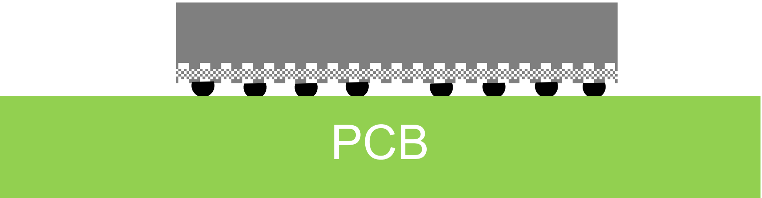
Package simulations – FEA

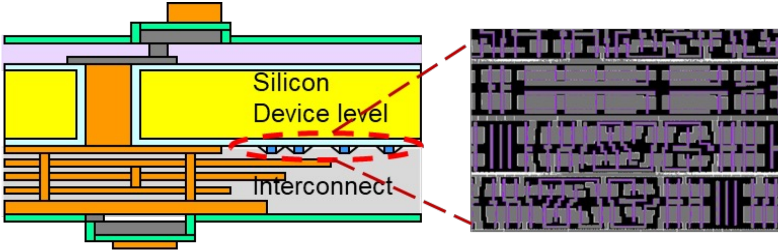
Required input: geometry description; material properties; assembly process conditions

Layout analysis

Details of non-uniform composite blocks (metal layers, diff layer, C4, microbumps,…)

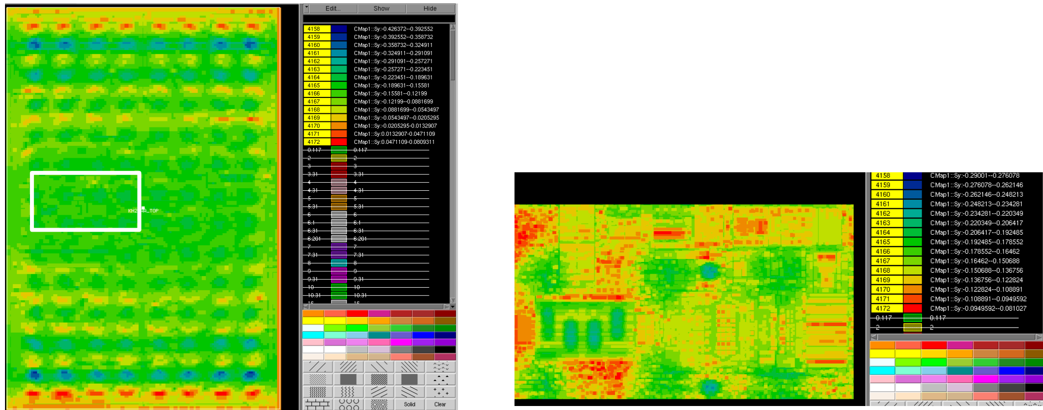
Locations/orientations of devices



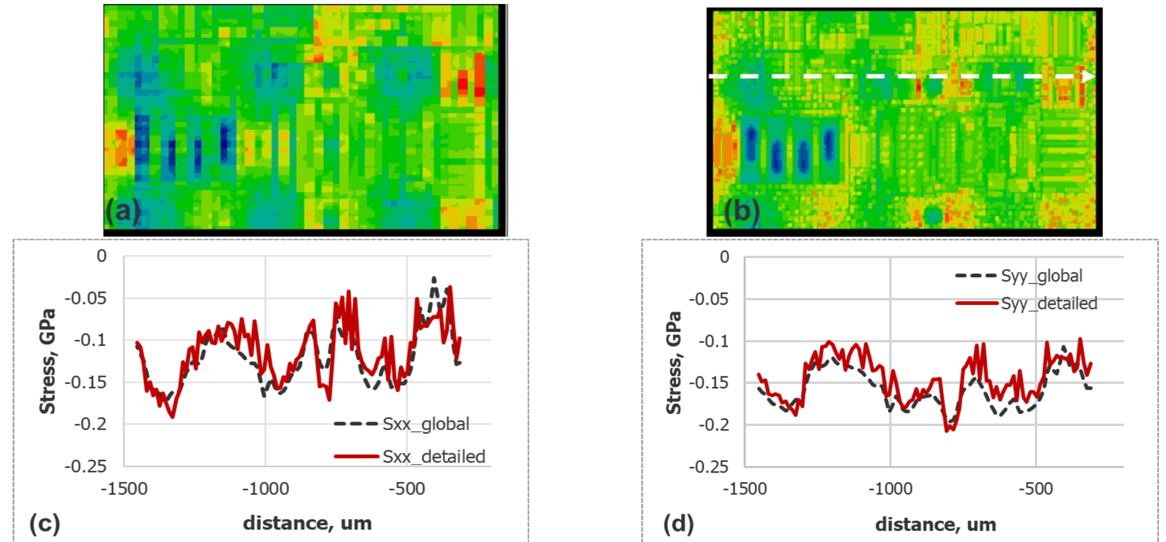


Multi-Scale Simulation - results

- Distribution of thermal stress component (Sxx) inside an IP block obtained from (a) global-scale, and (b) sub-modeling.
- 1D profiles of Sxx and Syy reveal the difference of the order of tens of MPa in stress components for the two scales.
- Performing only global-scale modeling can lead to inaccuracy in predicting device characteristics.



Bending stress simulation



Thermomechanical stress simulation

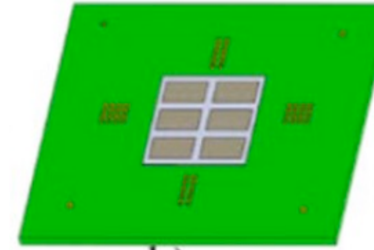
A. Kteyan et. al, Proc. International Symposium on Physical Design (ISPD), (2022)

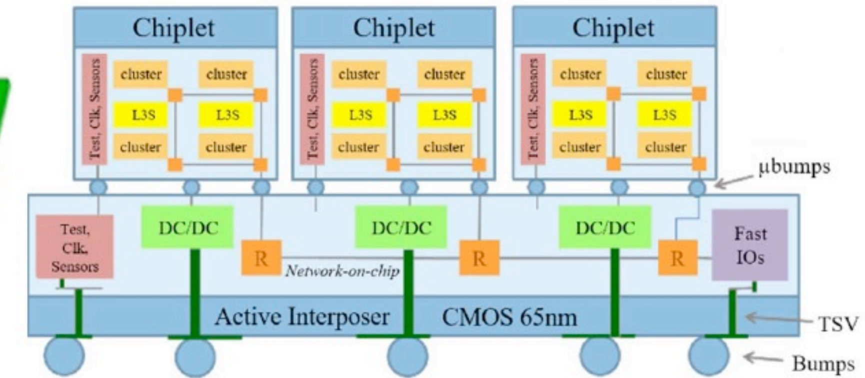
mCPI: mechanical

leti
cea tech
TECHNOLOGY RESEARCH INSTITUTE
SIEMENS

mCPI: calibration on warpage measurements

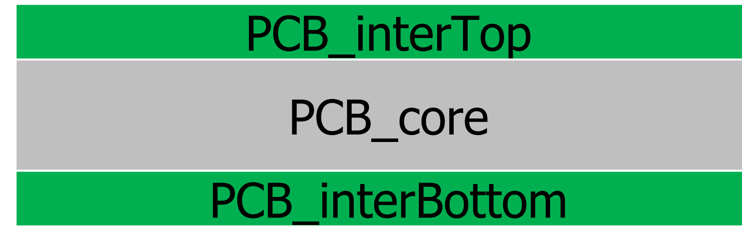
- We explore possibility to use warpage measurements on package components for model calibration, when electrical measurements are NOT available in pre-design stage during process development.
- Altitude measurements during heating, and subsequent cooling, on INTACT package components – chiplet, interposer, PCB will be used.
- Measurement tool: Altisurf 520 (Altimet)

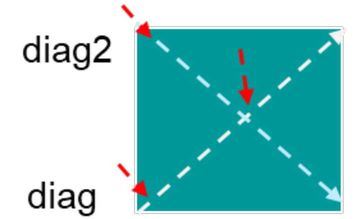




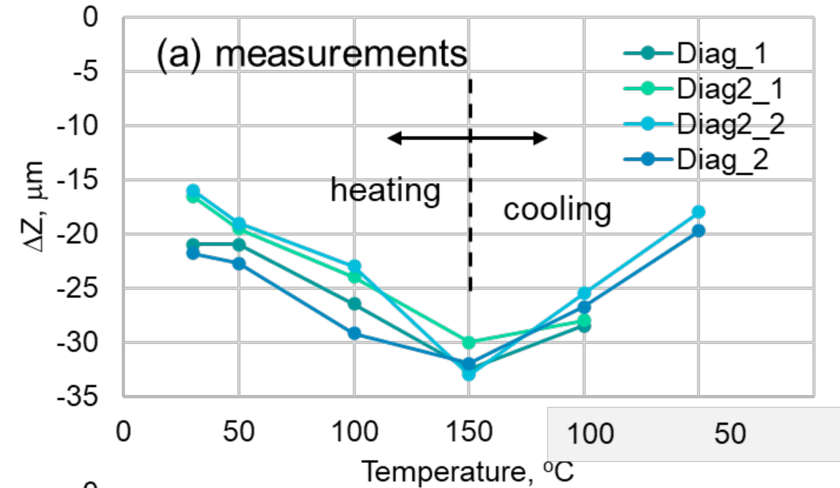
leti ceatech TECHNOLOGY RESEARCH INSTITUTE SIEMENS

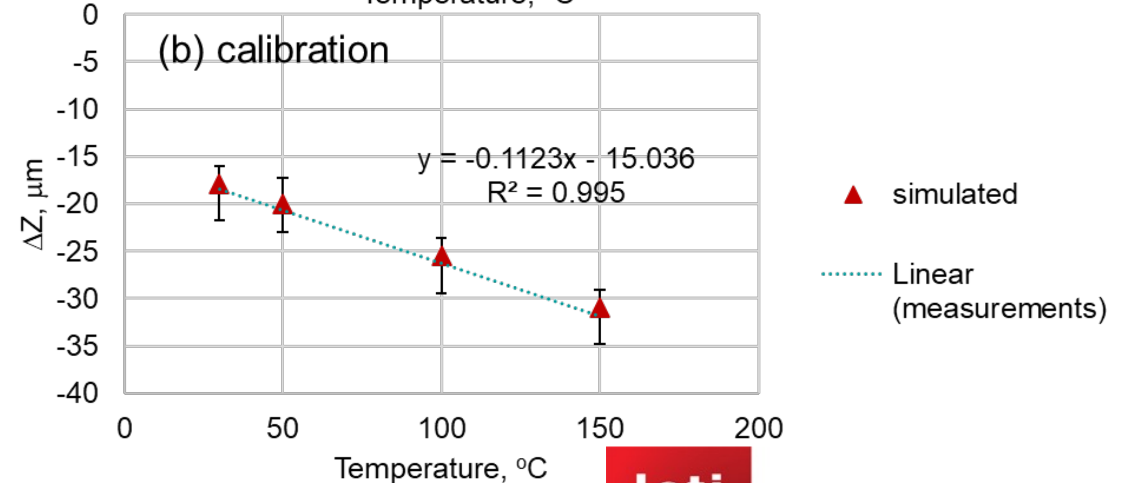
mCPI: calibration on PCB





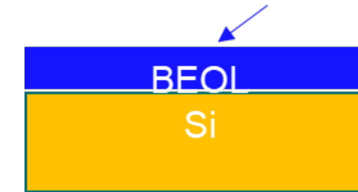
- Three block PCB: each block consists of uniform smeared EMPs that are calculated from known thermo-mechanical properties of {conductor, insulator}, and thickness for each layer.
- These properties are further calibrated by fitting temperature-dependent warpage measurements: altitude measurements on a top surface of a stand alone PCB, across diagonal directions during heating and cooling.
- After parameters adjustment, good agreement is found between measured average altitude (ΔZ), and simulated warpage values.

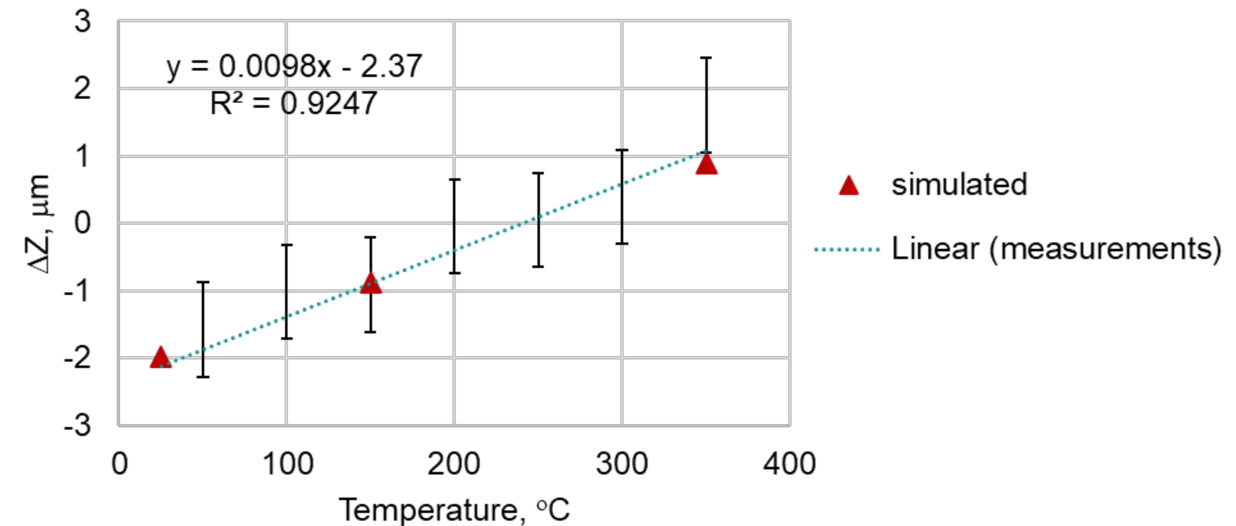




mCPI: calibration on chiplet

- Warpage on BEOL top surface.
- Uniform smeared BEOL properties are calculated from thermo-mechanical properties of {conductor, insulator}, and thickness for each layer.
- These properties are further calibrated by fitting temperature-dependent warpage measurements.
- After parameters adjustment, good agreement is found between measured average altitude (ΔZ), and simulated warpage values.

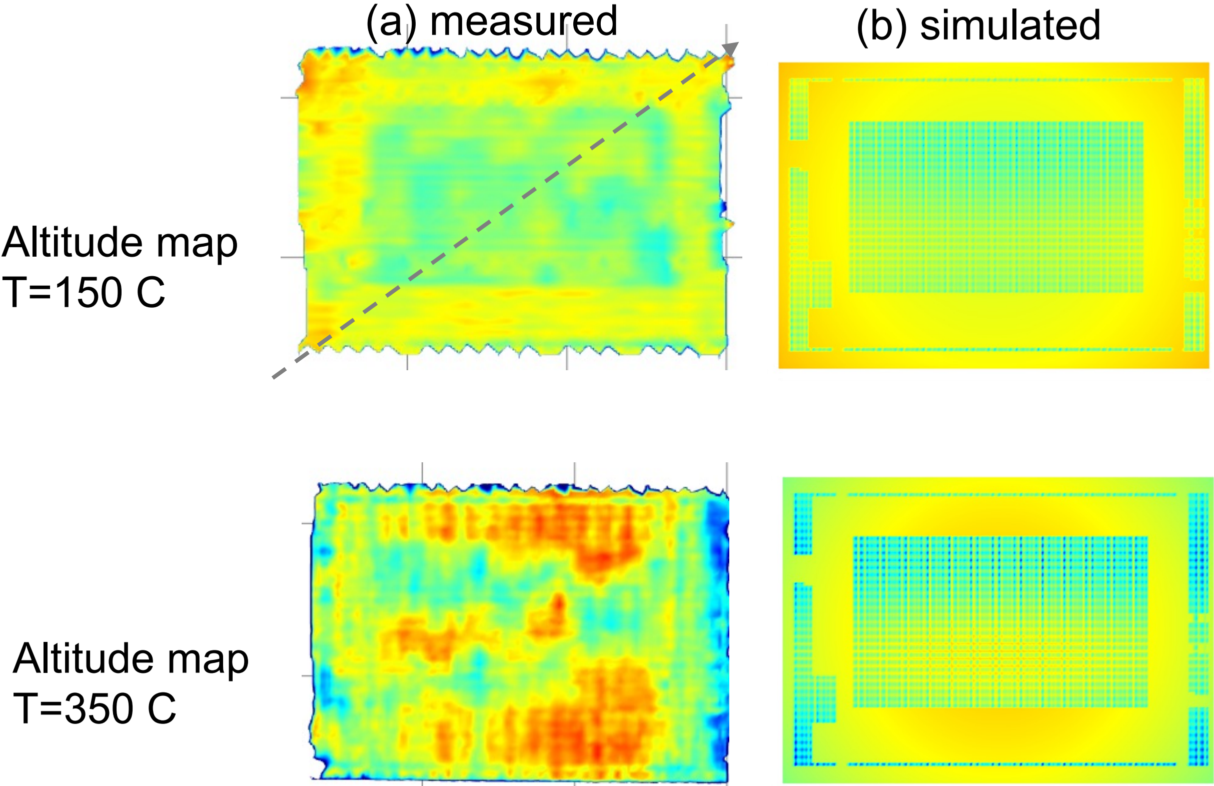


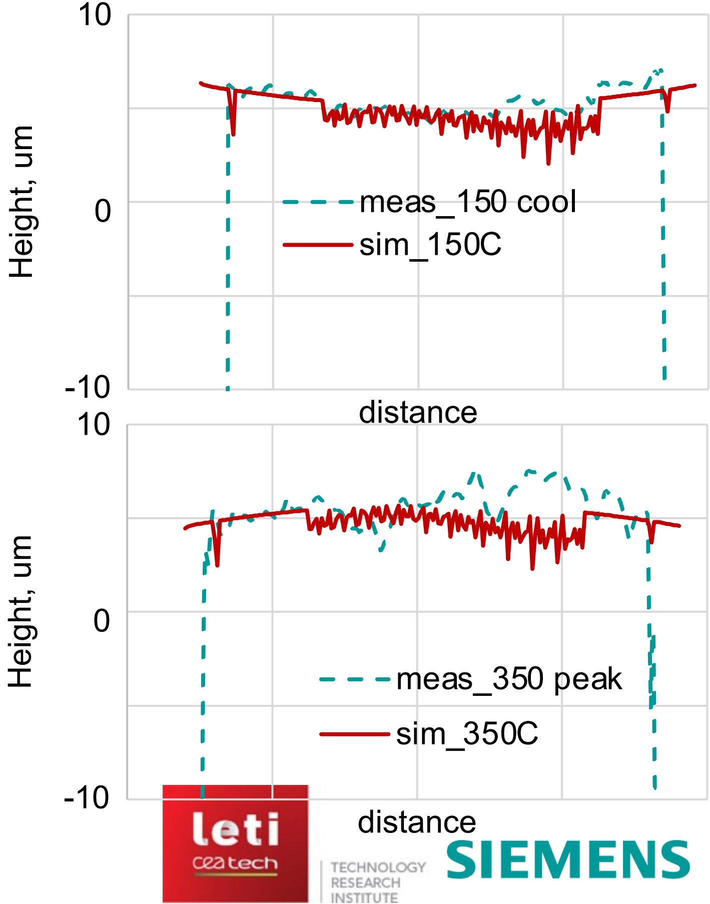


leti ceatech TECHNOLOGY RESEARCH INSTITUTE SIEMENS

mCPI: chiplet warpage simulation

- Simulation results at two temperatures: transition in warpage profile from convex (150 °C) to concave (350 °C) matches the measurements.
- The simulated and measured profiles agree well.

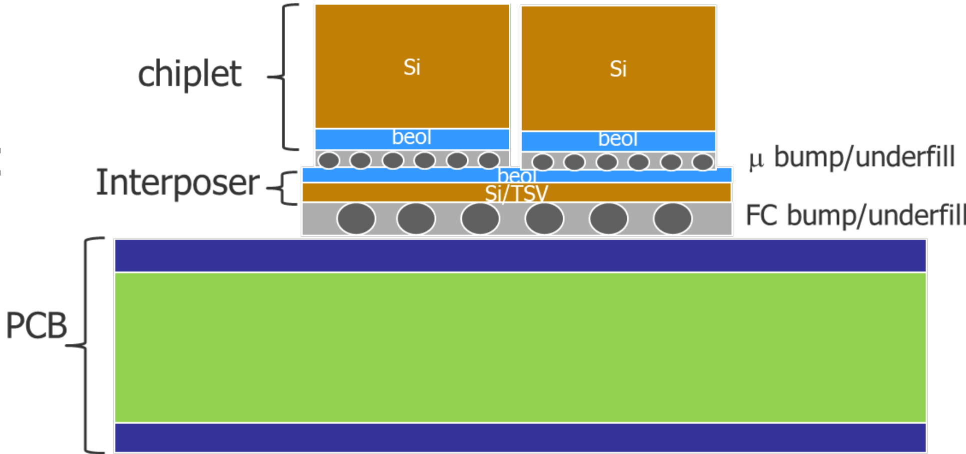


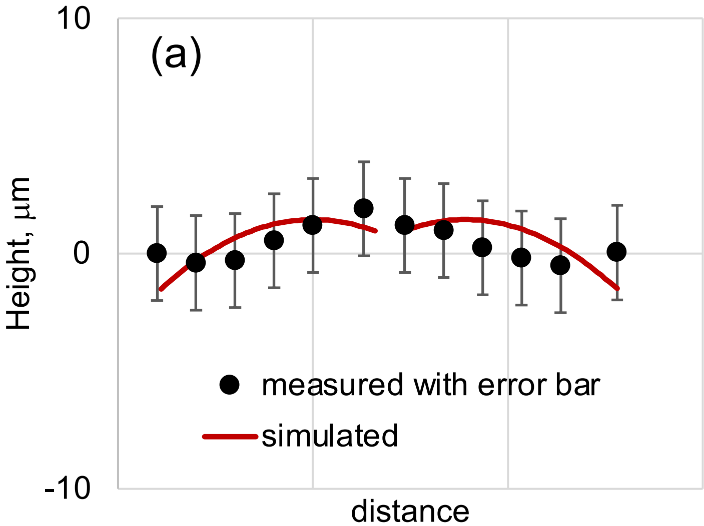


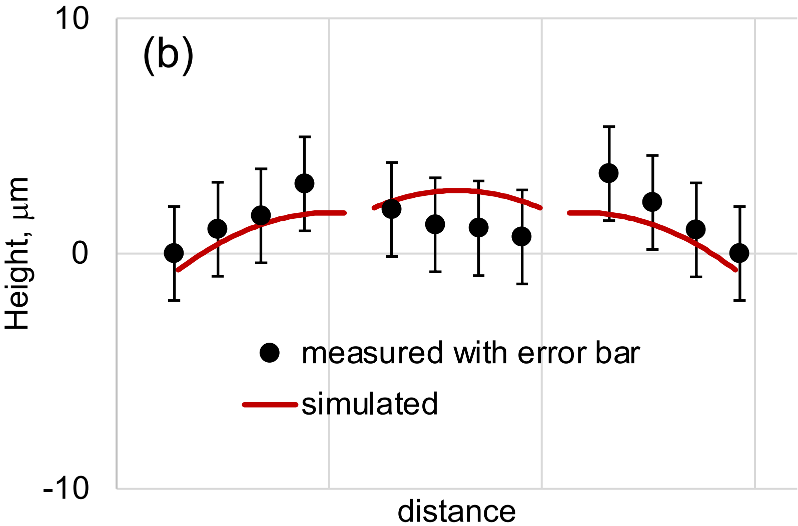
leti ceatech | TECHNOLOGY RESEARCH INSTITUTE SIEMENS

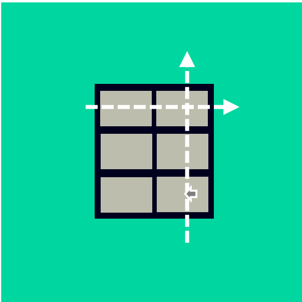
mCPI: warpage prediction on full stack package

- Simulated 1D profile on a full stack package at room temperature, after model calibration.
- The effects of the following additional factors are found negligible on the height profile of the full stack package:
  - prior thermal history of individual blocks,
  - transient thermal effects, and,
  - plasticity of solder joints.





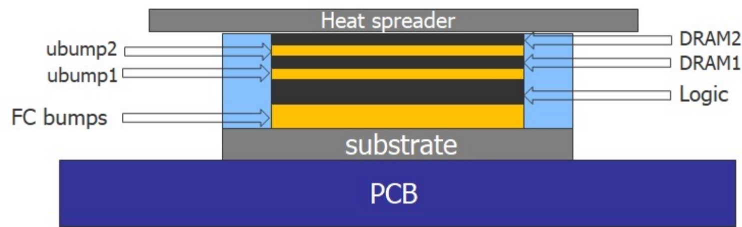


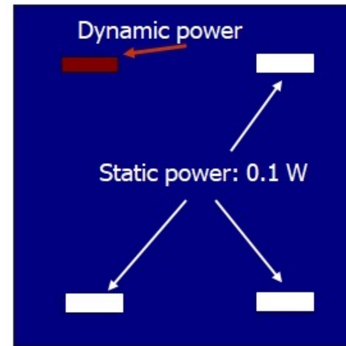


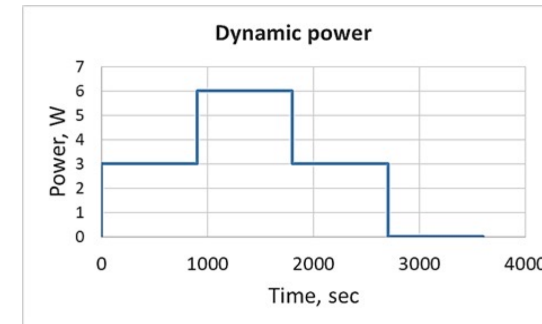
leti ceatech
TECHNOLOGY RESEARCH INSTITUTE
SIEMENS

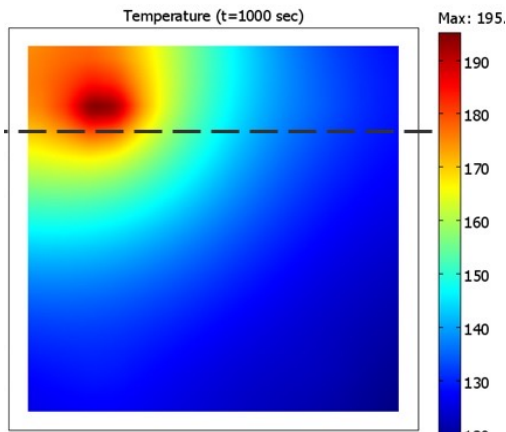
Assessment of Temperature and Stress During Chip Operation

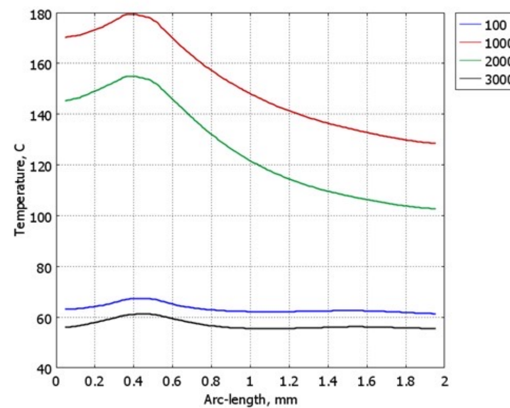
Thermal-mechanical FEA allows assessing the stress in the stack during chip operation

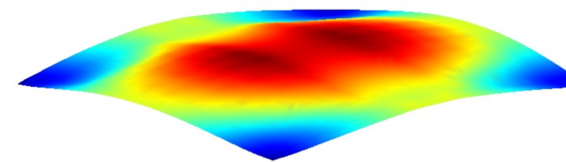




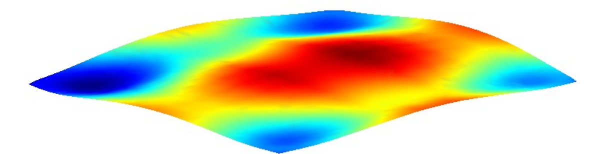








Packaging induced warpage (t=0)



Warpage evolution due to heating (t=1000)

SIEMENS

Conclusions

- The newly developed CPI stress analysis EDA tool combines FEA simulations with layout analysis capabilities, and allows obtaining CPI stresses with any desired resolution, by applying multi-scale simulation technique.
- The study demonstrates that, for the purpose of mechanical failure analysis in the early stage of a package design, the warpage measurements can be used for the tool's model calibration.
- CPI stress-induced reliability analysis under chip operation condition, can be performed when the linked thermal & mechanical simulations is enabled.

SIEMENS