Unified 3D-IC Multi-Chiplet System Design Solution

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Outline

• 3D-IC Multi-Chiplet System Design Overview & Challenges

• Unified Multi-Chiplet System Design Solution

• Summary
Unleashing the Power of Possibility by 3D-IC
3D-IC Development Challenges

- 3D-IC heterogeneous design integration challenges
- System design challenges from planning, implementation to signoff
- Ecosystem challenges among Foundry/Customer/EDA

Heterogeneous Integration

System Design

- Power
- Thermal
- Timing
- Test
- Platform DB
- DRC
- LVS
- Routing
- SIPI
- System Planning

Si-Interposer
RDL-Interposer
Organic substrate
Digital Die
Analog Die
Silicon bridge
RDL bridge
F2F, F2B, Embedded
Bump, TSV, Ball
Overview 3D-IC Multi-Chiplet System Design flow

3D feasibility planning → Implementation → Signoff

Native 3D Flows
- 3D Memory on Logic
- 3D Placer and Unfold
- Partition

System-Level Planning
- 3D-IC Design Stack
- Die Floorplan
- I/O and Bump/TSV Planning

Implementation
- Assemble in System Planner for System-Level Planning

Top Die
- P/G Synth

Bottom Die
- P/G Synth

Early Analysis
- Thermal Analysis
  - Celsius™
- Timing STA
  - Temps™
- Power IR/EM
  - Voltus™/Clarity™
- SI Analysis
  - Sigtry™

Verification
- DRC/LVS
  - Pegasus™
- LEC
  - Conformal®
Unified 3D-IC Multi-Chiplet System Design Solution “Integrity 3D-IC”

Industry’s first integrated, high-capacity 3D-IC platform that enables 3D design planning, implementation and system analysis in a single, unified cockpit.
Platform Database for 3D Heterogeneous Integration

Database innovation: Can handle **multiple technology nodes**

**Integrity™ Platform Database**

- Netlist
- DEF or OpenAccess
- mcm
- SDC
- PDK
- MMMC (view definition)
- FlexILM
- ILM
- LEF
- Parasitic
- Metal Fill (physical context)
- SPEF
- Thermal map
- Timing context
- Boundary model
- GDS
- ...

**Hierarchical, Multi-Technology, Multi-Level, Multi-Model On-Demand DB**
3D Native Partitioning and Floorplan Synthesis (3D-EFS)

- 3D IC block-level partitioning and placement.
- Considers 3D wire length, number of I/O ports/bumps/TSVs, different process node and timing.
- Allow user to assign the die ID for hierarchical modules.
- Per-die timing budgeting and bump assignment to enable per-die P&R or convert to pseudo 3D.
System Planning Capability
Heterogeneous Integration Management & Optimization

Hierarchical Planning and Optimization of System-level Design and Connectivity

- Chip(let)-chip(let)-package-board signal-mapping
- Stack management
- Interface alignment validation
- System-level connectivity verification
- Advanced bump/TSV planning
- Bundle/bus-driven pin optimization

- Digital implementation
- Third-party die
- Analog layout
- BGA/LGA design
- Interposer
- Complete system-level view
Global Bump Planning, Optimization and Evaluation

- Bump/TSV/Ball assignment impacts 3D-IC System PPA.
- Connection optimization driven bump assignment improves routing congestion and wirelength.

![Diagram showing bump pattern design and connection optimization](image)

### Bump Pattern design

- **Covered**
- **Not Covered**

### Connection optimization (Signal)

- Frontside pin
- Backside pin

### Power, Ground bump quality evaluator

- Improve routing congestion compared with tapeoute design
Multi-Chiplet Display in 2D/3D Viewing

2D Canvas and Stack View (side by side)

3D Stack View (w/ Connections)

3D Canvas View (Selected Objects)

3D Canvas View (Wirebond)

3D Thermal View
Implementation Technologies with Digital, Analog, RDL Routers

- Each type of design has different design constraints and routing style.
- Co-design integration with Digital, Analog, RDL routers.
Early System-Level Analysis and Signoff Flow

**Volts™/Celsius™ Early Rail (Power and Thermal) Analysis**

**Integrity™ Flow Manager**
*Guided Flow*
- System Planning
- Implementation
- Power/Thermal/Timing/SIPI Analysis
- System DRC/LVS

**Tempus™ Timing Analysis**
- STA
  - Die1
  - Coupling Block
  - Die2
  - Model Extraction (Quantus™)
- Die1 SPEF
- Die1-Die2 SPEF
- Die2 SPEF
- Signoff STA

**3D Analysis with RAID Technology**

**Pegasus™ Physical Verification (DRC/LVS)**

**Clarity/Sigriety™ Signal/Power Integrity Analysis**

**System-Level Power and Thermal Analysis**

**System-Level SIPI Analysis**

**Inter-Die Connectivity Checking**
IR/Thermal Early Feasibility Analysis

**IR-drop**

- Model the 3D design as a resistance network
  - Abstract a chiplet’s metal stack as a grided 2D resistance network
  - Represent bumps/TSVs as resistors
  - Chiplets are connected through bumps and TSVs

**Thermal**

- Model the 3D design as a layer-based stacking
  - Condense chiplets into conductor or insulator layers
  - Represent bump as a layer affixed to chiplets
  - Model LID/TIM/PCB/Molding as a single structure of homogeneous properties

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![Diagram of IR/Thermal Early Feasibility Analysis](image-url)
New 3D-IC Open Standard - 3Dblox™
(https://3dblox.org/)

- 3Dblox Standard aims to streamline the 3D-IC package solutions in Planning, Implementation and Signoff.

3D/2.5D
3Dblox Language Focus

Top-Down Design Methodology
Inter-operability
Chiplet Reuse
Modulization

3Dblox™ 1.0
System Design Infrastructure
2022/10

3Dblox™ 1.5
Global Bump Optimization
2023/04

3Dblox™ 2.0
System Prototyping
2023/09

Key Enablers
Close partnership with TSMC on 3Dblox™

- Integrity 3D-IC platform offers full flow solution

### 3DFabric EDA Tool Certification Status

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As of 1/31/2024

EDA Alliance - Taiwan Semiconductor Manufacturing Company Limited (tsmc.com)
Summary – Unified 3D-IC Multi-Chiplet System Design Solution

- System PPAC is goal
- Heterogenous integration capability
- A common platform DB
- Full system level multi-physics analysis technology for Thermal, Power, SI/PI and Physical Verification
- Ecosystem with leading foundries

Cadence Integrity 3D-IC Platform

3D System Planning

3D Partitioning, Digital Implementation

Innovus

Analog/RF Implementation

Virtuoso

Package Design

Allegro

Multi-Technology Database

3D Analysis

(On-Chip and Off-Chip)

Thermal

Power

Timing

LVS/DRC

SI/PI