Unified 3D-IC Multi-Chiplet System Design Solution

Thunder Lay, Software Engineering Group Director

03/12/2024

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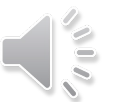
Outline

- 3D-IC Multi-Chiplet System Design Overview & Challenges
- Unified Multi-Chiplet System Design Solution
- Summary



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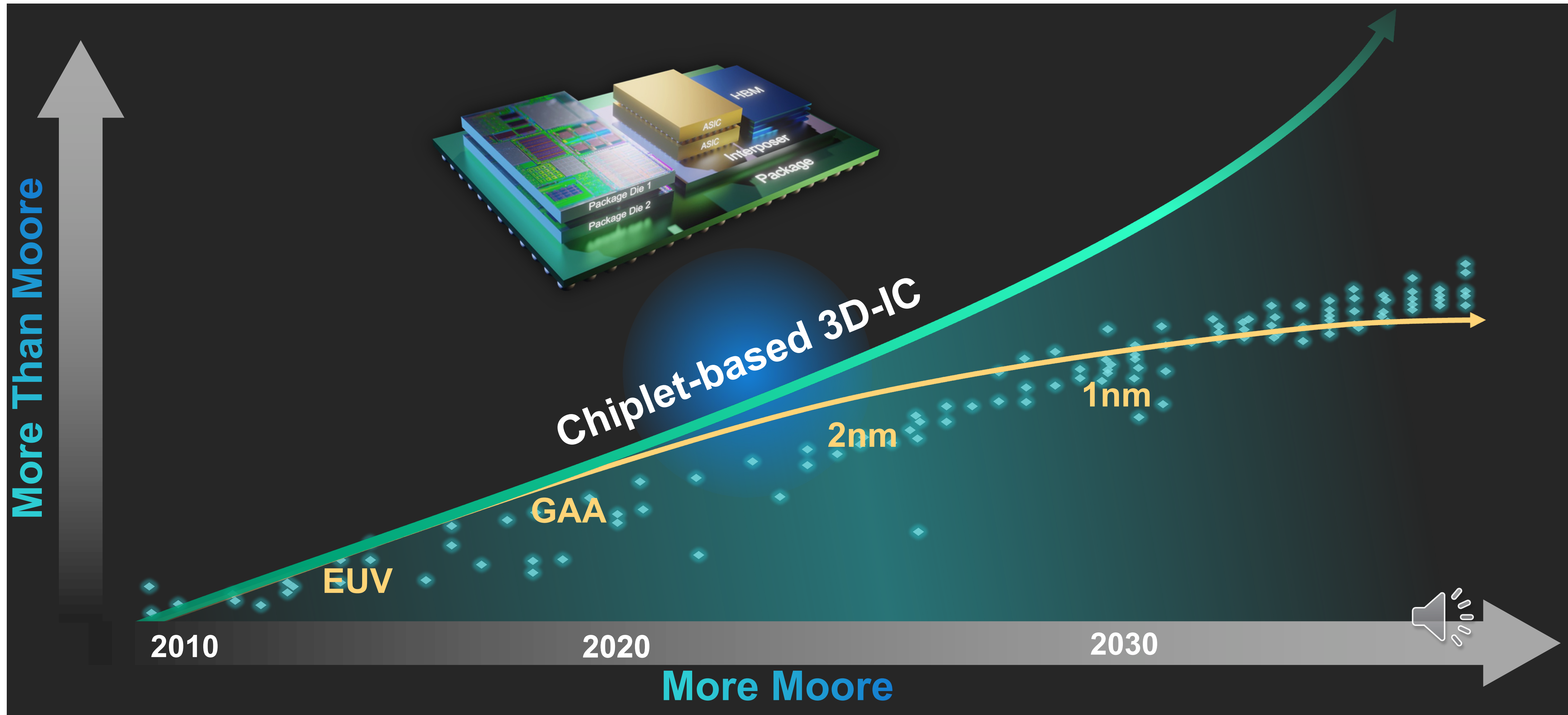
Unleashing the Power of Possibility by 3D-IC



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3D-IC Development Challenges

- 3D-IC heterogeneous design integration challenges
- System design challenges from planning, implementation to signoff
- Ecosystem challenges among Foundry/Customer/EDA

Heterogeneous Integration

Si-Interposer

RDL-Interposer

Organic substrate

Digital Die

Analog Die

Silicon bridge

RDL bridge

F2F, F2B, Embedded

Bump, TSV, Ball

System Design

Power

System Planning

Thermal

SIPI

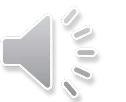
Timing

Routing

Test

DRC LVS

Platform DB



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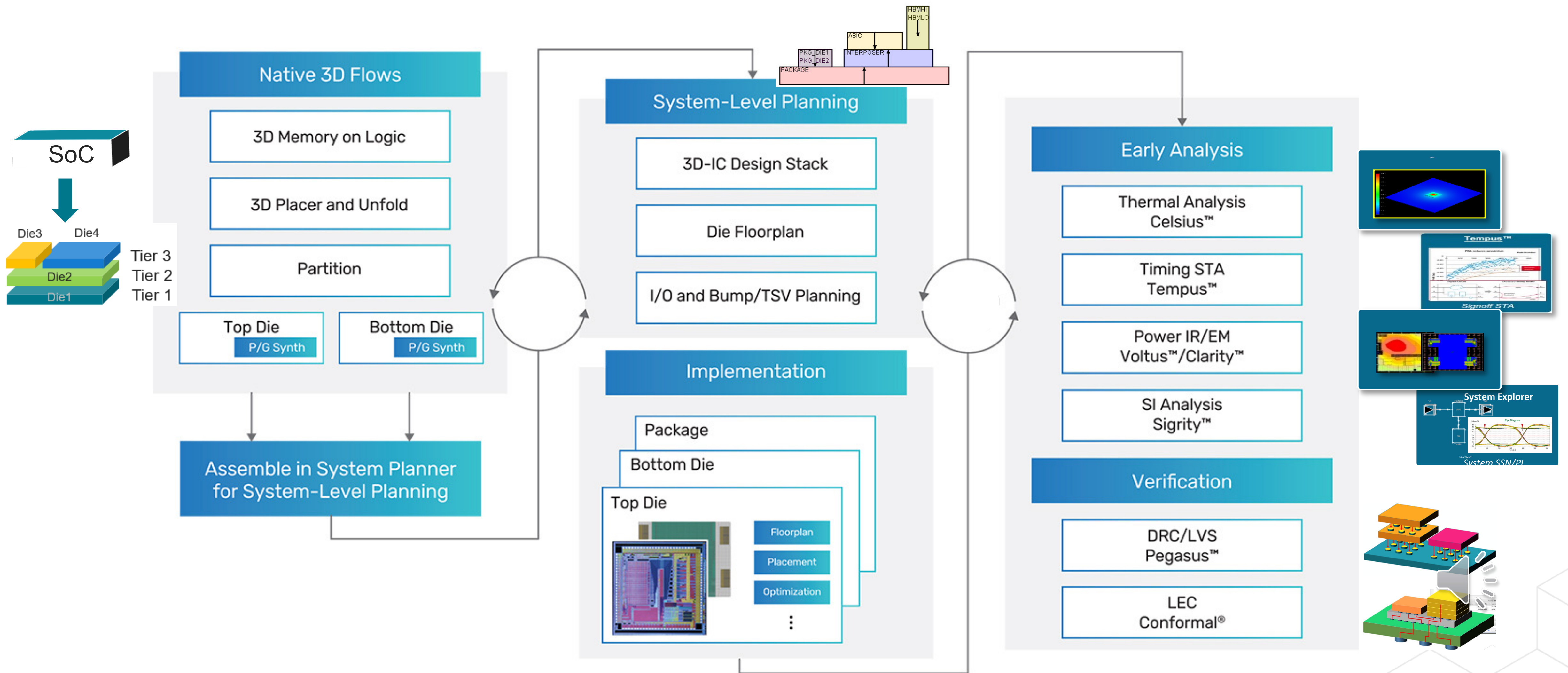
Overview 3D-IC Multi-Chiplet System Design flow



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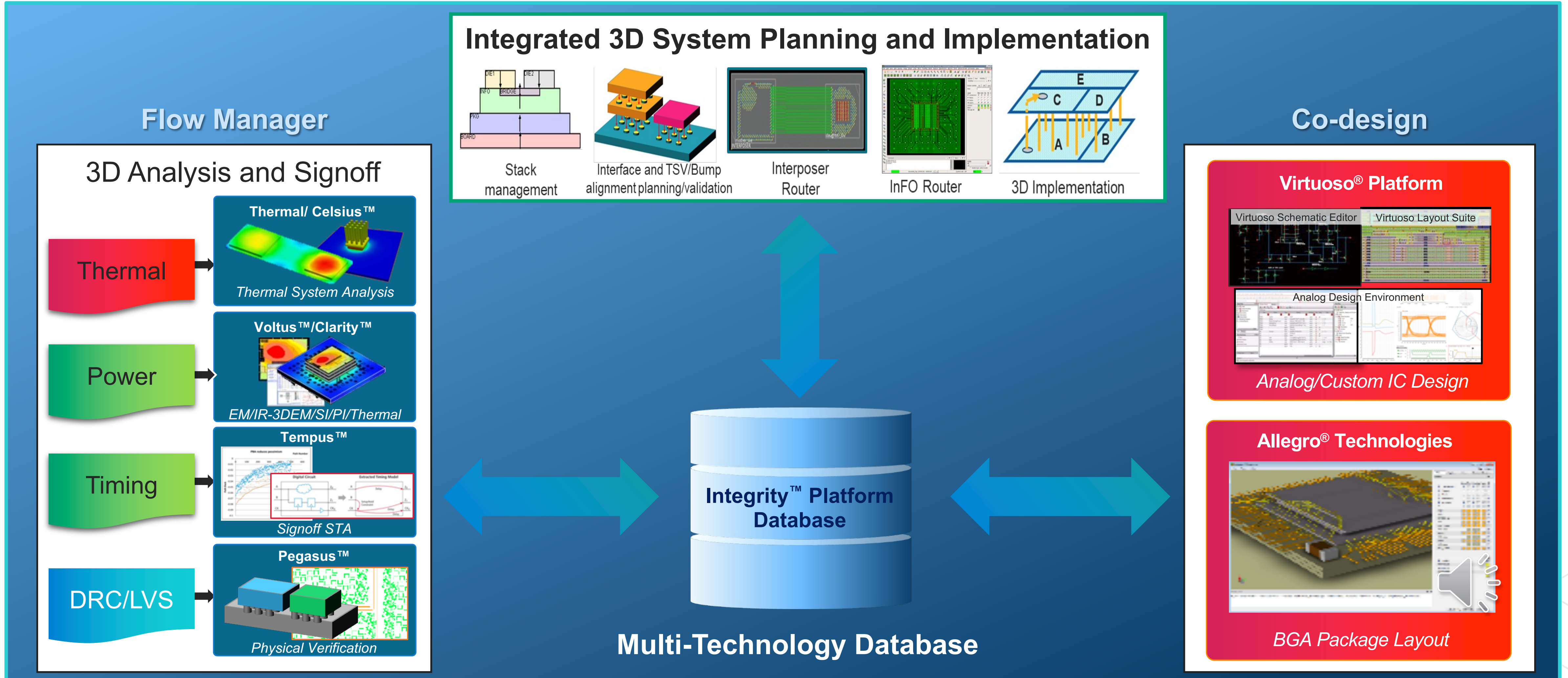
Unified 3D-IC Multi-Chiplet System Design Solution "Integrity 3D-IC"

Industry's first integrated, high-capacity 3D-IC platform that enables 3D design planning, implementation and system analysis in a single, unified cockpit



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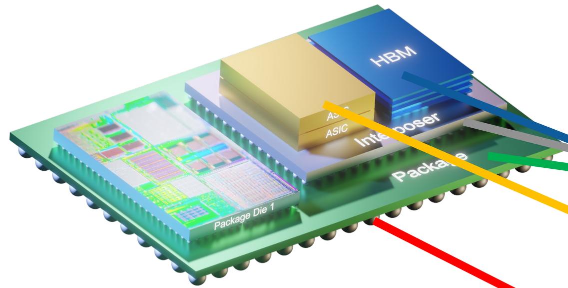
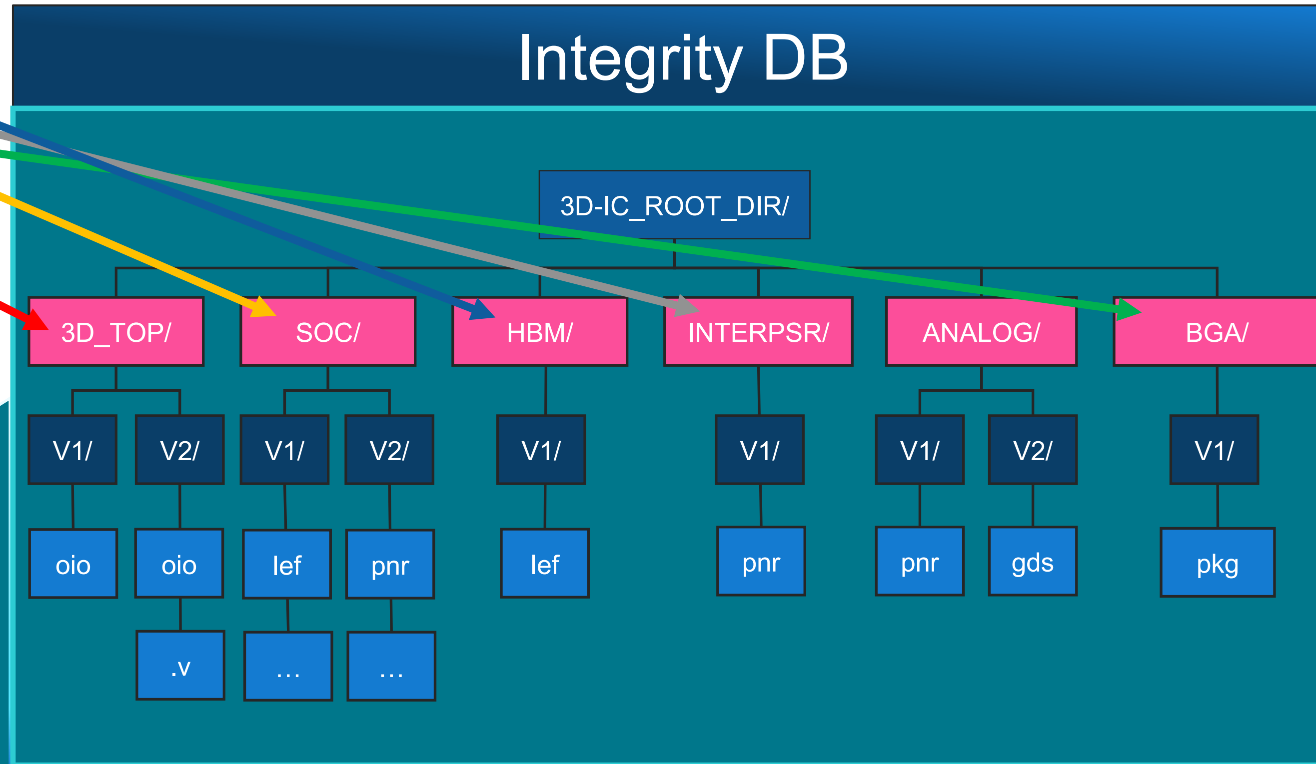
Platform Database for 3D Heterogeneous Integration

Database innovation: Can handle multiple technology nodes





- Netlist
- DEF or OpenAccess
- mcm
- SDC
- PDK
- MMMC (view definition)
- FlexILM
- ILM
- LEF
- Parasitic
- Metal Fill (physical context)
- SPEF
- Thermal map
- Timing context
- Boundary model
- GDS
- …

Hierarchical, Multi-Technology, Multi-Level, Multi-Model On-Demand DB

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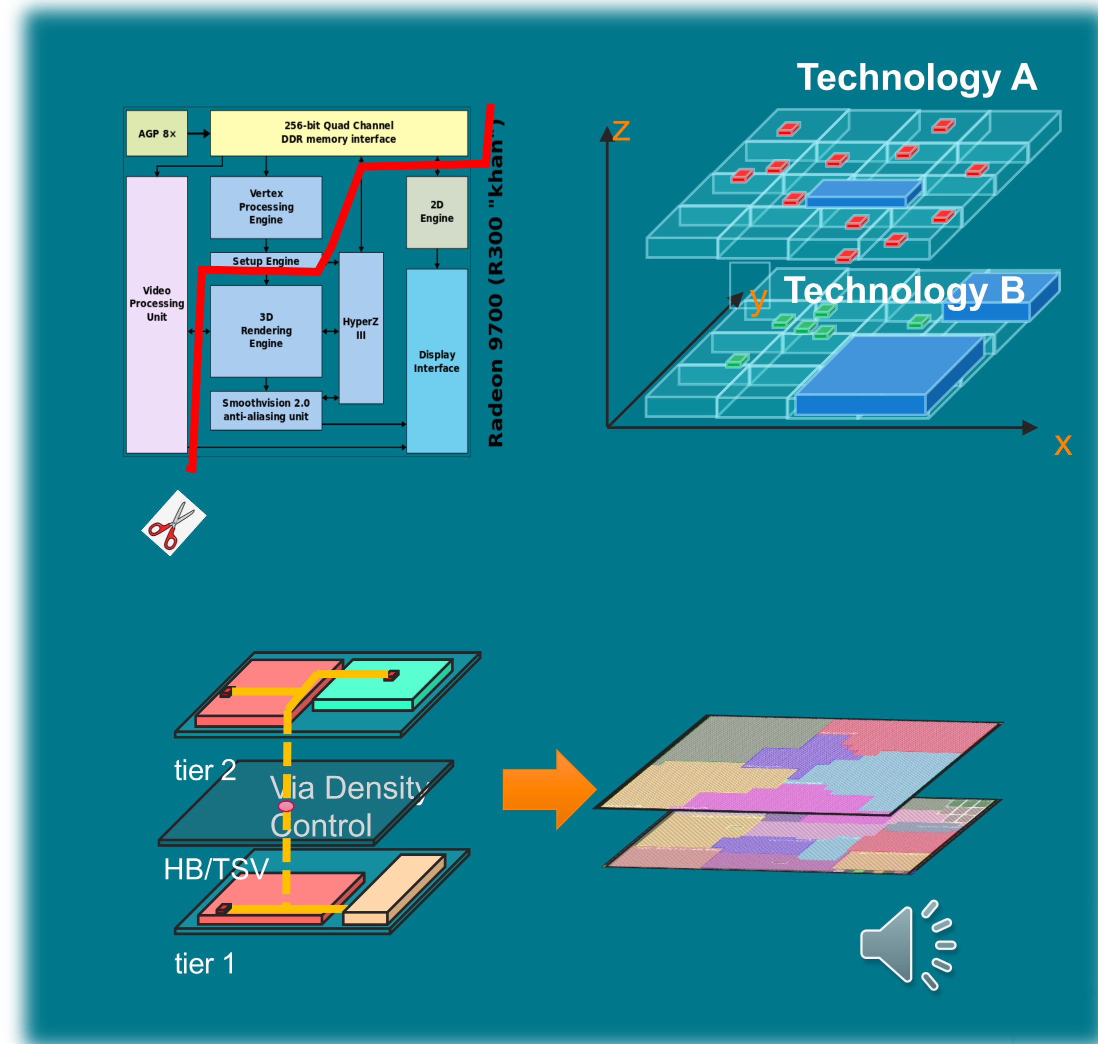
3D Native Partitioning and Floorplan Synthesis (3D-EFS)

- 3D IC block-level partitioning and placement.
- Considers 3D wire length, number of I/O ports/bumps/TSVs, different process node and timing
- Allow user to assign the die ID for hierarchical modules
- Per-die timing budgeting and bump assignment to enable per-die P&R or convert to pseudo 3D



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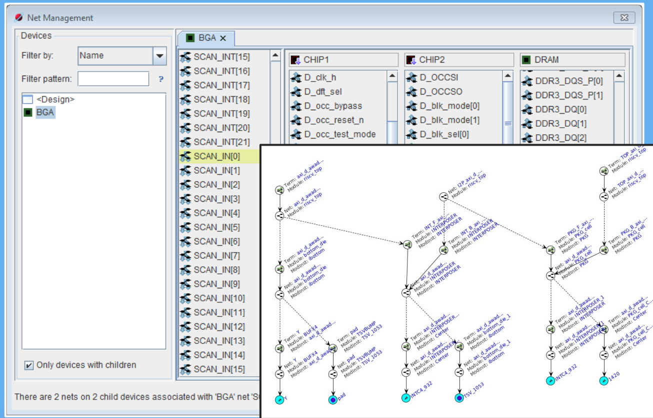
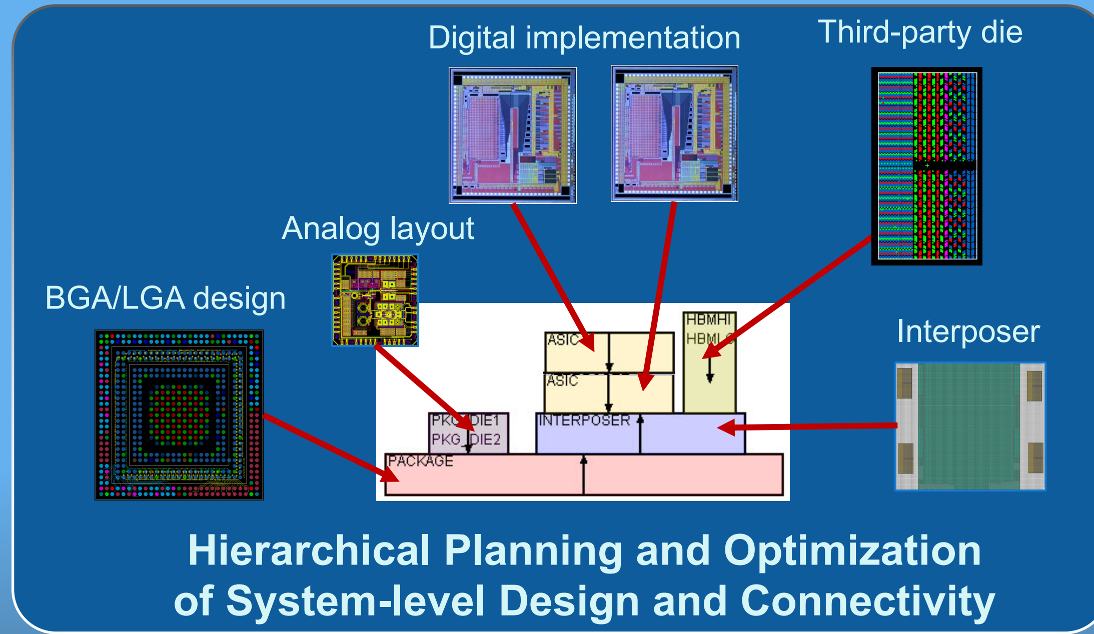
System Planning Capability

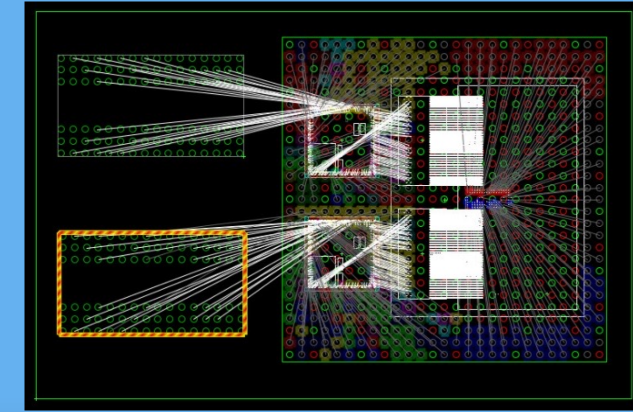
Heterogeneous Integration Management & Optimization



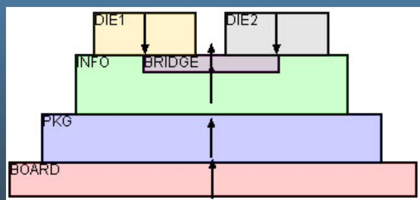
Chip(let)-chip(let)-package-board signal-mapping



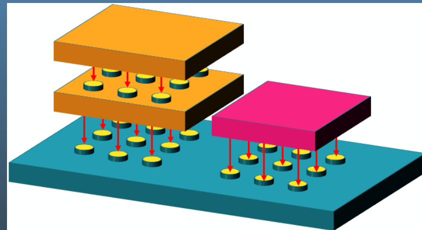
Hierarchical Planning and Optimization of System-level Design and Connectivity



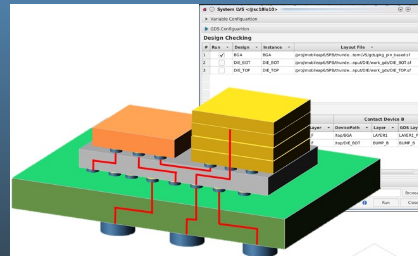
Complete system-level view



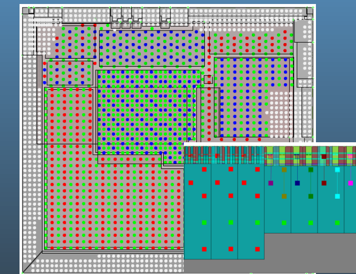
Stack management



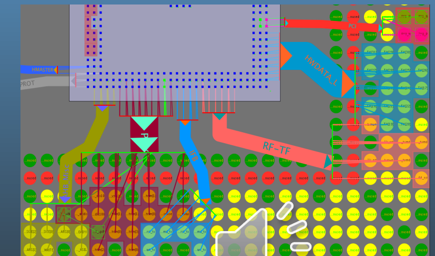
Interface alignment validation



System-level connectivity verification



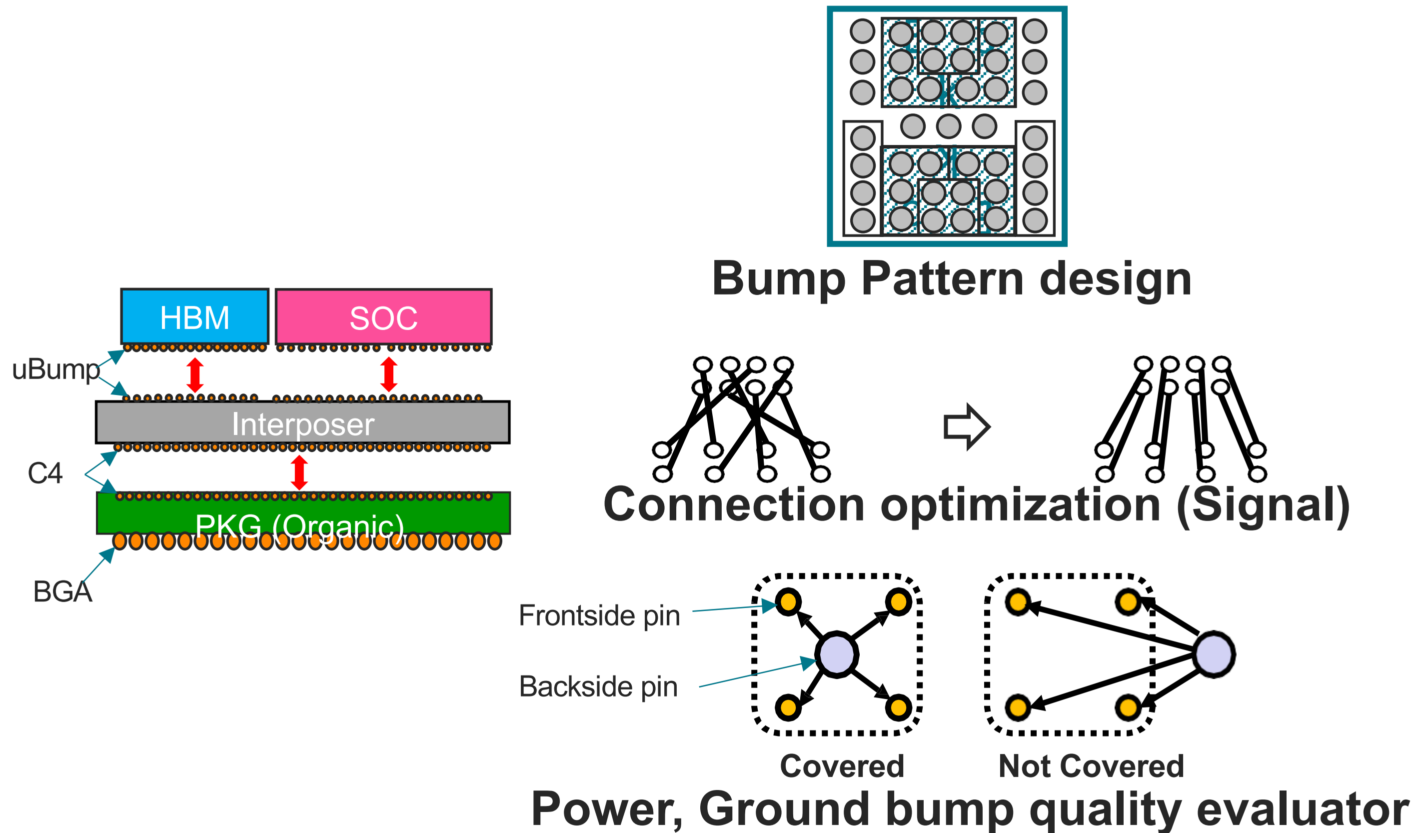
Advanced bump/TSV planning

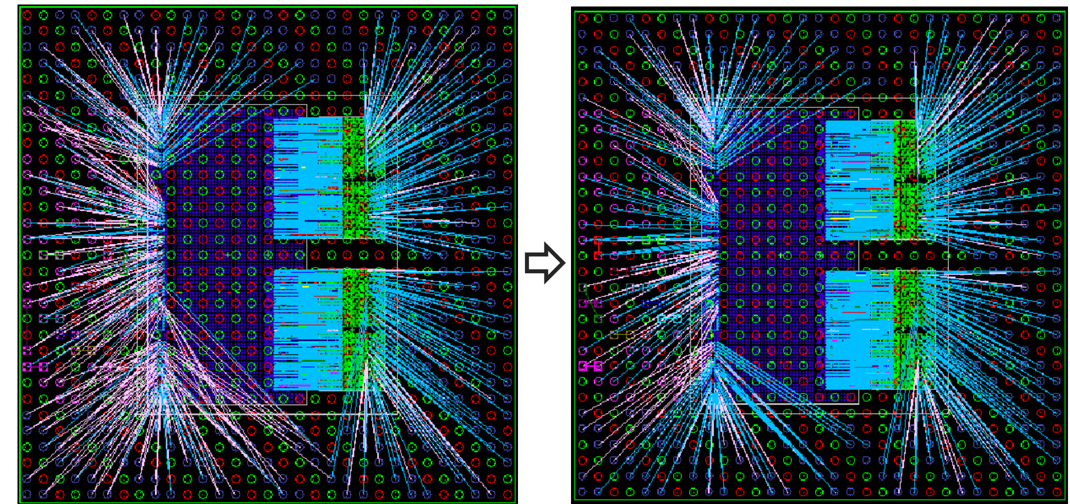


Bundle/bus-driven pin optimization

Global Bump Planning, Optimization and Evaluation

- Bump/TSV/Ball assignment impacts 3D-IC System PPA.
- Connection optimization driven bump assignment improves routing congestion and wirelength.





Improve routing congestion compared with tapeoute design

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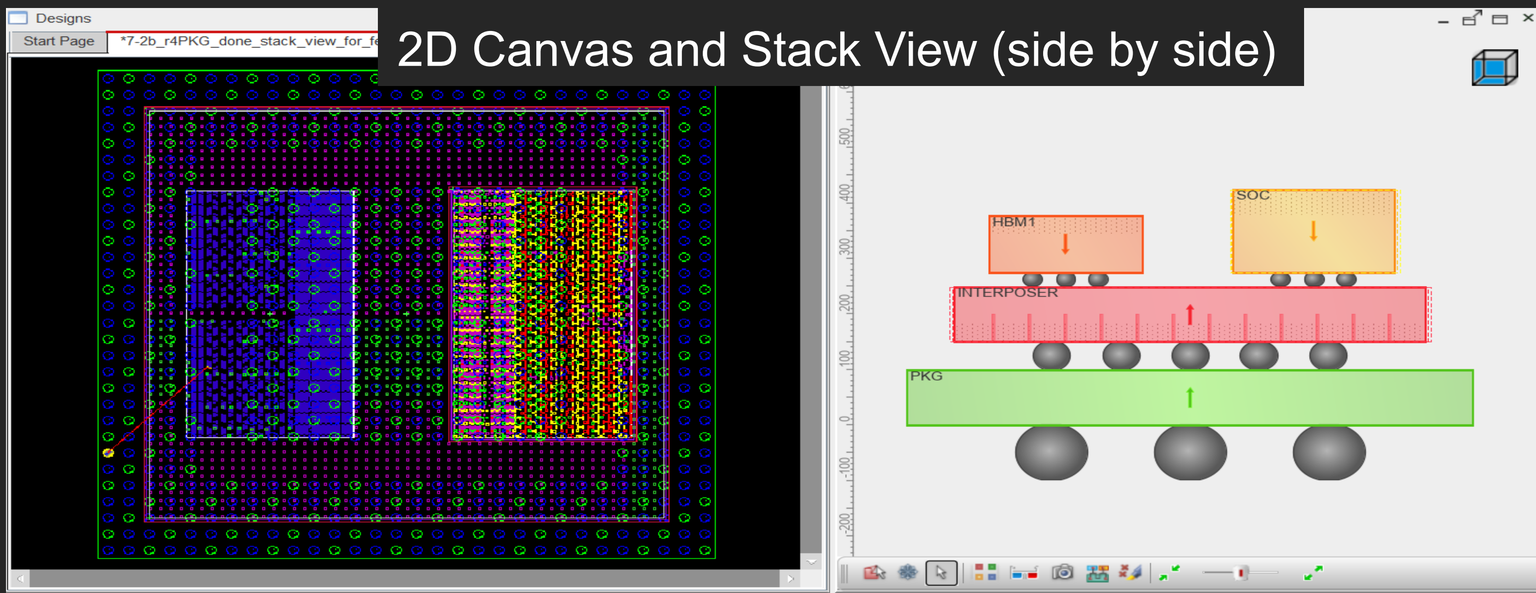
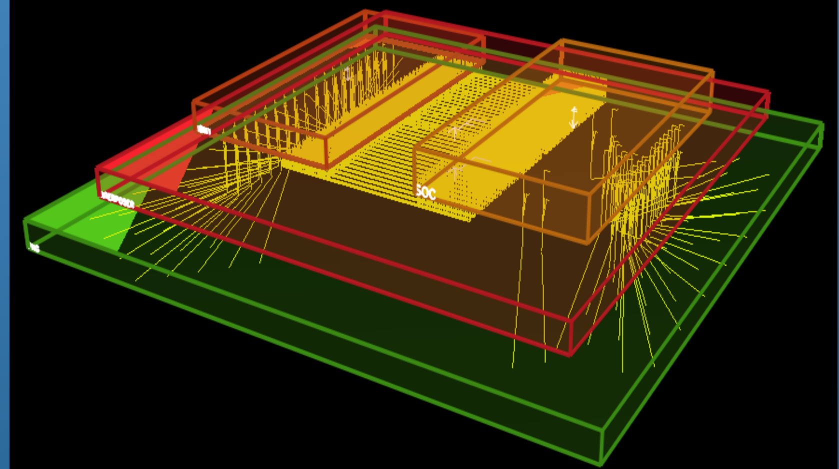
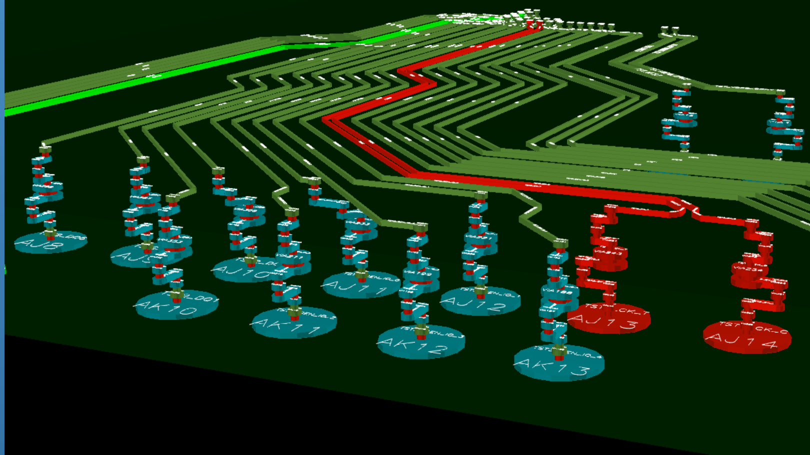
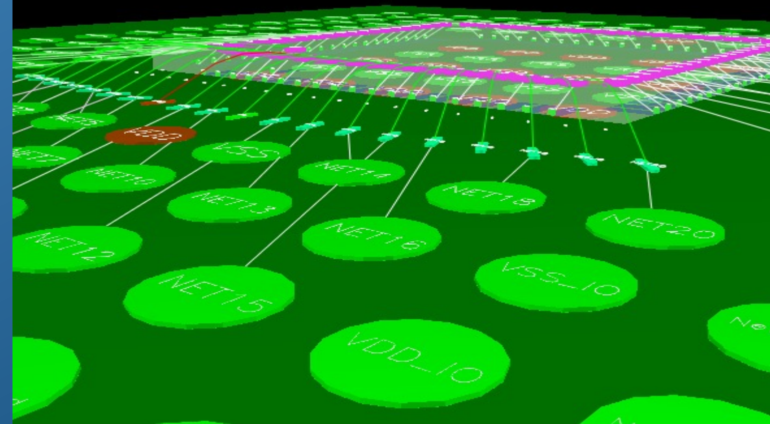
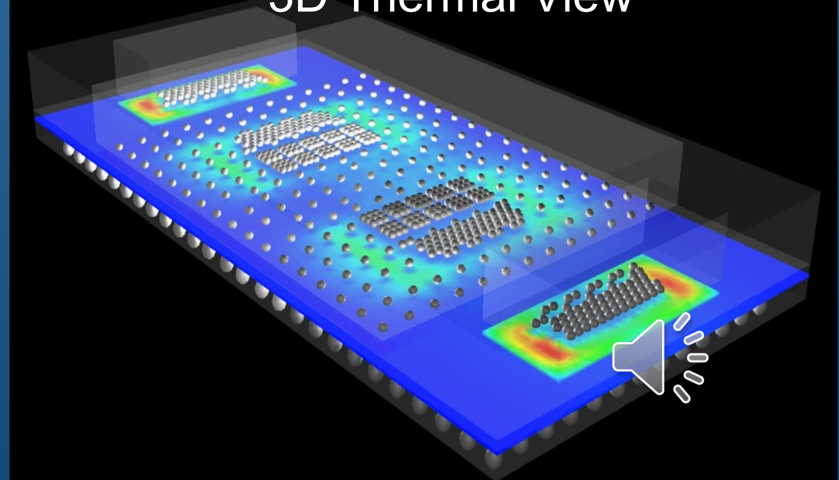
Multi-Chiplet Display in 2D/3D Viewing











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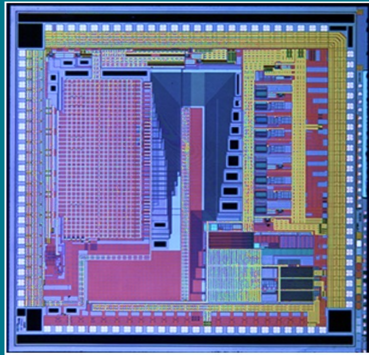
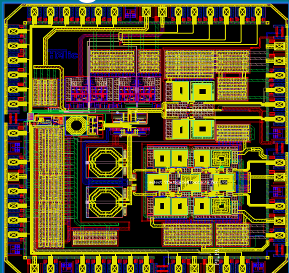
Implementation Technologies with Digital, Analog, RDL Routers

- Each type of design has different design constraints and routing style.
- Co-design integration with Digital, Analog, RDL routers.

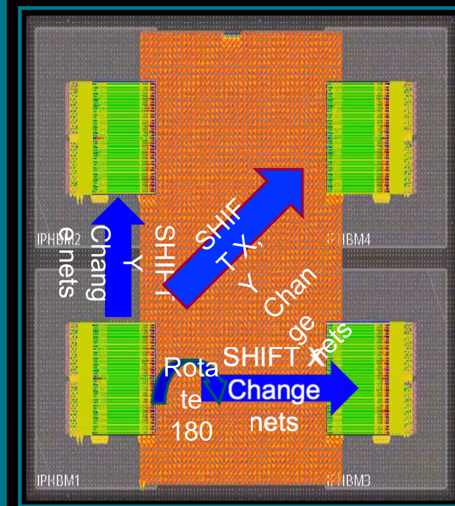
Digital Die Routing

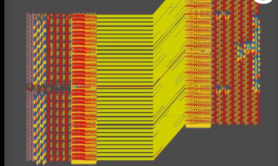


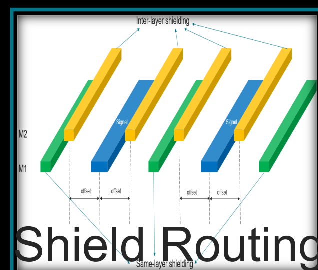
Analog Die Routing



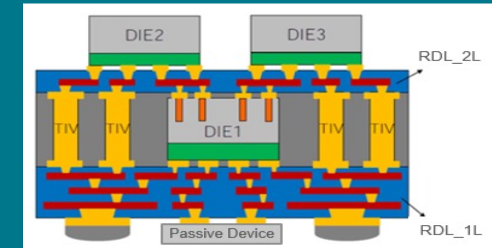
Si-Interposer Routing

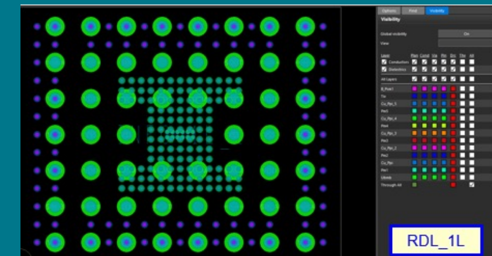


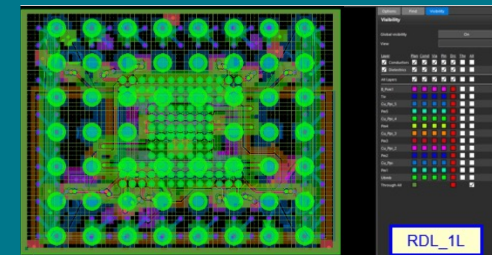




RDL Interposer/Package Routing







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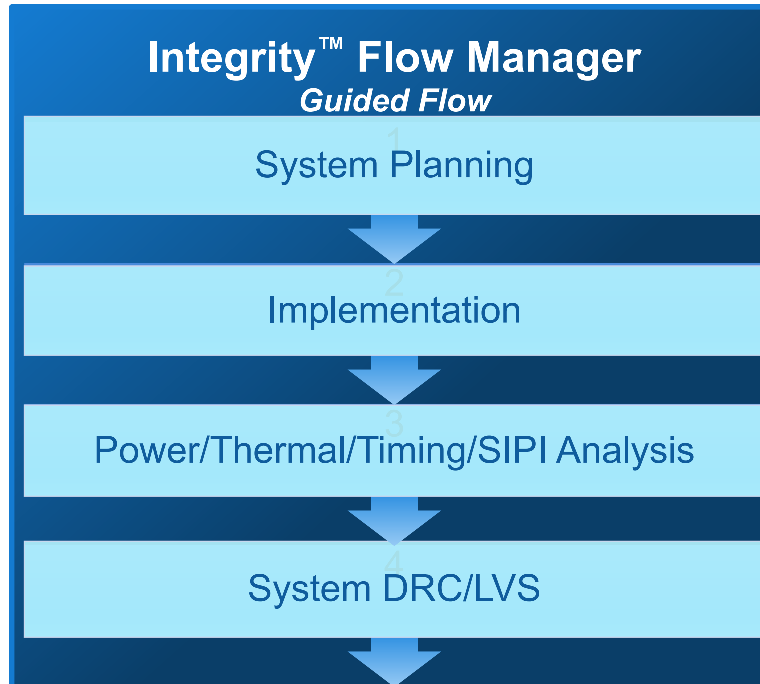
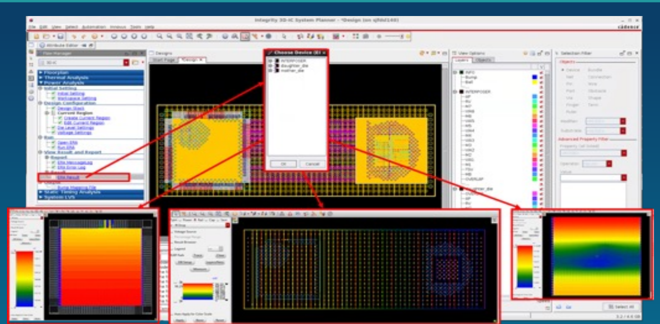
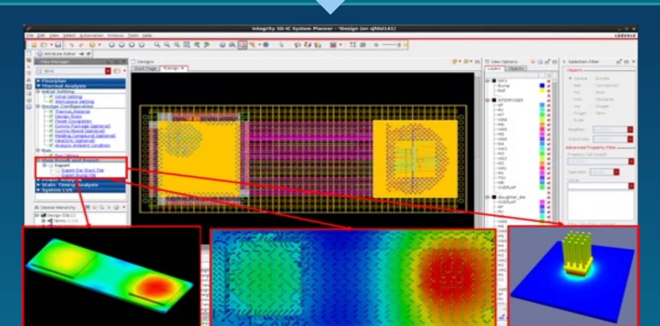
Early System-Level Analysis and Signoff Flow



Voltus™/Celsius™
Early Rail (Power and Thermal) Analysis





System-Level Power and Thermal Analysis

Pegasus™
Physical Verification (DRC/LVS)

Inter-Die Connectivity Checking

Tempus™
Timing Analysis

STA
Die1
Coupling Block
Die2
Model Extraction (Quantus™)
Die1 SPEF
Die1-Die2 SPEF
Die2 SPEF
Tempus
Signoff STA

3D Analysis with RAID Technology

Clarity/Sigrity™
Signal/Power Integrity Analysis

subckt
3D FEM
Eye Diagram

System-Level SIPI Analysis

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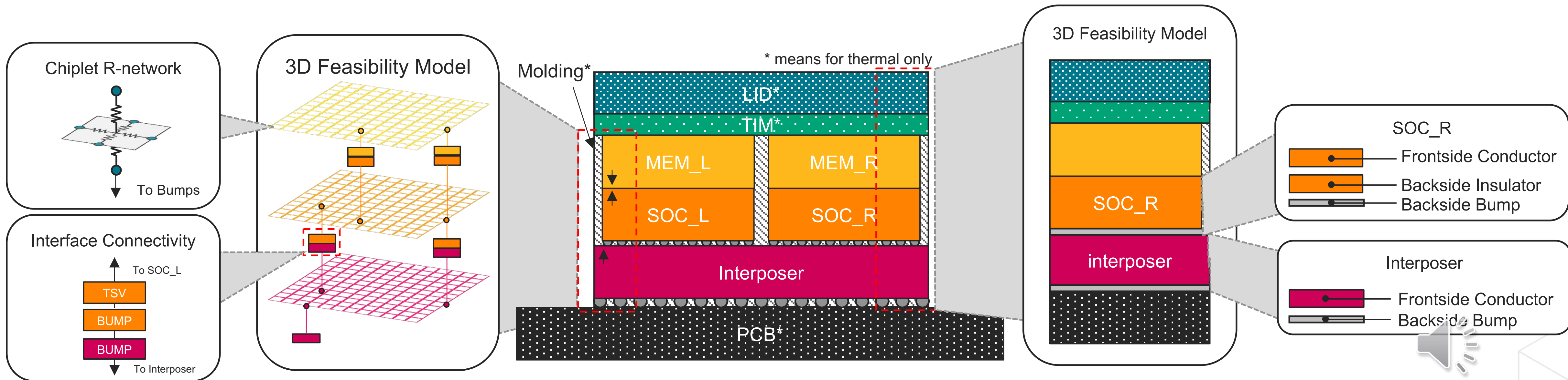
IR/Thermal Early Feasibility Analysis

IR-drop

- Model the 3D design as a resistance network
  - Abstract a chiplet's metal stack as a grided 2D resistance network
  - Represent bumps/TSVs as resistors
  - Chiplets are connected through bumps and TSVs

Thermal

- Model the 3D design as a layer-based stacking
  - Condense chiplets into conductor or insulator layers
  - Represent bump as a layer affixed to chiplets
  - Model LID/TIM/PCB/Molding as a single structure of homogeneous properties



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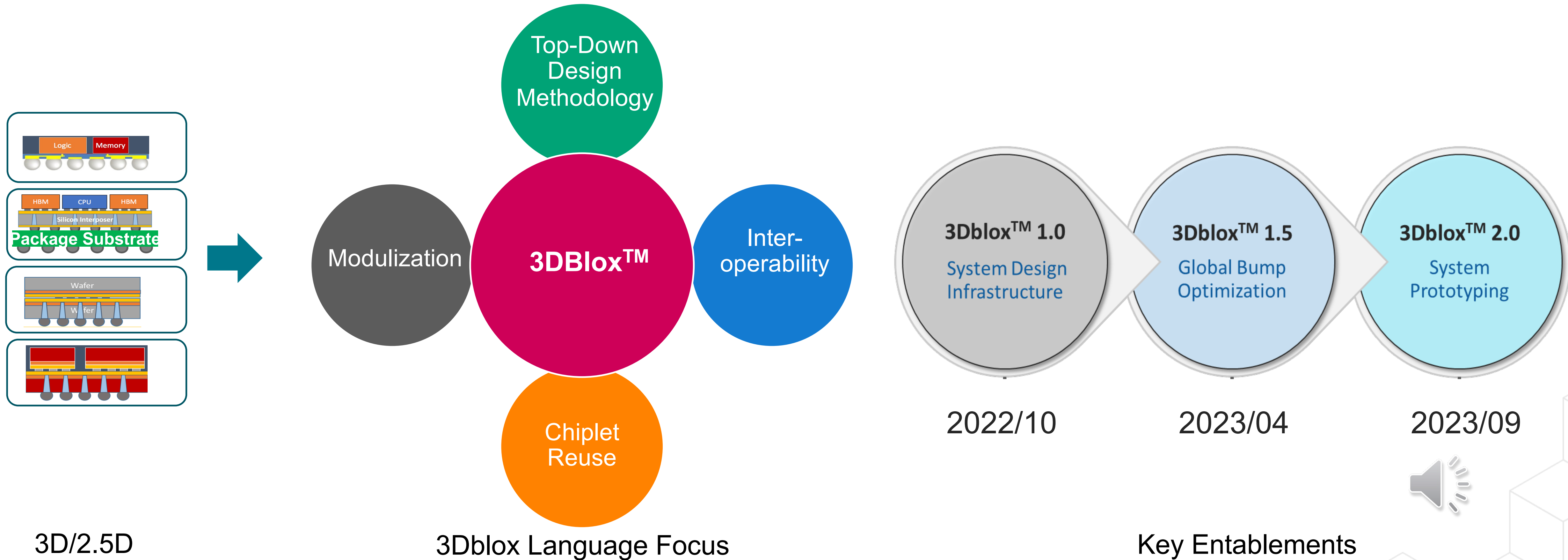
New 3D-IC Open Standard - 3Dblox™ (https://3dblox.org/)

- 3Dblox Standard aims to streamline the 3D-IC package solutions in Planning, Implementation and Signoff.



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Close partnership with TSMC on 3Dblox™

- Integrity 3D-IC platform offers full flow solution

Planning

Implementation

Signoff

3DFabric EDA Tool Certification Status

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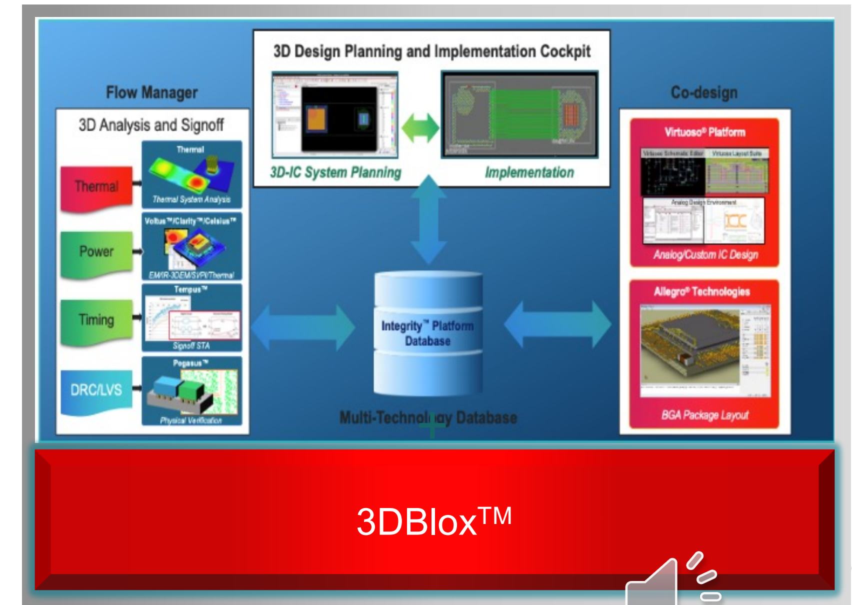
As of 1/31/2024

Design Solution		Ansys	Cadence	Siemens EDA	Synopsys
3Dblox™	System Prototyping and Reuse	●	●	●	●
	Auto Bump Synthesis		●		●
	Architecture Definition Language	●	●	●	●
Macro Lib	Design Macro		●		●
Implementation	APR		●		●
Physical Verification	DRC		●	●	●
	LVS		●	●	●
	Interface LVS		●	●	●
Electrical Verification	RCX		●	● (yellow)	●
	IR Drop Analysis	●	●		Ansys*
	Cross-die STA Complexity Reduction		●		●
Thermal	Static and Transient Analysis	●	●		Ansys*
DFT	Multi-chip Testing		●	●	●

[EDA Alliance - Taiwan Semiconductor Manufacturing Company Limited (tsmc.com)](tsmc.com)



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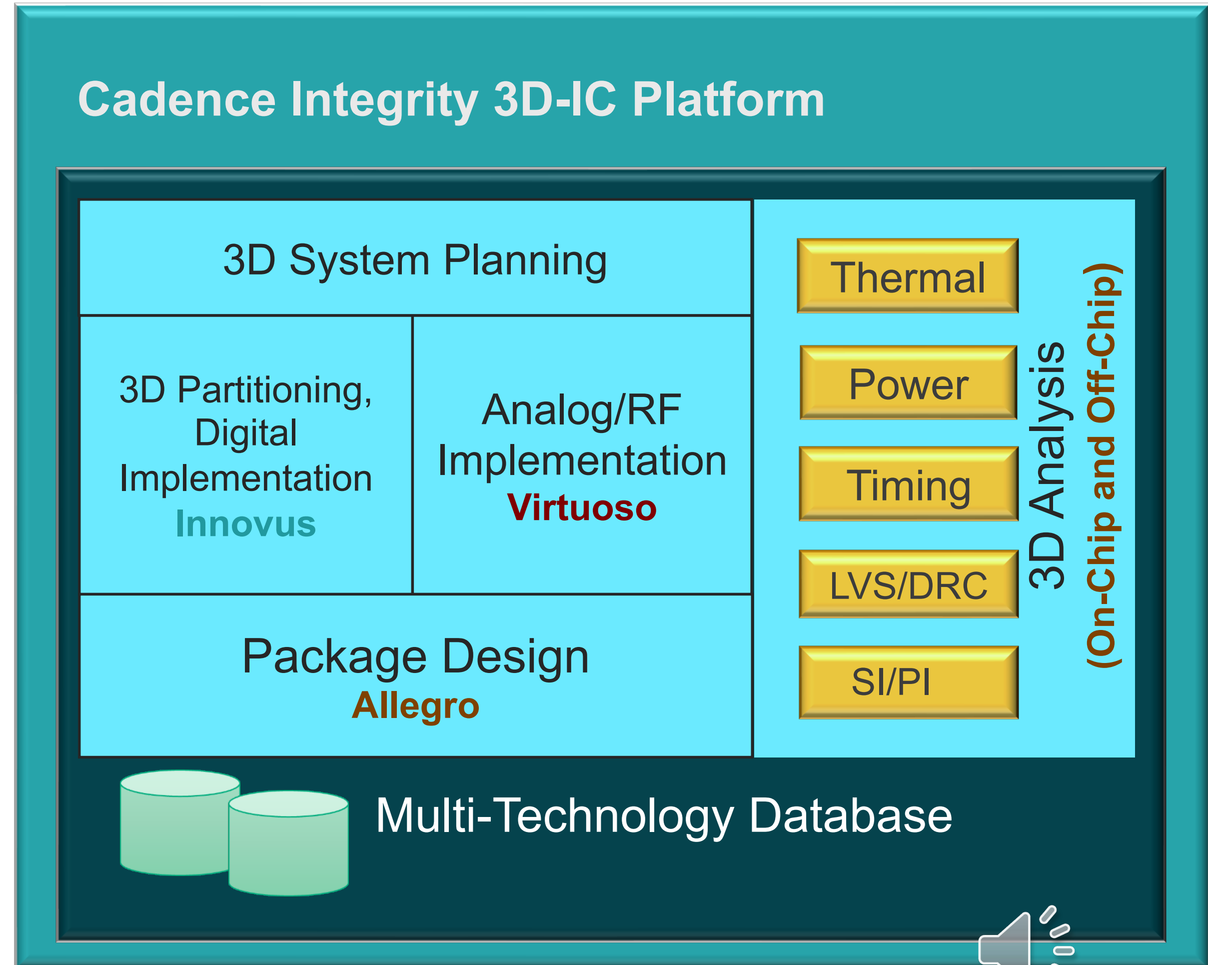
Summary – Unified 3D-IC Multi-Chiplet System Design Solution

- System PPAC is goal
- Heterogenous integration capability
- A common platform DB
- Full system level multi-physics analysis technology for Thermal, Power, SI/PI and Physical Verification
- Ecosystem with leading foundries



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