International Symposium on Physical Design

Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs

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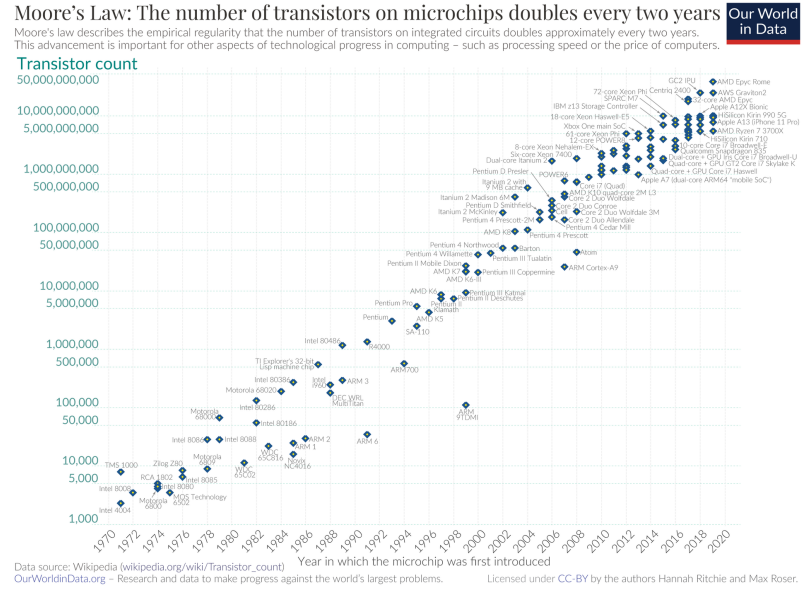
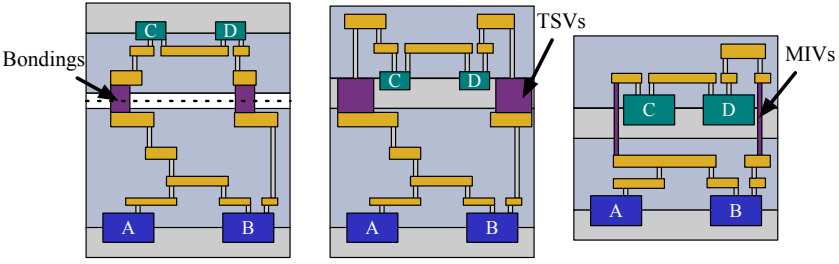
Outline

Why 3D IC?



Transistor Trend [Wikipedia]

Inter-die Connection



(a) F2F bondings (b) F2B with TSVs (c) F2B with MIVs

Connection	Cross-Silicon	Heterogeneous
Bonding	N	Y
TSV	Y	Y
MIV	Y	N

Bonding Terminal Planning

Problem Definition

Given a set of 3D nets $E = \{e_1, e_2, \cdots, e_n\}$, we need to determine the position of their bonding terminals to guarantee the signal path connection and expected post-route performance.

Challenges

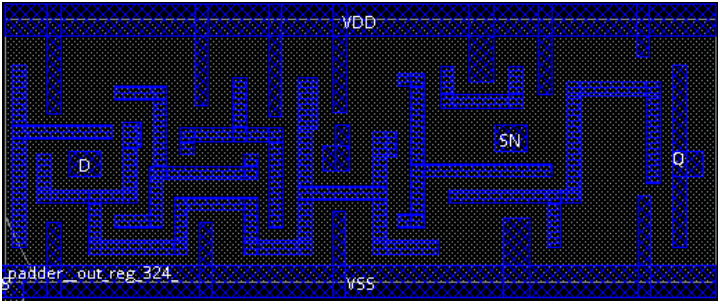
- Scaling Challenge.
- Post-route performance evaluation.
- Hard to handle multiple-to-one bonding terminals.

Challenge 1

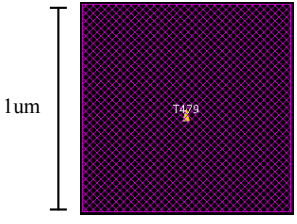
Scaling Challenge

Scaling Challenge

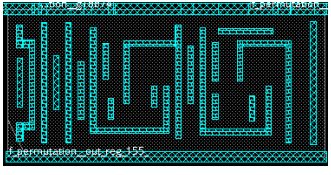
Nangate45



Bonding Terminal



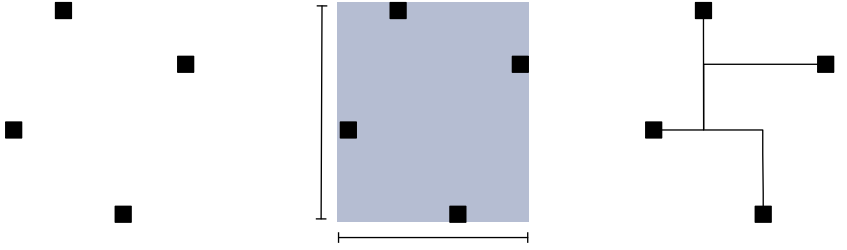
Nangate15



Challenge 2

Post-route Performance Evaluation

Post-route Wirelength Evaluation

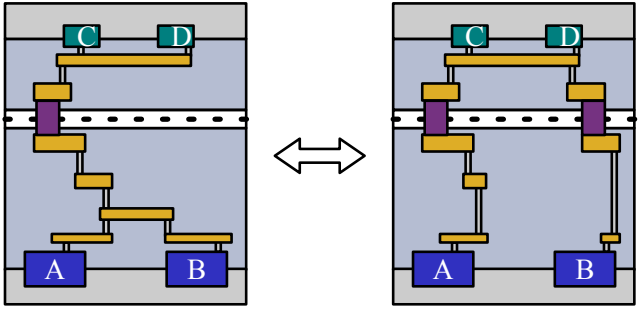


- As for the wirelength evaluation, the efficiency and accuracy cannot be guaranteed at the same time.
- Previous bonding terminal planning works focus on the HPWL optimization.

Challenge 3

Multiple-to-one Planning

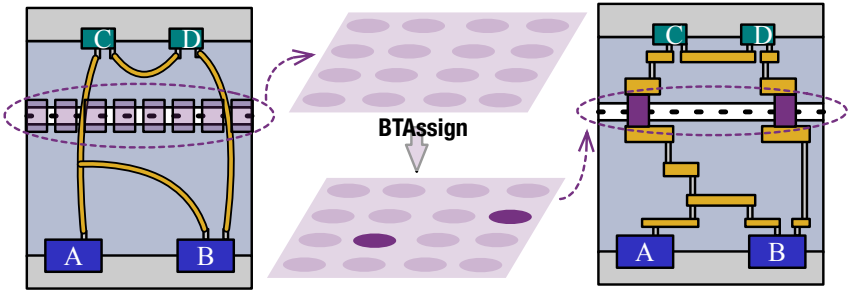
Multiple Matching



- Multiple matching benefits the wirelength but leads to NP-hard generalized assignment problem.

Bonding Terminal Assignment

Bonding Terminal Assignment



Routing-aware Bonding Terminal Assignment (BTAssign)

Given a set of 3D nets $E = \{e_1, e_2, \cdots, e_n\}$ and bonding terminals $T = \{t_1, t_2, \cdots, t_m\}$, our task is to find a surjection solution $f : T \to E$ for better post-route wirelength performance.

Formal Formulation

Generalized Assignment Formulation

$$
\begin{aligned}
\min \quad & \sum_{i=1}^{n} c(T_i), \\
\text{s.t.} \quad & C_i^l \leq \sum_{j=1}^{m} x_{ij} \leq C_i^u, \\
& \sum_{i=1}^{n} x_{ij} \leq 1, x_{ij} \in \{0,1\},
\end{aligned}
$$

- Candidate evenly-distributed bonding terminals $T = \{t_1, t_2, \cdots, t_m\}$.
- $t_j \sim e_i$: assignment. $T_i = \{t_j \in T \mid t_j \sim e_i\}$.
- $c(T_i)$: The pre-calculated routing cost of the assignment T_i.
- x_{ij}: $t_j \sim e_i$.
- C_i^l, C_i^u: pair constrain to limit the minimal/maximal number of matching bonding terminals for net e_i.

Memory Issue

- Consider the multi-to-one assignment in single round.
- Memory usage: $\sum_{i=1}^{n}(\sum_{z=C_i^l}^{C_i^u}\binom{m}{z})$

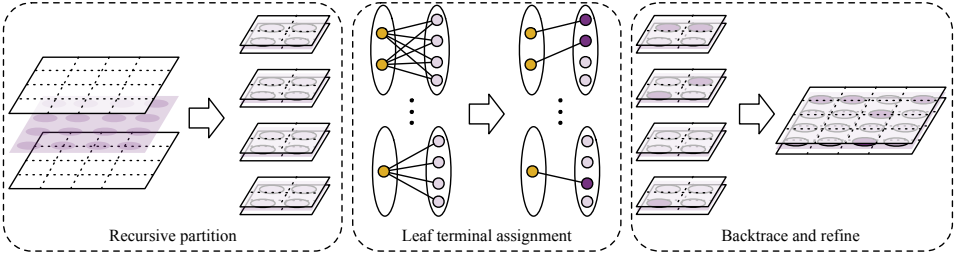
Incremental Assignment

- $x_{ij}^{(k-1)}$: accumulated assignment of previous $(k-1)$ iterations on $t_j \sim e_i$.
- $y_{ij}^{(k)}$: The kth assignment in current round.

k-th iteration

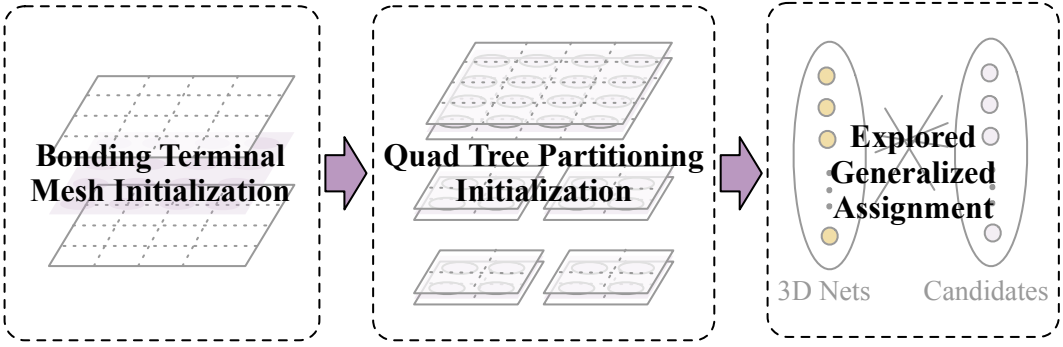
$$
\begin{aligned}
\min \quad & \sum_{i=1}^{n} c(T_i^{(k-1)} \cup \{t_j \mid y_{ij}^{(k)} = 1\}), \\
\text{s.t.} \quad & C_i^l \le \sum_{j=1}^{m} (x_{ij}^{(k-1)} + y_{ij}^{(k)}) \le C_i^u, \\
& \sum_{i=1}^{n} (x_{ij}^{(k-1)} + y_{ij}^{(k)}) \le 1, \\
& \sum_{j=1}^{m} y_{ij}^{(k)} \le 1, \\
& x_{ij}^{(k-1)} = \{0,1\}, \quad y_{ij}^{(k)} = \{0,1\}.
\end{aligned}
$$

Incremental Assignment - Partition & Backtrace

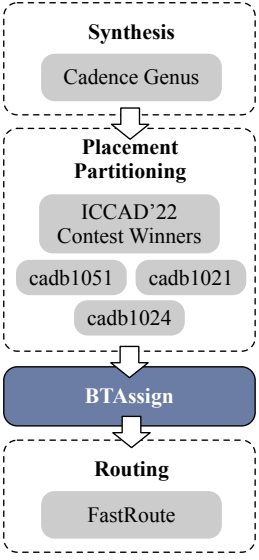


- During each iteration in the incremental assignment, only one-to-one assignment is considered.
- After each level of terminal assignment, the assigned terminals are masked to the next level as shown in the backtrace and refine stage.

BTAssign


Bonding Terminal
Mesh Initialization
Quad Tree Partitioning
Initialization
Explored
Generalized
Assignment
3D Nets
Candidates

Experimental Setting



Design	Die Area (um^2)	#Instances	#Nets
ethmac	136.023 × 134.4	23771	25151
jpegencode	419.753 × 268.8	173469	206046
mor1kx	176.7 × 268.8	57197	38198
or1200	659.562 × 403.2	326845	339318
sha3	76.688 × 134.4	22797	22870
tinyaes	358.629 × 268.8	326136	326728

Top Die (Nangate15)		Bottom Die (Nangate45)	
Name	track-pitch (μm)	Name	track-pitch (μm)
M1	0.064	BT	Blocked
MINT1	0.064	metal6	0.28
MINT2	0.064	metal5	0.28
MINT3	0.064	metal4	0.28
MINT4	0.064	metal3	0.14
MINT5	0.064	metal2	0.19
MINT6	0.064	metal1	0.14

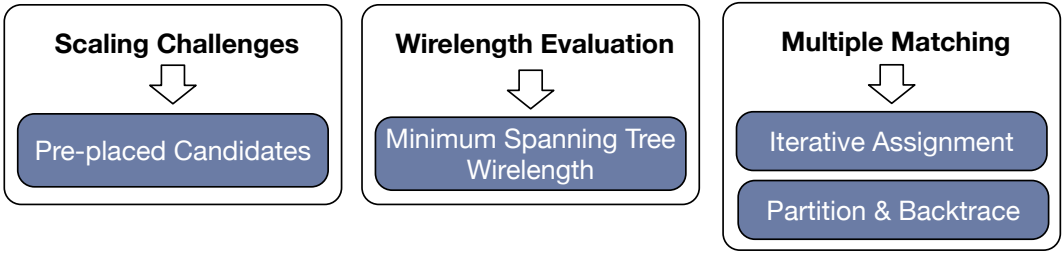
Results

Table: Experimental results on real-world open-source designs with three placers.

Design		FastRoute (Only HPWL)			w/ viaLegal[1] (HPWL & mesh)			w/ BTAssign		
		wl (μm)	# vias	rt-route (s)	wl (μm)	# vias	rt-all (s)	wl (μm)	# vias	rt-all (s)
cadb1024	ethmac	186.81	281883	5.99	189.10	283396	16.08	178.39	279194	11.41
	jpegencode	1437.11	3104739	48.08	1445.62	3109616	336.00	1394.64	3085740	119.66
	mor1kx	584.20	722950	24.64	586.80	726698	67.36	566.02	718771	44.29
	or1200	4559.60	3010540	114.60	4626.86	3062008	933.15	4397.76	2943050	373.29
	sha3	170.95	373479	7.98	171.73	373905	19.16	162.39	368041	19.42
	tinyaes	1934.92	6706891	87.36	1938.77	6710108	173.79	1910.34	6689367	125.39
cadb1021	ethmac	179.67	480896	12.70	179.88	481134	17.78	174.11	479606	10.11
	jpegencode	1319.08	4176215	52.23	1318.47	4176845	168.79	1257.06	4157969	95.29
	mor1kx	592.65	1174821	18.62	593.19	1175284	51.27	583.70	1171429	49.58
	or1200	4490.04	6979948	126.29	4490.04	6981306	655.61	4443.75	6967324	228.29
	sha3	161.81	469271	6.16	161.83	469205	10.72	158.37	468771	18.30
	tinyaes	1662.31	7629955	82.13	1661.34	7629853	204.48	1614.66	7610934	124.32
cadb1051	ethmac	172.87	241985	5.19	178.71	245379	20.64	167.90	240768	14.81
	jpegencode	1263.82	3080798	49.07	1283.94	3094259	297.98	1207.32	3058096	171.04
	mor1kx	605.03	573297	24.66	629.23	588623	143.99	599.65	576116	94.14
	or1200	3996.45	5163098	116.06	4026.81	5189696	1204.45	3959.78	5154037	372.53
	sha3	167.14	313924	7.55	173.77	317453	36.01	162.20	311601	69.91
	tinyaes	2093.40	6066197	95.60	2119.49	6091509	290.27	2044.98	6041593	214.06
Ratio		1.000	1.000	**1.000**	1.011	1.005	5.252	**0.972**	**0.995**	2.436

[1]S.Pentapati, and et al,"On legalization of die bonding bumps and pads for 3D ICs,", ISPD2023

How BTAssign[2] Solves



Future

- Better post-route evaluation should be proposed to enable more accurate and efficient optimization process.
- The bonding terminal position should not be fixed after single stage.

[2]Open source: https://github.com/Lusica1031/BTAssign