

# Challenges in Floorplanning and Macro Placement for Modern SoCs

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# Preliminary (at Advanced Nodes)

Wafer costs are extremely high

A modern SoC: Billions of transistors in various subsystems (e.g., CPU, GPU, NPU, ISP, modem, etc.)

- A subsystem can be further partitioned into circuit blocks (e.g., < 5M InstCnt)

(Chip-Top-Level) Floorplanning & (Block-Level) SRAM Macro Placement are critical

- **Floorplanning** involves determining the dimensions/locations of circuit blocks (which typically have rectilinear frames) by considering wire connections, port assignments, feedthrough nets, channels (white spaces), etc.
- **Macro Placement** involves determining the locations/orientations of SRAM macros (within a circuit block)
- **Macro Placement** outcomes can significantly affect PPA (e.g., Routing Congestion, Timing, Power, IR Drop, etc.)
- [Block-Level] Physical-Aware **Logic Synthesis**: Physical design info needed!

# Preliminary (Block-Level Flows)

## A sample/simplified **SYN**-flow (physical-aware) :

- Input: RTL Code (and a circuit block's Frame with placed Ports/Macros)
- Logic Synthesis (incl. Generic Netlist Generation & Technology Mapping)
- DFT Insertion
- Global/Detailed Cell Placement (Timing-Driven, Ideal Clock, with Global Routing)
- Gate-Level Netlist Generation (& PPA reporting)

## A sample/simplified **APR**-flow:

- Input: A gate-level Netlist and a rectilinear Frame (with placed Ports/Macros)
- SRAM Macro Placement (or adjustments of the placed macros)
- Power/Ground Mesh Generation & Power Switch Cell Placement
- Detailed Cell Placement (Timing-Driven, Pre-CTS)
- CTS
- Detailed Routing (Timing-Driven) (& PPA reporting)

# Some Digital Design Challenges at Advanced Nodes



Long runtimes for a block (< 5M InstCnt)

SYN-flow Runtime: 150 hrs (~6 days)

APR-flow Runtime: 450 hrs (~19 days)



AI/RL-based design flow parameter tuning can extend SYN/APR-flow runtimes and can require more iterations



Auto Macro Placement results usually cannot be used directly

This may hinder the automatic RTL-to-GDSII flow (while using the AI/RL-based tuning)



Many engineers are needed

e.g., for running SYN/APR jobs, analyzing PPA results, fixing congestion/timing/IR-drop/DRC issues, etc.



Redesign iterations

(Modified) RTL Code → Floorplanning (incl. Resizing Blocks) → Macro Placement → P&R with PPA results → Floorplanning → .....

# Conclusion

High-Quality Floorplanning & Macro Placements are critical in the design of modern SoCs.

Floorplanning & Macro Placements challenges encountered in the industry, and the obstacles preventing complete automation of these processes need to be re-examined.

With ongoing advancements in EDA/AI/ML, we anticipate a substantial improvement and/or potential automation in the iterative aspects of these design processes.

Advancements in EDA/AI/ML technologies will not only boost engineers' productivity but also improve the overall QoR (Quality of Results) in chip designs.

