# Novel Airgap Insertion and Layer Reassignment for Timing Optimization Guided by Slack Dependency

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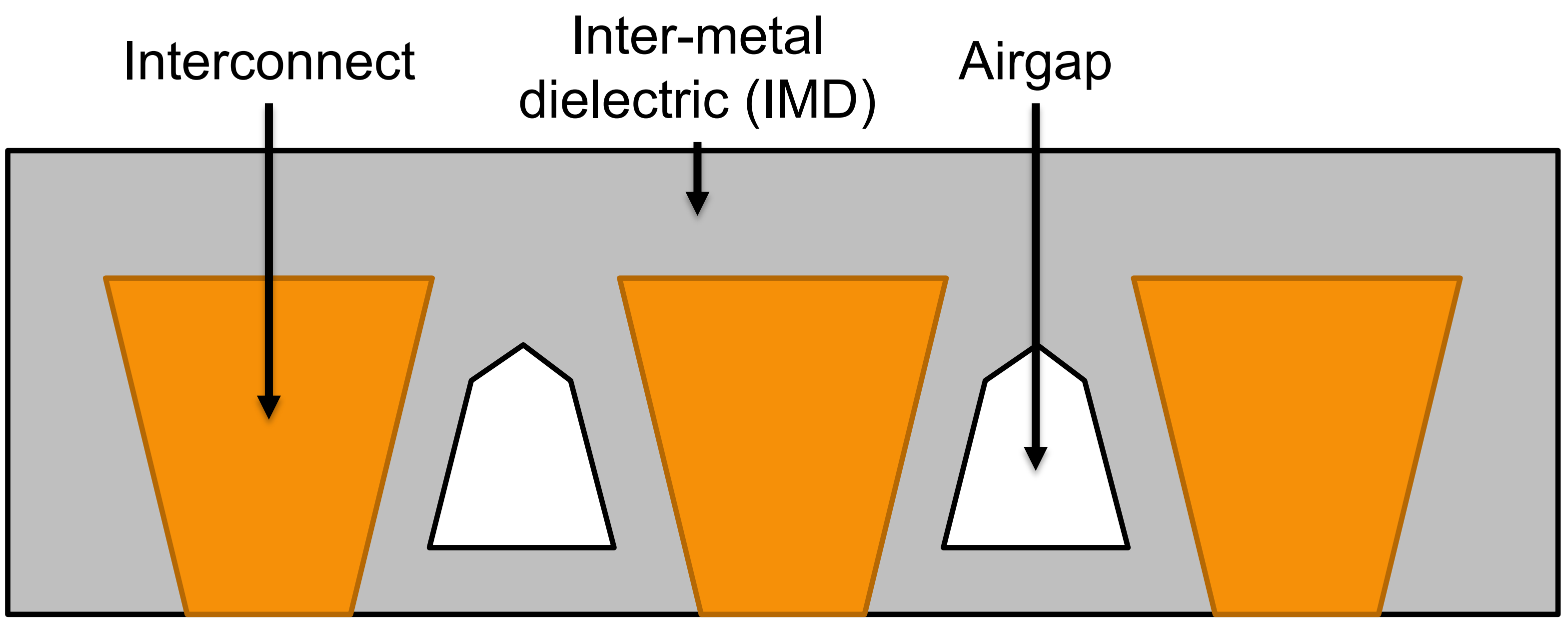
# Outline

- Introduction
- Slack Dependency Graph
- Airgap-Wire Optimization
- Experimental Results
- Conclusion

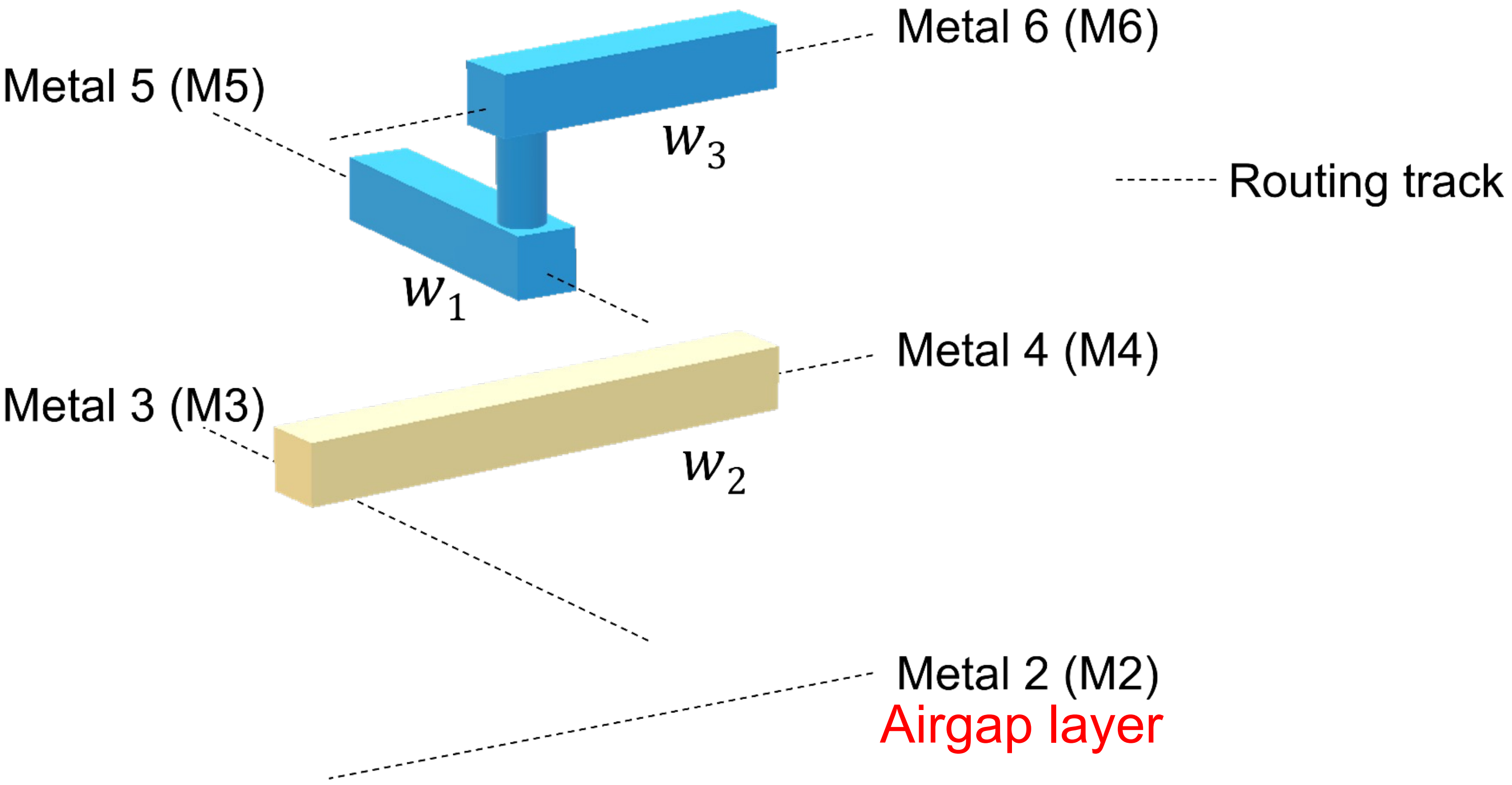
# Introduction - Airgap

- What is Airgap?
  - Replace solid low-k dielectrics between interconnects with air-filled or vacuum pockets
  - Lower the inter-metal dielectric (IMD) permittivity → lower line-to-line capacitance



# Introduction - Airgap

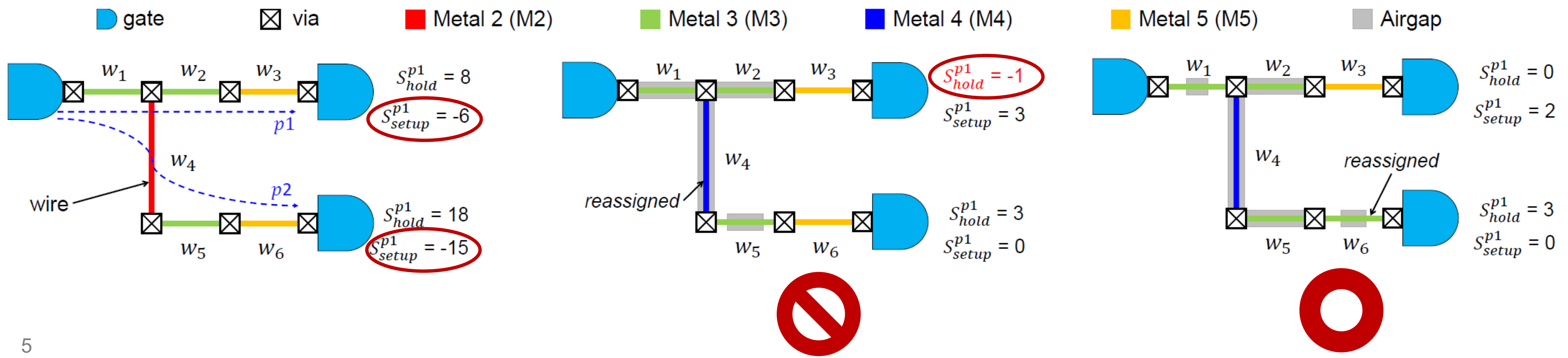
- Benefits of Airgap
  - Reduced line-to-line capacitance
  - Reduced interconnect delay, ~20% reduction
- Limitations of Airgap
  - Manufacturing cost
    → few airgap layers
  - Requires layer reassignment



# Introduction – Problem Formulation

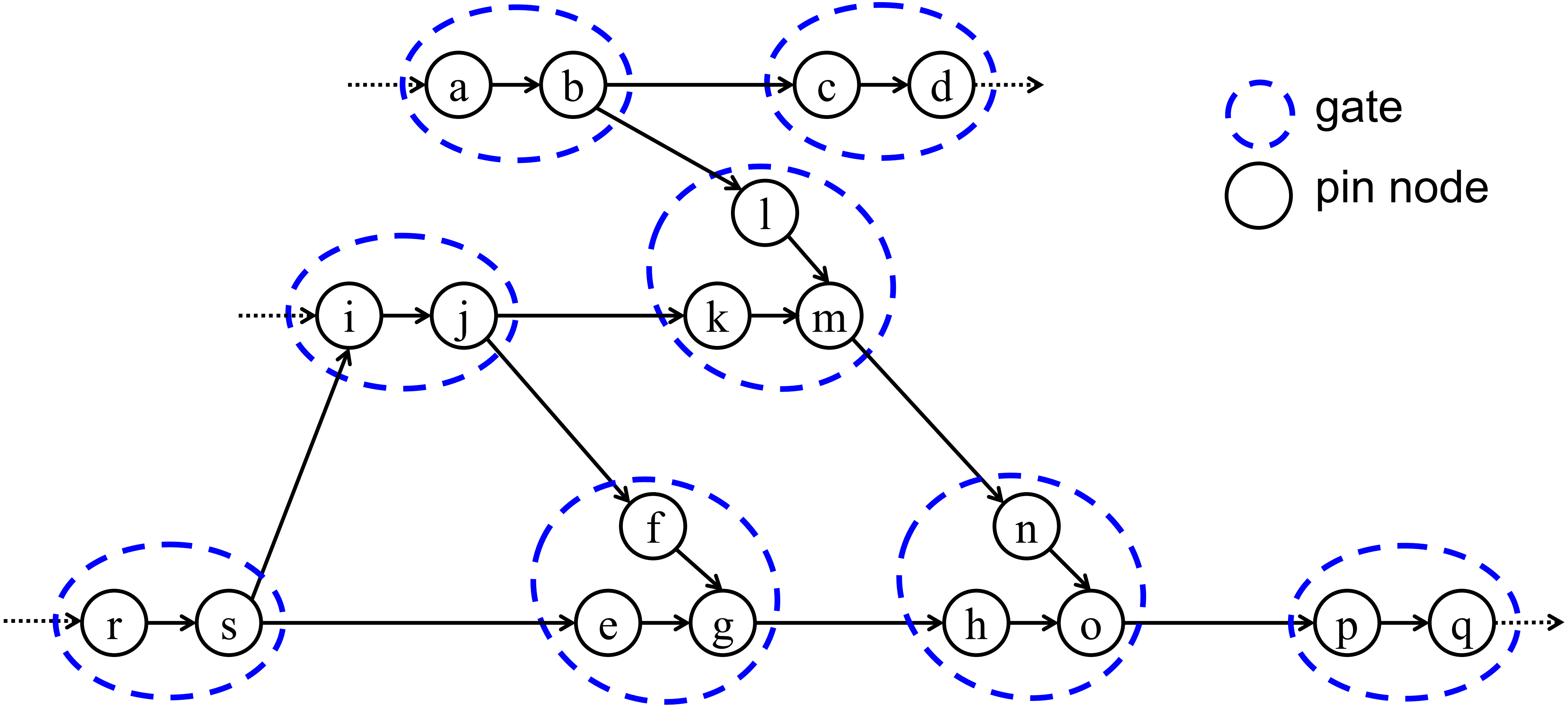
- Objective: timing optimization
  - Given: routed design
  - Optimize: total negative slack (TNS)
  - Constraints: legal airgap assignment and no hold time violations

- The shortened interconnect delay is beneficial to setup timing but harmful to hold timing.



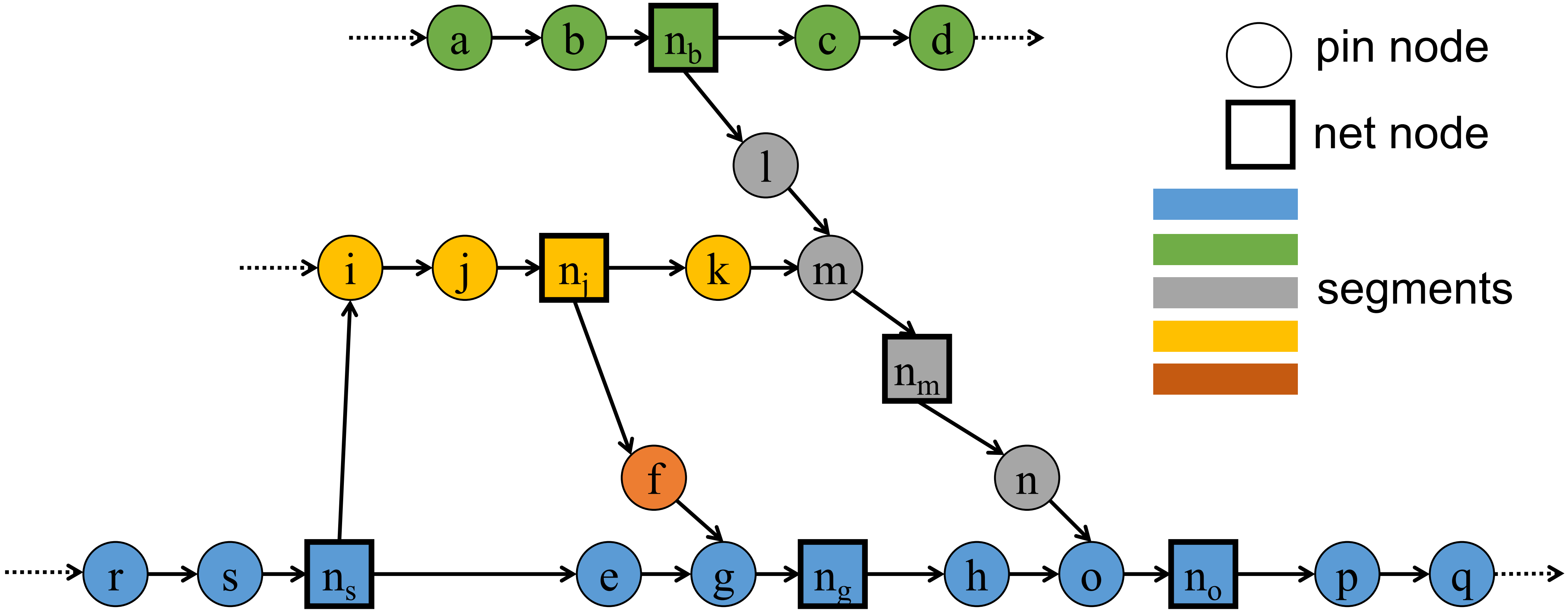
# Slack Dependency Graph (SDG)

- Conventional circuit graph



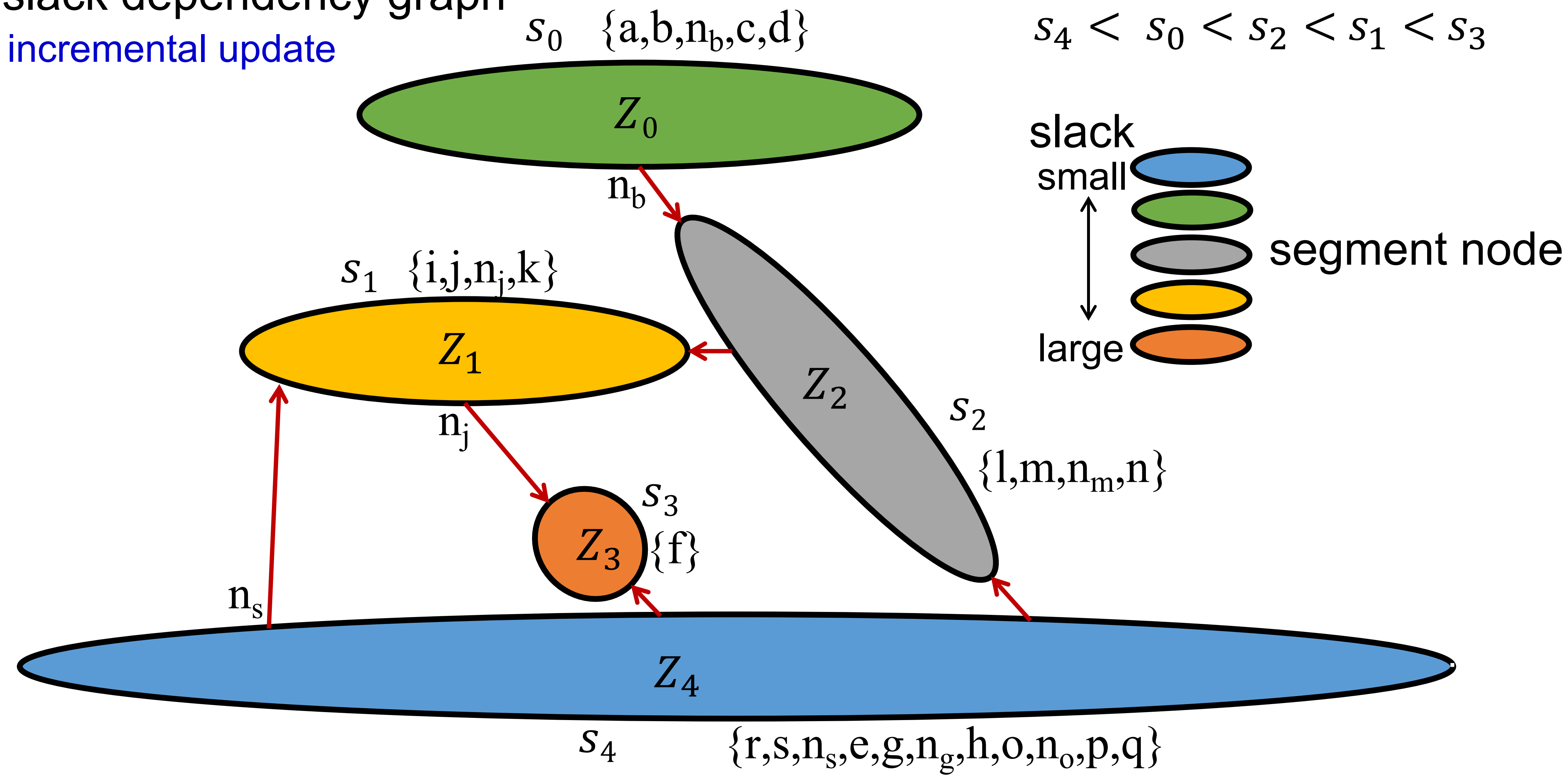
# Slack Dependency Graph (SDG)

- Add a net node to represent a net
  - Our optimization is performed on a wire belonging to a particular net



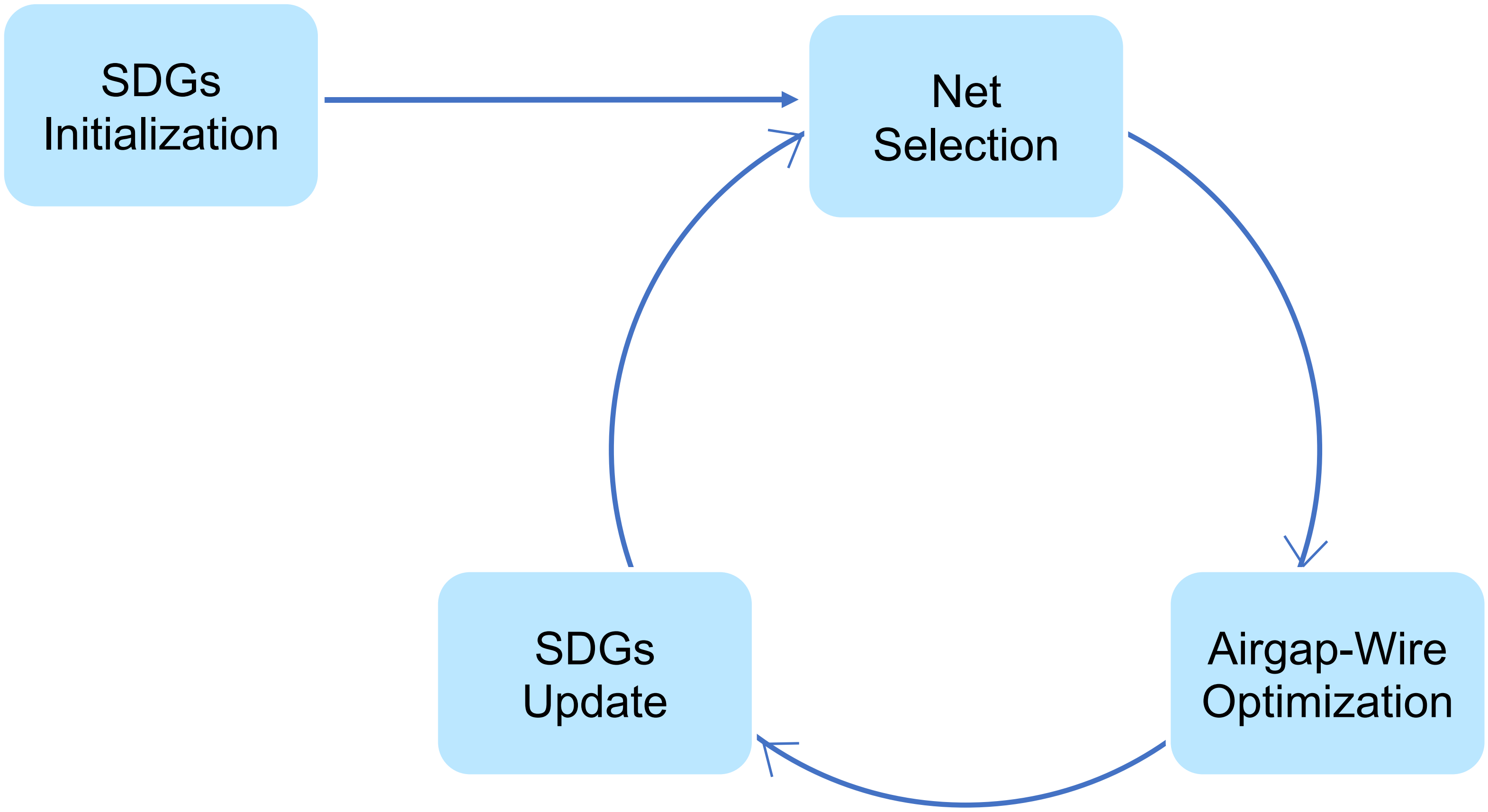
# Slack Dependency Graph (SDG)

- Final slack dependency graph
  - Fast incremental update



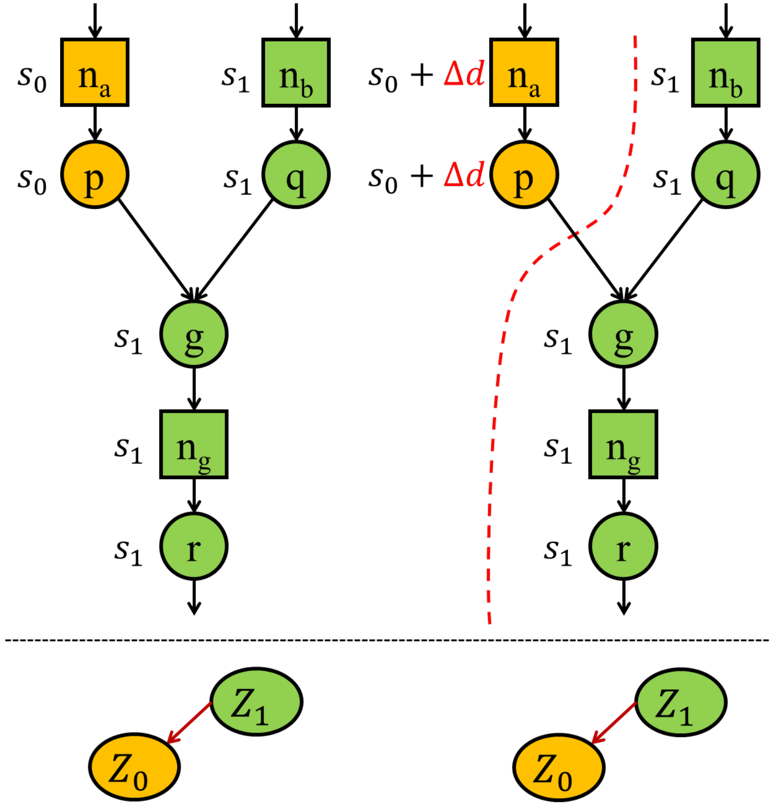
# Airgap-Wire Optimization

- Flow overview

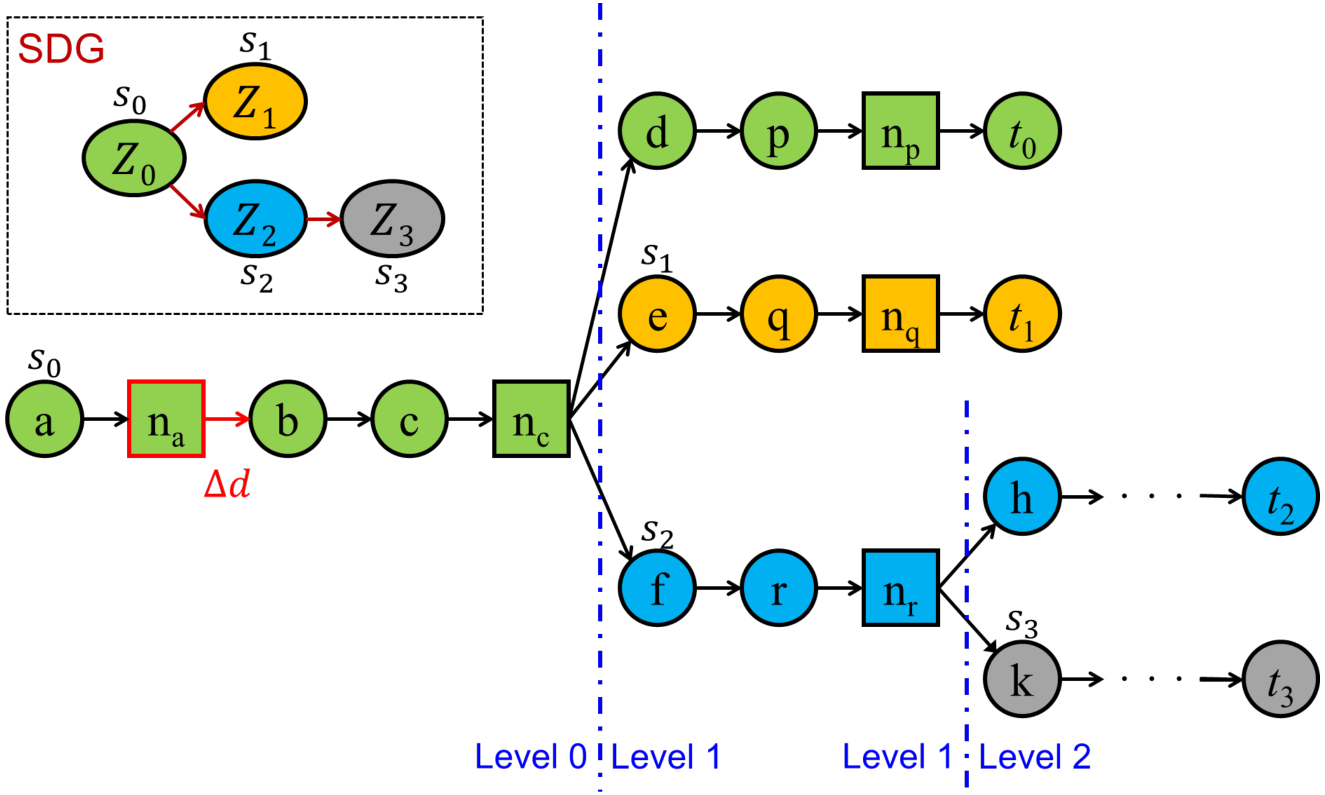


# Airgap-Wire Optimization

- Global Optimization – Net Selection
  - Most critical segment first (always effective)
  - Highest path usage first (contributes most to total negative slack)




(a) (b)

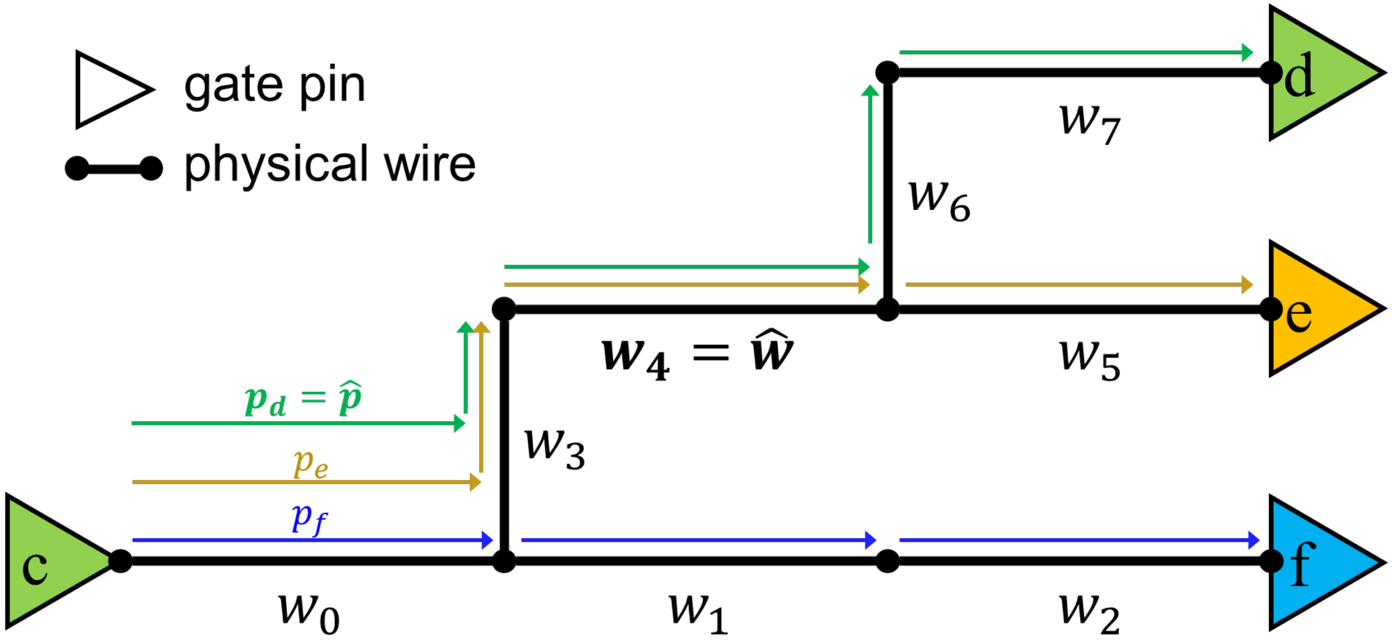


# Airgap-Wire Optimization

- Local Optimization – Airgap Insertion (on the selected net)
  - Check if the inserted airgap is legal and indeed reduces the delay
  - Formulate Elmore delay

$$d_n^p = \sum_{w \in W_n} c_w \sum_{i \in U_w} \gamma_i^p r_i = \sum_{w \in W_n} c_w \alpha_w^p$$

$$\Delta d_{\hat{w}}^{\hat{p}} = \Delta c_{\hat{w}} \alpha_{\hat{w}}^{\hat{p}}$$



# Airgap-Wire Optimization

- Local Optimization – Airgap Insertion (on the selected net)
  - LP formulation for each wire segment

$$\max_{\sigma_{\hat{w}}} \quad \sigma_{\hat{w}} \tag{15}$$

subject to

$$0 \leq \sigma_{\hat{w}} \leq 1 \tag{16a}$$

The amount of airgap

$$\Delta d_{\hat{n}}^{\hat{p}} \geq 0 \tag{16b}$$

Delay improvement

$$u_{\hat{n}}^{p} + \Delta d_{\hat{n}}^{p} \leq 0, \forall p \in P_{\hat{n}}^{s} \tag{16c}$$

Setup time

$$h_{\hat{n}}^{p} - \Delta d_{\hat{n}}^{p} \geq 0, \forall p \in P_{\hat{n}}^{h} \tag{16d}$$

Hold time

# Benchmark Statistics

- # Component: the number of wires of interest
- # $P_{setup}$: the number of setup paths
- # $P_{hold}$: the number of hold paths

| Benchmark | # Component | # Critical Net | # $P_{setup}$ | # $P_{hold}$ |
|---|---|---|---|---|
| s1196_TAU | 930 | 100 | 13 | 359 |
| systemcdes_TAU | 7935 | 2859 | 188 | 2564 |
| usb_funct_TAU | 40234 | 7507 | 281 | 7687 |
| vga_lcd_TAU | 138383 | 1762 | 867 | 104960 |
| leon3mp_TAU | 884385 | 2678 | 1144 | 24283 |

# Experimental Results

| Benchmark | Initial | | | The Min-Cost Network Flow Method [19] | | | | |
|---|---|---|---|---|---|---|---|---|
| | WNS (ns) | TNS (ns) | WHS (ns) | WNS (ns) | ΔWNS (%) | TNS (ns) | ΔTNS (%) | Runtime (s) |
| s1196_TAU | -0.0517 | -0.5077 | 0.0008 | -0.0504 | 2.51 | -0.4896 | 3.57 | 0.056 |
| systemcdes_TAU | -0.7170 | -62.8912 | 0.0023 | -0.7066 | 1.45 | -61.8041 | 1.73 | 6.144 |
| usb_funct_TAU | -0.6036 | -67.9476 | 0.0032 | -0.5994 | 0.70 | -67.4971 | 0.66 | 43.039 |
| vga_lcd_TAU | -1.1806 | -144.9361 | 0.0050 | -1.0892 | 7.74 | -34.6062 | 76.12 | 533.102 |
| leon3mp_TAU | -1.4405 | -843.1260 | 0.0011 | -1.0105 | 29.85 | -549.2453 | 34.86 | 1289.08 |
| ratio | - | - | - | 1.020 | 0.826 | 1.263 | 0.740 | 42.029 |

TNS: total negative slack
WNS: worst negative slack

Slack dependency graph helps
- Identify the most critical nets
- Ensure effective optimization
- Perform very fast update

| Benchmark | The Shortest-Path-Based Method [12] | | | | | Ours | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | WNS (ns) | ΔWNS (%) | TNS (ns) | ΔTNS (%) | Runtime (s) | WNS (ns) | ΔWNS (%) | TNS (ns) | ΔTNS (%) | Runtime (s) |
| s1196_TAU | -0.0505 | 2.32 | -0.4913 | 3.23 | **0.073** | **-0.0487** | **5.80** | **-0.4746** | **6.52** | 0.786 |
| systemcdes_TAU | -0.7066 | 1.45 | -61.8077 | 1.72 | 72.156 | **-0.6997** | **2.41** | **-61.0237** | **2.97** | **1.746** |
| usb_funct_TAU | **-0.5991** | **0.75** | -67.2468 | 1.03 | 167.061 | -0.6023 | 0.22 | **-59.2837** | **12.75** | **5.603** |
| vga_lcd_TAU | -1.0700 | 9.37 | -34.4020 | 76.26 | 1853.03 | **-1.0382** | **12.06** | **-20.3185** | **85.98** | **13.226** |
| leon3mp_TAU | -1.0125 | 29.71 | -551.5734 | 34.58 | 1886.09 | **-0.9992** | **30.64** | **-424.1012** | **49.70** | **23.166** |
| ratio | 1.015 | 0.853 | 1.266 | 0.740 | 89.348 | **1.000** | **1.000** | **1.000** | **1.000** | **1.000** |

[12] Y. Jung, D. Hyun, and Y. Shin, Integrated airgap insertion and layer reassignment for circuit timing optimization., ASP-DAC 2024. 32–37.
[19] B. Yu, D. Liu, S. Chowdhury, and D. Z. Pan, TILA: Timing-driven incremental layer assignment, ICCAD 2015, 110–117.

# Conclusion

- Present a novel way of viewing slack relationship – slack dependency graph
- Allow flexible amount of airgap to be generated
- Achieve significant speed up and quality improvement


# Thank You!