My Journey in EDA

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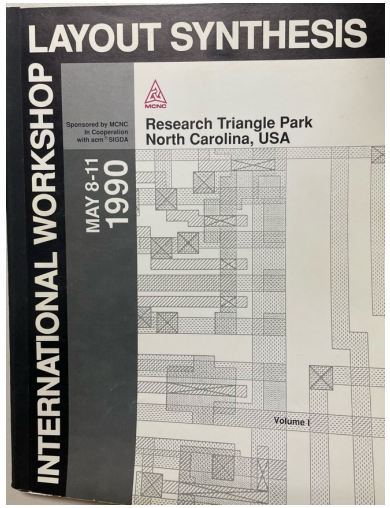
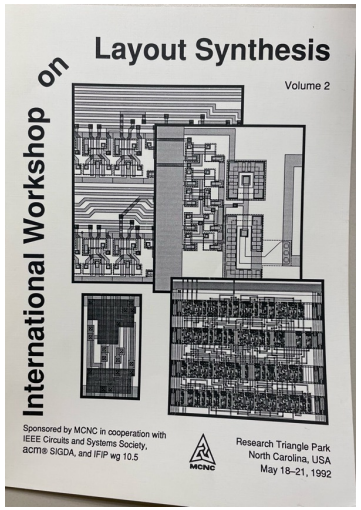
History of ISPD

Predecessors

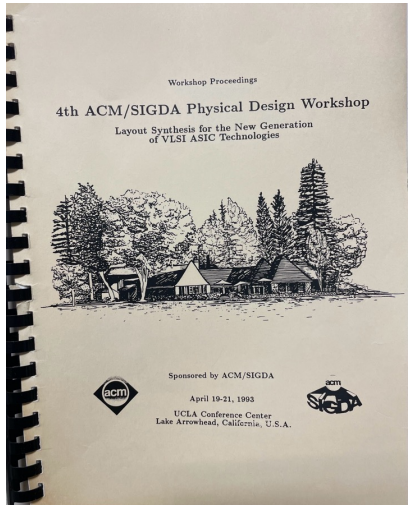
- ACM SIGDA Physical Design Workshop: 1987, 1989, 1991, 1993, 1996
- MCNC Layout Synthesis Workshop: 1988, 1990, 1992



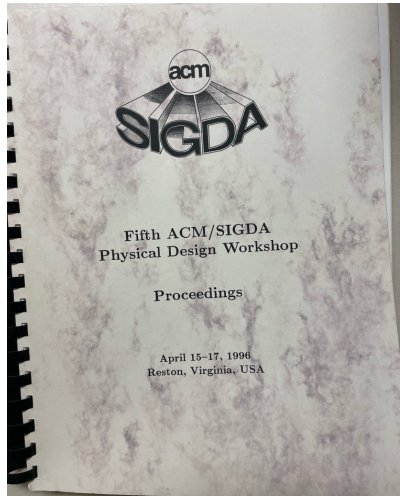
1990



1992



1993

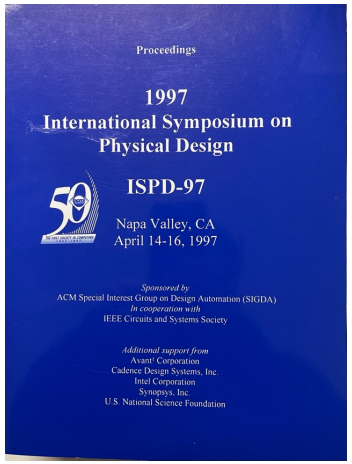


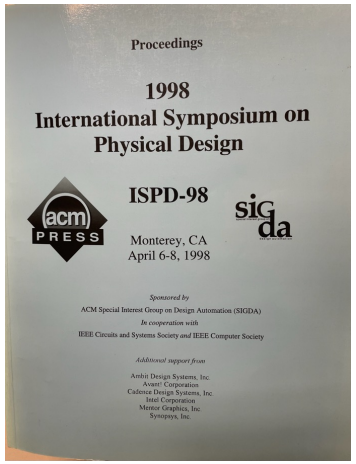
1996

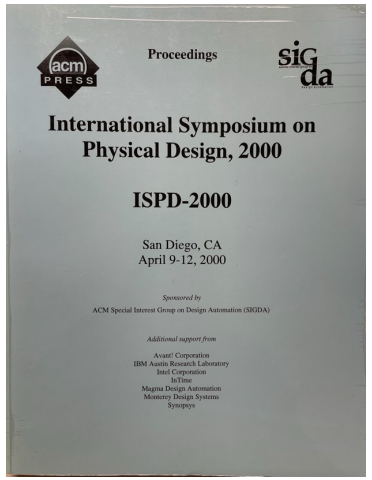
History of ISPD

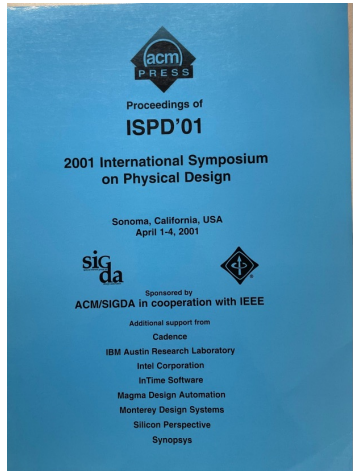
Annual Symposium 1997-Present

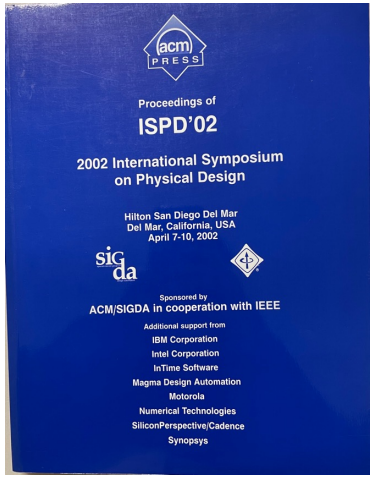
1997-2008

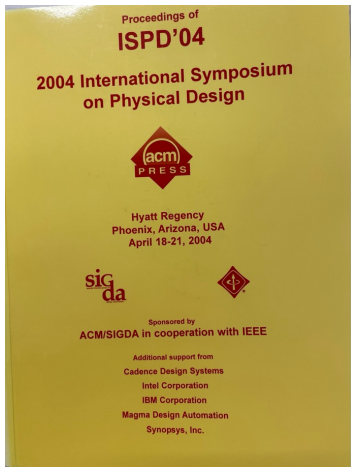


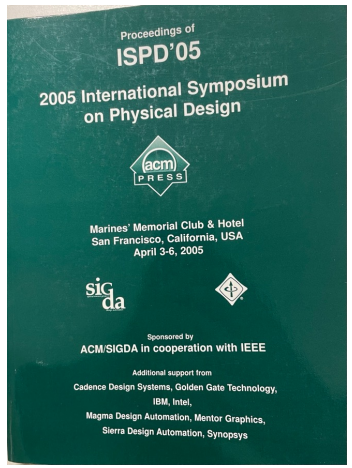


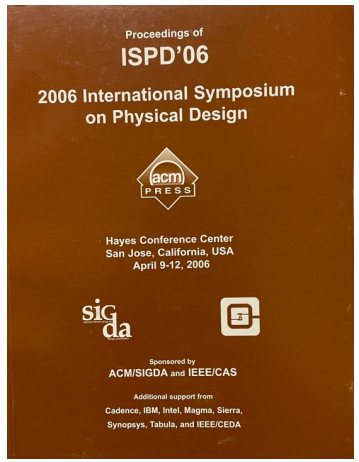


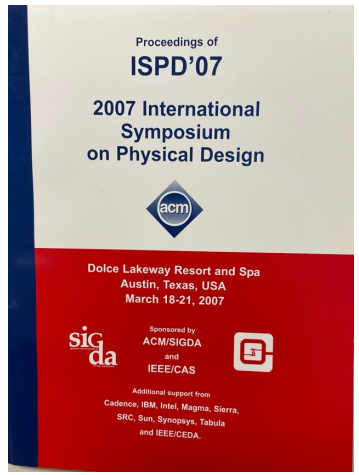


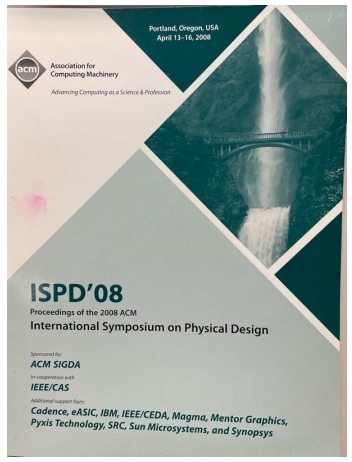












Souvenirs

1998

1999

2000

2001

ISPD 1999

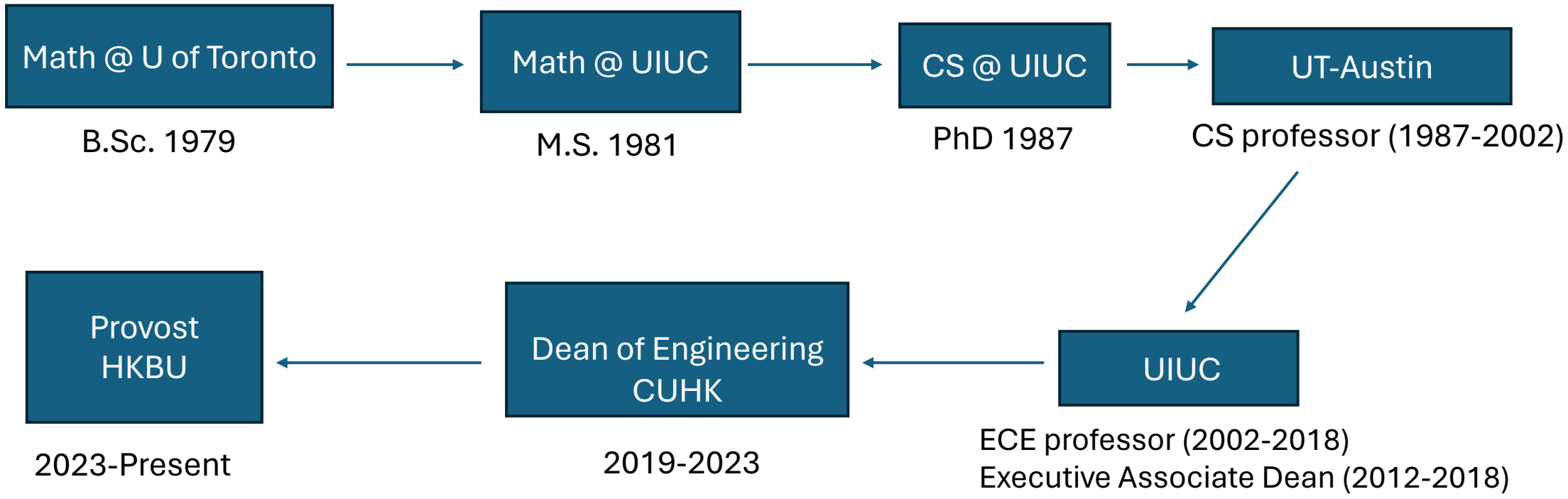
TPC Chair: Martin Wong
General Chair: Majid Sarrafzadeh

Lucky Draw!

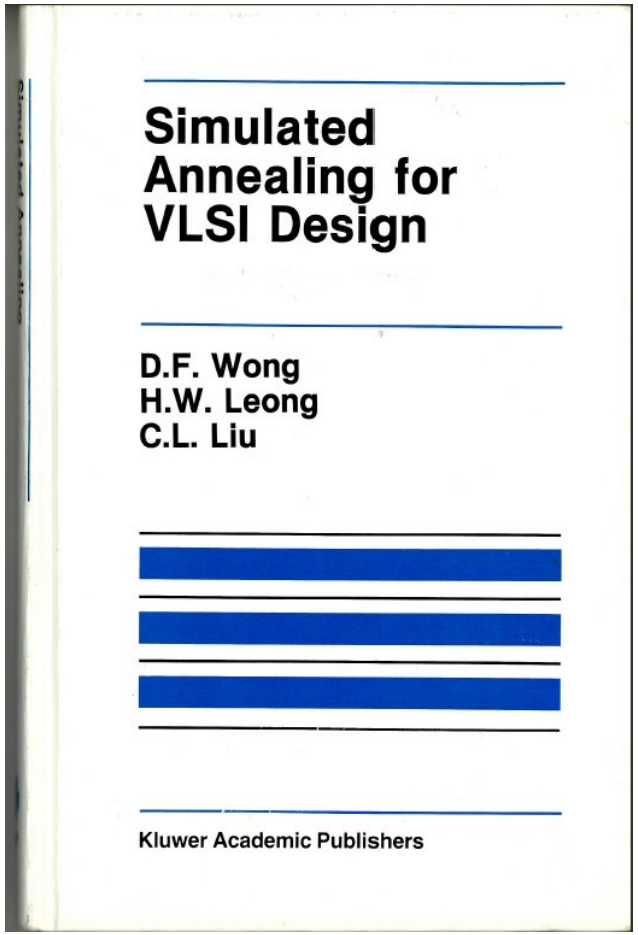
IBM Thinkpad 310

Thickness: 2 Inches!
2X of Surface Pro + McBook Air

My Background



Prof. C. L. Liu was my PhD Supervisor



1988

Several chapters in my PhD thesis were on “Simulated Annealing for VLSI Design”

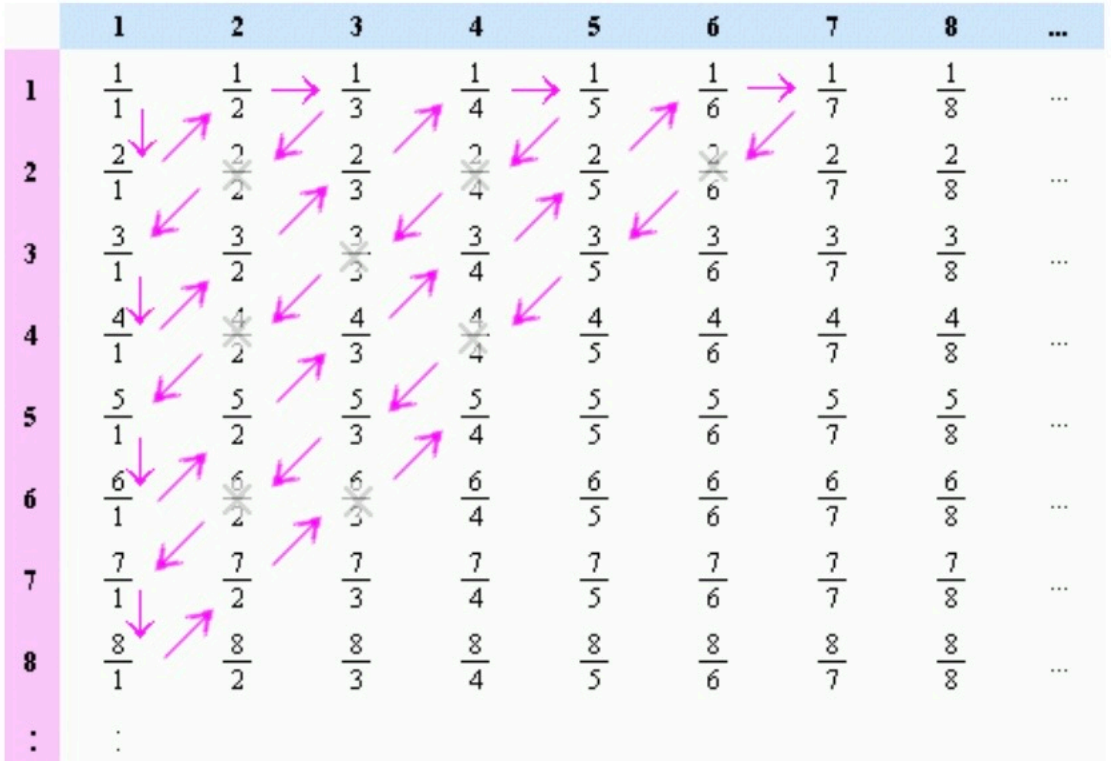
Did my Math background influence my research?

- Yes, it indirectly influenced my research style and approach
- Will present some unpublished observations/results in EDA influenced by 3 concepts in mathematics
  - Rational numbers vs Real numbers
  - Geometry
  - Elementary Proof

Example 1

Rational Numbers vs Real Numbers

- **Infinity**: Countable and Uncountable
- 1,2,3,4, ... (Countable)
- 0,-1,1,-2,2, ... (Countable)
- Rational numbers (*p*/*q*) is countable!
- Real numbers are uncountable!
- Rational numbers are dense in **R**



Every interval contains at least one rational number!

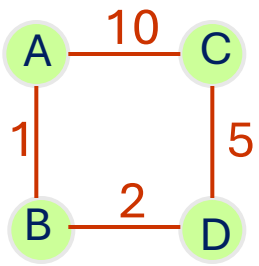
Floorplan Design

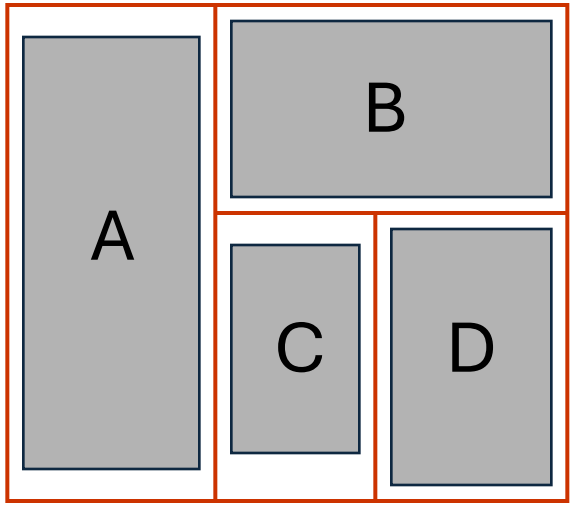
Pack modules on a rectangular chip to optimize total area, interconnect cost and other performance measure.

Module:

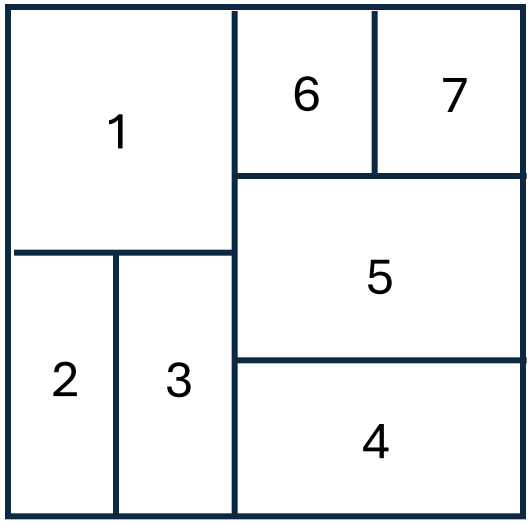
- Hard modules
- Soft modules

Connectivity:

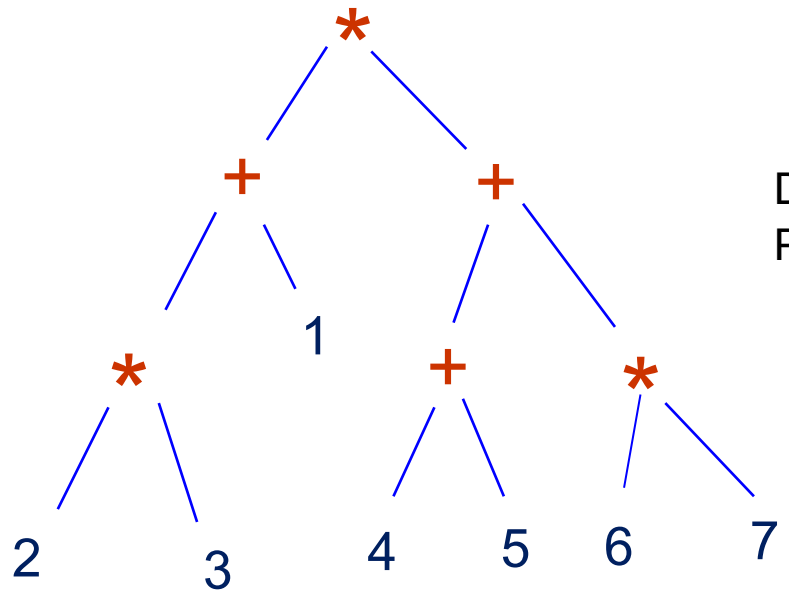




Algorithm



Slicing Floorplan



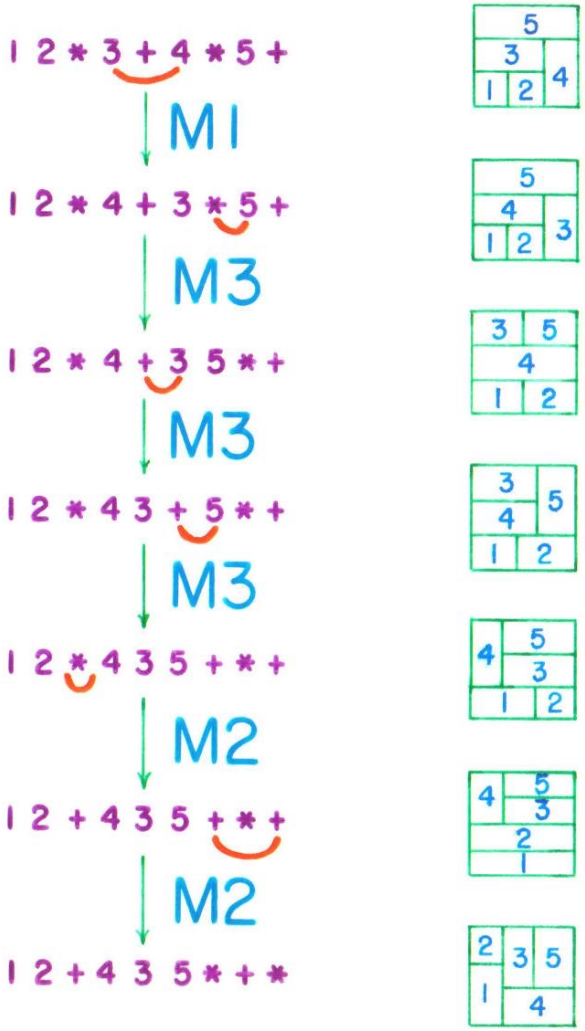
DAC 1986
PDW 1987

Slicing Tree

2 3 * 1 + 4 5 + 6 7 * + *

Polish Expression

Algorithm



Results for Soft Blocks

Experimental results => slicing is good for soft modules

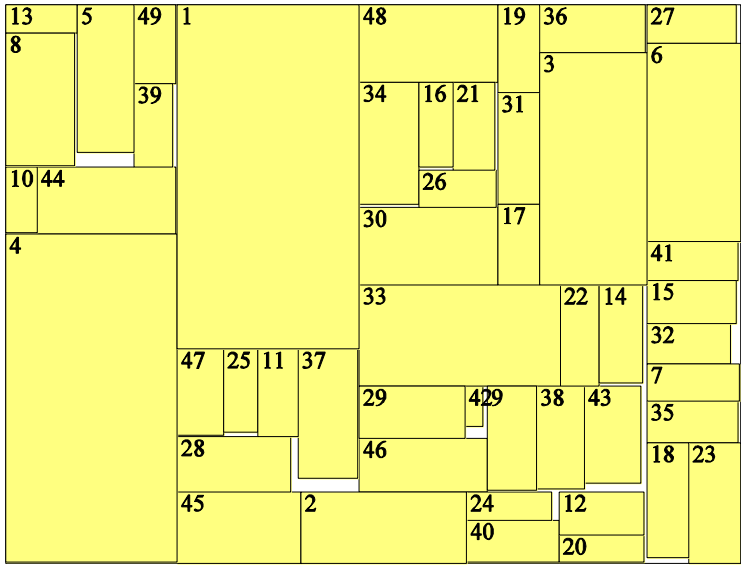
Circuit	*No. of Modules*	*runtime(s)*	*deadspace(%)*
apte	9	0.31	0.74
xerox	10	0.38	0
hp	11	0.45	0
ami33	33	3.22	0.01
ami49	49	6.93	0.13

*all modules have aspect ratio between 0.5 and 2

Results for Hard Blocks

MCNC benchmark	Problem Size	Fast-SP Area	ECBL Area	Enhanced Q-seq Area	TBS Area	Enhanced O-tree Area	Slicing Area
apte	9	46.92	45.93	46.92	47.44	46.92	46.92
xerox	10	19.80	19.91	19.93	19.78	20.21	20.20
hp	11	8.947	8.918	9.03	8.48	9.16	9.03
ami33	33	1.205	1.192	1.194	1.196	1.242	1.183
ami49	49	36.5	36.70	36.75	36.89	37.73	36.24

- Excellent results by slicing for the largest MCNC benchmarks (Cheng, Deng, Wong, ASPDAC 2005)



Can we mathematically explain these excellent empirical results?

Theoretical Analysis

Theorem [Young and Wong ISPD-97]

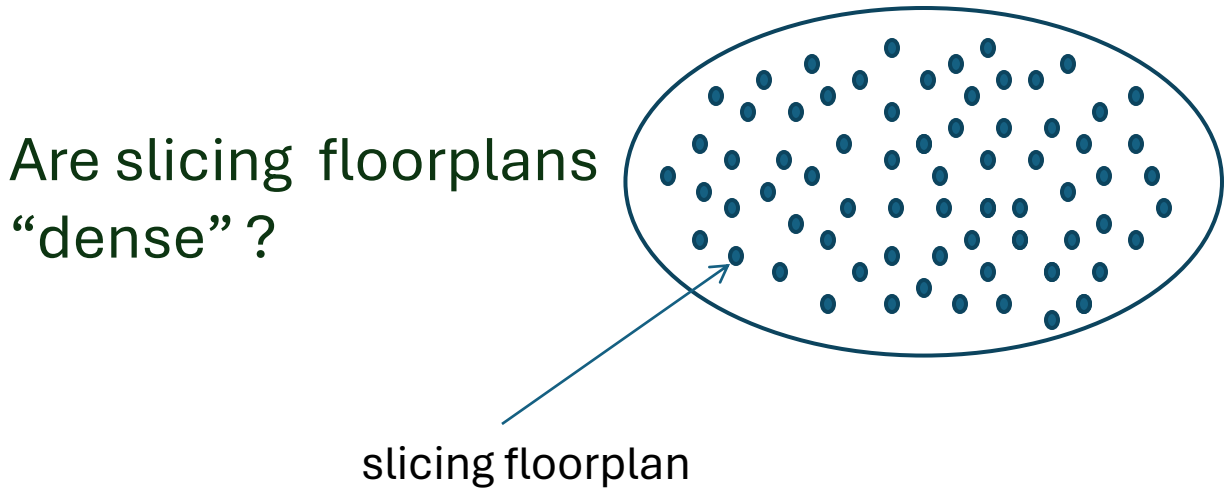
Given a set of soft blocks of total area A_{total} , maximum area A_{max} and shape flexibility $r \geq 2$, there exists a slicing floorplan ***F*** of these blocks such that:

$$area(F) \leq \min\left\{\left(1+\frac{1}{\sqrt{r}}\right), \frac{5}{4}, (1+\alpha)\right\} A_{total}$$

where $\alpha = \sqrt{\frac{2A_{max}}{rA_{total}}}$

Can we do better?

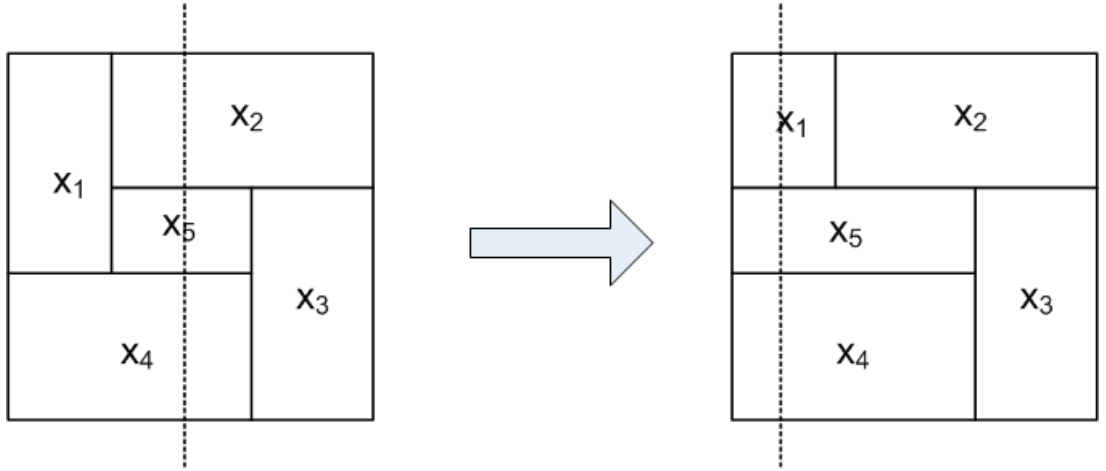
Conjecture: For each non-slicing floorplan, there exists a slicing floorplan with “similar” area and topology.



Wheel Floorplans with Squared Blocks

Lemma Given any wheel floorplan with 5 squared blocks, there is a "neighboring" slicing floorplan with equal/smaller area.

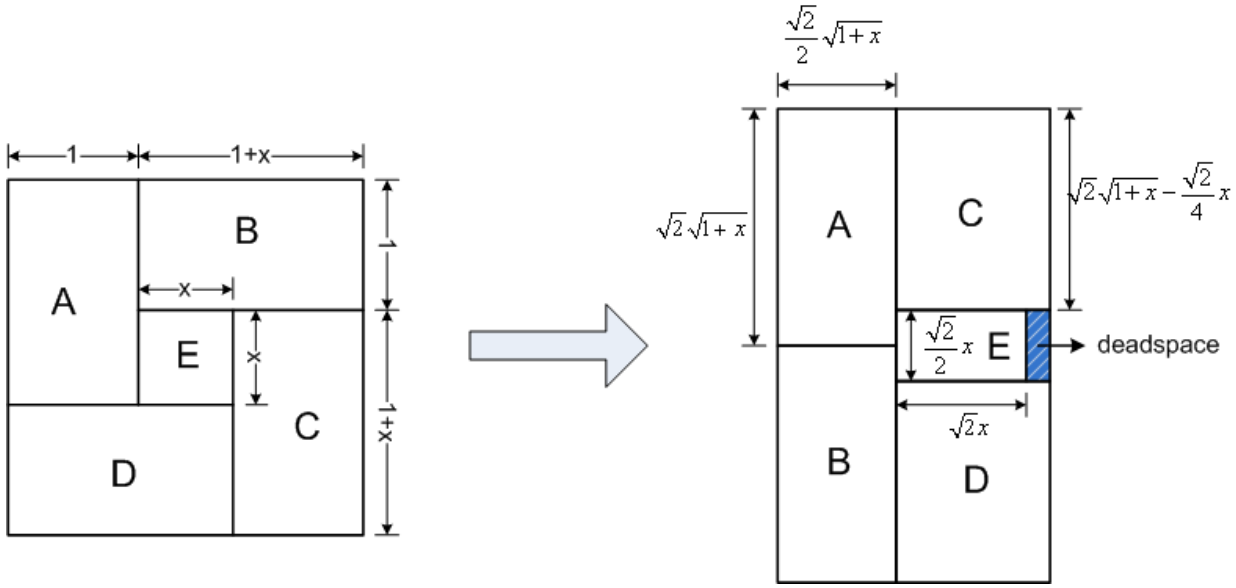
- It is not possible that x1 > x2 and x2 > x3 and x3 > x4 and x4 > x1. Otherwise, x1 > x1!
- We may assume x1 ≤ x2. It is easy to see that there is a "neighboring" slicing floorplan which is smaller!



$x_1+x_5+x_4 \le x_2+x_5+x_4$

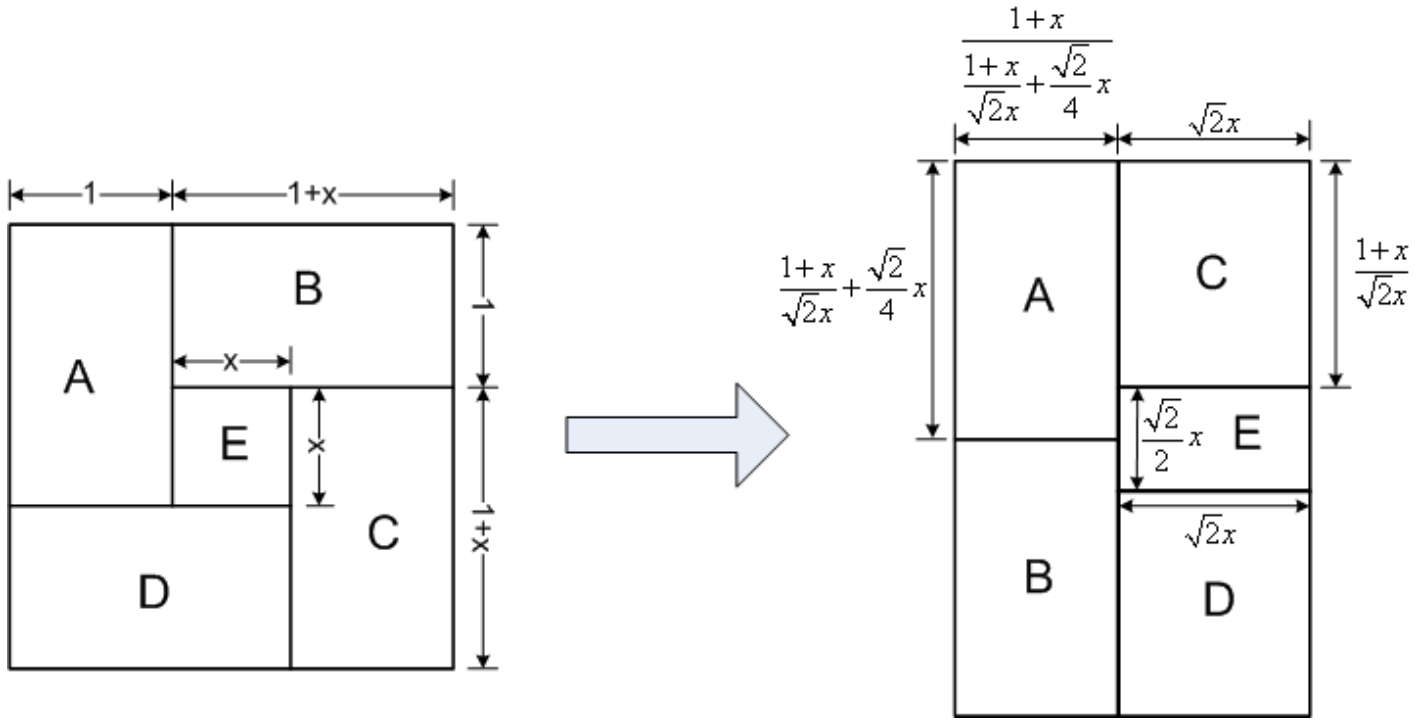
Tightly Packed Wheel Floorplans

- Tightly packed wheel floorplans
  - 5 blocks: A, B, C, and D are identical; E is a square
  - $0 \le x \le 1$; block aspect ratio is in [1/2,2]
- When $0 \le x < 0.783$
  - There is a neighboring slicing floorplan with area at most 1.77% larger



Tightly Packed Wheel Floorplans

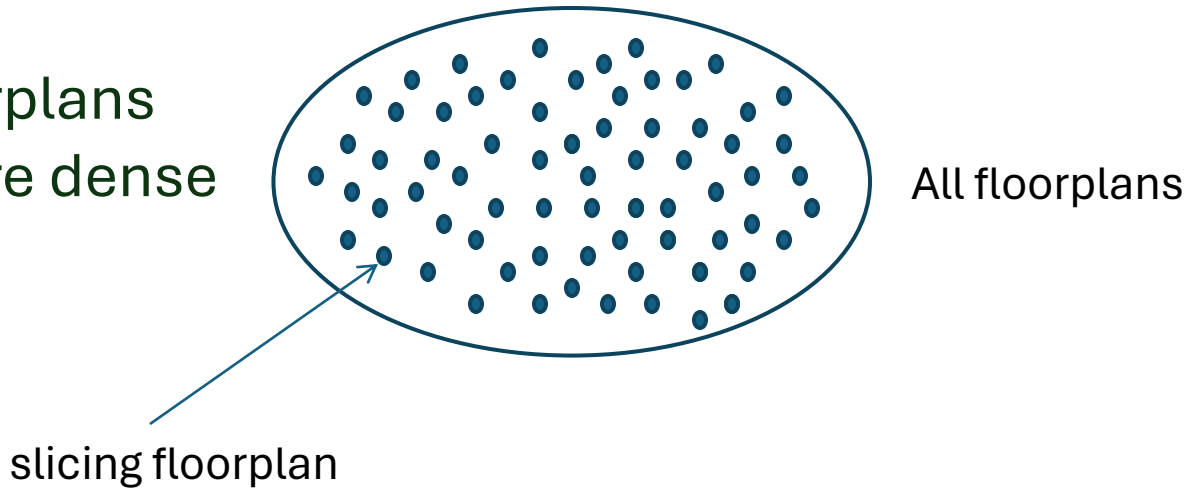
- When $0.783 \leq x \leq 1$
  - The neighboring slicing floorplan can be packed with zero dead-space



Conjecture is still open

Conjecture: For each non-slicing floorplan, there exists a slicing floorplan with “similar” area and topology.

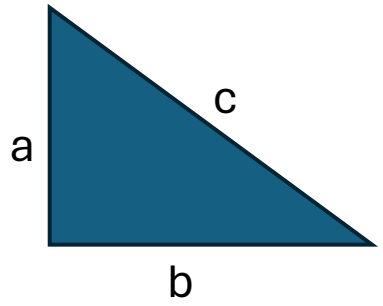
Are slicing floorplans
“dense” among all floorplans
like rational numbers are dense
among real numbers?



Example 2

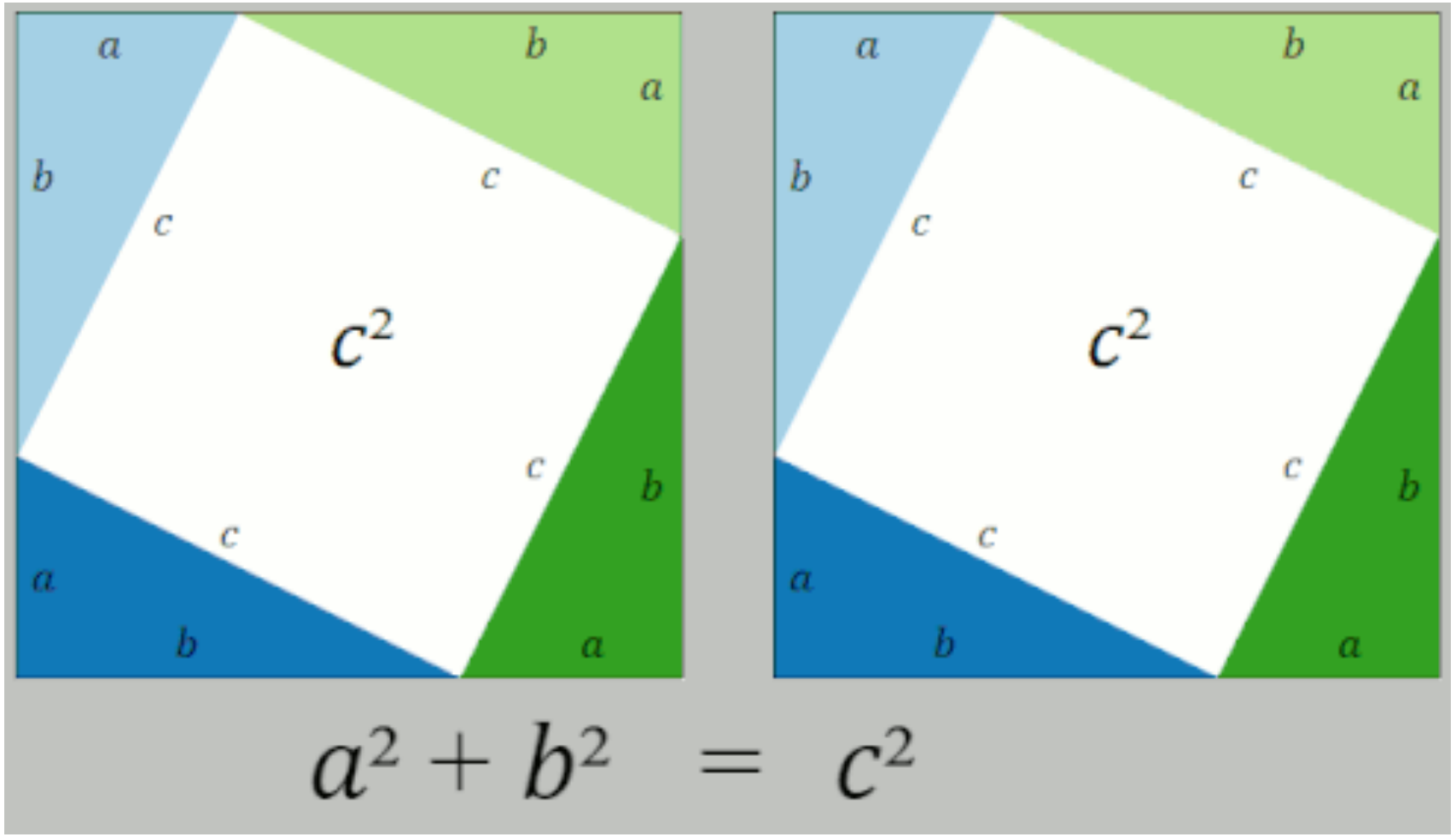
Geometry Helps

- Pythagoras Theorem

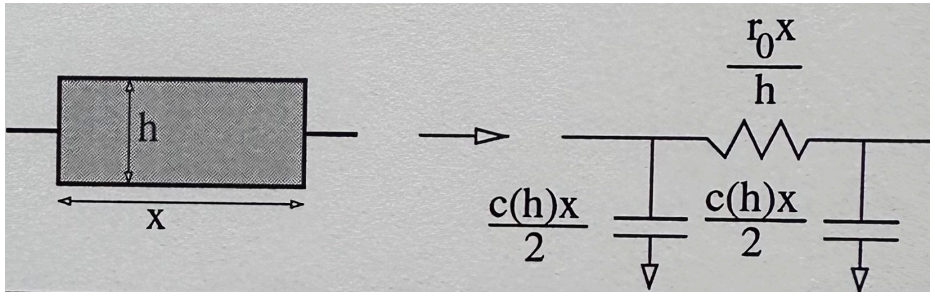


$$a^2 + b^2 = c^2$$

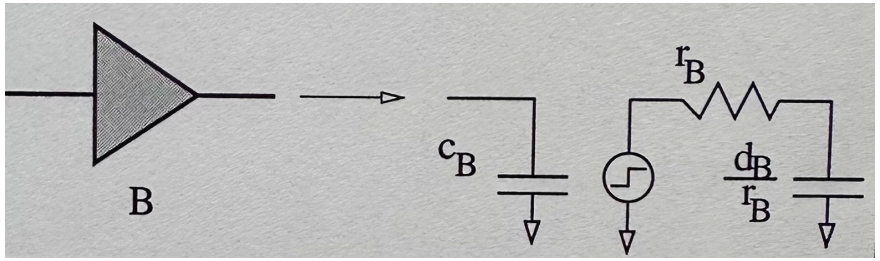
- Geometric Proof!



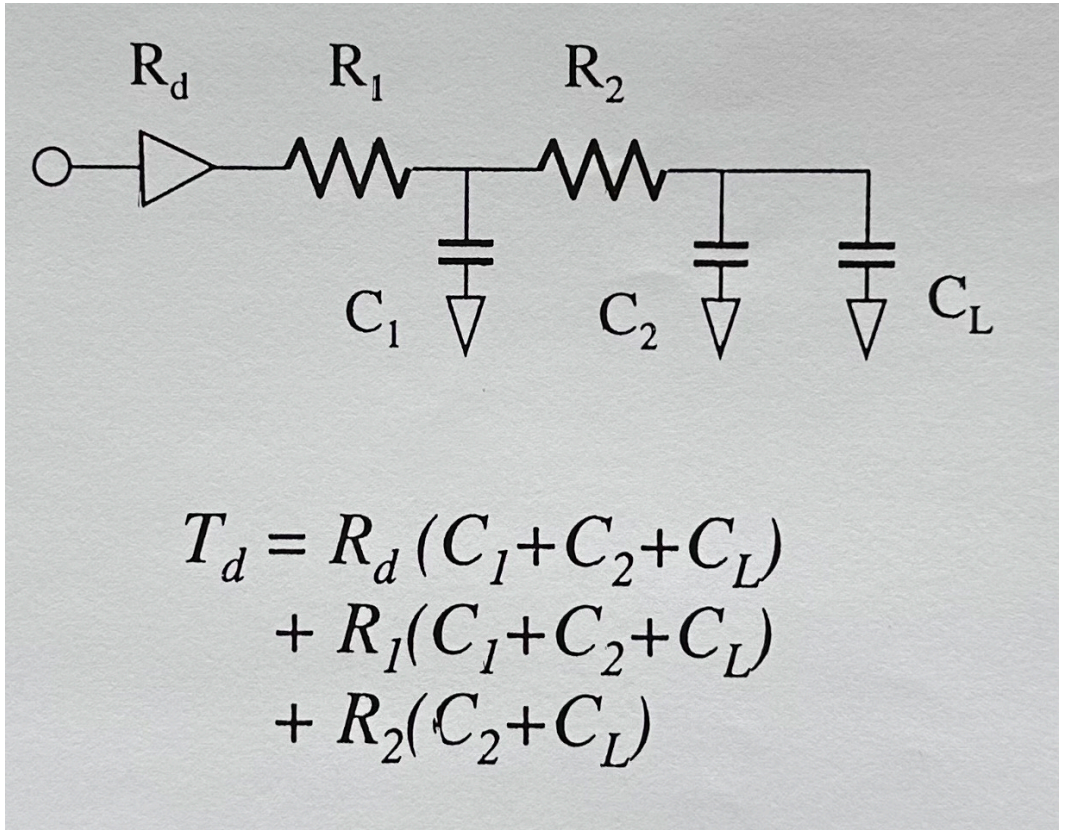
Interconnect Optimization



Wire Model



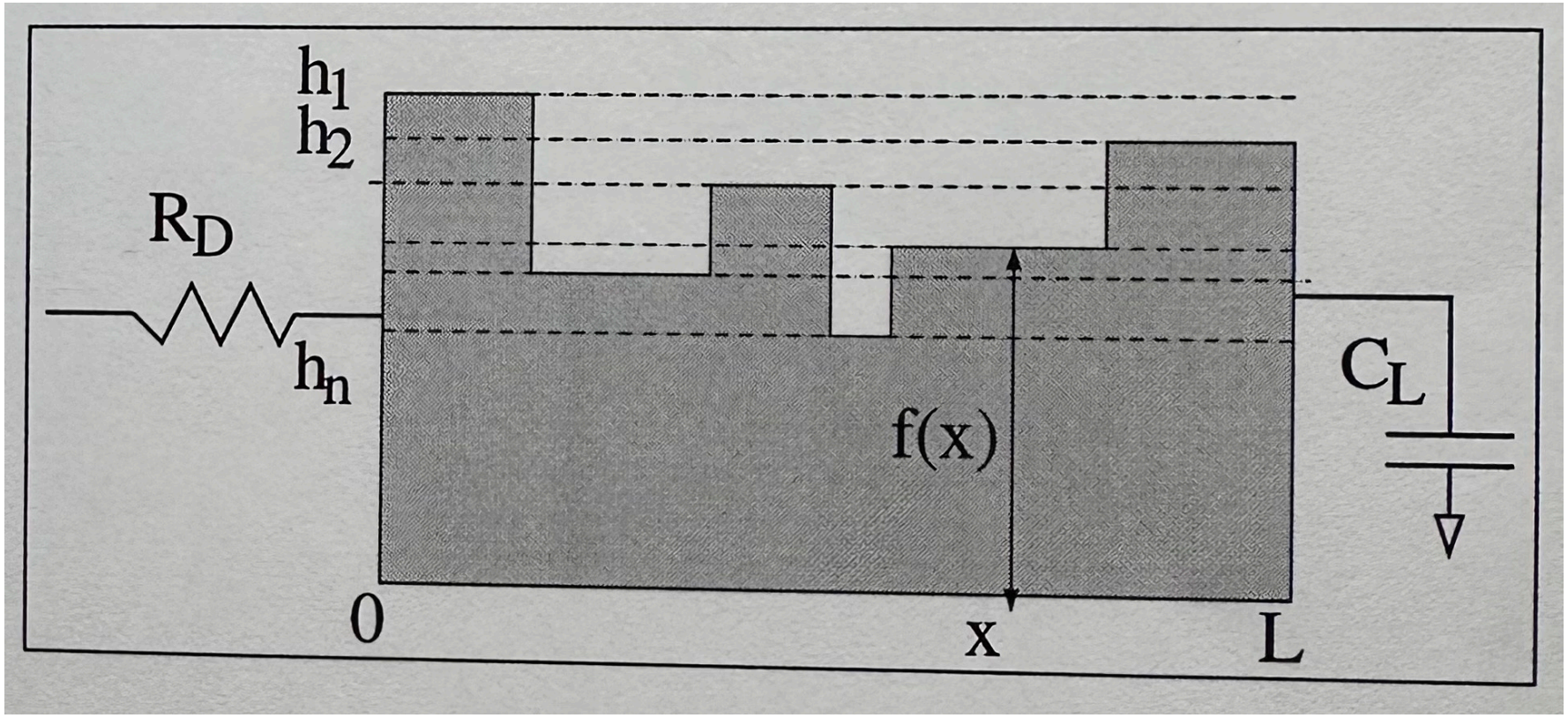
Buffer Model



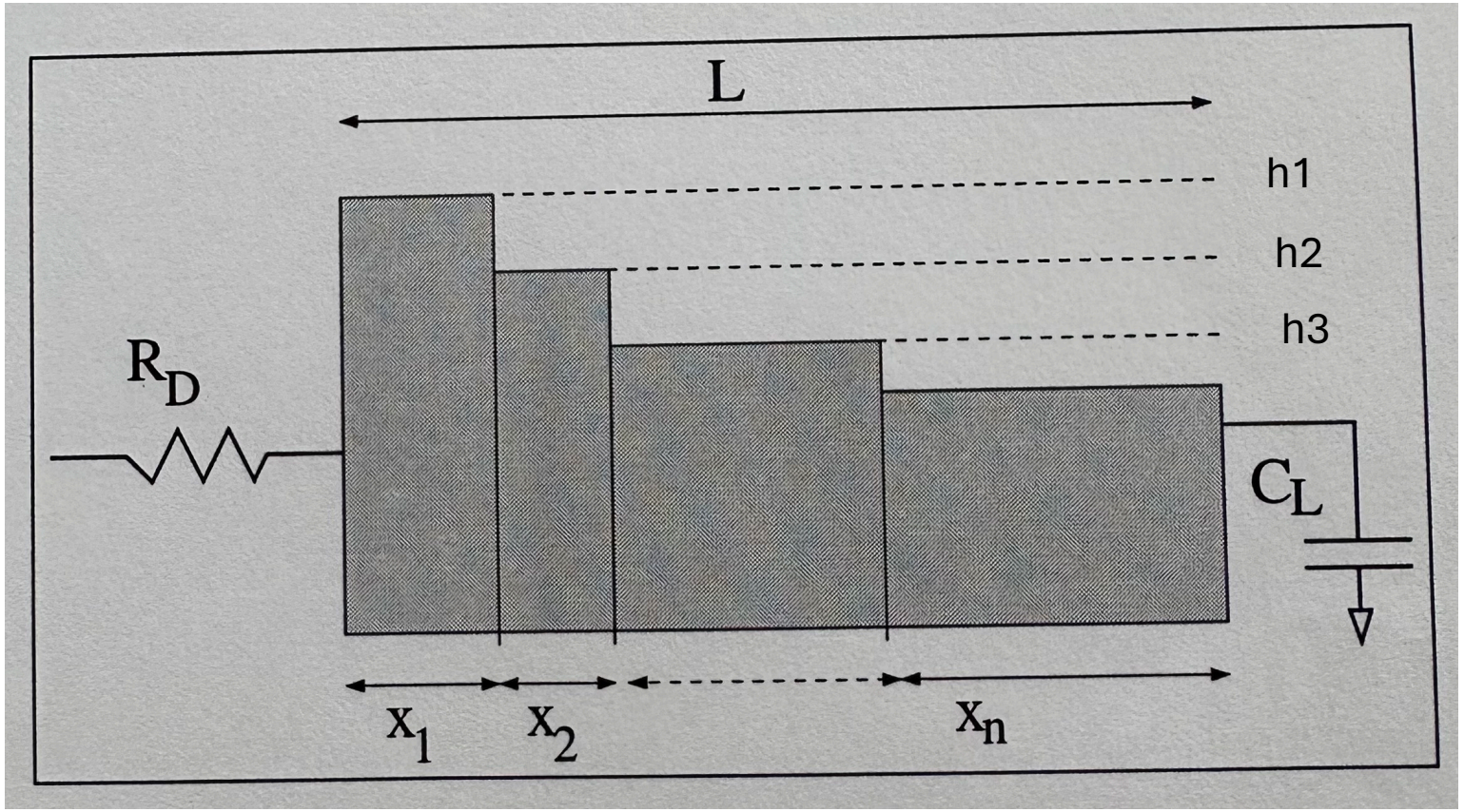
Elmore Delay Model

Wire Sizing

- Fixed set of allowable wire widths: h_1, h_2, h_3, …, h_n
- For continuous wire width, see closed form solution in PDW-96 (last PDW) and ISPD-97 (first ISPD)



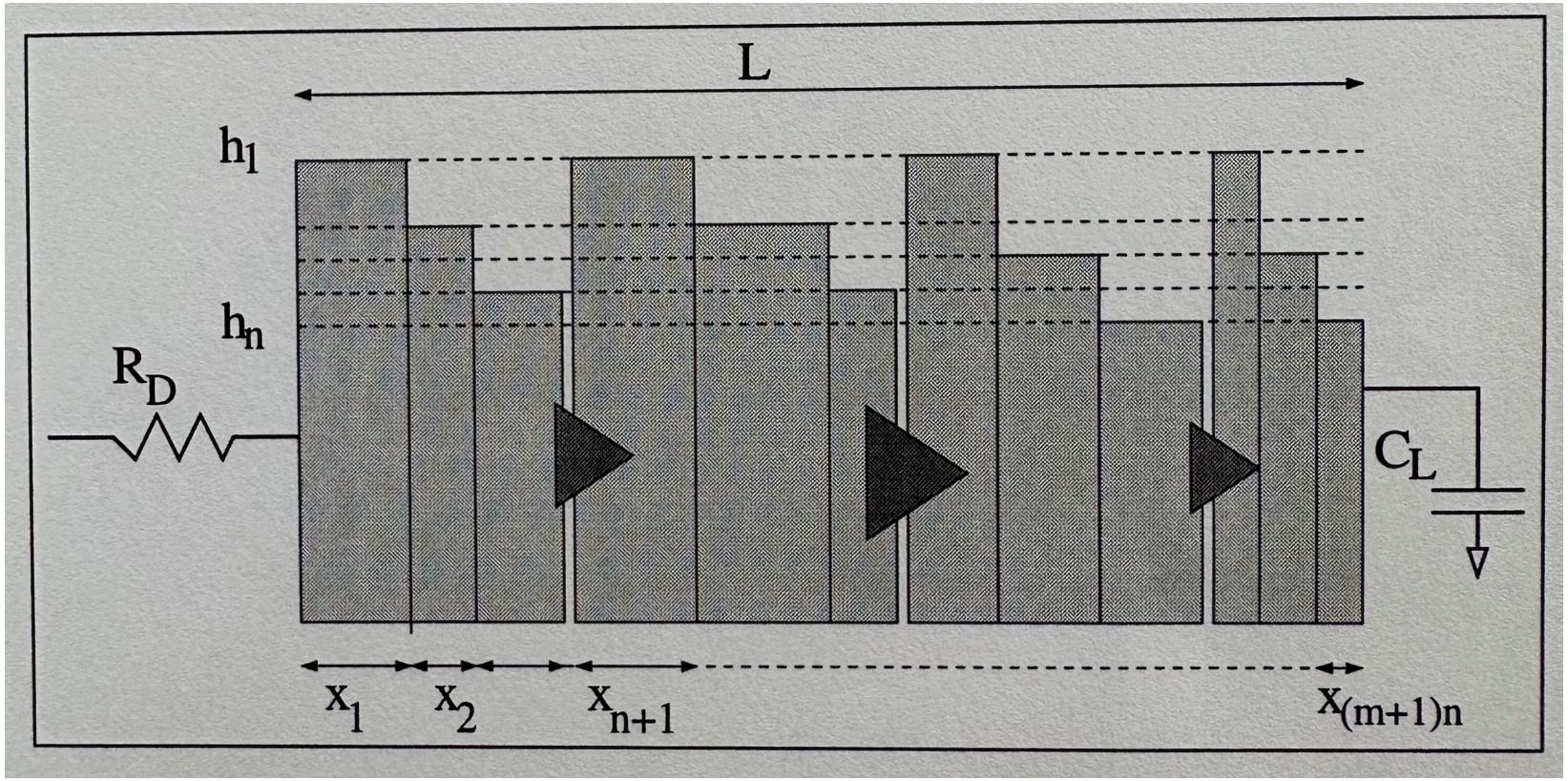
Wire Sizing



$$d = \frac{1}{2}\mathbf{x}^T\mathbf{A}\mathbf{x} + \mathbf{b}^T\mathbf{x} + R_D C_L$$

Ellipsoid!

Wire Sizing and Buffer Insertion



$$d = \frac{1}{2}\mathbf{x}^T \mathcal{A}\mathbf{x} + \boldsymbol{\rho}^T \mathbf{x} + \sum_{k=0}^{m} r_{B_k} c_{B_{k+1}} + \sum_{k=1}^{m} d_{B_k}$$

Ellipsoid!

Mathematical Formulation

Wire Sizing

$$d = \frac{1}{2}\mathbf{x^T A x} + \mathbf{b}^T\mathbf{x} + R_D C_L$$

$$\begin{aligned} \text{minimize} \quad & \tfrac{1}{2}\mathbf{x^T A x} + \mathbf{b^T x} \\ \text{subject to} \quad & x_1 + \cdots + x_n = L \\ & x_i \geq 0 \ \text{ for } \ 1 \leq i \leq n \end{aligned}$$

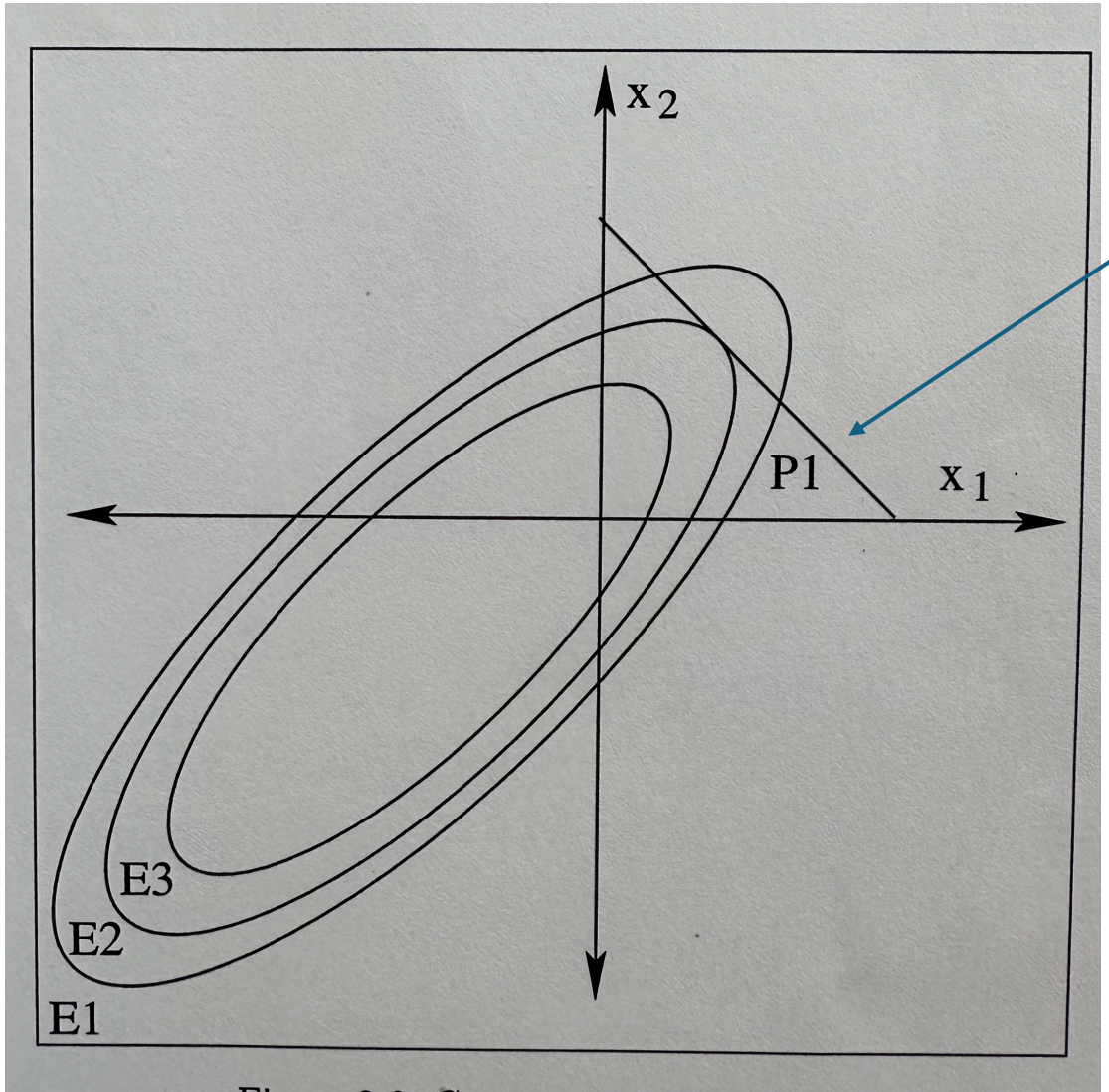
Wire Sizing and Buffer Insertion

$$d = \frac{1}{2}\mathbf{x}^T \boldsymbol{\mathcal{A}}\mathbf{x} + \boldsymbol{\rho}^T\mathbf{x} + \sum_{k=0}^{m} r_{B_k} c_{B_{k+1}} + \sum_{k=1}^{m} d_{B_k}$$

$$\begin{aligned} \text{minimize} \quad & \tfrac{1}{2}\mathbf{x}^T \boldsymbol{\mathcal{A}}\mathbf{x} + \boldsymbol{\rho}^T\mathbf{x} \\ \text{subject to} \quad & x_1 + \cdots + x_{(m+1)n} = L \\ & x_i \geq 0 \ \text{ for } \ 1 \leq i \leq (m+1)n \end{aligned}$$

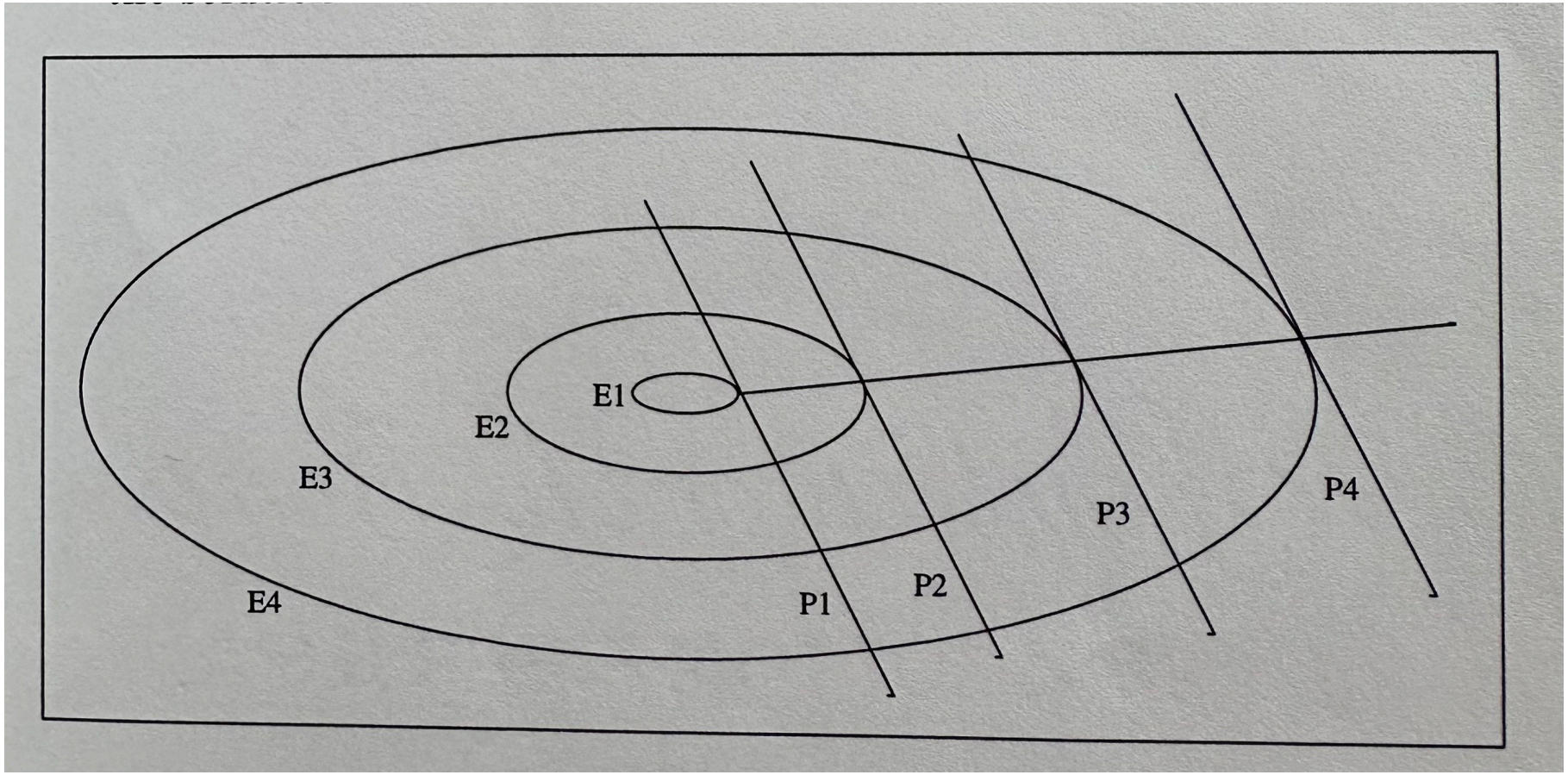
Tangent point is the solution

True only when L is not too small

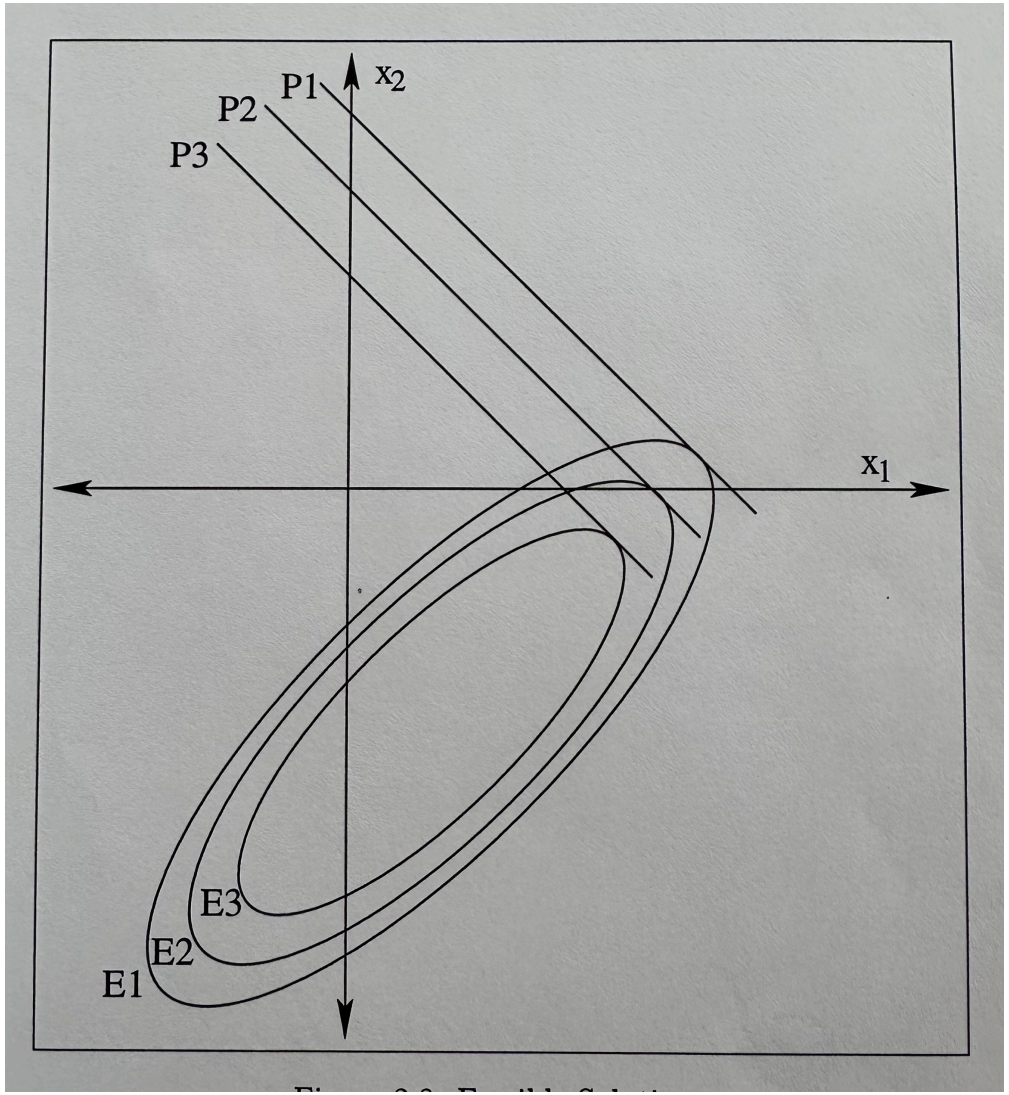


P1: X1 + X2 = L

Tangent points and ellipsoid center all lie on the same line for all line length L



Tangent point may not be a physical solution when L is too small



- For all $L \geq L0$, all tangent points are physical solutions
- Solutions for various L are **linearly scaled** for $L \geq L0$
- **Closed form solution** can be derived!

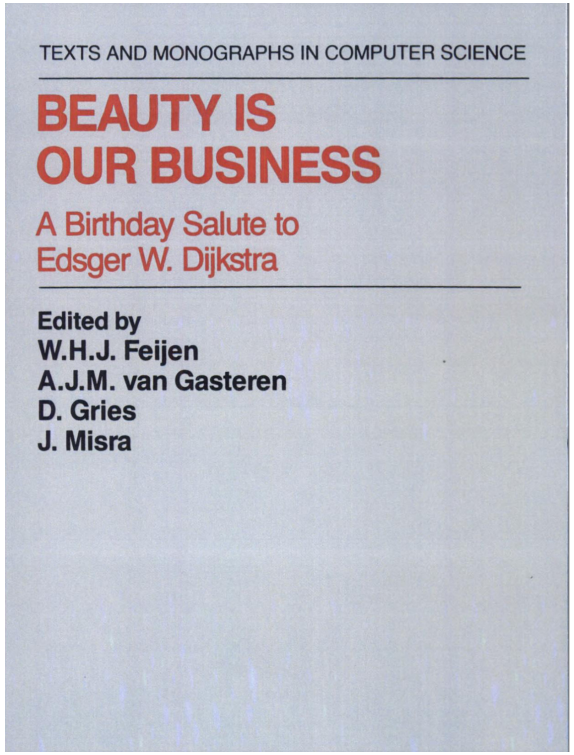
Example 3

Elementary Proof

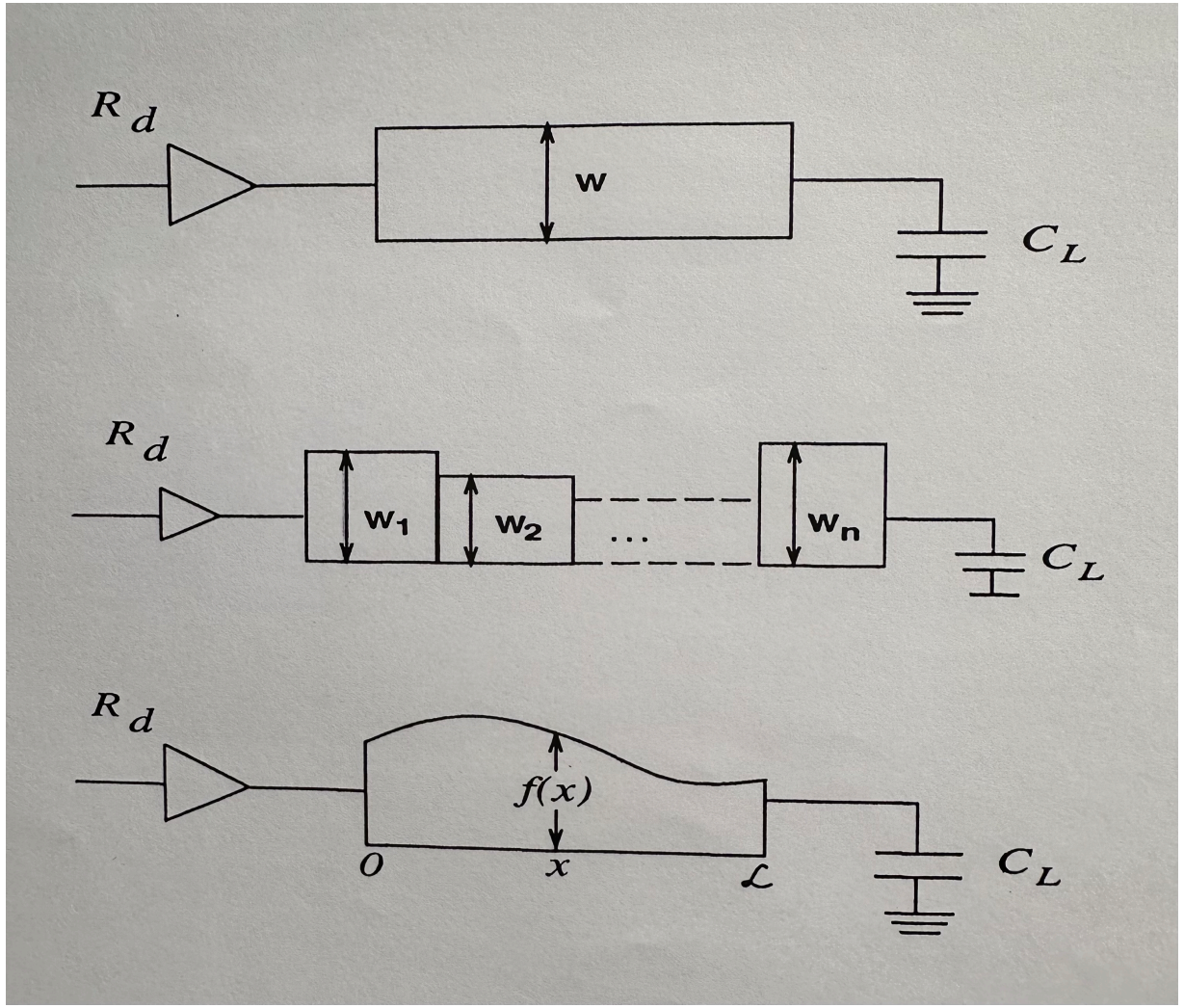
- A mathematical proof that only uses "**basic**" techniques
- Prime Number Theorem:

$$\pi(x) \sim \frac{x}{\log x}$$ where $\pi(x)$ is the # of primes $\leq x$

- First proof in 1896 by Hadamard and de la Vallee Poussin using sophisticated complex analysis (e.g., Rieman Zeta function)
- First **elementary proof** without using complex analysis was done in 1949 by Selberg and Erdos.

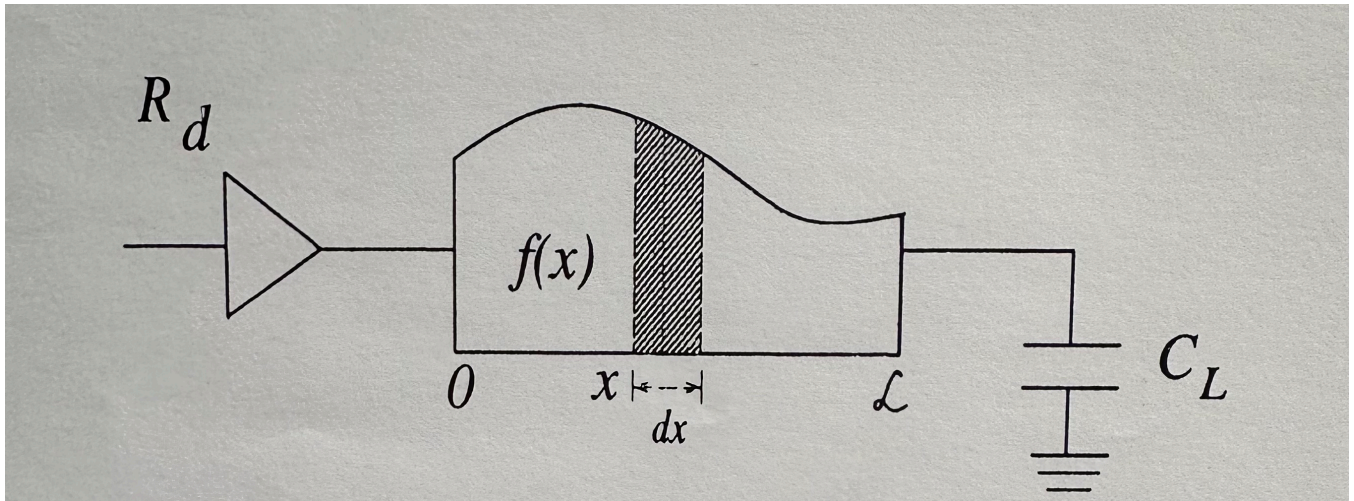


Wire-Sizing for Delay Minimization



1996 ACM SIGDA Physical Design Workshop

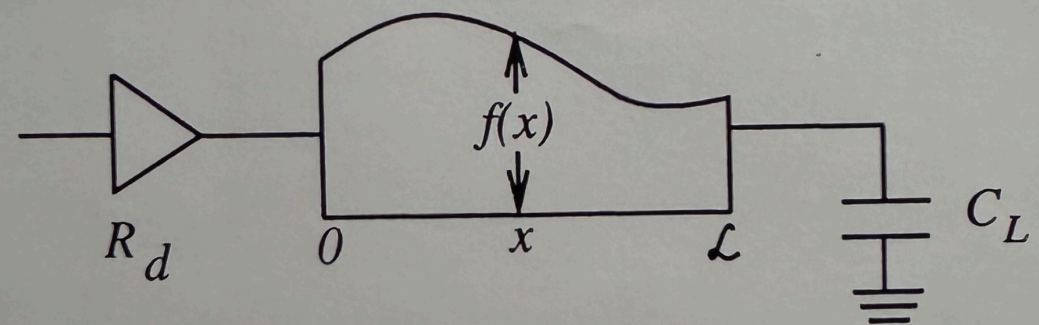
Elmore Delay



$$D = R_d(C_L + \int_0^{\mathcal{L}} c_0 f(x)dx) + \int_0^{\mathcal{L}} \frac{r_0}{f(x)} \left(\int_x^{\mathcal{L}} c_0 f(t)\, dt + C_L\right) dx$$

Theorem. Let f be an optimal wire-sizing function. We have

$$f^2(x) = \frac{r_0(C_L + c_0 \int_x^{\mathcal{L}} f(t)dt)}{c_0(R_d + r_0 \int_0^x \frac{1}{f(t)}dt)} = \frac{r_0 \mathcal{C}(x)}{c_0 \mathcal{R}(x)}$$



$\mathcal{C}(x)$ = Downstream Capacitance

$\mathcal{R}(x)$ = Upstream Resistance

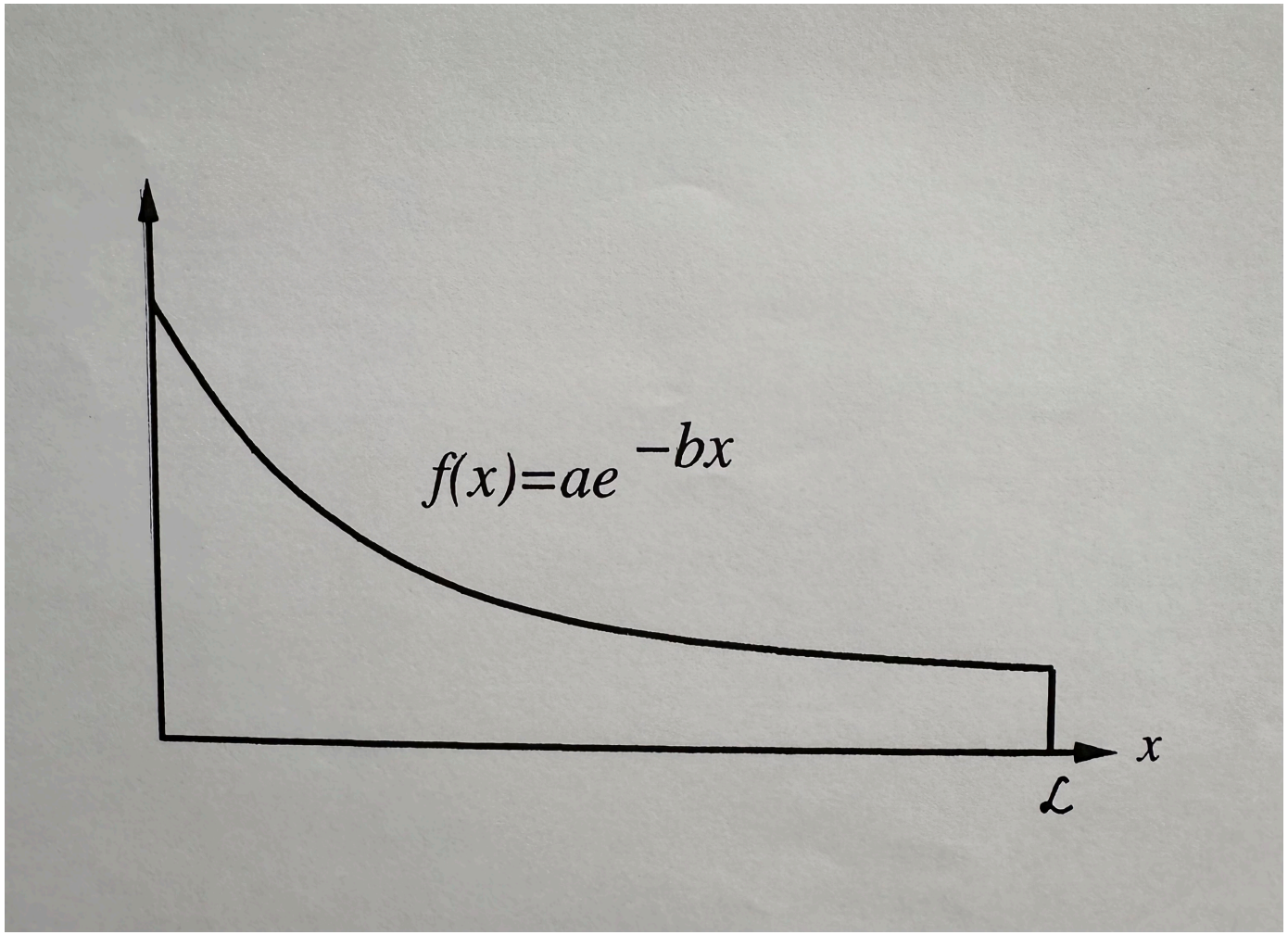
Theorem. Let $f(x)$ be an optimal wire-sizing function.

We have

$$f''(x)f(x) = f'(x)^2$$

- This differential equation has closed-form solution!

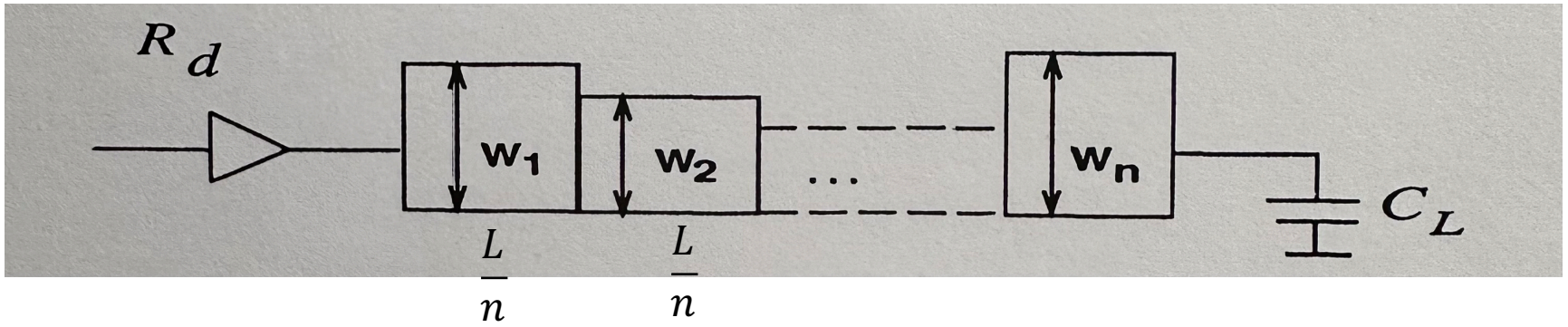
Optimal Wire-Sizing Function



Any **elementary proof** that exponential wire shape is optimal?

- Calculus of Variation (Fishburn and Schevon 1995)
- Ordinary Differential Equation (Chen and Wong 1996)
- Can we do it without using Calculus?

Elementary Proof



Proof Sketch

1. W1 $\geq$ W2 $\geq$ ... $\geq$ Wn
2. Uniform delay at each segment (d1 = d2 = d3 = ... = dn = d)
3. W2/W1 = W3/W2 = ... = Wn-1 /Wn = d/(d+h) where h = L/n
4. d/(d+h) = D/n (D/n + L/n) = D/(D+L) = r < 1
5. Wi = r^{n-i}Wn = K r^{n-i}
6. As n → ∞, W(x) = K r^{L-X} = A e^{-BX}

Step 3

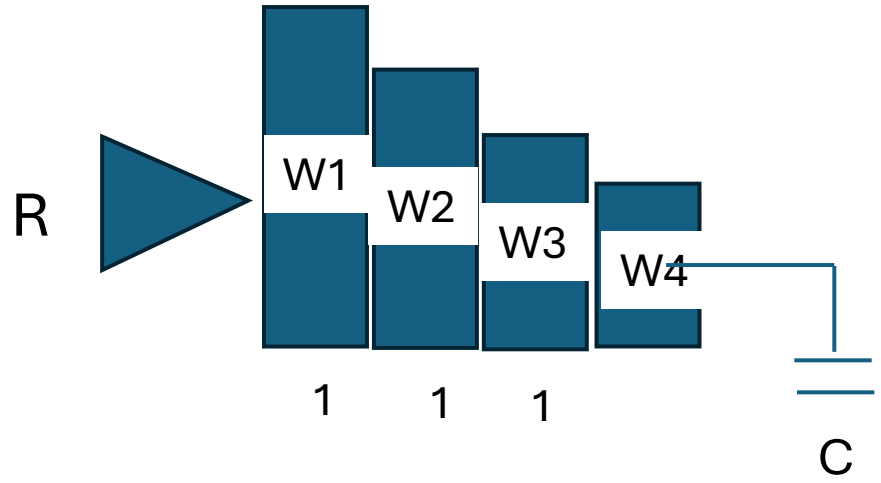
D = R (w1+ w2+ … + wn + C)

(1) +1/x1 (x2 + x3 + x4+C) (= d)

(2) +1/x2 (x3 + x4 +C) (= d)

(3) +1/X3 (x4 + C) (= d)

(4) + C/x4 (= d)



Rewrite (2): d = x1/x2 (x3/x1+ x4/x1+ C/x1)

Sub into (1): d = (1+d) x2/x1 → x2/x1 = d/(1+d)

Rewrite (3): d = (x4/x2 + C/x2) x2/x3

Sub into (2): d = (1+d) x3/x2 → x3/x2 = d/(1+d)

Rewrite (4): d = C/x4 = x3/x4 (C/x3)

Sub into (1): d = x4/x3 (1+d) → x4/x3 = d/(1+d)

Conclusion

- My math background had indirectly influenced my research style and approach
- Presented some unpublished observations/results
- Three 3 examples
  - Rational numbers vs Real numbers → Slicing floorplans vs All floorplans
  - Geometry helps → Geometric approach to interconnect optimization
  - Elementary proof → Exponential wire shape is optimal

The End