

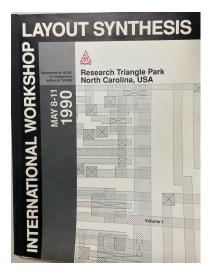
# **My Journey in EDA**

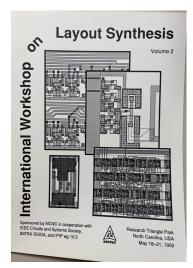
Martin D. F. Wong Hong Kong Baptist University

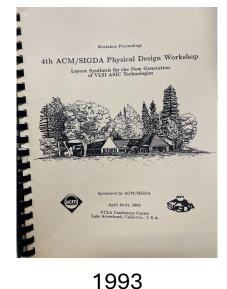
### History of ISPD

#### Predecessors

- ACM SIGDA Physical Design Workshop: 1987, 1989, 1991, 1993, 1996
- MCNC Layout Synthesis Workshop: 1988, 1990, 1992









1990

1992

## History of ISPD

#### **Annual Symposium 1997-Present**

#### PRESS acm) PRESS Proceedings Proceedings Proceedings siGa ACM) siGda Proceedings ACM PRESS 1997 1998 Proceedings of 1999 Proceedings of International Symposium on International Symposium on **International Symposium on** ISPD'02 ISPD'01 **International Symposium on Physical Design** Physical Design, 2000 **Physical Design Physical Design** 2002 International Symposium 2001 International Symposium on Physical Design on Physical Design ISPD-97 50 **ISPD-2000** ISPD-98 ISPD-99 siGa Hilton San Diego Del Mar Del Mar, California, USA April 7-10, 2002 Sonoma, California, USA April 1-4, 2001 Napa Valley, CA (acm) April 14-16, 1997 San Diego, CA PRESS Monterey, CA Monterey, CA siga April 9-12, 2000 April 6-8, 1998 siga April 12-14, 1999 Sponsored by ACM Special Interest Group on Design Automation (SIGDA) In cooperation with IEEE Circuits and Systems Society Snonsored by ACM/SIGDA in cooperation with IEEE ACM/SIGDA in cooperation with IEEE Sponsored by ACM Special Interest Group on Design Automation (SIGDA) CM Special Interest Group on Design Automation (SIGD A Additional support from In cooperation with Additional support from Cadence IBM Corporation Systems Society and IEEE Communer' IRM Austin Research Laboratory Intel Corporation Intel Corporation InTime Software InTime Software Magma Design Automation Magma Design Automation Motorola Monterey Design Systems Numerical Technologies Silicon Perspective iliconPerspective/Cadence Synopsys Synopsys Proceedings of Proceedings of ISPD'03 ISPD'04 Proceedings of Proceedings of Proceedings of ortland, Oregon, I April 13–16, 200 2003 International Symposium ISPD'06 ISPD'07 2004 International Symposium Association for Computing Machinery 2005 International Symposium on Physical Design on Physical Design 2006 International Symposium on Physical Design 2007 International on Physical Design Symposium ACM) on Physical Design PRESS (acm) PRESS acm Doubletree Hotel Monterey, California, USA April 6-9, 2003 Hyatt Regency Phoenix, Arizona, USA April 18-21, 2004 Marines' Memorial Club & Hotel San Francisco, California, USA April 3-6, 2005 Hayes Conference Center San Jose, California, USA April 9-12, 2006 siga Dolce Lakeway Resort and Spa Austin, Texas, USA March 18-21, 2007 SiGa $\langle \Phi \rangle$ ISPD'08 sig da Ð ACM/SIGDA in cooperation with IEEE Sponsored by ACM/SIGDA in cooperation with IEEE oceedings of the 2008 ACM International Symposium on Physical Design SIG ACM/SIGDA Ð ACM/SIGDA in cooperation with IEEE da and IEEE/CAS dditional support from e Desian System adence Design Systems Sponsored by ACM/SIGDA and IEEE/CAS ACM SIGDA Additional support from Intel Corporation nce Design Systems, Golden Gate Technology IEEE/CAS IBM Corporation Additional support from IBM, Intel Magma Design Automatio Magma Design Automation, Mentor Graphics, Cadence, IBM, Intel, Magma, Sierra SRC, Sun, Synopsys, Tabula and IEEE/CEDA, Cadence, eASIC, IBM, IEEE/CEDA, Magma, Mentor Graphics, Numerical Technologies Synopsys, Inc. Synopsys, Tabula, and IEEE/CEDA Pyxis Technology, SRC, Sun Microsystems, and Synopsys Synopsys, Inc Sierra Design Automation, Synopsys

1997-2008

### **Souvenirs**







#### **ISPD 1999**

### **TPC Chair:** Martin Wong **General Chair:** Majid Sarrafzadeh

Lucky Draw!

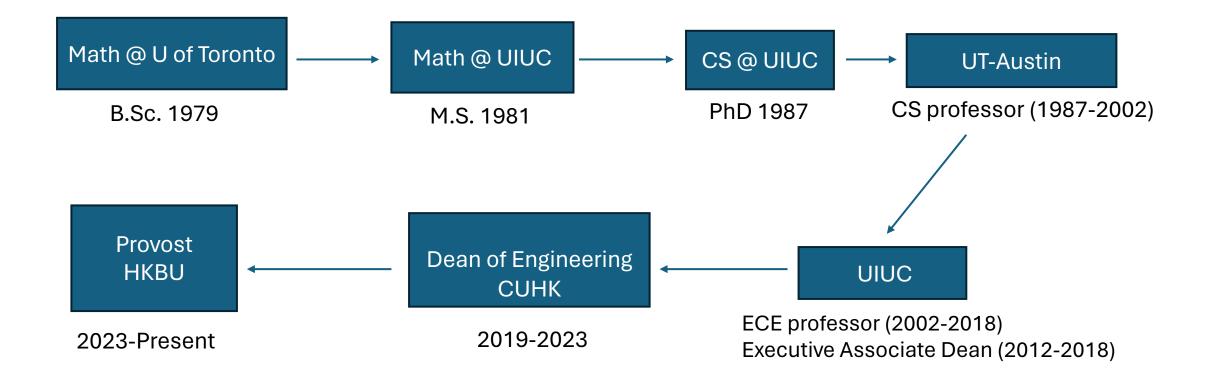


IBM Thinkpad 310

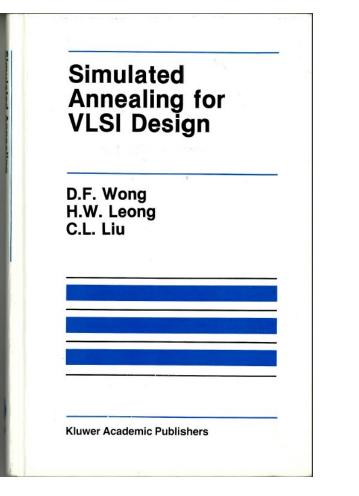


Thickness: 2 Inches! 2X of Surface Pro + McBook Air

## My Background



#### Prof. C. L. Liu was my PhD Supervisor





Several chapters in my PhD thesis were on "Simulated Annealing for VLSI Design"

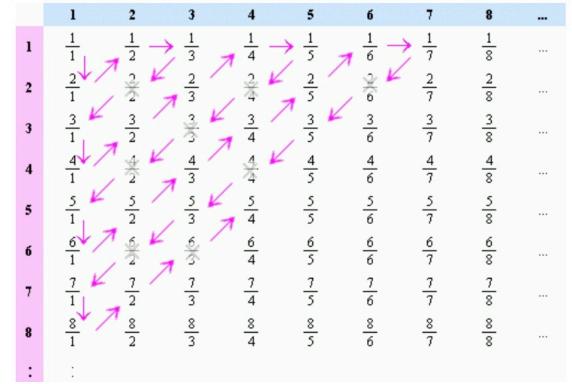
#### Did my Math background influence my research?

- Yes, it indirectly influenced my research style and approach
- Will present some unpublished observations/results in EDA influenced by 3 concepts in mathematics
  - Rational numbers vs Real numbers
  - Geometry
  - Elementary Proof

## Example 1

### Rational Numbers vs Real Numbers

- Infinity: Countable and Uncountable
- 1,2,3,4, ..... (Countable)
- 0,-1,1,-2,2, ..... (Countable)
- Rational numbers (p/q) is countable!
- Real numbers are uncountable!
- Rational numbers are dense in R



Every interval contains at least one rational number!

### Floorplan Design

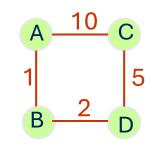
Pack modules on a rectangular chip to optimize total area, interconnect cost and other performance measure.

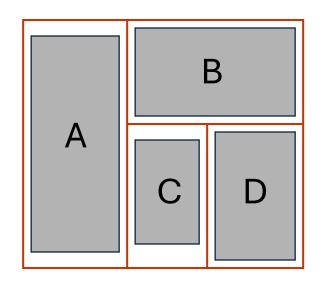
Module:

- Hard modules

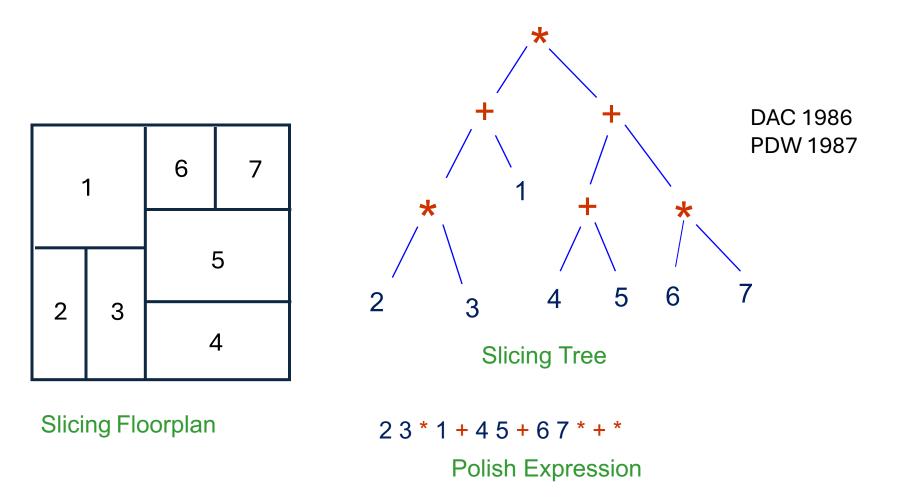
Soft modules

Connectivity:



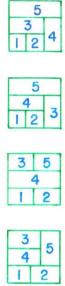


#### Algorithm



### Algorithm

12*	3+4*5+ MI
12*	4+3*5+ M3
12*	4 <del>+</del> 3 5 * + ↓ M3
12*	43+5*+ ↓M3
12*	435+*+ ↓ M2
12+	<sup>4 3 5</sup> †*† ↓ M2
12+	435*+*







#### **Results for Soft Blocks**

Experimental results => slicing is good for soft modules

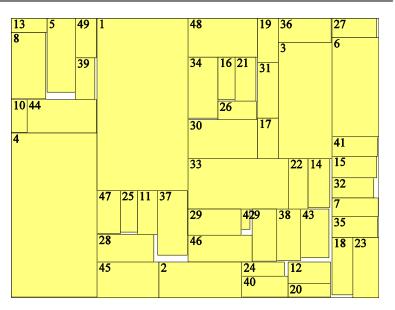
Circuit	No. of Modules	runtime(s)	deadspace(%)	
apte	9	0.31	0.74	
xerox	10	0.38	0	
hp	11	0.45	0	
ami33	33	3.22	0.01	
ami49	49	6.93	0.13	

\*all modules have aspect ratio between 0.5 and 2

#### **Results for Hard Blocks**

	MCNC	Problem	Fast-SP	ECBL	Enhanced Q-seq	TBS	Enhanced O-tree	Slicing
b	penchmark	Size	Area	Area	Area	Area	Area	Area
	apte	9	46.92	45.93	46.92	47.44	46.92	46.92
	xerox	10	19.80	19.91	19.93	19.78	20.21	20.20
	hp	11	8.947	8.918	9.03	8.48	9.16	9.03
	ami33	33	1.205	1.192	1.194	1.196	1.242	1.183
	ami49	49	36.5	36.70	36.75	36.89	37.73	36.24

 Excellent results by slicing for the largest MCNC benchmarks (Cheng, Deng, Wong, ASPDAC 2005)



Can we mathematically explain these excellent empirical results?

#### **Theoretical Analysis**

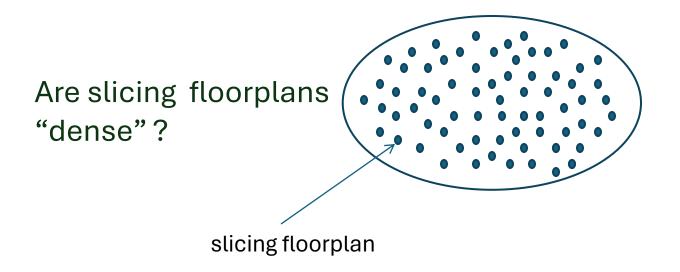
**Theorem** [Young and Wong ISPD-97]

Given a set of soft blocks of total area  $A_{total}$ , maximum area  $A_{max}$  and shape flexibility  $r \ge 2$ , there exists a slicing floorplan F of these blocks such that:

$$area(F) \le \min\left\{ (1 + \frac{1}{\sqrt{r}}), \frac{5}{4}, (1 + \alpha) \right\} A_{total}$$
where  $\alpha = \sqrt{\frac{2A_{max}}{rA_{total}}}$ 

#### Can we do better?

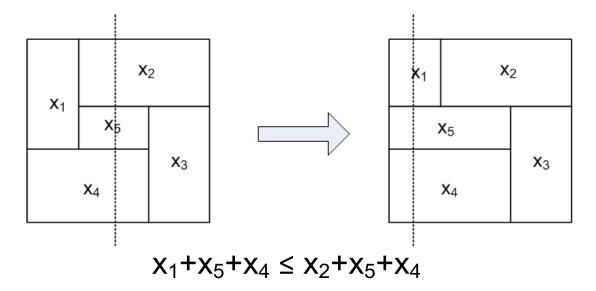
**Conjecture:** For each non-slicing floorplan, there exists a slicing floorplan with "similar" area and topology.



#### Wheel Floorplans with Squared Blocks

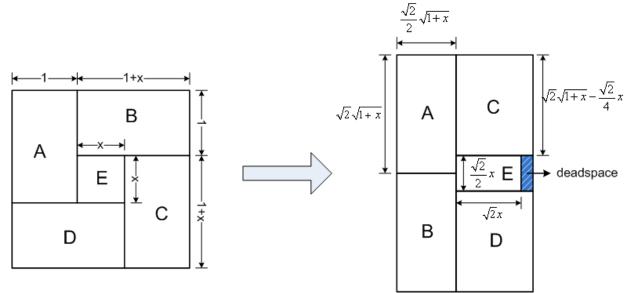
**Lemma** Given any wheel floorplan with 5 squared blocks, there is a "neighboring" slicing floorplan with equal/smaller area.

- It is not possible that x1 > x2 and x2 > x3 and x3 > x4 and x4 > x1.
   Otherwise, x1 > x1!
- We may assume x1 ≤ x2. It is easy to see that there is a "neighboring" slicing floorplan which is smaller!



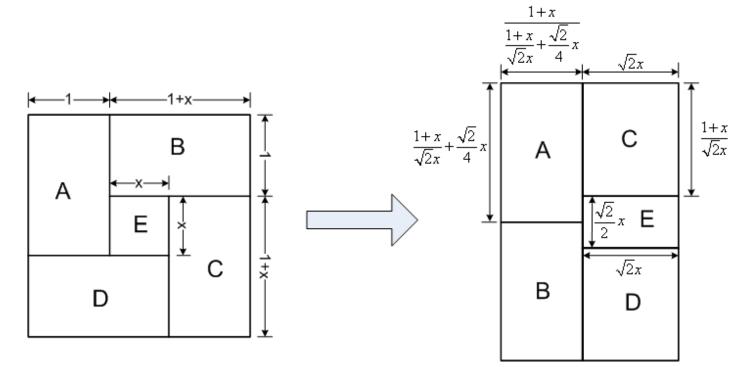
#### **Tightly Packed Wheel Floorplans**

- Tightly packed wheel floorplans
  - 5 blocks: A, B, C, and D are identical; E is a square
  - $0 \le x \le 1$ ; block aspect ratio is in [1/2,2]
- When  $0 \le x < 0.783$ 
  - There is a neighboring slicing floorplan with area at most 1.77% larger



#### **Tightly Packed Wheel Floorplans**

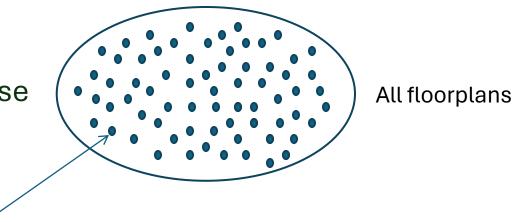
- When  $0.783 \le x \le 1$ 
  - The neighboring slicing floorplan can be packed with zero deadspace



#### Conjecture is still open

**Conjecture:** For each non-slicing floorplan, there exists a slicing floorplan with "similar" area and topology.

Are slicing floorplans "dense" among all floorplans like rational numbers are dense among real numbers?

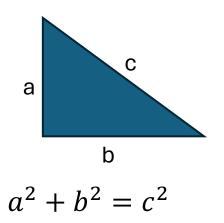


slicing floorplan

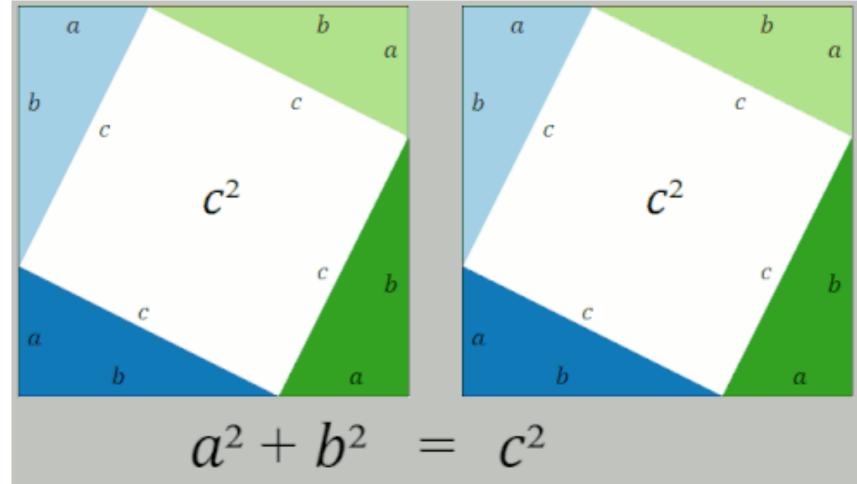
## Example 2

### **Geometry Helps**

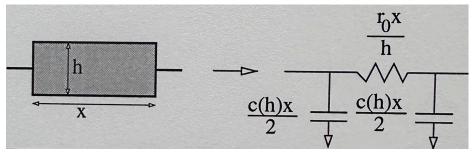
• Pythagoras Theorem



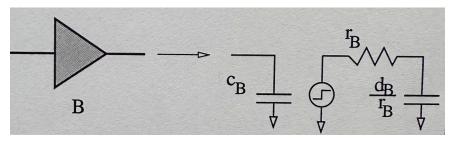
• Geometric Proof!



#### **Interconnect Optimization**



Wire Model



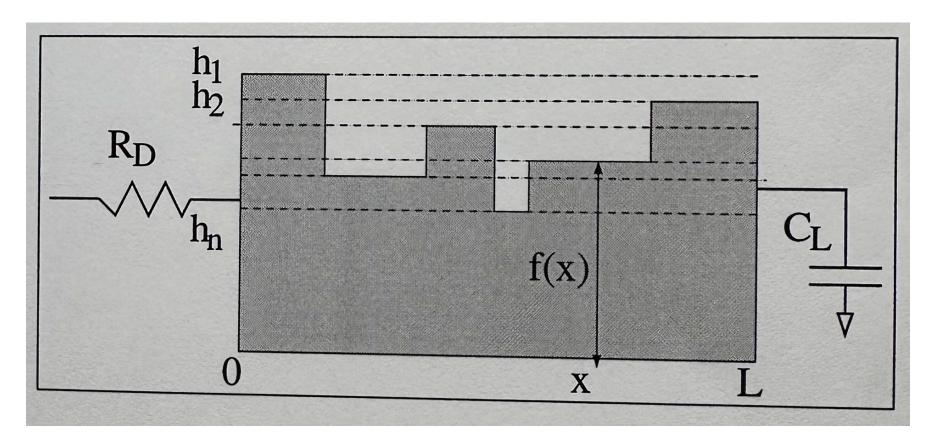
**Buffer Model** 

R<sub>d</sub>  $R_1$  $\mathbf{R}_2$  $C_{L}$ C  $C_1$  $T_d = R_d \left( C_1 + C_2 + C_L \right)$  $+ R_{I}(C_{I}+C_{2}+C_{I})$  $+ R_2(C_2 + C_I)$ 

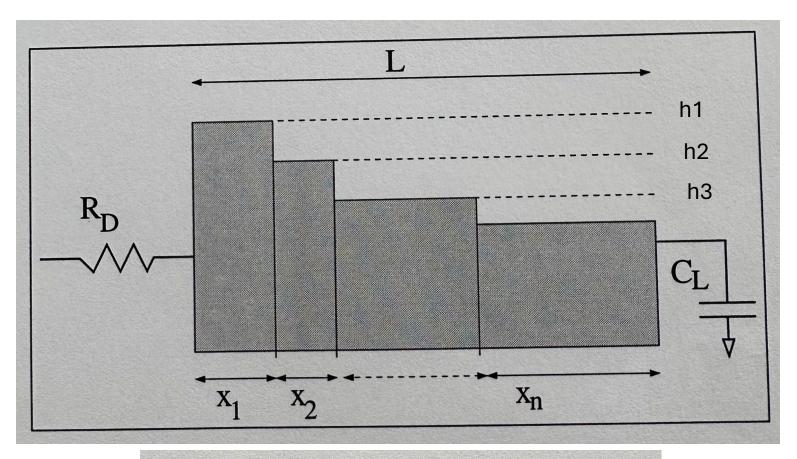
Elmore Delay Model

## Wire Sizing

- Fixed set of allowable wire widths: h1, h2, h3, ..., hn
- For continuous wire width, see closed form solution in PDW-96 (last PDW) and ISPD-97 (first ISPD)



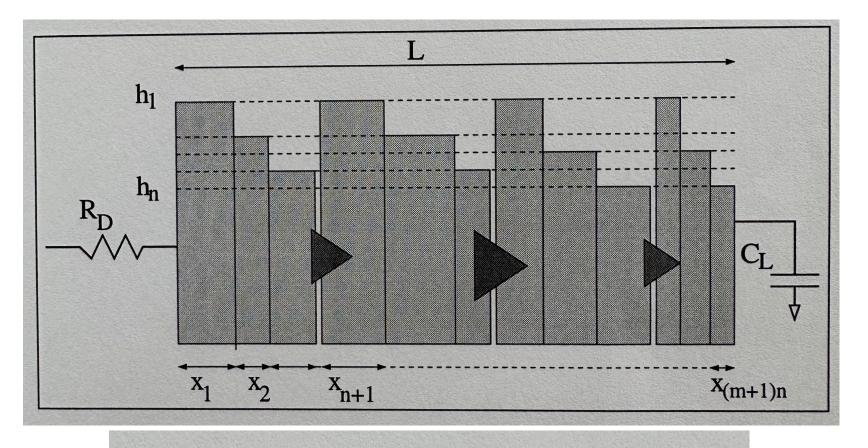
## Wire Sizing



$$d = \frac{1}{2}\mathbf{x}^{\mathrm{T}}\mathbf{A}\mathbf{x} + \mathbf{b}^{T}\mathbf{x} + R_{D}C_{L}$$

Ellipsoid!

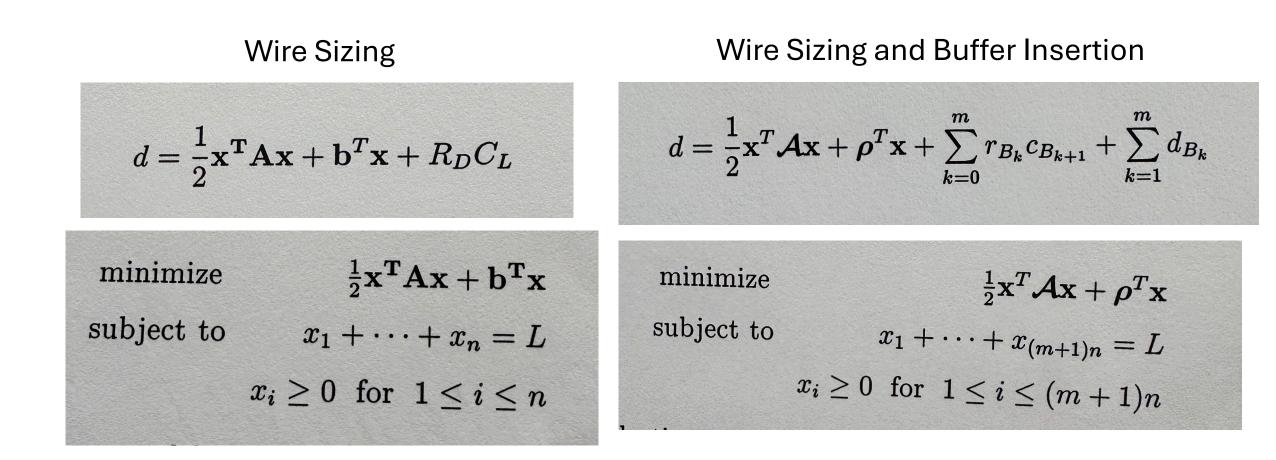
### Wire Sizing and Buffer Insertion



 $d = \frac{1}{2}\mathbf{x}^{T}\mathcal{A}\mathbf{x} + \boldsymbol{\rho}^{T}\mathbf{x} + \sum_{k=0}^{m} r_{B_{k}}c_{B_{k+1}} + \sum_{k=1}^{m} d_{B_{k}}$ 

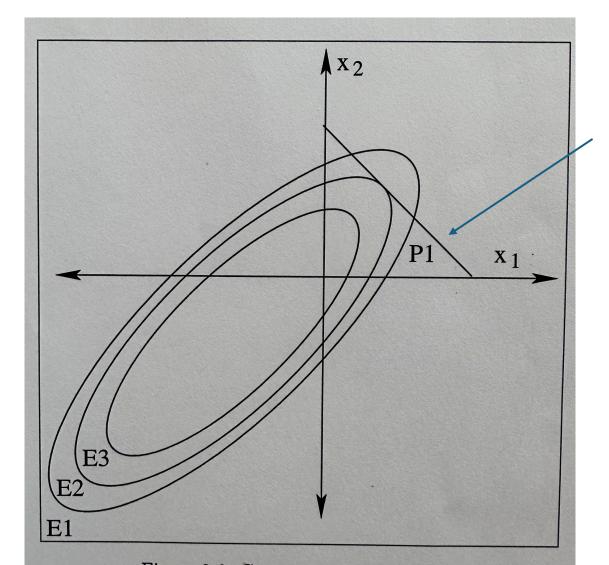
#### Ellipsoid!

#### **Mathematical Formulation**



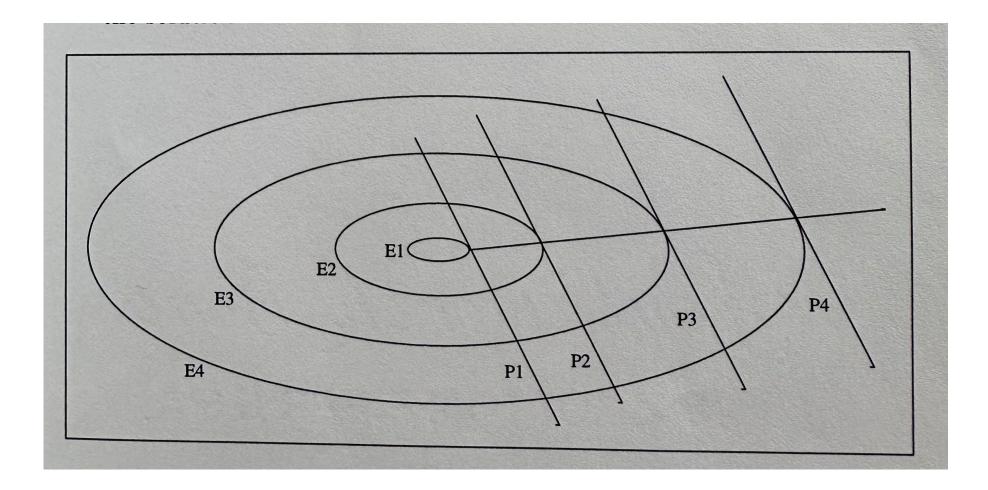
#### Tangent point is the solution

True only when L is not too small

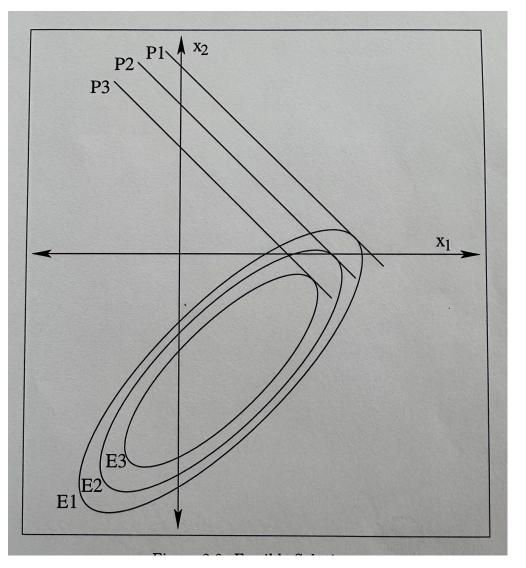


**P**1: X1 + X2 = L

# Tangent points and ellipsoid center all lie on the same line for all line length L



#### Tangent point may not be a physical solution when L is too small



- For all  $L \ge L0$ , all tangent points are physical solutions
- Solutions for various L are **linearly scaled** for  $L \ge L0$
- **Closed form solution** can be derived!

### Example 3

### **Elementary Proof**

- A mathematical proof that only uses "basic" techniques
- Prime Number Theorem:

 $\pi(x) \sim \frac{x}{\log x}$  where  $\pi(x)$  is the # of primes  $\leq x$ 

- First proof in 1896 by Hadamard and de la Vallee Poussin using sophisticated complex analysis (e.g., Rieman Zeta function)
- First **elementary proof** without using complex analysis was done in 1949 by Selberg and Erdos.

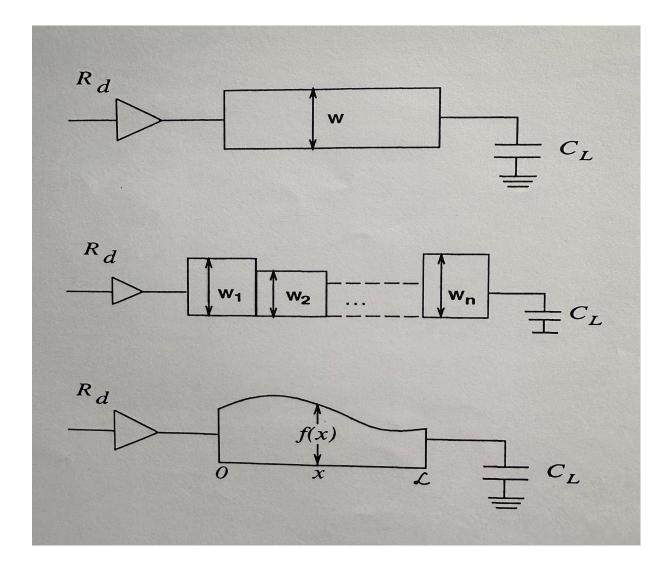
TEXTS AND MONOGRAPHS IN COMPUTER SCIENCE

#### BEAUTY IS OUR BUSINESS

A Birthday Salute to Edsger W. Dijkstra

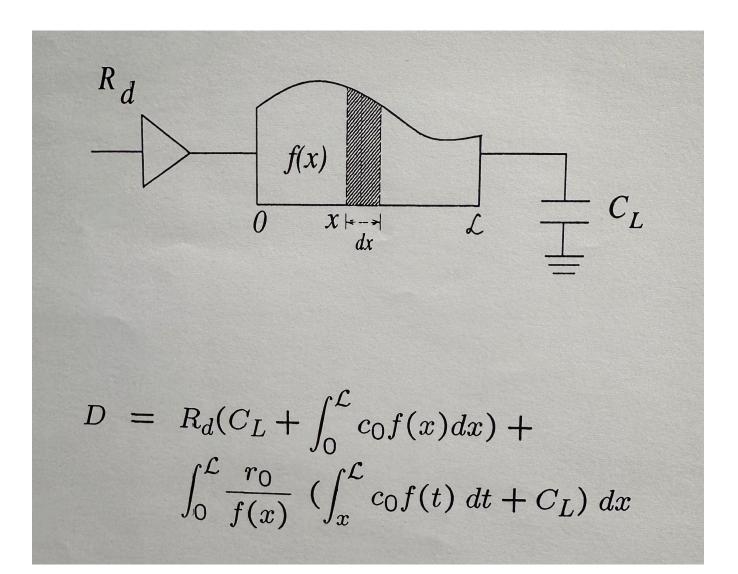
Edited by W.H.J. Feijen A.J.M. van Gasteren D. Gries J. Misra

#### Wire-Sizing for Delay Minimization

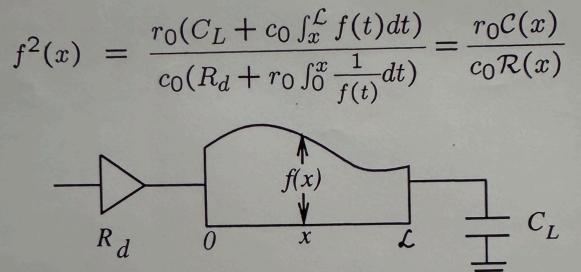


1996 ACM SIGDA Physical Design Workshop

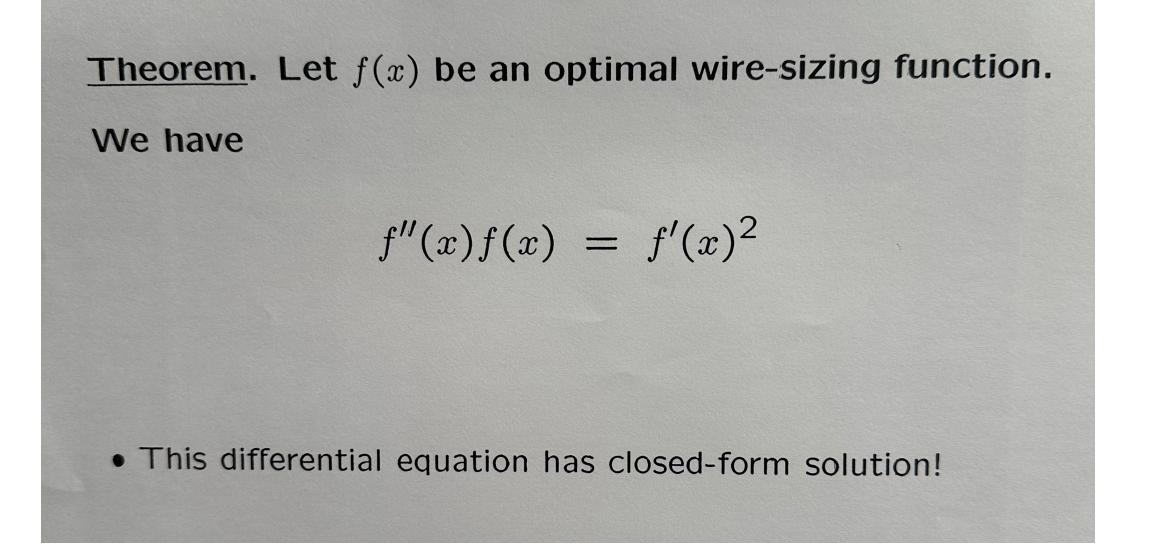
### **Elmore Delay**



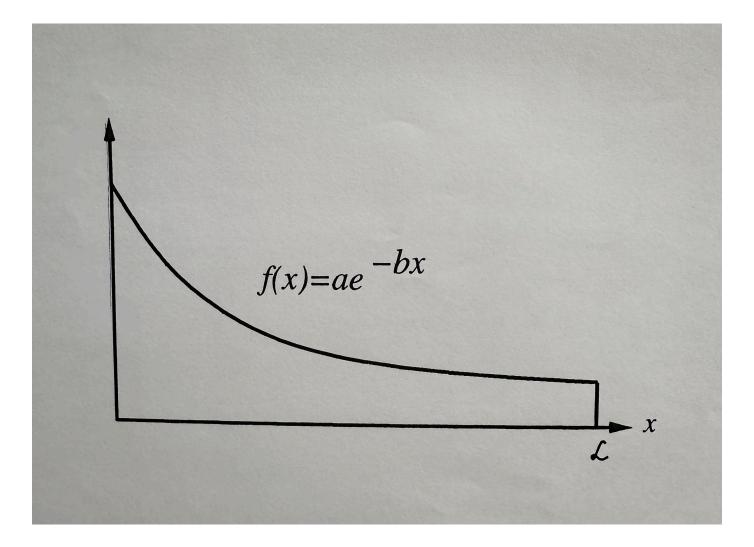
Theorem. Let f be an optimal wire-sizing function. We have



C(x) = Downstream Capacitance  $\mathcal{R}(x) =$  Upstream Resistance



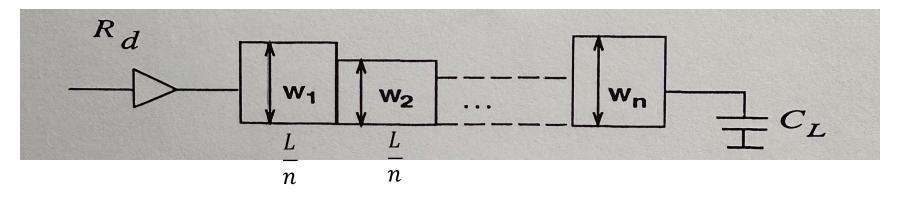
#### **Optimal Wire-Sizing Function**



# Any **elementary proof** that exponential wire shape is optimal?

- Calculus of Variation (Fishburn and Schevon 1995)
- Ordinary Differential Equation (Chen and Wong 1996)
- Can we do it without using Calculus?

#### **Elementary Proof**



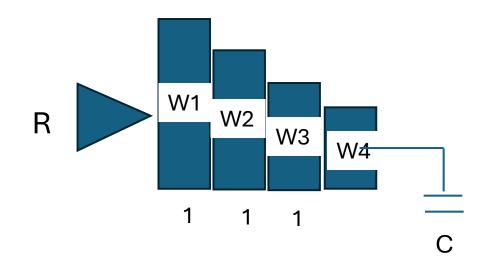
**Proof Sketch** 

- 1. W1  $\geq$  W2  $\geq$  ...  $\geq$  Wn
- 2. Uniform delay at each segment (d1 = d2 = d3 = .... = dn = d)
- 3. W2/W1 = W3/W2 = ... = Wn-1/Wn = d/(d+h) where h = L/n
- 4. d/(d+h) = D/n (D/n + L/n) = D/(D+L) = r < 1
- 5. Wi =  $r^{n-i}$ Wn = K  $r^{n-i}$
- 6. As  $n \rightarrow \infty$ , W(x) = K  $r^{L-X}$  = A  $e^{-BX}$

### Step 3

- D = R (w1 + w2 + ... + wn + C)
- (1) +1/x1(x2 + x3 + x4 + C) (= d)
- (2) +1/x2(x3 + x4 + C) (= d)
- (3) +1/X3(x4+C) (= d)

(4) + C/x4 (= d)



Rewrite (2):

Sub into (1):

Rewrite (3):

Sub into (2):

Rewrite (4):

Sub into (1):

- d = x1/x2 (x3/x1 + x4/x1 + C/x1) $d = (1+d) x2/x1 \rightarrow x2/x1 = d/(1+d)$
- d = (x4/x2 + C/x2) x2/x3
- $d = (1+d) \times 3/x2 \rightarrow \frac{x3}{x2} = \frac{d}{(1+d)}$
- d = C/x4 = x3/x4 (C/x3)
- $d = x4/x3 (1+d) \rightarrow x4/x3 = d/(1+d)$

#### Conclusion

- My math background had indirectly influenced my research style and approach
- Presented some unpublished observations/results
- Three 3 examples
  - Rational numbers vs Real numbers  $\rightarrow$  Slicing floorplans vs All floorplans
  - Geometry helps  $\rightarrow$  Geometric approach to interconnect optimization
  - Elementary proof  $\rightarrow$  Exponential wire shape is optimal



The End	