Pioneering Contributions of Professor Martin D. F. Wong to Automatic Floorplan Design

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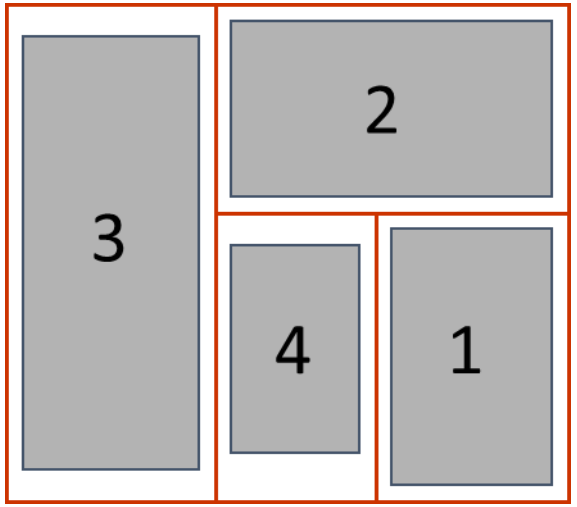
ISPD 2024

Outline

- Introduction
- Slicing Floorplan Design
- Non-slicing Floorplan Design
- Conclusion

Introduction

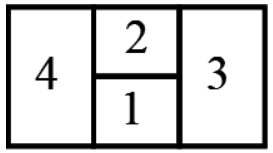
- Floorplan design is to allocate spaces to circuit modules in a chip to minimize some cost measure.



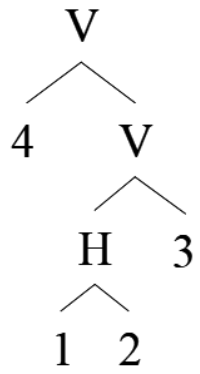
- Two types of floorplans: slicing and non-slicing floorplans

Slicing Floorplan & (Skewed) Slicing Tree

- The hierarchical structure of a slicing floorplan can be described by a slicing tree.
- A slicing tree is skewed if there is no node and its right child have the same cut type.
- Every slicing floorplan has a unique skewed slicing tree, but a skewed slicing tree may represent more than one slicing floorplan (as no dimensional information is associated with each internal node).
- The set of slicing floorplans for n modules can be partitioned into equivalent classes, where each class of slicing floorplans corresponds to a different skewed slicing tree with n leaves.



(a)



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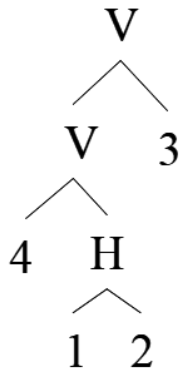
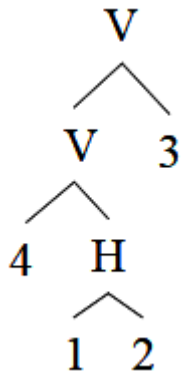


(c)

Normalized Polish Expression
[DAC 1986]

- For a skewed slicing tree, the corresponding normalized Polish expression is defined and obtained by performing the postorder traversal of the tree.
- There is a 1-1 correspondence between the set of normalized Polish expressions and the set of skewed slicing trees.



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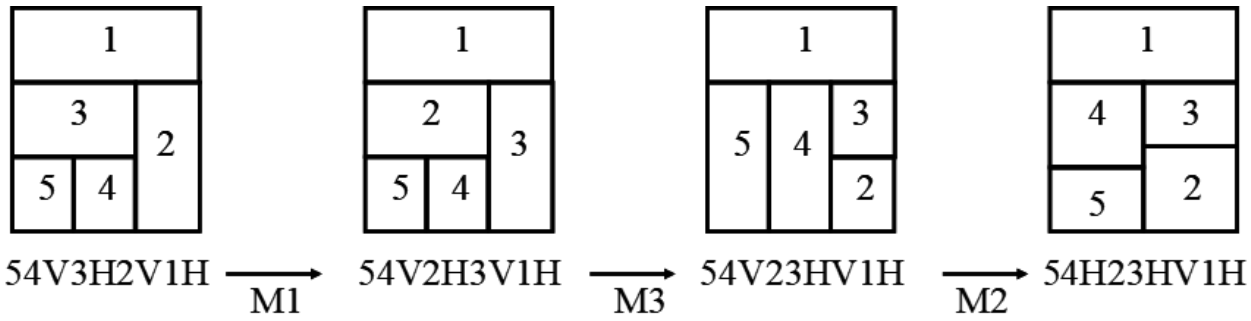
Simulated Annealing based Slicing Floorplan Design
[DAC 1986]

- The Wong-Liu algorithm employs the technique of simulated annealing to simultaneously minimize the floorplan area and the total wirelength.
- It uses the set of normalized Polish expressions as the solution space.
- Three types of moves, M_1, M_2, and M_3, are used to modify a normalized Polish expression and get a neighboring one.
  - M_1: Swap two adjacent modules.
  - M_2: Complement a chain of cuts.
  - M_3: Swap two adjacent module and cut.

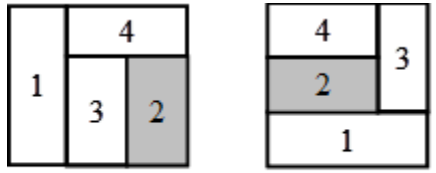


Simulated Annealing based Slicing Floorplan Design [DAC 1986]

- Cost function (to evaluate a normalized Polish expression)
  - $\Phi = A + \lambda W$
    - A: area of a minimum-area floorplan
    - W: total wirelength of a minimum-area floorplan
    - λ: user-specified parameter
- The calculation of a minimum-area floorplan can be efficiently done in an incremental manner.

Slicing Floorplan Design Considering Boundary Constraints
[ASP-DAC 1999]

- A boundary constraint enforces some modules to be positioned along one of the four sides of the floorplan.
  - For example, for the two slicing floorplans shown in figures (a) and (b), if module 2 is constrained to be placed along the left boundary, then the one in Figure (a) is infeasible while the one in Figure (b) is feasible.

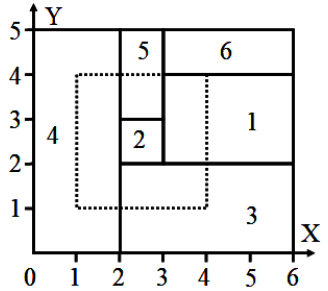


(a) (b)

- To evaluate a normalized polish expression
  - It checks a normalized Polish expression to see whether the given boundary constraints are satisfied.
  - It fixes the violated constraints (if any) as much as possible, and includes in the cost function a term to penalize the remaining violations.

Slicing Floorplan Design Considering Range Constraints
[ISPD 1999]

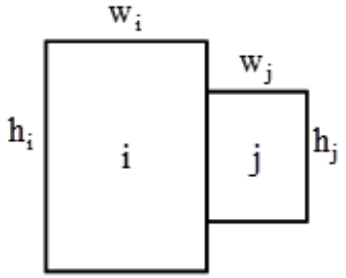
- A range constraint enforces a module to be placed within a given rectangular region in the floorplan.
  - Example: module 1 with a pre-placed constraint must be placed with its lower left comer at (3, 2) and module 2 with a range constraint must be placed within the dotted-line region.



- To evaluate a normalized polish expression
  - It computes the range constraint and dimensional information of each sub-floorplan
  - If not all range constraints are satisfied, it adds into the cost function a penalty term which is measured by the total distance of the modules having range constraints from their desired regions.

Slicing Floorplan Design Considering Abutment Constraints
[TCAD 2001]

- An abutment constraint enforces some modules to abut
  - A horizontal abutment example

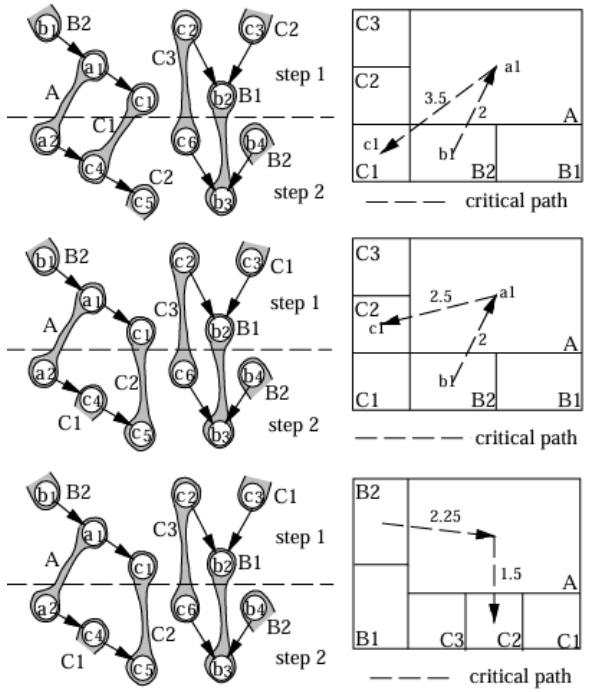


- To evaluate a normalized polish expression
  - It scans the expression once to find the top, bottom, left, and right neighbors of every module.
  - Once the neighbors of each module are known, each abutment constraint is checked
  - If not all abutment constraints are satisfied, it will swap modules to satisfy the abutment constraints as much as possible.
  - If some constraints are still violated after all the possible swappings, a penalty term is added in the cost function to penalize those violations.

Reference: F. Y. Young, H. H. Yang, and D. F. Wong. On extending slicing floorplans to handle L/T-shaped modules and abutment constraints. TCAD 2001.

Slicing Floorplan Design Considering Functional-Unit Binding
[ICCAD 1994]

- It uses a performance-driven binding algorithm as part of the procedure for cost function evaluation.



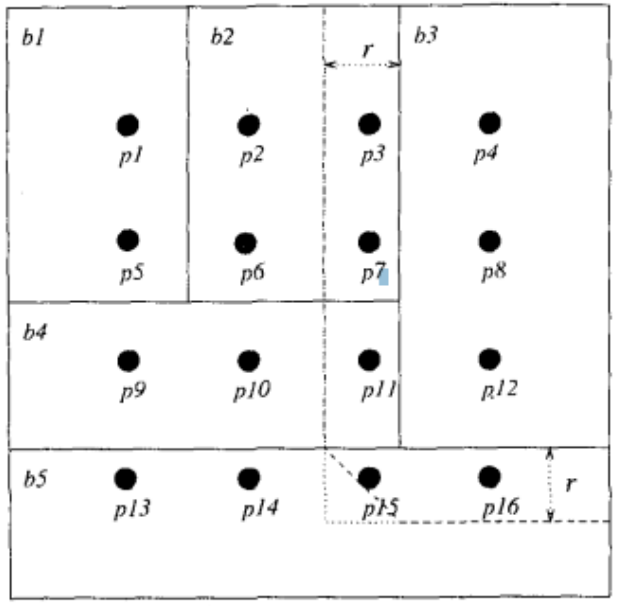
(a) Original binding

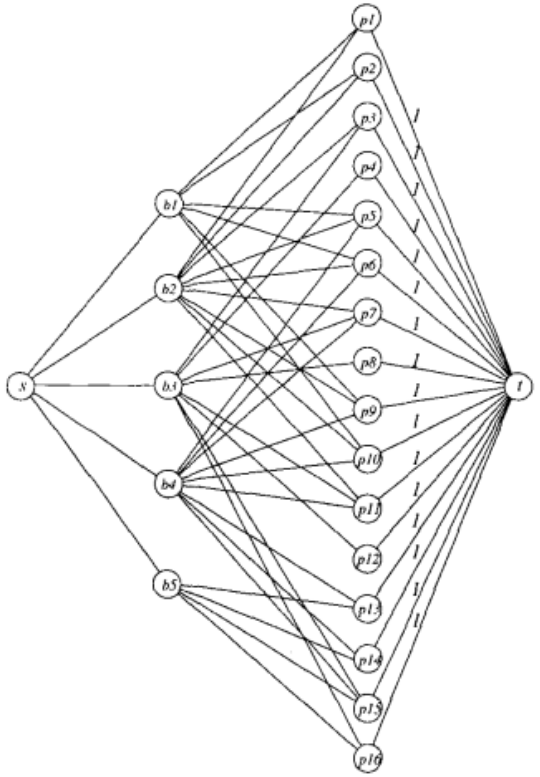
(b) New binding

(c) New binding + new floorplan

Slicing Floorplan Design Considering Power Supply Planning
[ASP-DAC 2001]

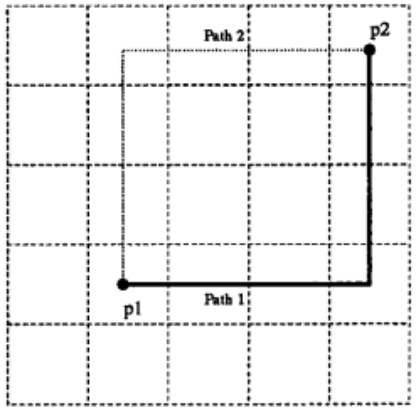
- A power supply planning algorithm based on network flow is incorporated.

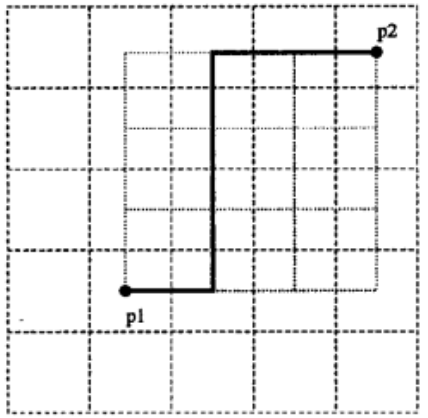




Slicing Floorplan Design Considering Interconnect Planning
[ICCAD 1999]

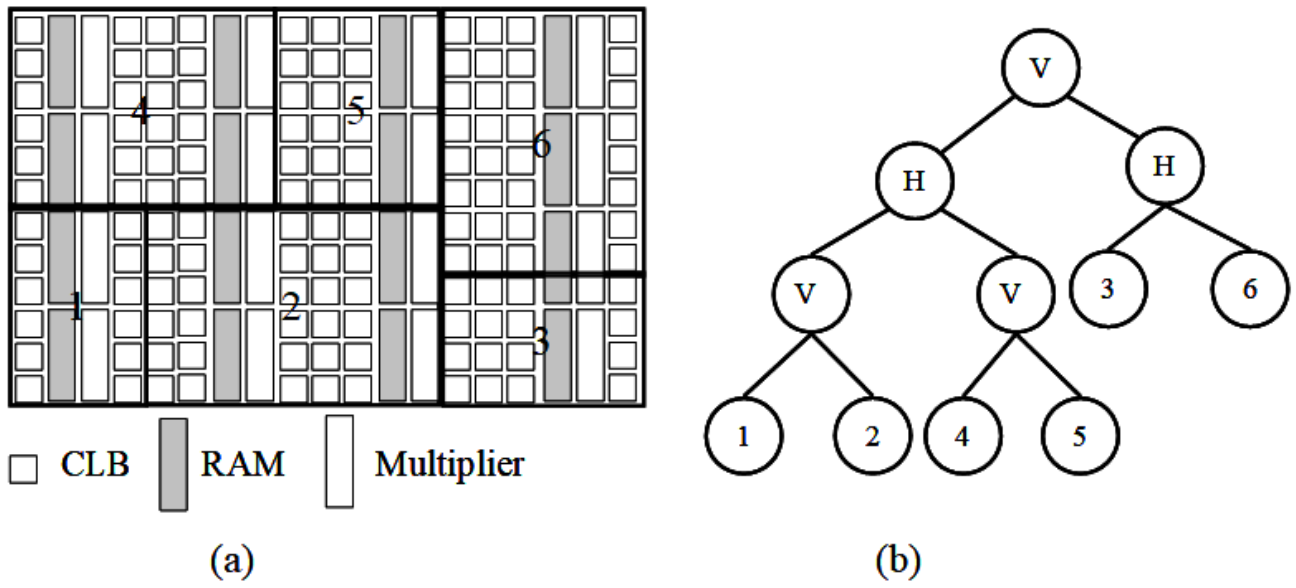
- Interconnect planning involves pin assignment, followed by simple-geometry routing based on L-shaped and Z-shaped wires.
- Multi-stage simulated annealing with different wirelength functions.
  1. When temperature is high: HPWL
  2. When temperature is medium: L-shaped wire length
  3. When temperature is low: Z-shaped wire length





Slicing Floorplan Design for FPGAs
[ICCAD 2004]

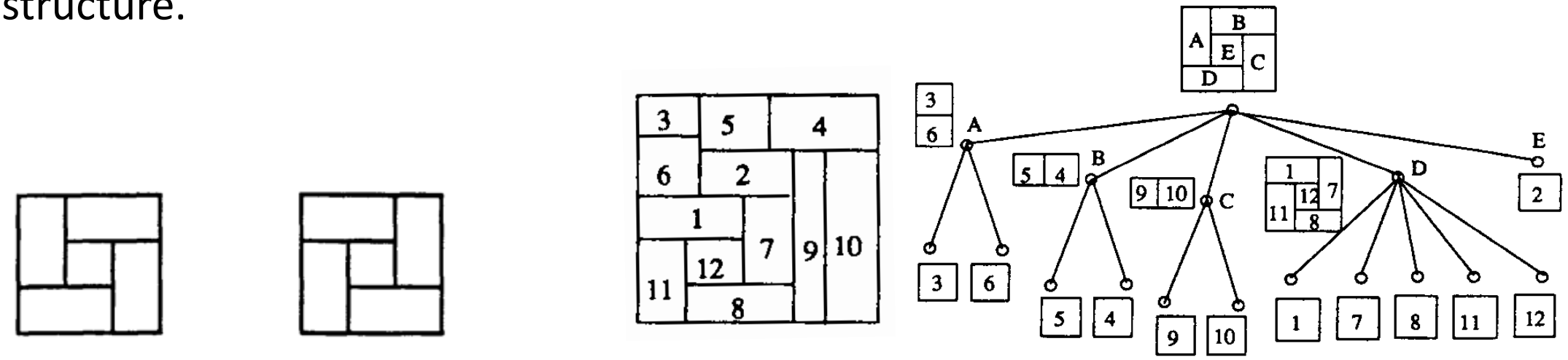
- It non-trivially extends prior slicing floorplan area optimization algorithms to find the optimal realization for each slicing tree.



Reference: L. Cheng and M. D. F. Wong Floorplan design for multimillion gate FPGAs. ICCAD 2004.

Non-Slicing Floorplan Design
[ICCAD 1989]

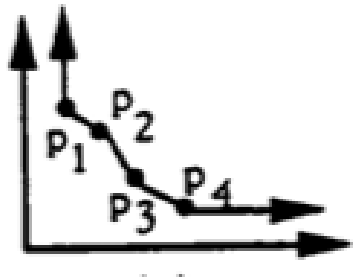
- Hierarchical floorplans of order 5: A special class of non-slicing floorplans, each of which can be obtained by recursively partitioning a rectangle into two parts by either a vertical line or a horizontal line or into five parts by a wheel.
- A natural but non-trivial extension of the Wong-Liu algorithm based on new floorplan representation (2-5 normalized Polish expression) and neighborhood structure.



(a) (b)

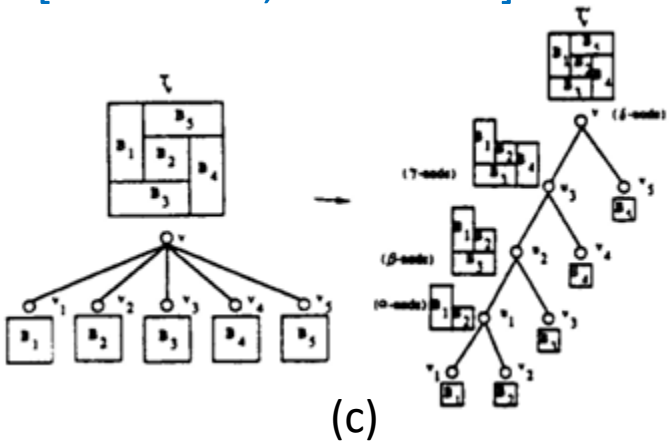
Area Optimization for Non-Slicing Floorplans

- Floorplan area optimization: Given a floorplan tree representing a hierarchical floorplan of order 5, determine the shape for each module such that the area of the floorplan is minimized.
  - Version 1: An infinite number of shapes for each module (a piecewise linear shape curve with a finite number of corners) [DAC 1989, EURO-DAC 1991]
  - Version 2: A finite number of shapes for each module [DAC 1990, DAC 1992]



(a)

(b)



(c)

References: D. F. Wong and P. Sakhamuri. Efficient floorplan area optimization. DAC 1989.
T.-C. Wang and D. F. Wong. An optima algorithm for floorplan area optimization. DAC 1990.
T.-C. Wang and D. F. Wong. Efficient shape curve construction in floorplan design. EURO-DAC 1991.
T.-C. Wang and D. F. Wong. A graph theoretic technique to speed up floorplan area optimization. DAC1992.

Conclusion

- Some of Prof. Wong's pioneering works in automatic floorplan design were highlighted.
- His contributions have not only advanced the field but have also served as inspirational sources for other researchers, including myself.
- Congratulations to Prof. Wong on receiving the ISPD 2024 Lifetime Achievement Award!