3Dblox:
Unleashing The Ultimate 3DIC Design Productivity

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Design Technology Platform
Outline

• Chiplet Architecture Complexity Drives For Advanced Solutions
• The 3Dblox Standard
• Key Productivity Features
• Summary
Abundant Choices of 3DIC Architectures

Design Complexity Is On The Rise!

TSMC 3DFabric™

- CoWoS®-S
- InFO-2D

- CoWoS®-L
- InFO-2D

- CoWoS®-R
- InFO-3D

TSMC-SolC®

WoW

1-Die

2-Die

3-Die

DTC / eDTC

IPD

iCap

RDL Interposer

- TSV
- TIV
- TMV

SolC Bond™

uBump

PM

BGA

C4

Interfaces

Active Dies

Passive Dies

Horizontal 2.5D Connection

Vertical 3D Connection

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Current 3DIC Design Representations

A Fragmented Design Ecosystem!

<table>
<thead>
<tr>
<th>Vendor A</th>
<th>Vendor B</th>
<th>Vendor C</th>
<th>Vendor D</th>
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<tbody>
<tr>
<td>PDN</td>
<td>PV</td>
<td>PDN / Thermal</td>
<td>APR</td>
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<td>APR</td>
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<td>RCX</td>
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<tr>
<th>Format</th>
<th>Physical-based</th>
<th>Connection-based</th>
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<tbody>
<tr>
<td>Logical connection</td>
<td>X</td>
<td>V</td>
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<tr>
<td>V</td>
<td>X</td>
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Mission Statements

• Find a way to **modularize** design and EDA tools to make 3DIC design flow simpler and efficient

• Ensure **standardized** EDA tools and design flows compliant to TSMC 3DFabric™ technology

3Dblox Standard
from TSMC & our OIP Partners
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Tackle Complexity with Eco-system Unification

- Top-Down Design Methodology
- 3Dblox Standard
- Inter-operability
- Modularization
- Chiplet Reuse

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<th>Connection-based</th>
<th>3Dblox</th>
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<tr>
<td>3D locations</td>
<td>V</td>
<td>X</td>
<td>V</td>
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<td>Logical Connection</td>
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<td>V</td>
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<tr>
<td>Assertions</td>
<td>X</td>
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<td>Hierarchical</td>
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</tr>
</tbody>
</table>
3Dblox Standard

- Generic 3Dblox language constructs aim for all current and future 3DFabric™ offerings.

3Dblox Components
- Die Interface
- RDL Interface
- Bridge Interface

3Dblox Language Constructs

Physical Constructs
Chiplet:
- List of physical

Connection Constructs
Conn:
- Chiplet ➔ Chiplet

3Dblox Full Stack Representations

Full Stack - Physical
- Chiplet 1
- Chiplet 2
- Chiplet 3

Full Stack - Connection
- Conn1: Chiplet 1 & 3
- Conn2: Chiplet 2 & 3

Path Assertions
- Path1: Chiplet 1 ➔ Chiplet 2
3Dblox Innovation – Full 3DIC Representation

- Captures key logical and physical information in 3DFabric™ designs.
- Pre-binds collaterals at the right silicon / RDL and interfaces.
- Assertions to enforce top-down design correctness.
- Support chiplet design reuse.
CoWoS-S Step-by-Step with 3Dblox

Path Assertion

Connectivity Declaration

Chiplet Instantiation

Chiplet Definition

SOC1
SOC2
HBM1

SOC1/r1
SOC2/r2
HBM1/r5
RDL1/r1
RDL1/r2
RDL1/r3
RDL1/r4
RDL1/r5
RDL1/r6

RDL1

SOC2
SOC1
HBM1

SOC2/r3
HBM1/r5

SOC1/r1
SOC2/r3
SOC1/r1
RDL1/r2
RDL1/r6

RDL1

RDL2

3Dblox Definitions
SOC
3Dblox Definition
HBM
3Dblox Definition
RDL

Instances
SOC1
SOC2
HBM1
RDL1

3Dblox - S Step - by - Step with 3Dblox

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TSMC Property

Unleash Innovation
CoWoS-L Example with Complex Structures

- 3Dblox models connectivity relationship explicitly with connection objects
- Transitive connectivity relationship builds full system connectivity

Connection Object Explicitly Defines Interface

Chiplets Relationship Derived From Connection Objects
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Interposer Hierarchy Auto-Creation

- Interposer Verilog hierarchy auto-creation to facilitate interposer design and verification
Interposer Auto-Routing

- Interposer Verilog hierarchy with TSMC technology files enables both silicon and RDL auto-routing.
One Format, Multiple Products

- One 3Dblox representation for all downstream analyses
- Replace hundreds of repetitive codes for each tool

Support from all EDA vendors creates unified design ecosystem
TSMC Offers 3Dblox Design Templates

Target Architecture

- Chiplet Definitions
- Interface Definitions
- Tech File Bindings
- Physical Assertions
- Path Assertions

TSMC 3Dblox

3Dblox Design Templates:
- CoWoS-S
- CoWoS-R
- CoWoS-L
- InFO-PoP
- InFO-2D
- InFO-3D
- SoIC-CoW
- SoIC-WoW
3Dblox Design Template Bootstrap Design Starts

1. Define die stackings
2. Bind DRC/LVS/APR/RCX/Thermal tech files
3. Define interface
4. Bind interface DRC/LVS
5. Define connectivity among dies
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Summary

• Modularized 3Dblox language constructs – chiplet, interface, and connection

• Language constructs designed to model all current and future 3DIC structures. Find 3dblox from http://3dblox.org

• Streamline EDA design flow and promote interoperability

• 3Dblox is open to all partners, customers, foundries and OSAT

Collaboration with OIP Partners Unleashes the Ultimate 3DIC Design Productivity!