Unleash Innovation

3Dblox:

Unleashing The Ultimate 3DIC Design Productivity

Jim Chang, Ph.D.

Deputy Director, 3DIC Design Methodology
Design Technology Platform

Outline

- Chiplet Architecture Complexity Drives For Advanced Solutions
- The 3Dblox Standard
- Key Productivity Features
- Summary

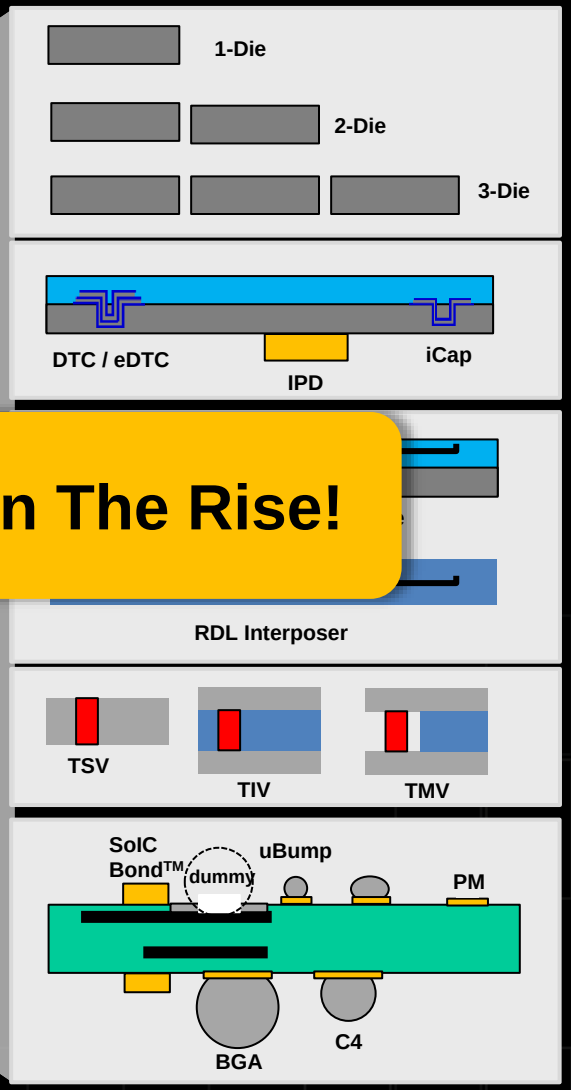
Abundant Choices of 3DIC Architectures

Unleash Innovation

TSMC 3DFabric™

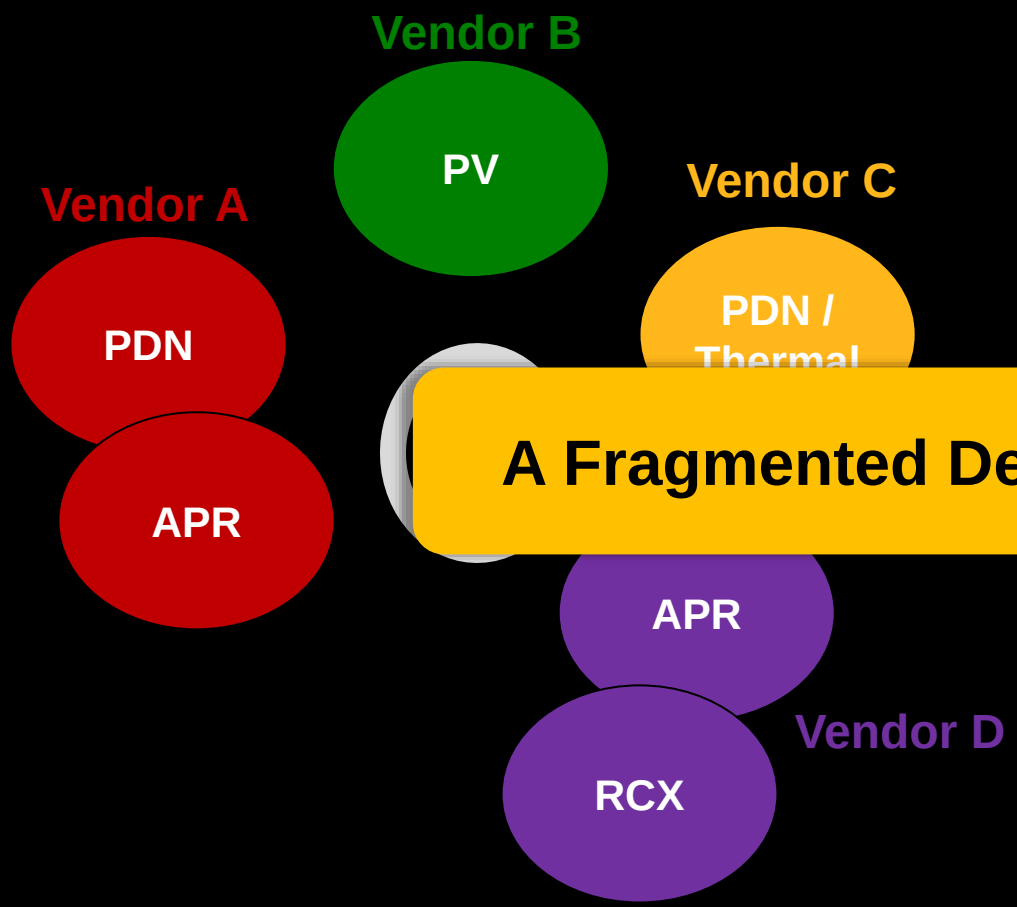
- CoWoS®-S
- InFO
- CoWoS®-L
- InFO-2D
- CoWoS®-R
- InFO-3D
- TSMC-SoIC® WoW

Design Complexity Is On The Rise!



- Active Dies
- Passive Dies
- Horizontal 2.5D Connection
- Vertical 3D Connection
- Interfaces

Current 3DIC Design Representations



A Fragmented Design Ecosystem!

Format	Physical-based	Connection-based
	V	X
connection	X	V

Mission Statements

- Find a way to modularize design and EDA tools to make 3DIC design flow simpler and efficient

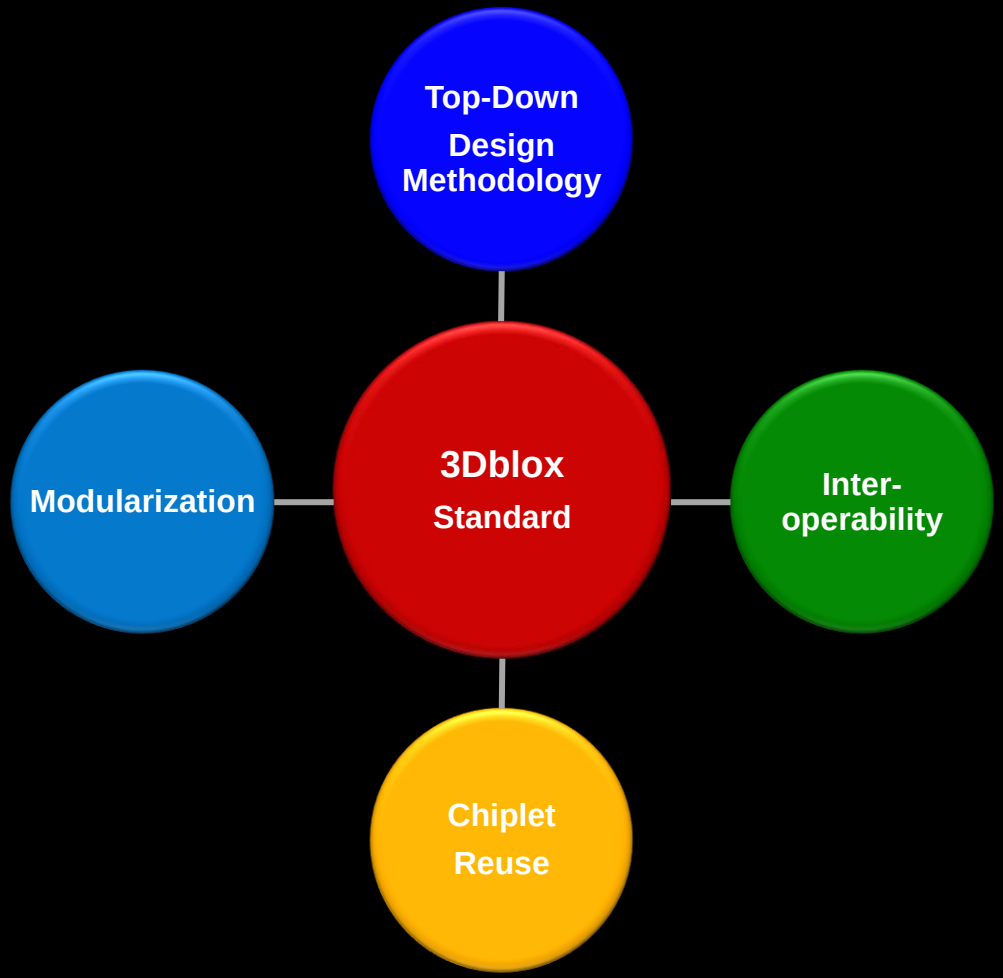
- Ensure standardized EDA tools and design flows compliant to TSMC 3DFabric™ technology

3Dblox Standard
from TSMC & our OIP Partners

Outline

- Chiplet Architecture Complexity Drives For Advanced Solutions
- The 3Dblox Standard
- Key Productivity Features
- Summary

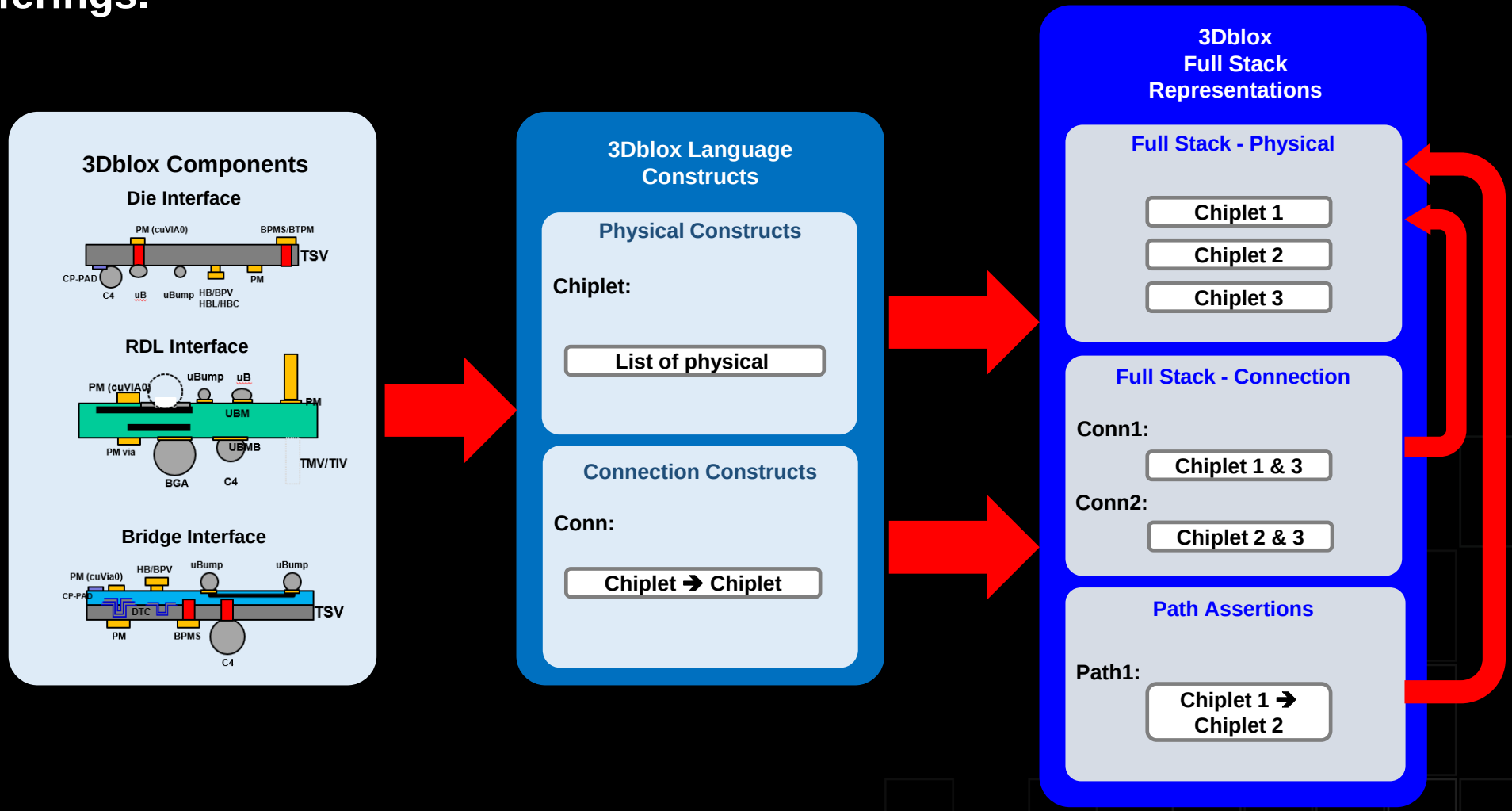
Tackle Complexity with Eco-system Unification



Format	Physical-based	Connection-based	3Dblox
3D locations	V	X	V
Logical Connection	X	V	V
Assertions	X	X	V
Hierarchical	X	X	V

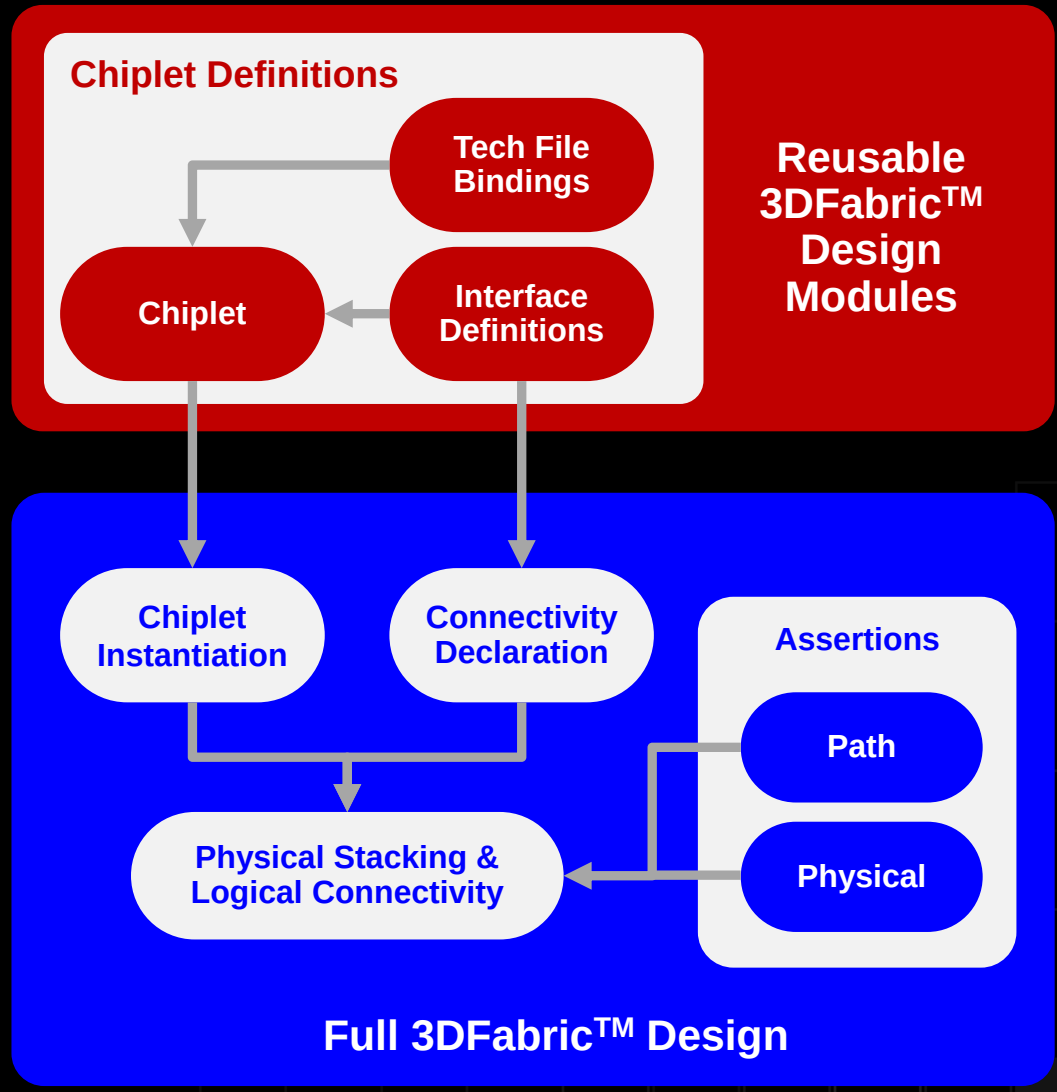
3Dblox Standard

- Generic 3Dblox language constructs aim for all current and future 3DFabric™ offerings.

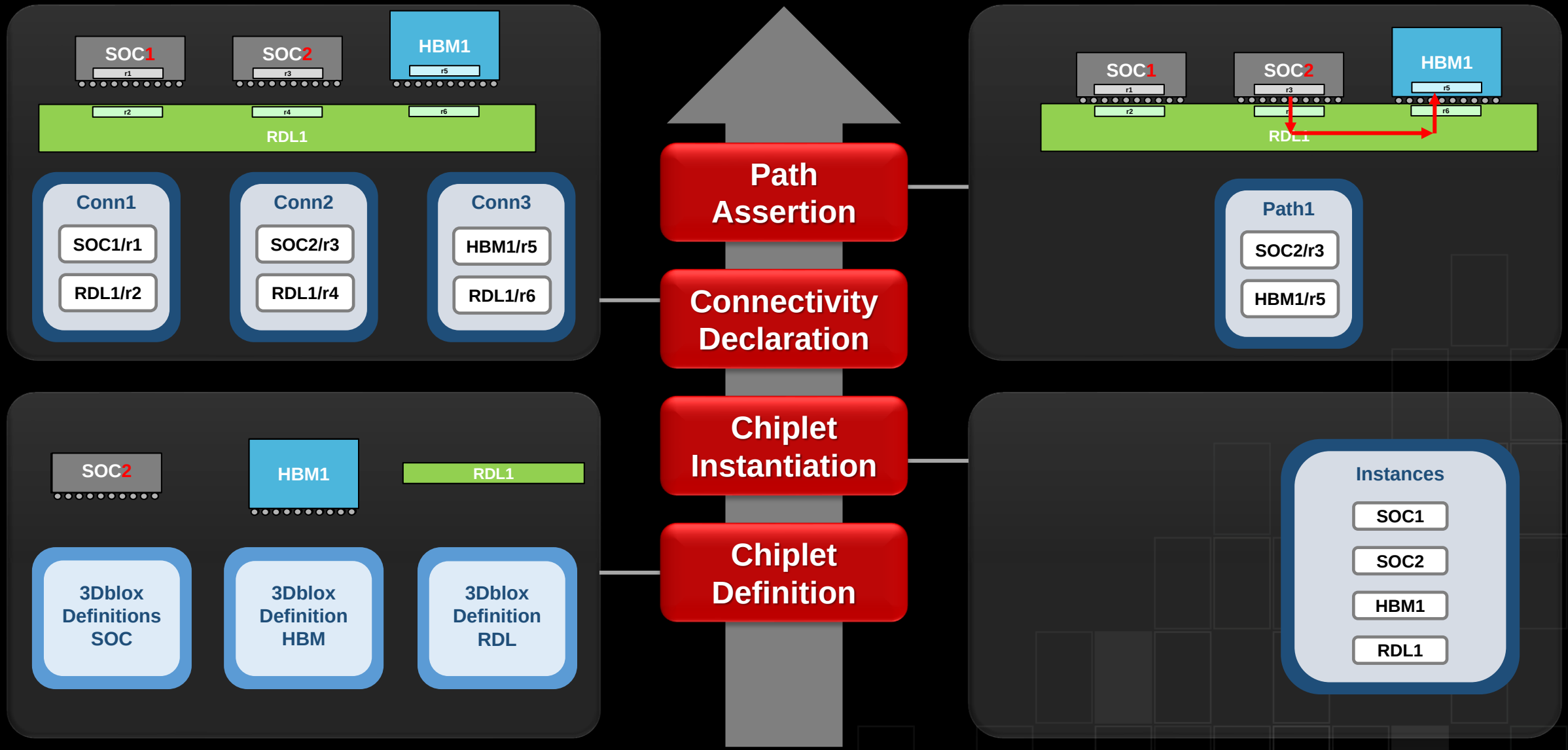


3Dblox Innovation – Full 3DIC Representation

- Captures key logical and physical information in 3DFabric™ designs.
- Pre-binds collaterals at the right silicon / RDL and interfaces.
- Assertions to enforce top-down design correctness.
- Support chiplet design reuse.

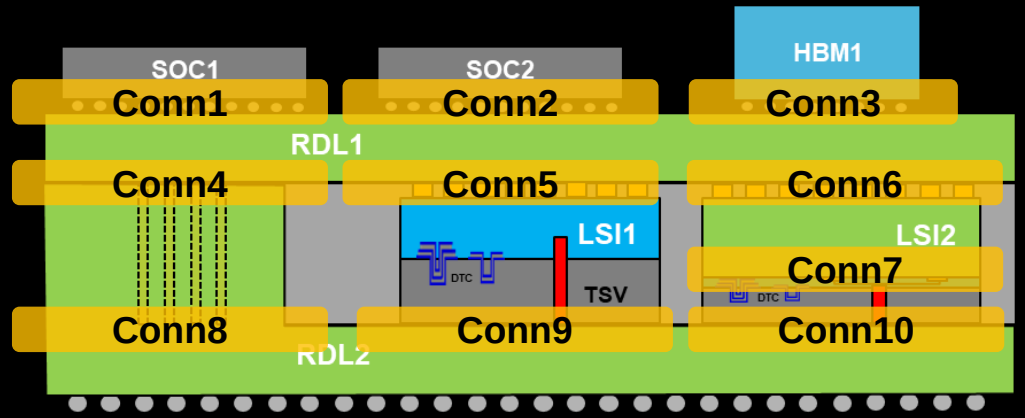


CoWoS-S Step-by-Step with 3Dblox

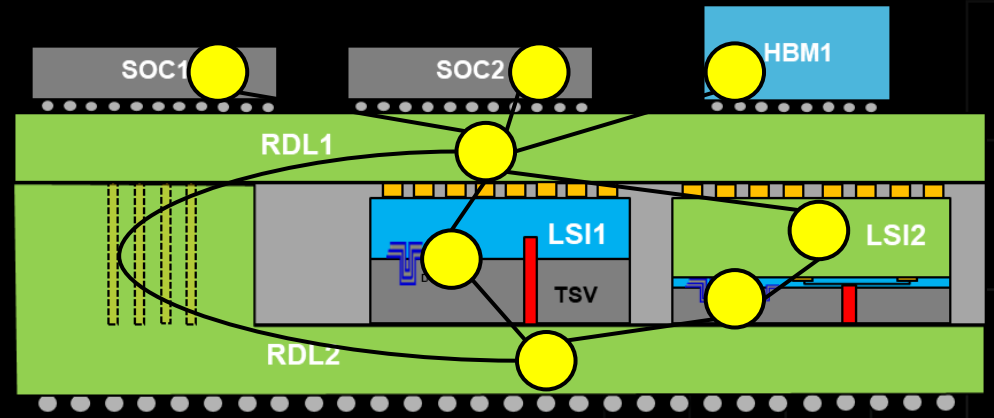


CoWoS-L Example with Complex Structures

- 3Dblox models connectivity relationship explicitly with connection objects
- Transitive connectivity relationship builds full system connectivity



Connection Object Explicitly Defines Interface



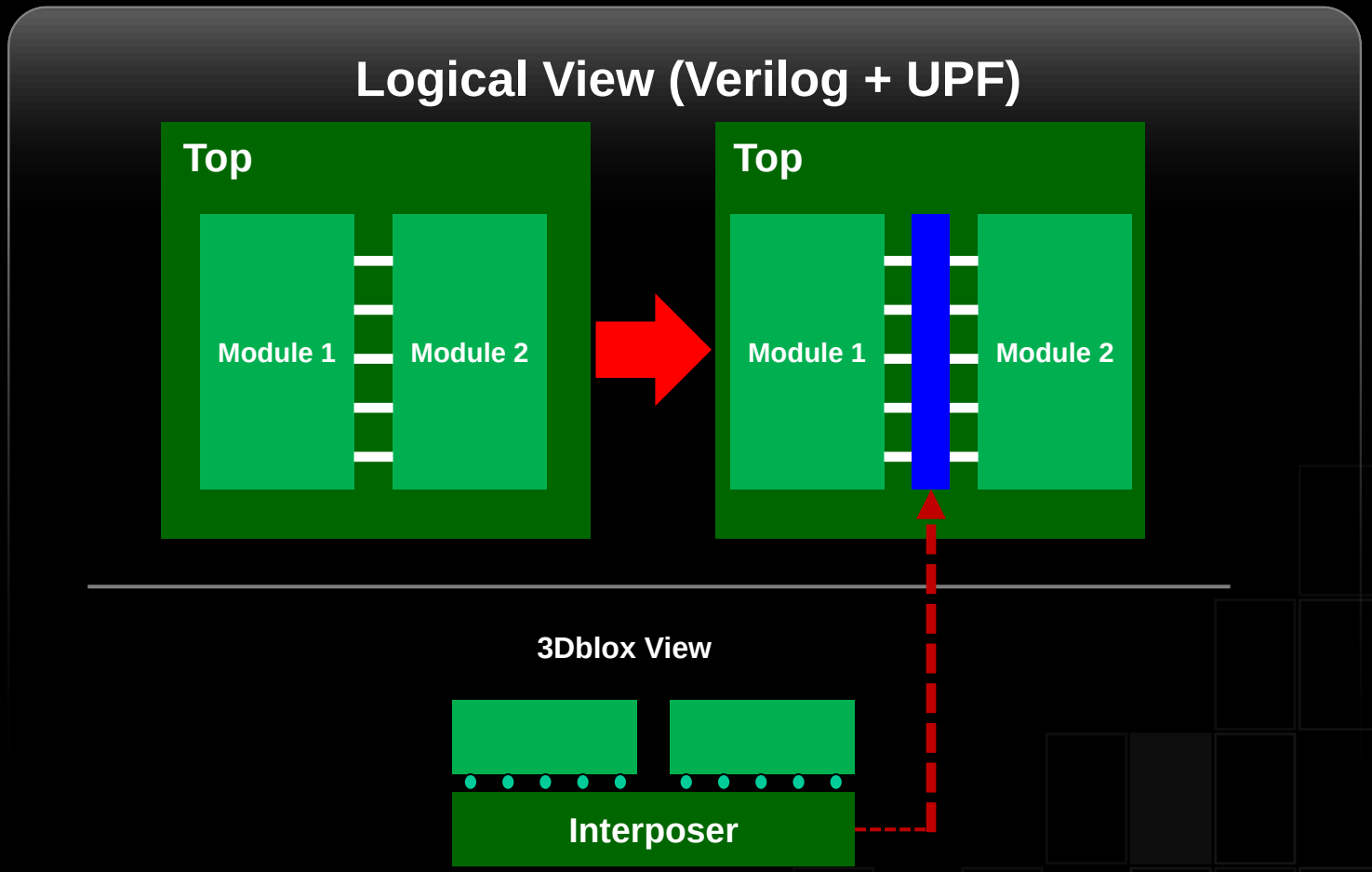
Chiplets Relationship Derived From Connection Objects

Outline

- Chiplet Architecture Complexity Drives For Advanced Solutions
- The 3Dblox Standard
- Key Productivity Features
- Summary

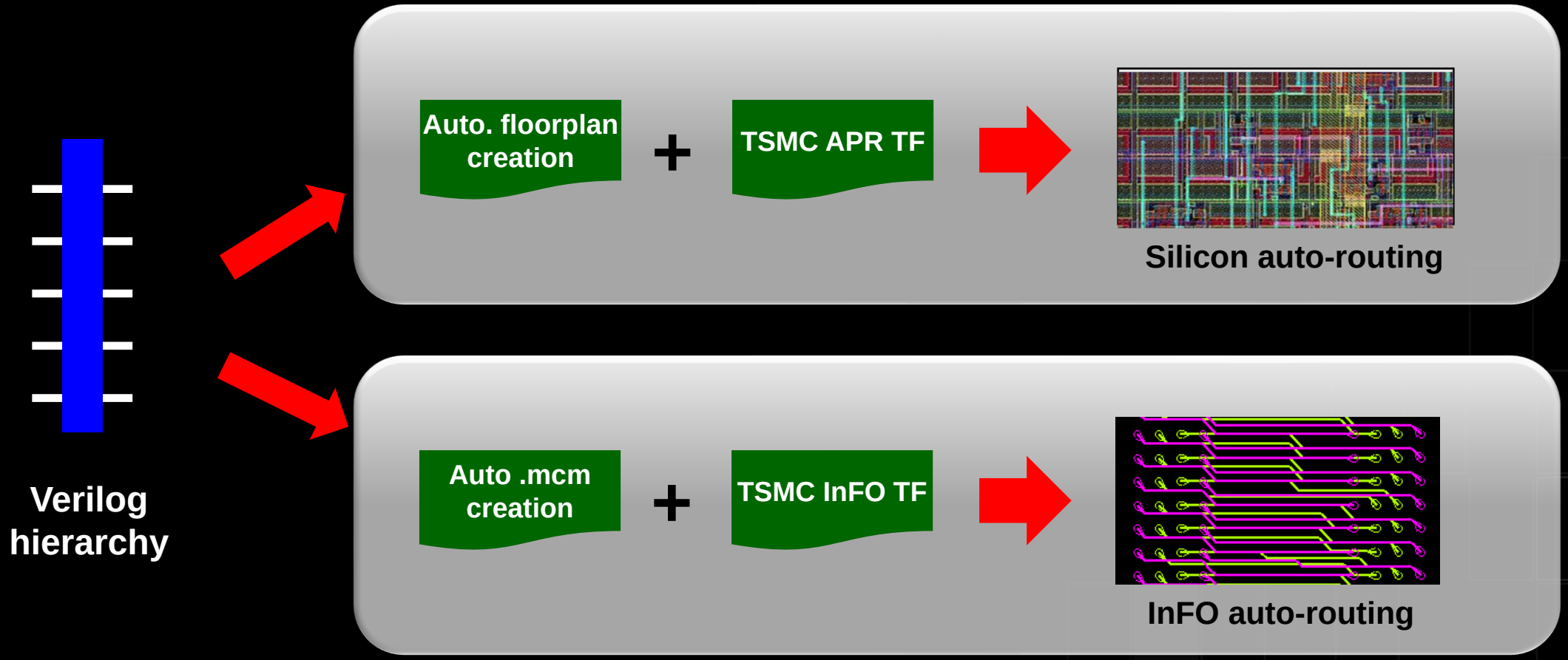
Interposer Hierarchy Auto-Creation

- Interposer Verilog hierarchy auto-creation to facilitate interposer design and verification



Interposer Auto-Routing

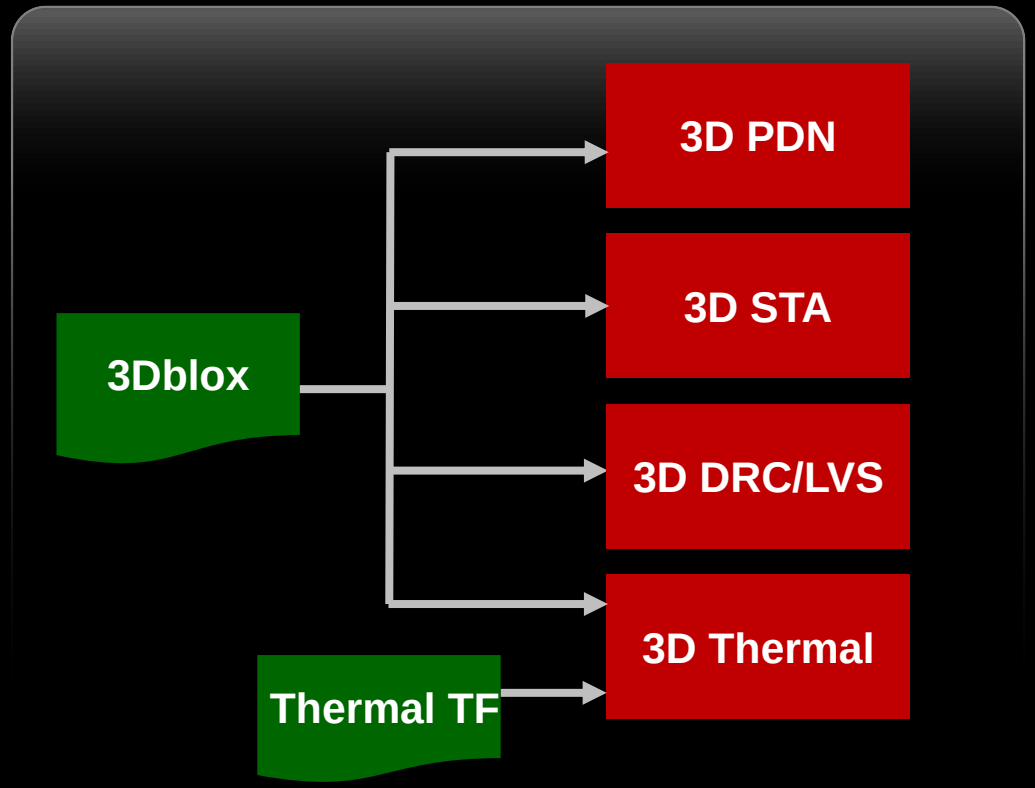
- Interposer Verilog hierarchy with TSMC technology files enables both silicon and RDL auto-routing

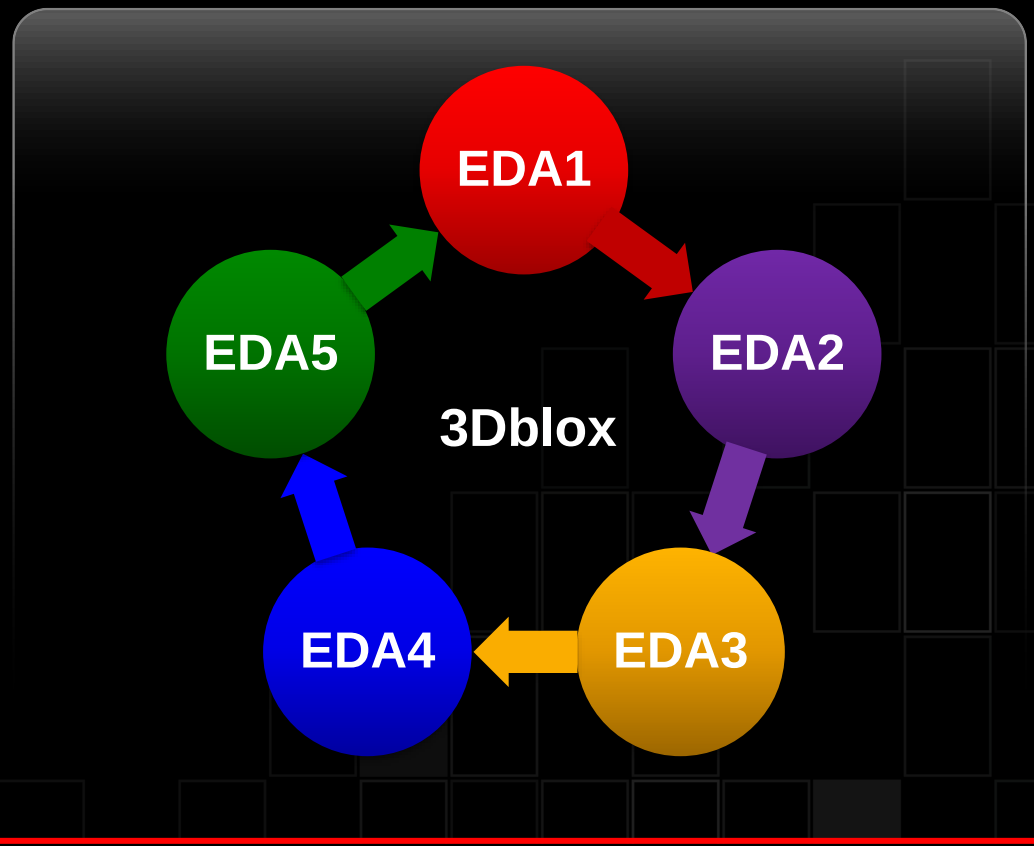


One Format, Multiple Products

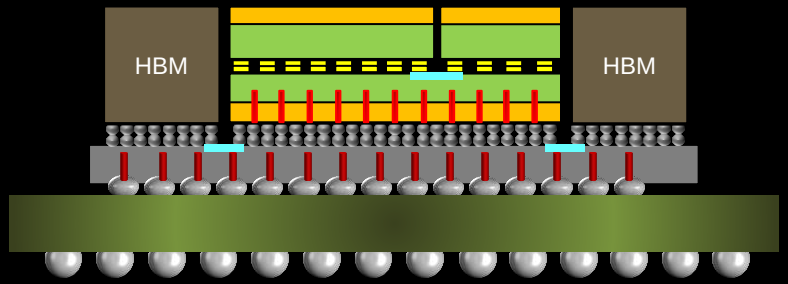
- One 3Dblox representation for all downstream analyses
- Replace hundreds of repetitive codes for each tool

- Support from all EDA vendors creates unified design ecosystem





TSMC Offers 3Dblox Design Templates



Target Architecture

- Chiplet Definitions
- Interface Definitions
- Tech File Bindings
- Physical Assertions
- Path Assertions

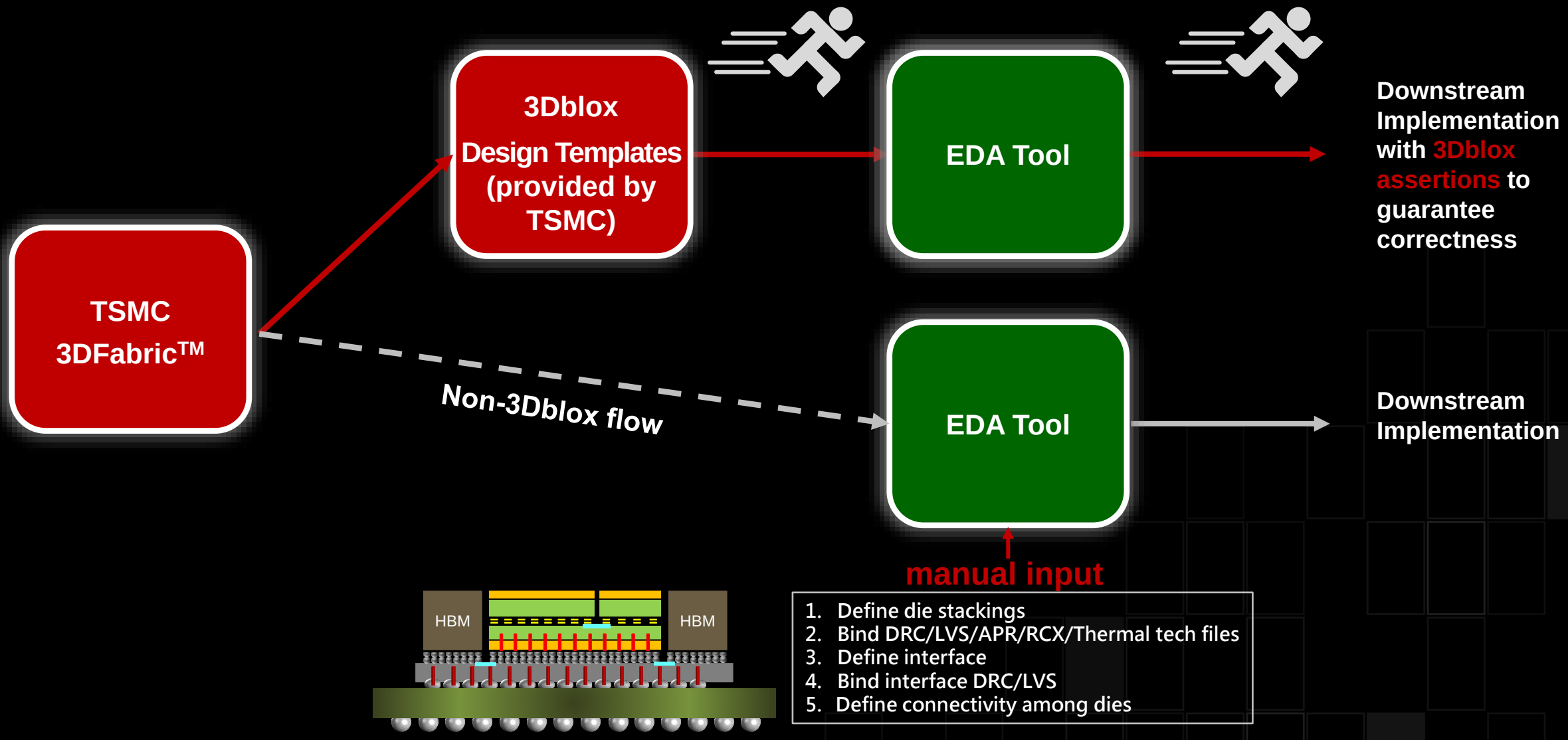
TSMC 3Dblox

3Dblox Design Templates

- CoWoS-S
- CoWoS-R
- CoWoS-L
- InFO-PoP
- InFO-2D
- InFO-3D
- SoIC-CoW
- SoIC-WoW

3Dblox Design Template Bootstrap Design Starts

Unleash Innovation



Outline

- Chiplet Architecture Complexity Drives For Advanced Solutions
- The 3Dblox Standard
- Key Productivity Features
- Summary

Summary

- Modularized 3Dblox language constructs – chiplet, interface, and connection
- Language constructs designed to model all current and future 3DIC structures. Find 3dblox from http://3dblox.org
- Streamline EDA design flow and promote interoperability
- 3Dblox is open to all partners, customers, foundries and OSAT

Collaboration with OIP Partners Unleashes the Ultimate 3DIC Design Productivity!