Introduction of 3D IC Thermal Analysis Flow

Alex Hung

Siemens EDA

Agenda

Challenge: Thermal
Introduction & Cases
Summary

Unrestricted | © Siemens 2023 | 2023-MM-DD | Alex Hung | Title | Siemens Digital Industries Software | Where today meets tomorrow.

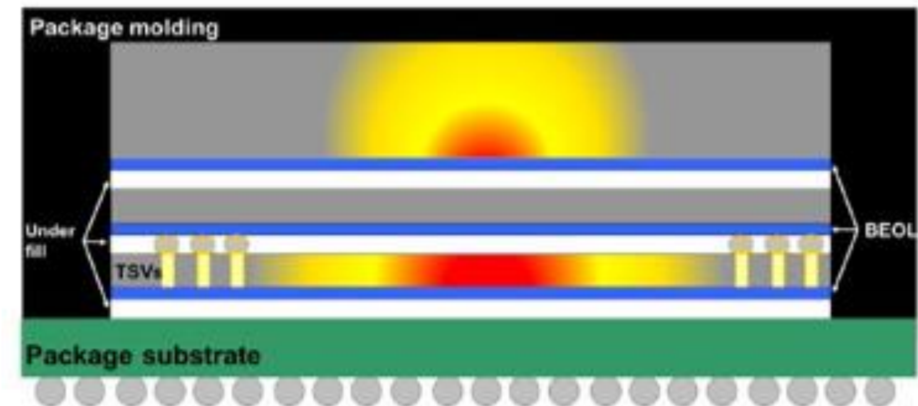
Thermal Challenges:
Accessing Package Level Electro-Thermal Impacts at the Chiplet Level

General Thermal Concerns

- Powering devices generates heat
  - Passing power through wires generates heat
  - High frequency device switching generates heat
- Heat impacts electrical behavior
  - Interconnect parasitics
  - Device behavior

3D IC Thermal Concerns

- Increased challenges for power distribution
- Impacts of heterogeneous environments
  - Can't address with DRC/LVS rules
  - More and new materials
  - Vertical thermal resistance
  - Increased distances to heat sink
- From general concerns for electronics



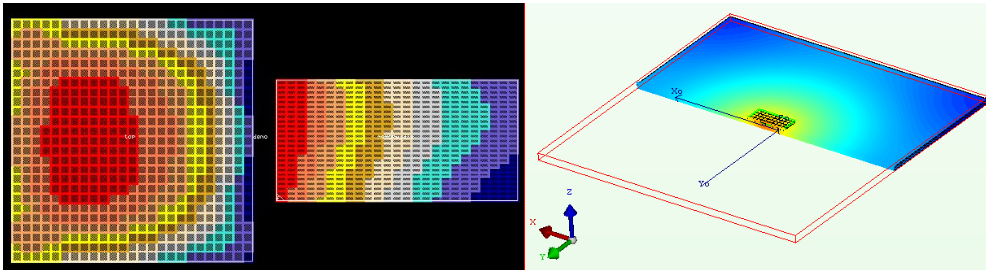
 Unrestricted | © Siemens 2024 | 2024-MM-DD | Alex Hung | Title | Siemens Digital Industries Software | Where today meets tomorrow.

SIEMENS

Thermal Analysis Flow
Calibre 3D Thermal

Sign-off Accurate Die-level Thermal Analysis from Package Assembly

- Solution implements thermal behavior considered as below:
  - Supported LEF/DEF, GDS import
  - Create detailed die thermal model of non-uniform thermal properties caused by metallization/TSVs
  - Generates fine-grain power maps to capture hotspot effects
  - Report temperature gradient and hotspot regions in stacking dies



XML

GDS
OASIS
LEFDEF

LEF
DEF
IPF

3DSTACK+ Configuration File
+ Boundary conditions
+ Package blocks e.g. TIM, heatsink
+ Thermal constraints

3D Thermal Configuration

Die/layers model

3D assembly

Power map

Calibre 3D Thermal

Static/Transient Thermal Simulation

Flotherm

3D IC/package Assembly View

Thermal and Power Maps

Thermal Waveforms

Summary Report

Thermal Results Database

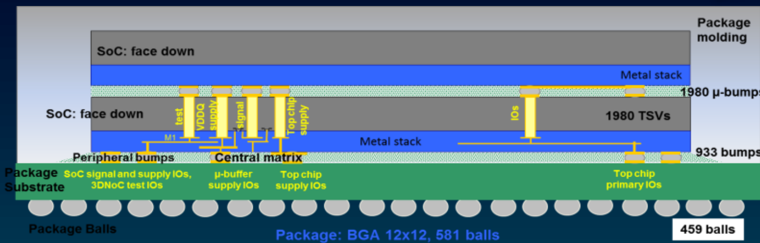
Unrestricted | © Siemens 2024 | 2024-MM-DD | Author | Title | Siemens Digital Industries Software | Where today meets tomorrow.

SIEMENS

Thermal-Aware IC Design
Flow and Accuracy Qualifications

CEA-Leti 3DNOC Case Study

65nm STMicroelectronics 70mm²
3000 TSVs and micro-bumps
1000 flip-chip bumps
TFBGA 12x12x1.2 - 581balls

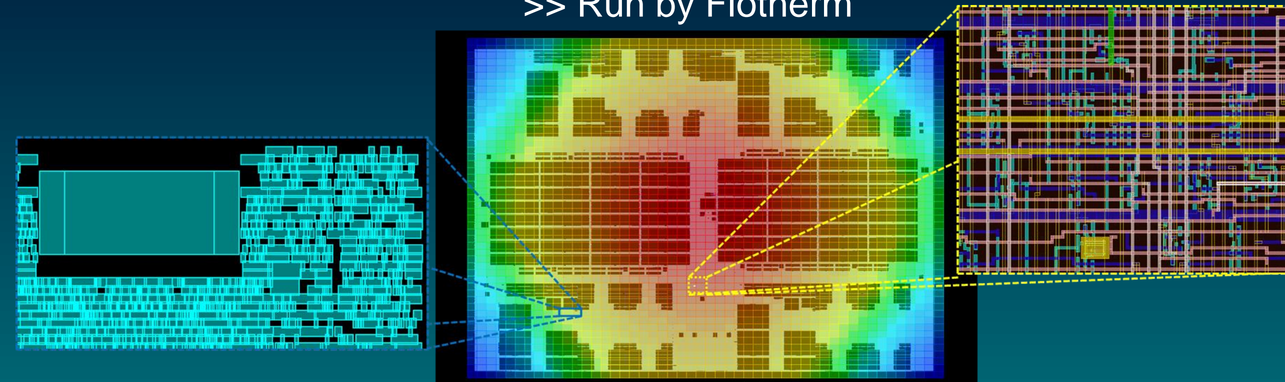


Logic-on-Logic version :
3DNOC = Mag3D + Mag3D

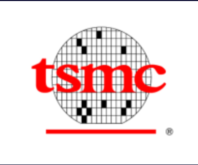
"The implemented thermal model presents very good accuracy, the worst case difference between simulation and measured data is equal to **3.75%** while the average difference considering all thermal sensors is lower than **2%**."*

Fine grain thermal simulation in large SoC designs:

- Address hot spot region affected by metal layers and power map



* P. Vivet, Y. Thonnart, R. Lemaire, C. Santos, E. Beigne, C. Bernard, F. Darve, D. Lattard, I. Miro-Panades, D. Dutoit, F. Clermidy, S. Cheramy, H. Sheibanyrad, F. Petrot, E. Flamand, J. Michailos, A. Arriordaz, L. Wang and J. Schloeffel, "A 4x4x2 Homogeneous Scalable 3D Network-on-Chip Circuit with 326 MFlit/s 0.66 pJ/bit Robust and Fault Tolerant Asynchronous 3D links", *IEEE Journal of Solid-State Circuits (Volume: 52, Issue: 1, January 2017).*



Thermal-Aware IC Design
Calibre Implements TSMC 3DFabric through 3Dblox

TSMC Reference Flows

FOR IMMEDIATE RELEASE
For more information, please contact:
Gene Forte
Mentor Graphics
Sonia Harrison
Mentor Graphics

3DIC Reference Flow – Mentor Track

Siemens partners with TSMC for 3nm product certifications and other technology milestones
26 October 2022
Plano, Texas, USA

To help mutual customers deploying 3D IC architectures in their next generation ICs, Siemens has enhanced its Calibre 3DSTACK software to support TSMC's 3Dblox standard for heterogeneous process DRC and LVS checking, as well as for thermal analysis through Siemens' Simcenter™ Flotherm™ software. For thermal analysis, the Calibre software combined with Simcenter Flotherm software has been certified fulfilling required accuracy and has been enhanced to enable automatic extraction, power map generation and simulation of the complete 3D IC assembly.

technology. Mentor also announced it has successfully completed reference flow materials in support of TSMC's innovative System-on-Integrated-Chips (TSMC-SoIC™) multi-chip 3D stacking technology.

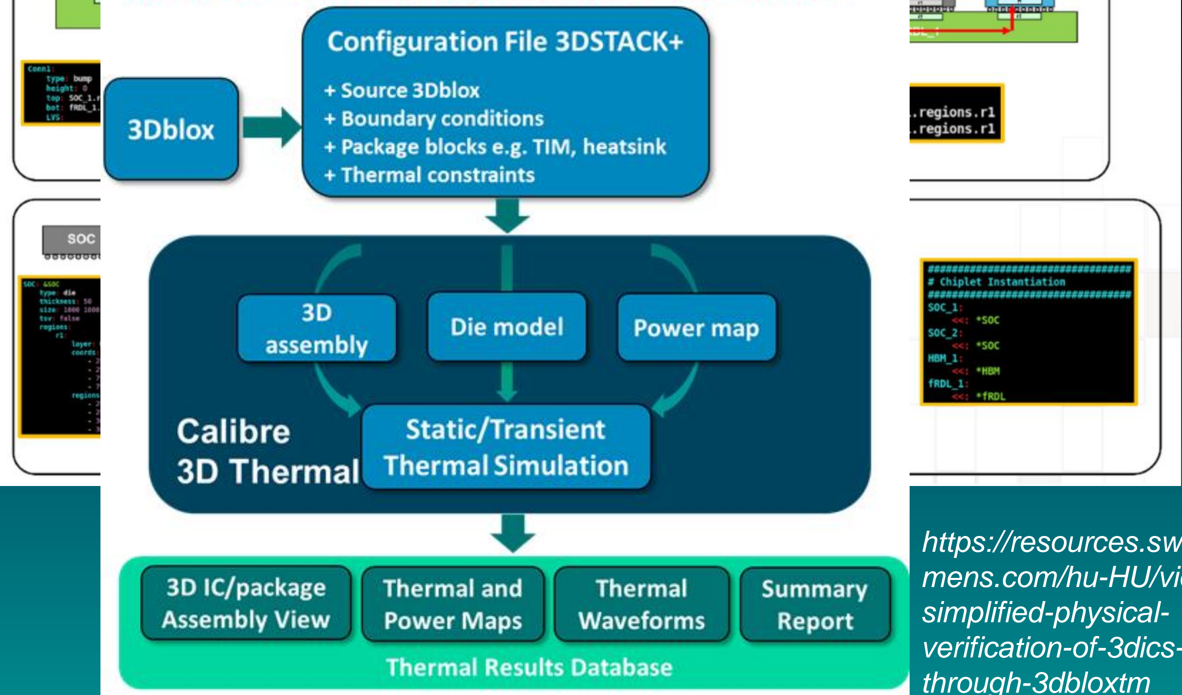
(EDA) technologies for our new processes, TSMC and our mutual customers."

Qualified in TSMC Reference Flows for CoWoS, 3DIC, InFO-oS, InFO-PoP, InFO-MS, WoW, SoIC, 3Dblox from 2012 – 2022

Simplified physical verification of 3DICs through 3Dblox

Simplified Physical Verification of 3DICs through 3Dblox™

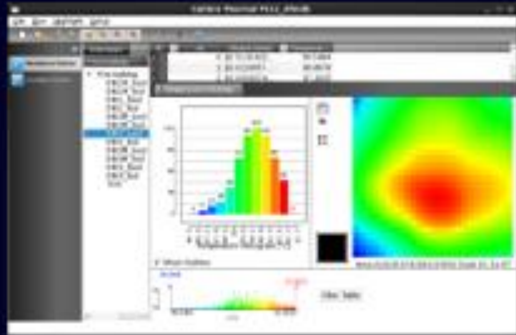
John Ferguson
Director, Product Management, Calibre nmDRC
October 2022



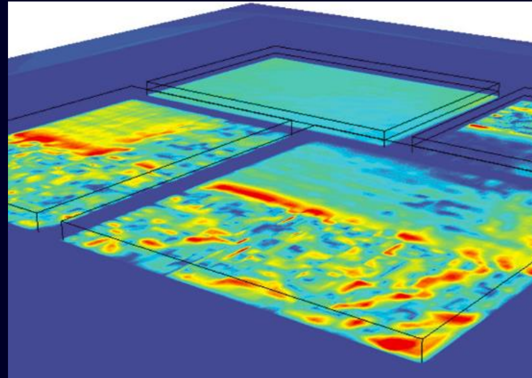
https://resources.sw.siemens.com/hu-HU/video-simplified-physical-verification-of-3dics-through-3dbloxtm

Unrestricted | © Siemens 2024 | 2024-MM-DD | Alex Hung | Title | Siemens Digital Industries Software | Where today meets tomorrow.

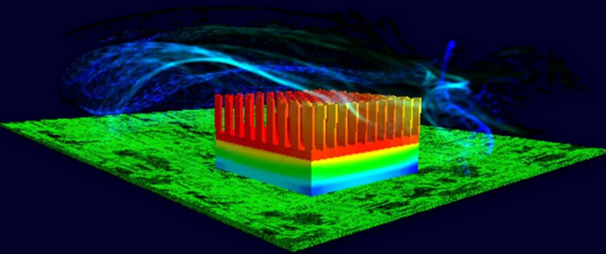
Calibre 3D Thermal

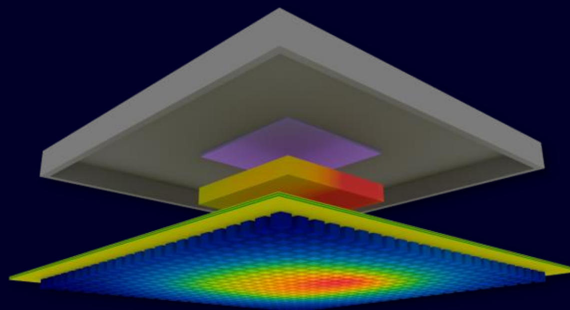


Automated Thermal Analysis Report



Detailed Die Level Thermal Models





Substrate and System Level Thermal Modeling

Flotherm, Calibre, Thermal Analysis

Key highlights

- Comprehensive thermal solution from transistor to system-level – chiplet, interposer, package, system
- Detailed die-level thermal analysis with accurate package and boundary conditions
- Optimization of thermal effects
- Leverage a common fast/robust solver across Calibre/Flotherm

Benefits/value

- Reduce cost - minimizes need for test chips
- Simulate/identify system reliability problems
- Delivering the sophisticated thermal solutions required for 2.5D/3D chiplet packaging

Contact

Alex Hung, Ph.D.
Foundry Lead
Siemens EDA

E-mail alex.hung@siemens.com

SIEMENS