Clock Tree Construction based on Arrival Time Constraints

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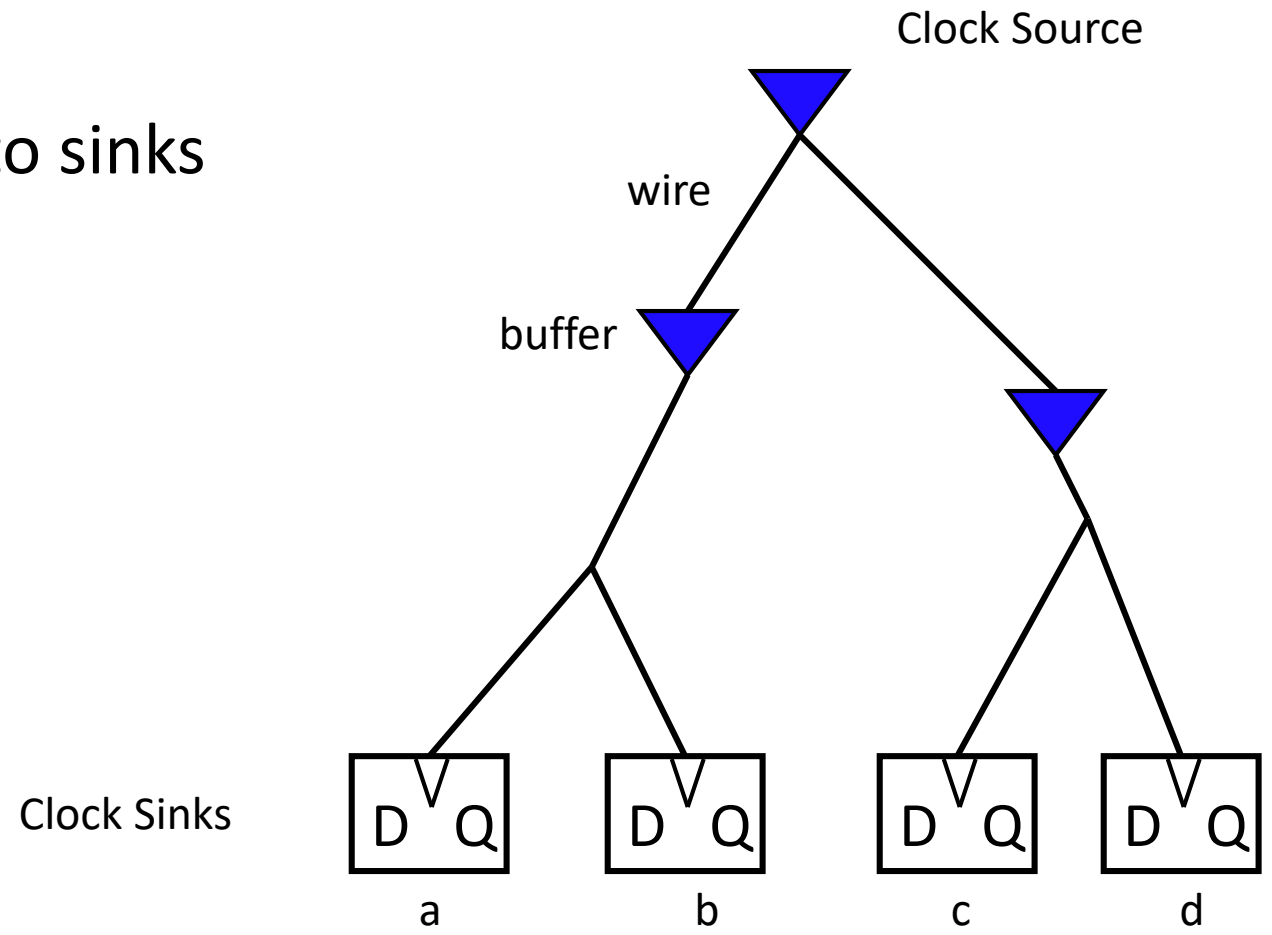
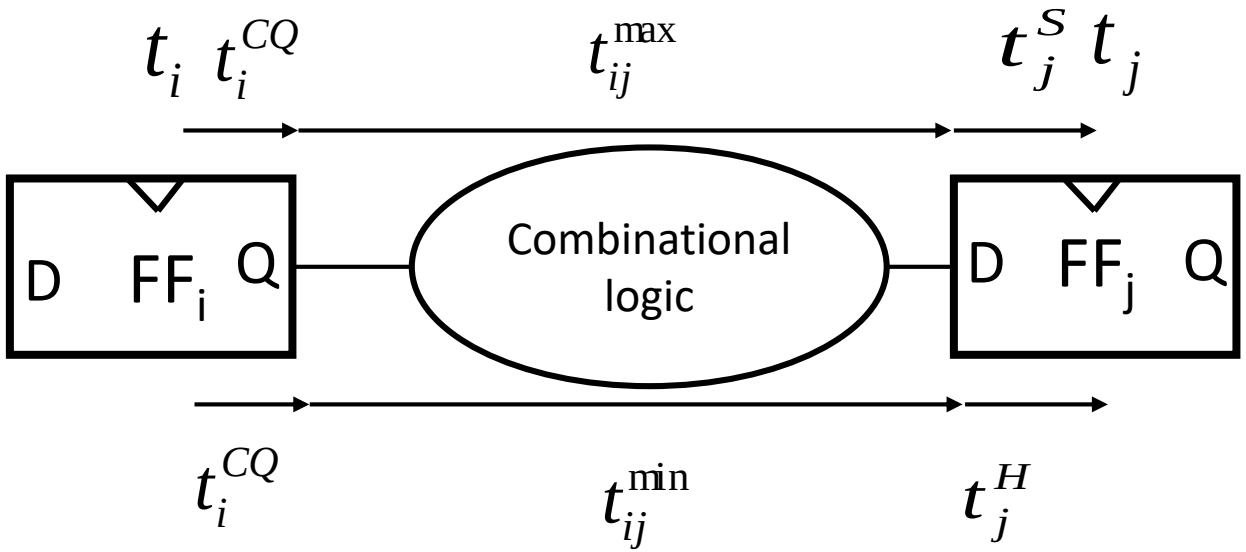
Clock Tree Synthesis

- Objective: Connect source to sinks
  - Buffers
  - Wires
- Constraints:
  - Transition time
  - Skew



Timing Constraints



$$u_{ij} = T - t_i^{CQ} - t_{ij}^{\max} - t_j^S$$

$$l_{ij} = t_j^H - t_i^{CQ} - t_{ij}^{\min}$$

$$l_{ij} \le t_i - t_j \le u_{ij}$$

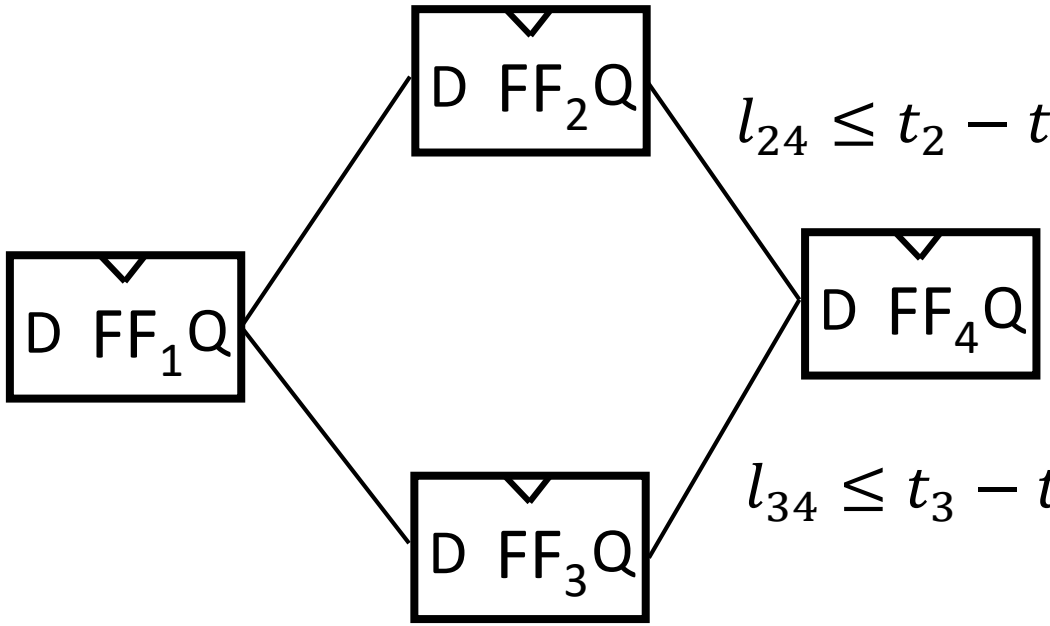
$$l_{ij} \le skew_{ij} \le u_{ij}$$

$$t_i + t_i^{CQ} + t_{ij}^{max} + t_j^S \le t_j + T$$

$$t_i + t_i^{CQ} + t_{ij}^{min} \ge t_j + t_j^H$$

Skew Constraint Graph (SCG)

$l_{12} \leq t_1 - t_2 \leq u_{12}$

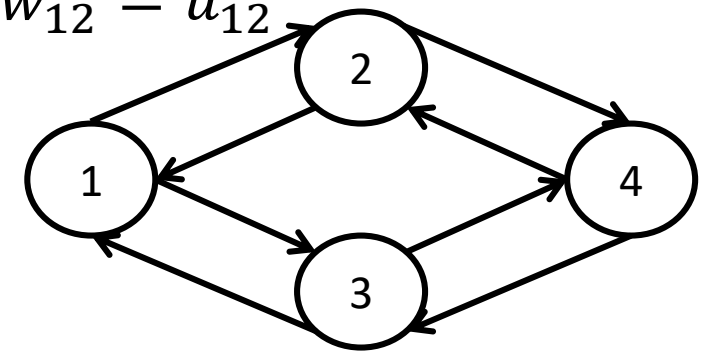


$l_{24} \leq t_2 - t_4 \leq u_{24}$

$l_{34} \leq t_3 - t_4 \leq u_{34}$

$l_{13} \leq t_1 - t_3 \leq u_{13}$

$w_{12} = u_{12}$



$w_{21} = -l_{12}$

$l_{12} \leq t_1 - t_2$

$t_1 - t_2 \leq u_{12}$

$t_2 - t_1 \leq -l_{12}$

$t_i - t_j \leq w_{ij}$

Outline

- Timing constraints
- **Outline**
- Previous works
- Proposed approach
- Proposed techniques
  - Clock tree construction based on arrival time constraints
  - Specification of arrival time constraints
- Methodology
- Experimental results

Timing Constraints

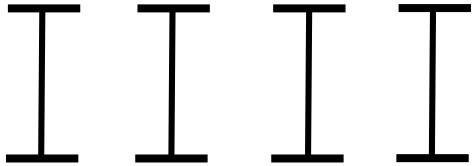
$$\frac{|V|(|V|-1|)}{2}$$

Dynamic implied skew constraints [17]

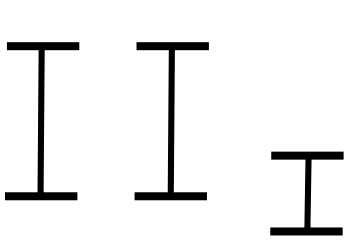
Static equal arrival time constraints [13]

Static useful arrival time constraints [11]

Static bounded arrival time constraints [5]



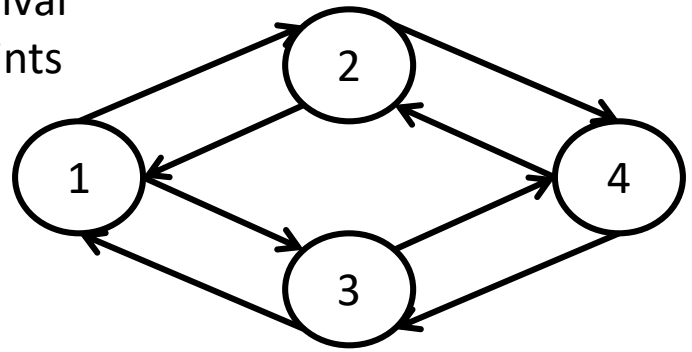
Static bounded useful arrival time constraints [2]

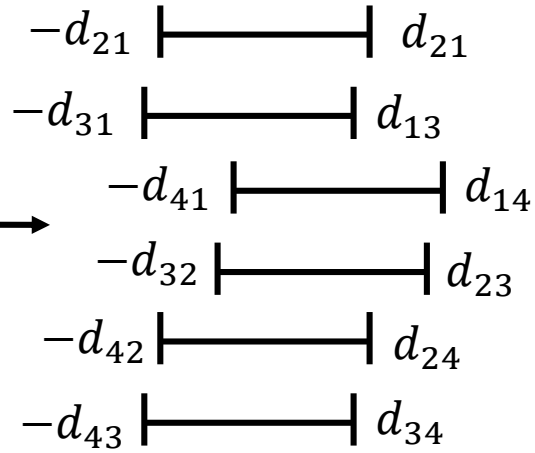


used in this work

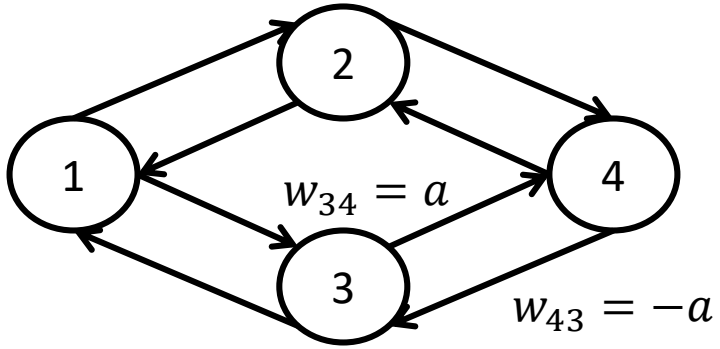
|V| static arrival time constraints

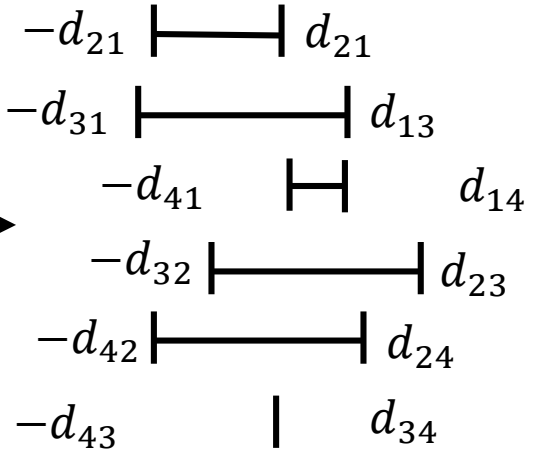
SCG





$t_3 - t_4 = skew_{34} = a$





Timing constraints

Static arrival time constraints

$$x_i^{lb} \le x_i^{ub}, \qquad \forall i \in V$$
$$x_i^{ub} - x_j^{lb} \le w_{ij}, \qquad \forall (i,j) \in E$$

$$t_i \in \left[x_i^{lb}, x_i^{ub}\right], \qquad \forall i \in V$$

Dynamic implied skew constraints

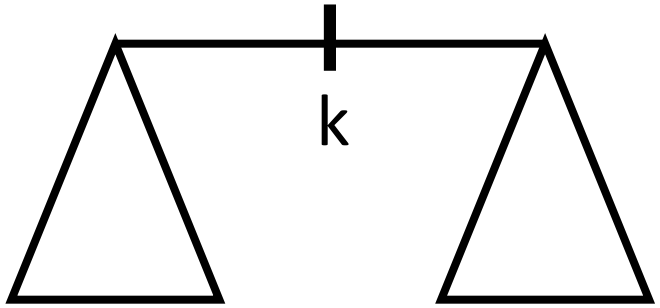
$$d_{ji} \le t_i - t_j \le d_{ij}$$

[2] C. Albrecht, B. Korte, J. Schietke, and J. Vygen. Maximum mean weight cycle in a digraph and minimizing cycle time of a logic chip. Discrete Applied Math., 123(1-3):103–127, 2002.
[5] J. Cong, A. B. Kahng, C.-K. Koh, and C.-W. A. Tsao. Bounded-skew clock and Steiner routing. ACM Trans. Des. Autom. Electron. Syst., 3(3):341–388, July 1998.
[11] J. Fishburn. Clock skew optimization. IEEE Transactions on Computers, pages 945–951, 1990.
[13] R.-S. Tsay. Exact zero skew. In ICCAD'91, 1991.
[17] C.-W. A. Tsao and C.-K. Koh. UST/DME: a clock tree router for general skew constraints. TODAES, pages 359–379, 2002.
[12] S. Held, B. Korte, J. Massberg, M. Ringe, and J. Vygen. Clock scheduling and clock tree construction for high performance asics. ICCAD'03, pages 232–239, 2003.

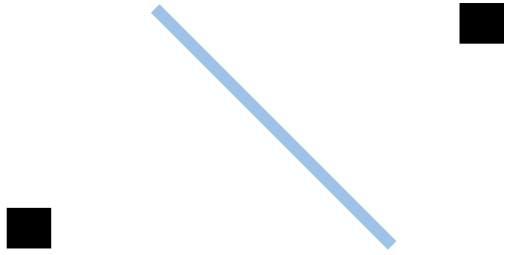
Previous Works – ZST and UST in [11,13]

$t_i == t_j$

FMR_k



Deferred Merge Embedding (DME)



Static equal arrival time constraints

Static useful arrival time constraints

off_1

ZST: $t_i = 0$ $t_j = 0$

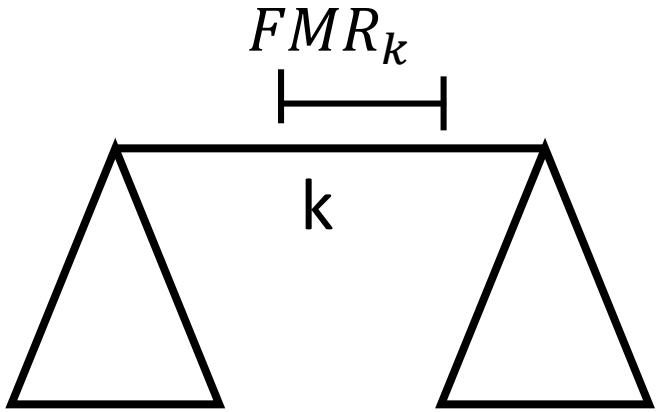
UST: $t_i = off_i$ $t_j = off_j$

- Low timing margin utilization
+ Useful skew

[11] J. Fishburn. Clock skew optimization. IEEE Transactions on Computers, pages 945–951, 1990.
[13] R.-S. Tsay. Exact zero skew. In ICCAD'91, 1991.

Previous works – BST in [5]

$$t_k^{max} - t_k^{min} \leq B$$

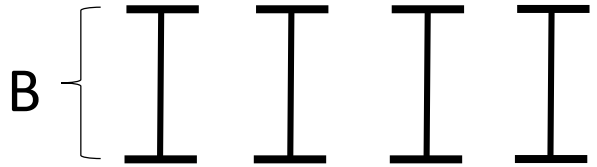


$t_i^{min} = 0$
$t_i^{max} = 0$

$t_j^{min} = 0$
$t_j^{max} = 0$

DME

Static bounded arrival time constraints

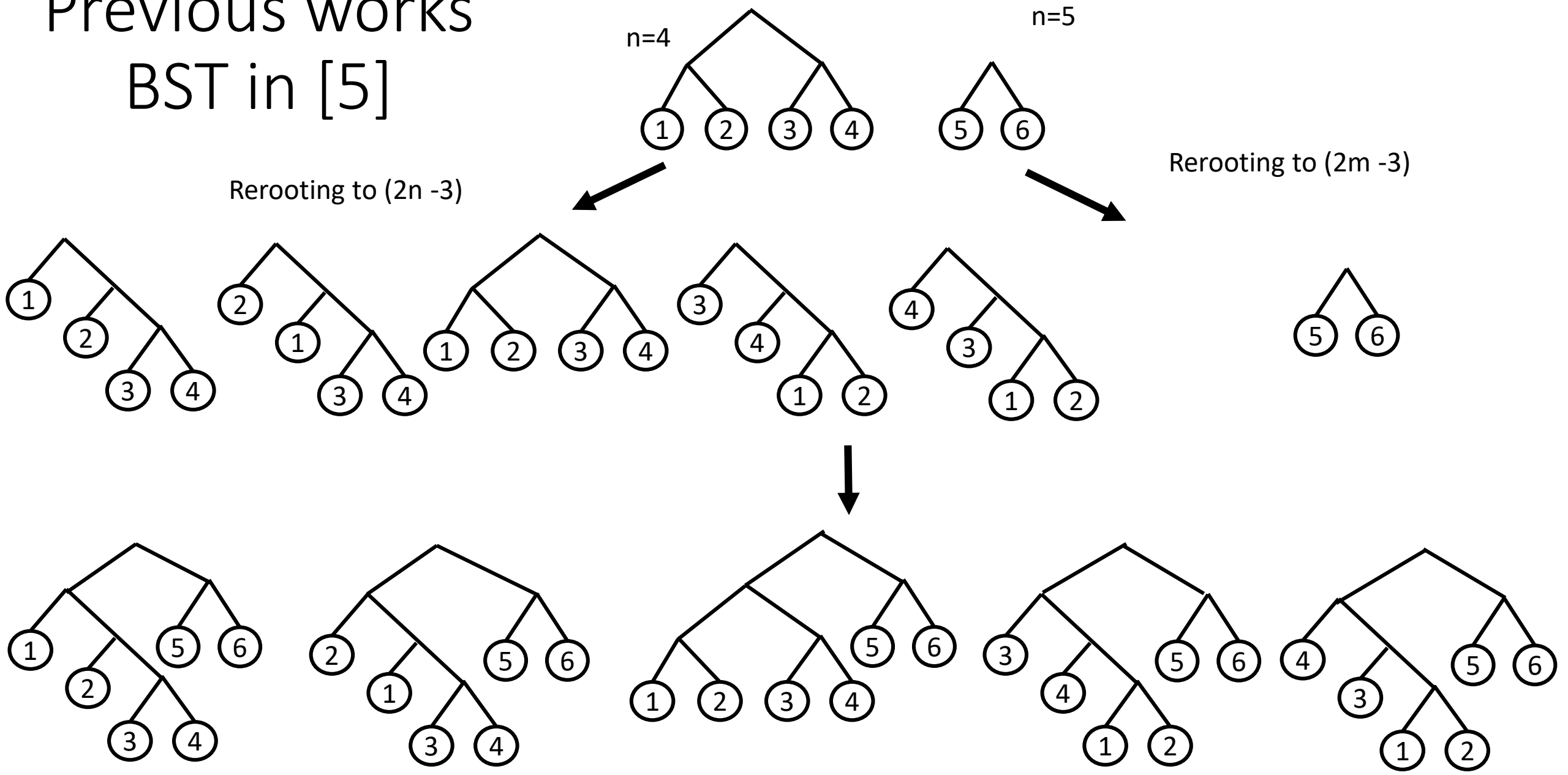


$$t_k^{min} = \min\{t_i^{min} + w(k,i), t_j^{min} + w(k,j)\}$$
$$t_k^{max} = \max\{t_i^{max} + w(k,i), t_j^{max} + w(k,j)\}$$

+ Medium timing margin utilization
+ Rerooting
- No useful skew

[5] J. Cong, A. B. Kahng, C.-K. Koh, and C.-W. A. Tsao. Bounded-skew clock and Steiner routing. ACM Trans. Des. Autom. Electron. Syst., 3(3):341–388, July 1998.

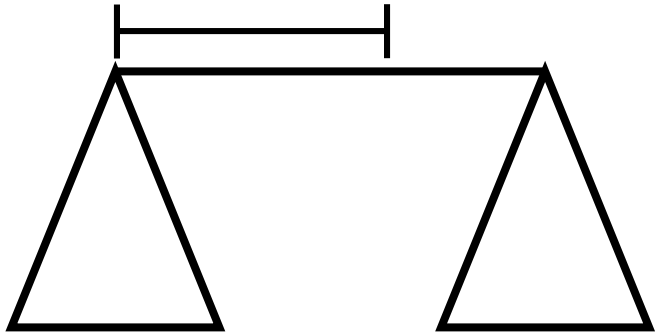
Previous works
BST in [5]

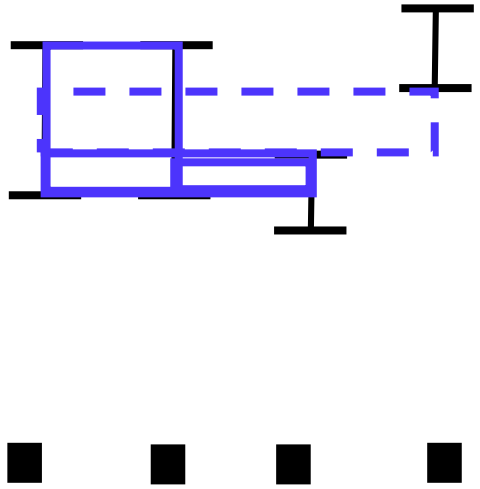


[5] J. Cong, A. B. Kahng, C.-K. Koh, and C.-W. A. Tsao. Bounded-skew clock and Steiner routing. ACM Trans. Des. Autom. Electron. Syst., 3(3):341–388, July 1998.

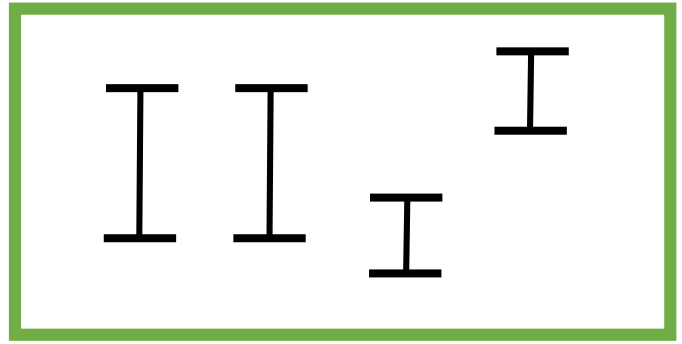
Previous works - UST in [2,12]

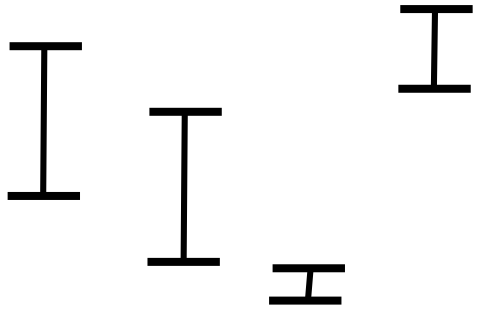
A FMR exists
but not used





Static bounded useful
arrival time constraints



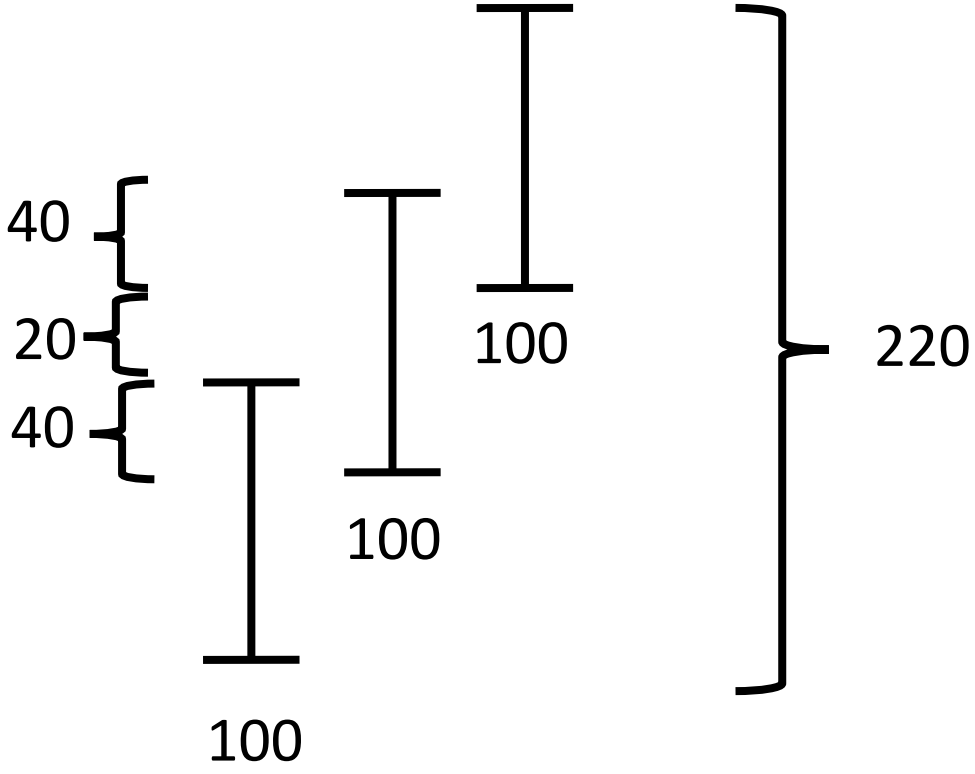


+ High timing margin utilization
+ Useful skew
- Interconnect delay not considered during merging

The length was
Lexicographically
maximized

[2] C. Albrecht, B. Korte, J. Schietke, and J. Vygen. Maximum mean weight cycle in a digraph and minimizing cycle time of a logic chip. Discrete Applied Math., 123(1-3):103–127, 2002.
[12] S. Held, B. Korte, J. Massberg, M. Ringe, and J. Vygen. Clock scheduling and clock tree construction for high performance asics. ICCAD'03, pages 232–239, 2003.

Previous Works – UST in [2,12]



$$t_1 - t_2 \leq 40$$
$$t_2 - t_3 \leq 40$$
$$t_3 - t_1 \leq 220$$

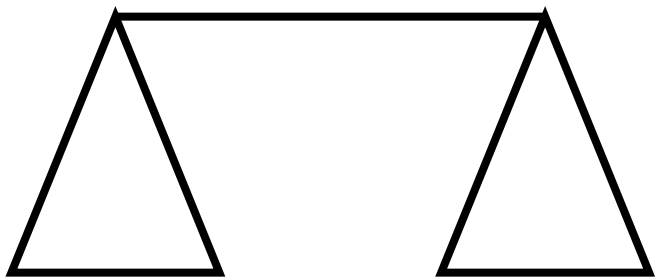
[2] C. Albrecht, B. Korte, J. Schietke, and J. Vygen. Maximum mean weight cycle in a digraph and minimizing cycle time of a logic chip. Discrete Applied Math., 123(1-3):103–127, 2002.
[12] S. Held, B. Korte, J. Massberg, M. Ringe, and J. Vygen. Clock scheduling and clock tree construction for high performance asics. ICCAD'03, pages 232–239, 2003.

Previous works – UST in [17,6]

$$FSR_{ij} = [-d_{ji}, d_{ij}]$$

$$\downarrow$$

$$FMR_{ij}$$



+ Full timing margin utilization
- Update of timing constraints required

- Computing FSR + update SCG
  - $O(V^2)$ in [17]
  - $O(V \log V + E)$ in [6]

DME

[17] C.-W. A. Tsao and C.-K. Koh. UST/DME: a clock tree router for general skew constraints. TODAES, pages 359–379, 2002.
[6] R. Ewetz, S. Janarthanan, and C.-K. Koh. Fast clock skew scheduling based on sparse-graph algorithms. ASP-DAC ’15, pages 472–477, 2014.

Previous works - Summary

*denotes that rerouting was not applied but would be easy to perform

Tree construction proposed in	Constraints	Update Required?	Ease of exploring topologies based on rerouting	Useful skews allowed	Degree of timing margin utilization	Considers interconnect delays during merging
[13]	Static equal arrival time [13]	No	easy*	No	Low	Yes
[13]	Static useful arrival time [11]	No	easy*	Yes	Low	Yes
[5]	Static bounded arrival time [5]	No	easy	No	Medium	Yes
[12]	Static bounded useful arrival time [2]	No	`n/a’	Yes	High	No
[17]	Dynamic implied skew [17]	Yes	difficult	Yes	Full	Yes
This paper	Static bounded useful arrival time [2]	No	easy	Yes	High	Yes

[2] C. Albrecht, B. Korte, J. Schietke, and J. Vygen. Maximum mean weight cycle in a digraph and minimizing cycle time of a logic chip. Discrete Applied Math., 123(1-3):103–127, 2002.
[5] J. Cong, A. B. Kahng, C.-K. Koh, and C.-W. A. Tsao. Bounded-skew clock and Steiner routing. ACM Trans. Des. Autom. Electron. Syst., 3(3):341–388, July 1998.
[11] J. Fishburn. Clock skew optimization. IEEE Transactions on Computers, pages 945–951, 1990.
[13] R.-S. Tsay. Exact zero skew. In ICCAD’91, 1991.
[17] C.-W. A. Tsao and C.-K. Koh. UST/DME: a clock tree router for general skew constraints. TODAES, pages 359–379, 2002.
[12] S. Held, B. Korte, J. Massberg, M. Ringe, and J. Vygen. Clock scheduling and clock tree construction for high performance asics. ICCAD’03, pages 232–239, 2003.

Proposed approach

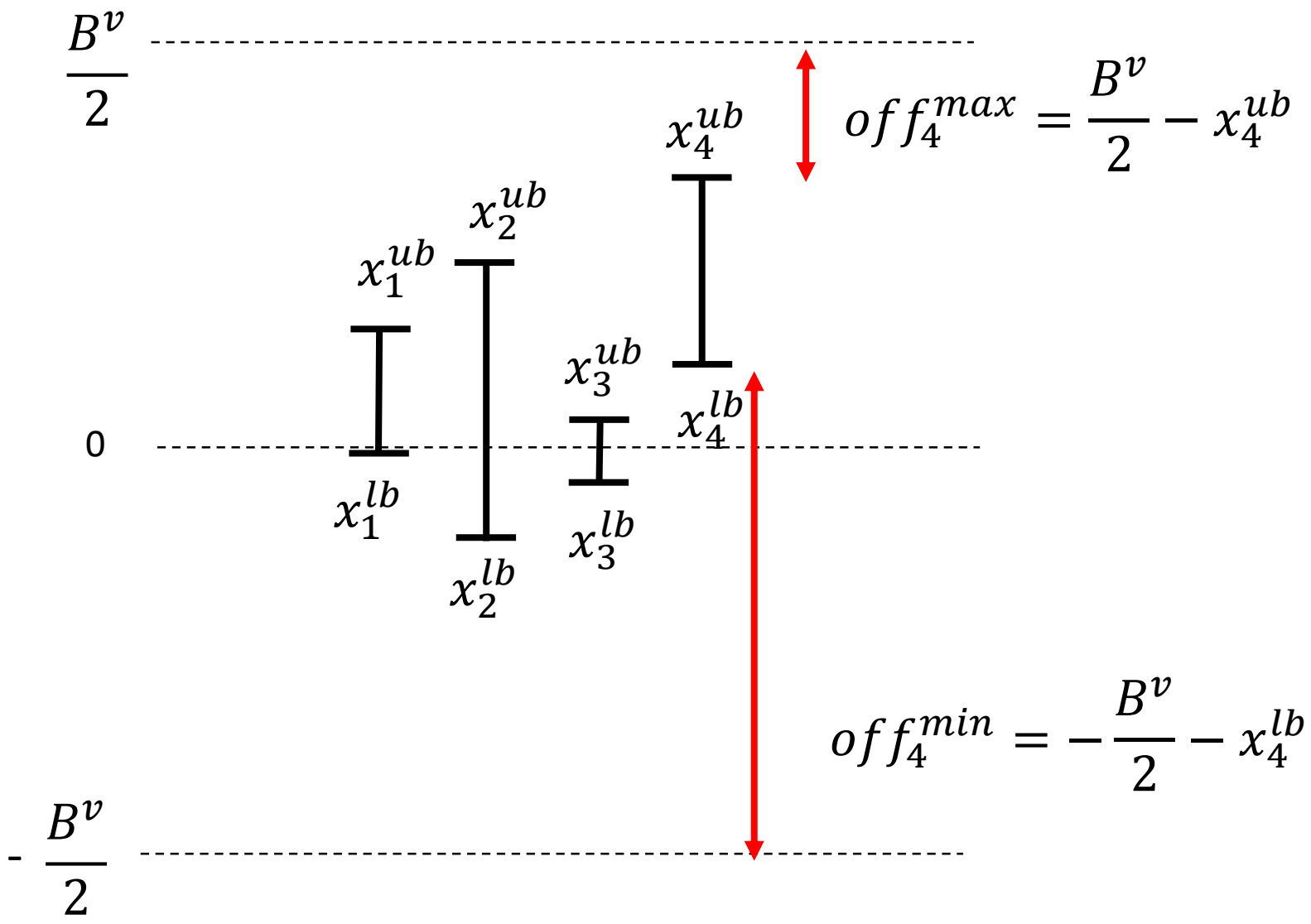
- Construct a clock tree
  - Minimum wire length and buffer area
  - Arbitrary skew constraints

- Proposed Approach
  - Construct a clock tree meeting bounded useful arrival time constraints
  - Specify the constraints to minimize cost

Proposed Clock Tree Construction

$$off_i^{min} = -\frac{B^v}{2} - x_i^{lb}$$

$$off_i^{max} = \frac{B^v}{2} - x_i^{ub}$$



Proposed clock tree construction

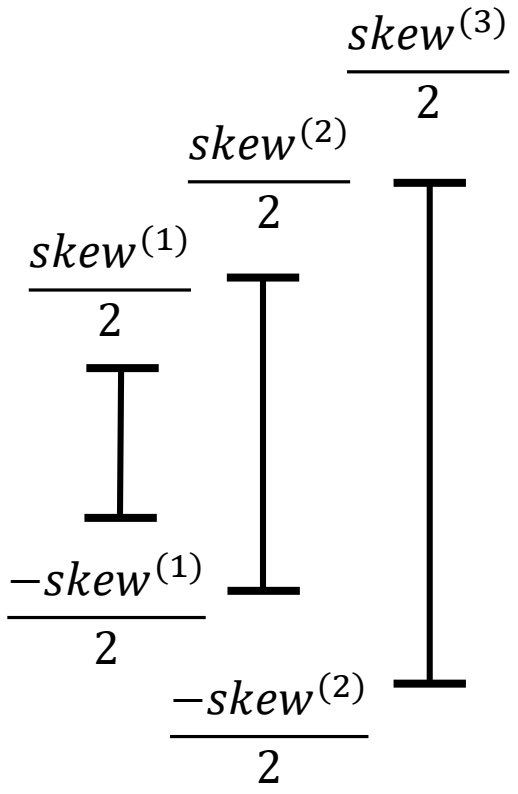
$$B^v$$

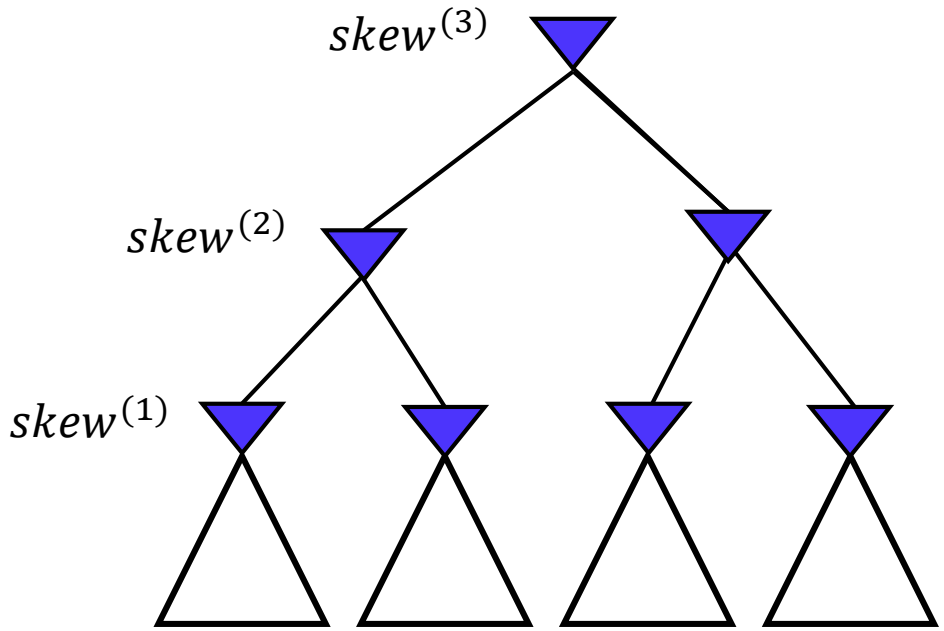
$$t_i^{min} = off_i^{min}$$

$$t_i^{max} = off_i^{max}$$

Specifying arrival time constraints

- Objectives:
  - Valid constraints
  - min x_i^{lb} and max x_i^{ub}
  - Alignment
  - Similar lengths



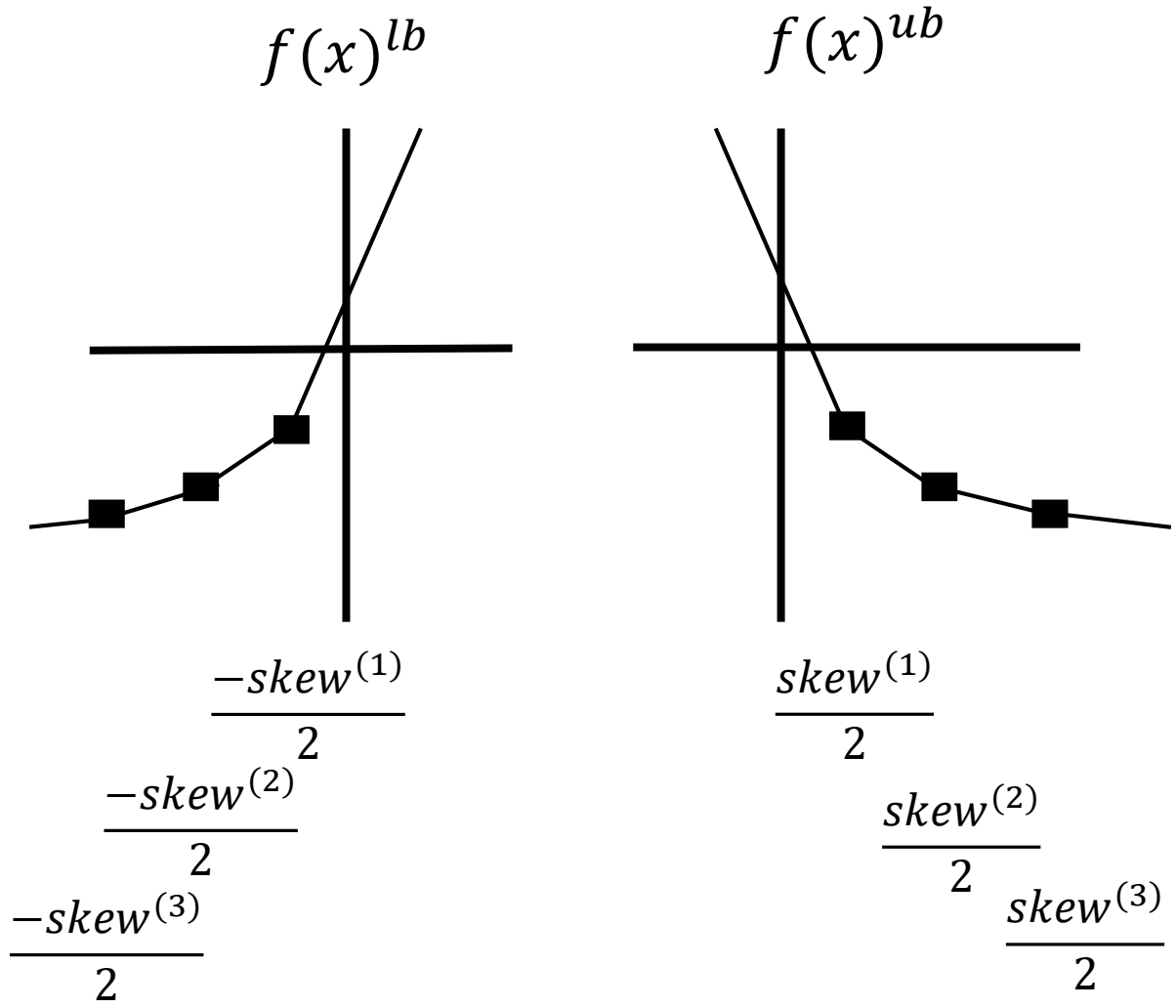


LP formulation

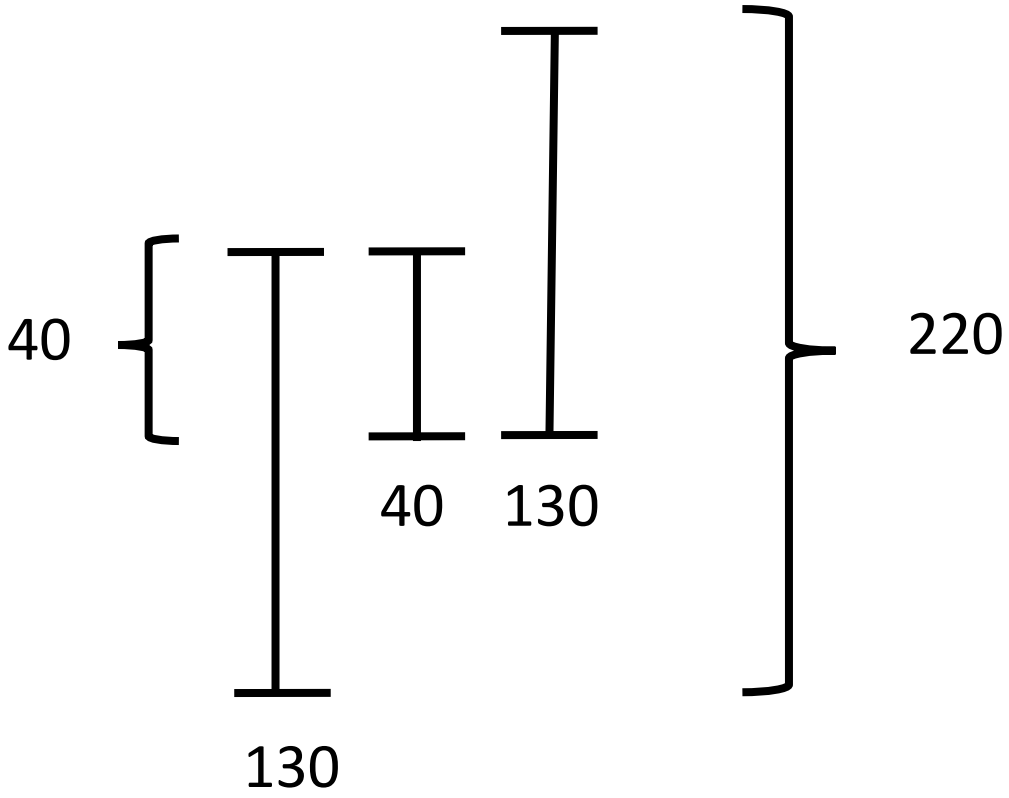
$$\min \sum_{i \in V} f(x_i^{lb})^{lb} + f(x_i^{ub})^{ub}$$

$$x_i^{lb} \leq x_i^{ub}, \qquad \forall i \in V$$
$$x_i^{ub} - x_j^{lb} \leq w_{ij}, \qquad \forall (i,j) \in E$$

- Objectives:
  - Valid constraints
  - min x_i^{lb} and max x_i^{ub}
  - Alignment
  - Similar lengths



Scheduling example



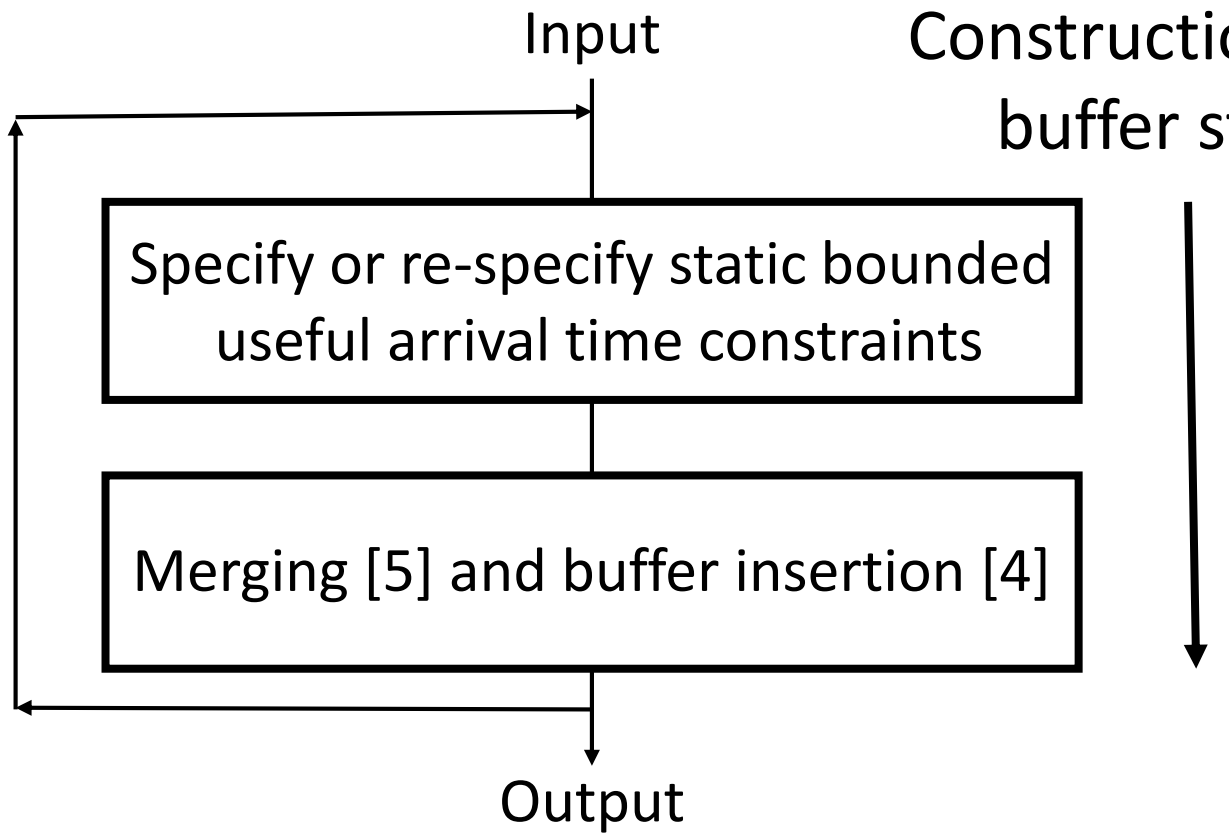
$skew^{(1)} = 40$

$t_1 - t_2 \leq 40$

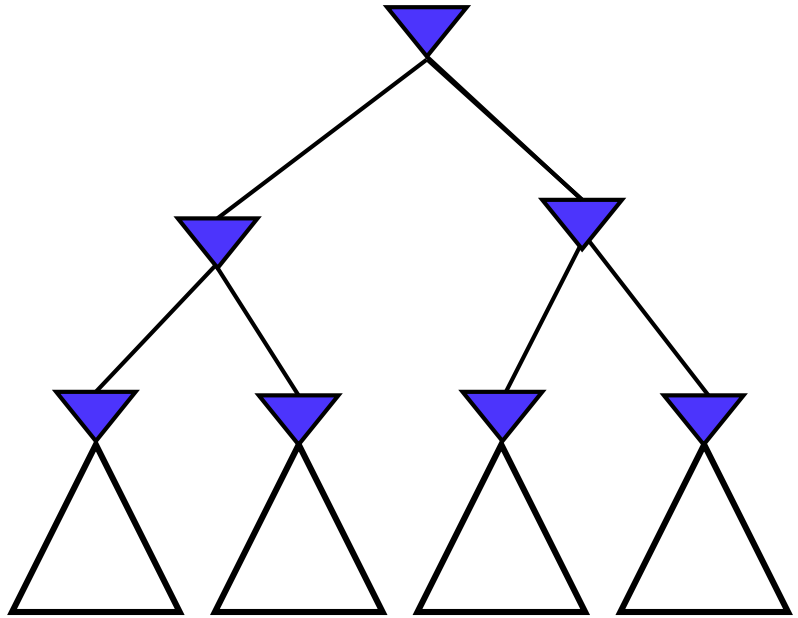
$t_2 - t_3 \leq 40$

$t_3 - t_1 \leq 220$

Proposed flow



Construction of a buffer stage



[4] Y. P. Chen and D. F. Wong. An algorithm for zero-skew clock tree routing with buffer insertion. EDTC'96, pages 230–237, 1996.
[5] J. Cong, A. B. Kahng, C.-K. Koh, and C.-W. A. Tsao. Bounded-skew clock and Steiner routing. ACM Trans. Des. Autom. Electron. Syst., 3(3):341–388, July 1998.

Experimental setup

- Arbitrary skew constraints

Circuit (name)	Used in	Sinks (num)	Skew Constraints (num)
scaled_s1423	[8]	74	78
scaled_s5378	[8]	179	175
scaled_15850	[8,10]	597	318
msp	[8]	683	44990
fpu	[8]	715	16263
ecg	[8,10]	7674	63440
aes	[10]	13216	53382
usbf		1765	33438
dma		2092	132834
pci_bridge32		3578	141074
des_peft		8808	17152
eht		10544	450762

[7] R. Ewetz, S. Janarthanan, and C.-K. Koh. Benchmark circuits for clock scheduling and synthesis. https://purr.purdue.edu/publications/1759, 2015
[16] C. N. Sze. ISPD 2010 high performance clock synthesis contest: Benchmark suite and results. ISPD'10, pages 143–143, 2010.

Evaluated Tree structures

- D-UST - dynamic implied skew constraints
- PS-UST – static useful arrival time constraints
- LS-UST – static bounded useful arrival time constraints in [2]
- S-UST - static bounded useful arrival time constraints specified using LP
- TS-UST - rerooting + S-UST
- RTS-UST – re-specify constraints + TS-UST

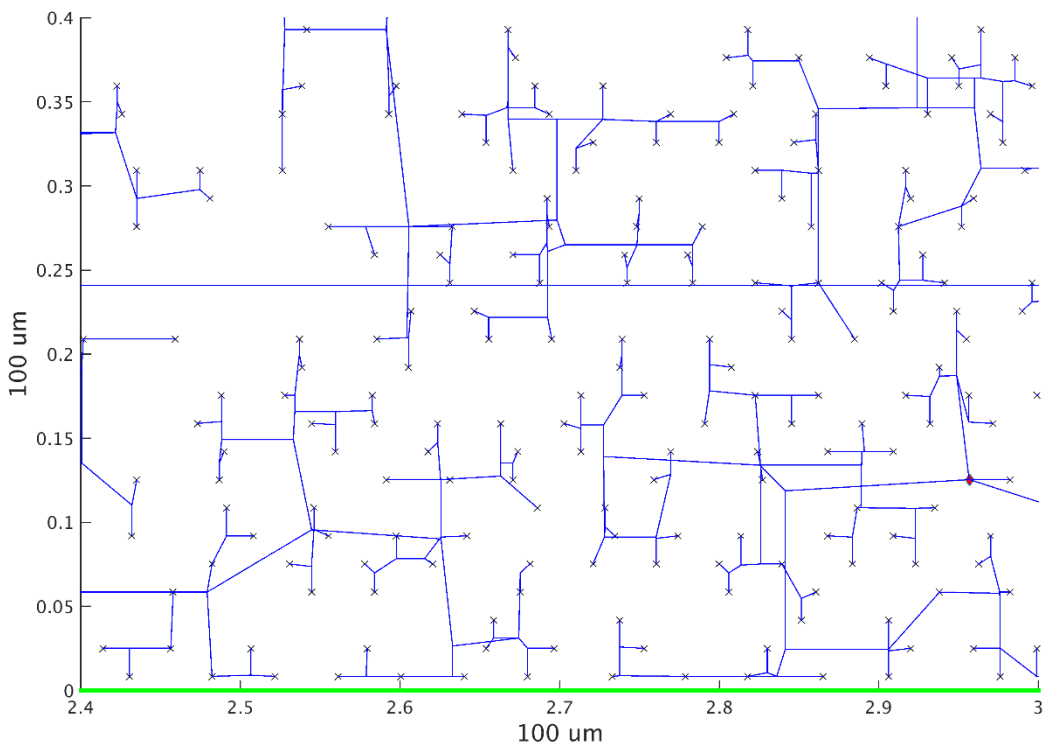
[2] C. Albrecht, B. Korte, J. Schietke, and J. Vygen. Maximum mean weight cycle in a digraph and minimizing cycle time of a logic chip. Discrete Applied Math., 123(1-3):103–127, 2002.

Evaluation after CTS

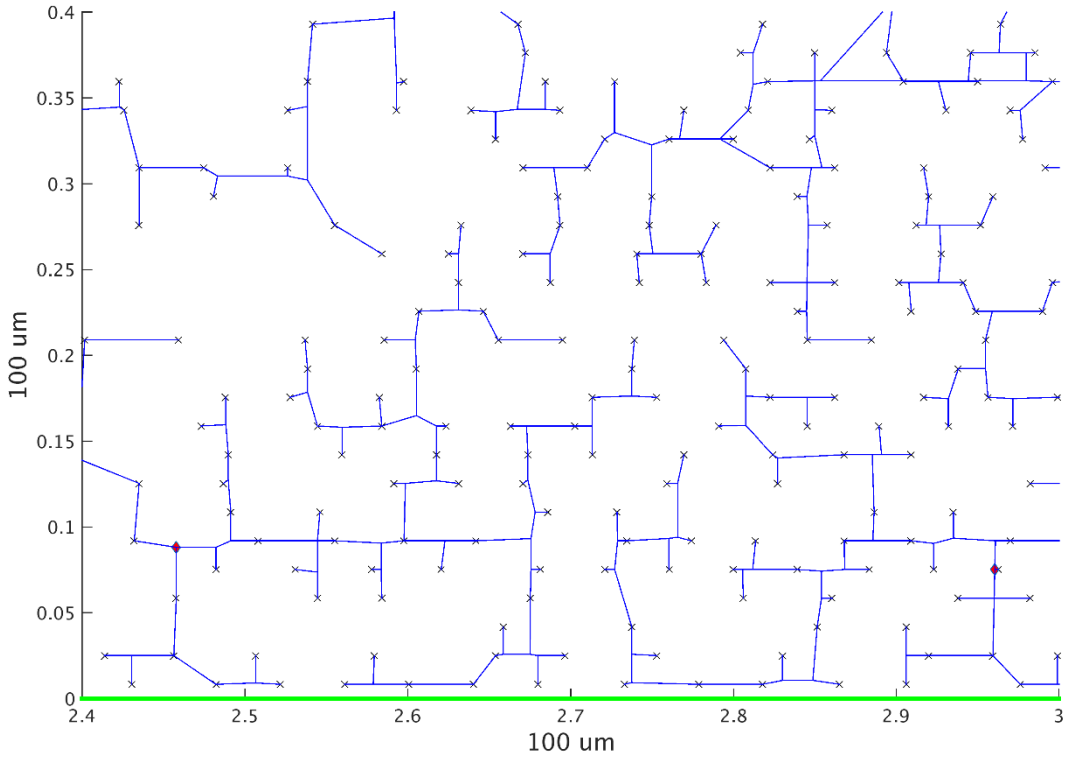
Circuits	Cap cost (pF)						Run-time (min)					
(name)	D-UST	PS-UST	LS-UST	**S-UST**	**TS-UST**	**RTS-UST**	D-UST	PS-UST	LS-UST	**S-UST**	**TS-UST**	**RTS-UST**
s1423	3.3	4.4	9.9	3.9	**3.2**	**3.2**	1	1	1	1	1	1
s5378	**5.7**	10.7	9.6	6.3	6.2	5.8	1	3	2	2	2	2
s15850	18.3	20.5	28.3	20.0	20.0	**17.5**	16	18	11	20	20	9
msp	1.7	2.5	1.8	1.8	1.5	**1.5**	1	2	5	1	4	4
fpu	2.1	2.9	2.0	2.0	1.9	**1.9**	1	1	1	1	4	4
ecg	34.5	50.3	76.4	30.4	28.3	**26.9**	26	20	64	23	53	63
aes	207.5	372.0	204.4	202.4	207.5	**207.5**	186	324	114	127	214	155
usbf	8.0	9.9	8.0	5.2	**4.5**	**4.5**	4	9	5	3	9	10
dma	7.3	11.9	6.4	5.8	**5.3**	**5.3**	4	11	5	3	14	14
pci_bridge	15.1	15.5	11.2	8.9	7.8	**7.7**	10	8	10	5	24	24
des_perf	19.2	29.8	44.1	22.7	19.7	**18.9**	8	14	20	16	36	32
eht	23.6	44.7	23.7	23.3	**21.2**	**21.2**	16	25	16	15	72	78
Norm.	1.00	1.48	1.30	0.95	0.857	**0.84**	8X			1X	8X	

Part of clock tree on ecg

D-UST

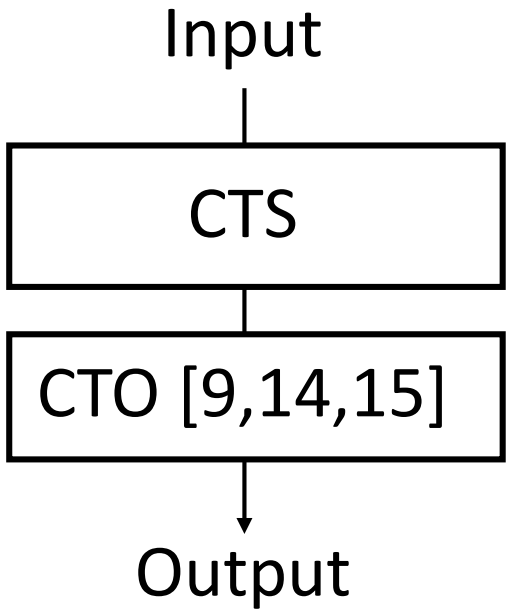


RTS-UST



Evaluation framework

- Monte Carlo Framework [7,8,16]
  - Process variations (10%)
  - Voltage variations (15%)
  - Temperature variations (30%)
- Tree structures
  - D-UST - in [8]
  - D-UST - in [10]
  - LD-UST – D-UST + latency opt. in [10]
  - RTS-UST – this work



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Evaluation after CTO

Circuit	Work	Structure	After CTS				After CTO			
(name)			Cap (pF)	Latency (ps)	Yield (ps)	Run-time (min)	Cap (pF)	Latency (ps)	Yield (ps)	Run-time (min)
s1423	[8]	D-UST	3.4	140	100	1	3.4	140	100	-
	this work	RTS-UST	3.2	128	100	1	3.2	138	100	-
s5378	[8]	D-UST	5.7	130	100	1	5.7	130	100	-
	this work	RTS-UST	5.8	205	57	2	5.8	205	100	1
s15850	[8]	D-UST	20.2	405	97	5	20.7	425	99.4	13
	[10]	D-UST	17.3	328	81	4	17.9	424	81.4	14
	[10]	LD-UST	17.7	291	99	5	18.1	313	100	11
	this work	RTS-UST	17.5	244	99	9	17.7	256	100	14
msp	[8]	D-UST	1.9	98	100	4	1.9	98	100	-
	this work	RTS-UST	1.5	89	100	4	1.5	89	100	-
fpu	[8]	D-UST	2.3	87	100	2	2.3	87	100	-
	this work	RTS-UST	1.9	109	93	4	1.9	109	100	1
ecg	[8]	D-UST	66.8	417	99.8	39	75.7	474	91.6	341
	[10]	D-UST	35.8	382	99.4	20	36.3	401	99.4	33
	[10]	LD-UST	35.0	318	94.6	29	35.2	345	100	51
	this work	RTS-UST	26.0	234	99.6	63	27.0	247	100	32
aes	[10]	D-UST	207.5	2207	82.8	245	208.3	2320	97.6	180
	[10]	LD-UST	233.9	1863	100.0	133	234.7	1933	99.0	152
	this work	RTS-UST	200.7	1172	86.8	155	202.0	1242	96.6	103
Norm.	[8]	D-UST	**1.36**				**1.43**			
	[10]	D-UST	**1.15**				**1.13**			
	[10]	LD-UST	**1.16**				**1.16**			
	this work	RTS-UST	**0.996**				**1.00**			

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Summary and Questions

- Clock tree construction based on static bounded useful arrival time constraints
- New LP formulation to specify the constraints