UC San Diego

Invited: Scaling Standard Cell Layout Using Track Height Compression and Design Technology Co-Optimization

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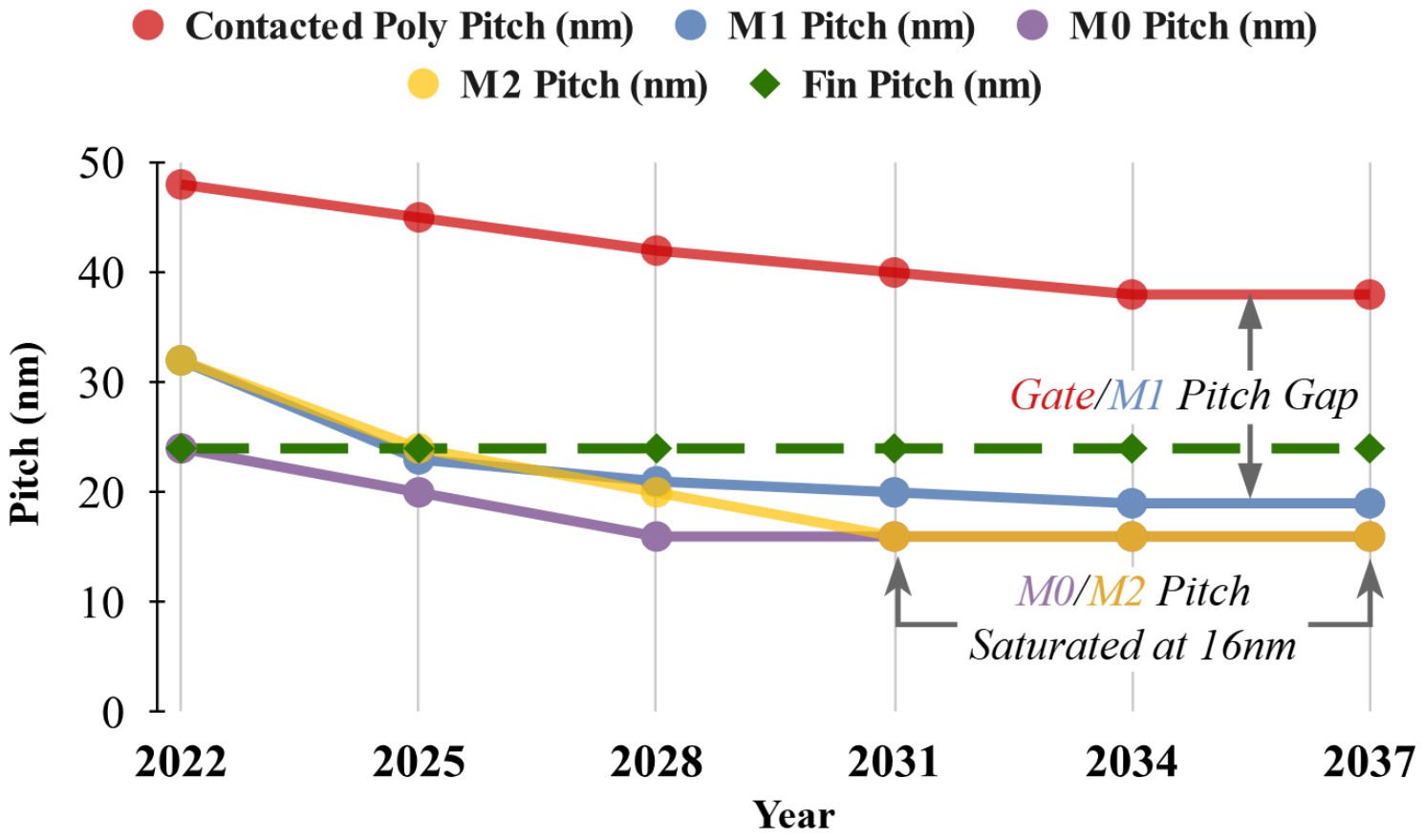
Outlines

- Preliminary: Motivation, Cell Height Compression, DTCO/STCO
- Design Knobs: Metal Pitch, Gate Cut and LISD, Double Row Cells, Power/Ground Distribution
- Experiments: Cell Layout, Block Level Layout
- Tool Release: SMTCell-MH

Preliminary: Motivation - Continue the Prophecy of Moore's Law

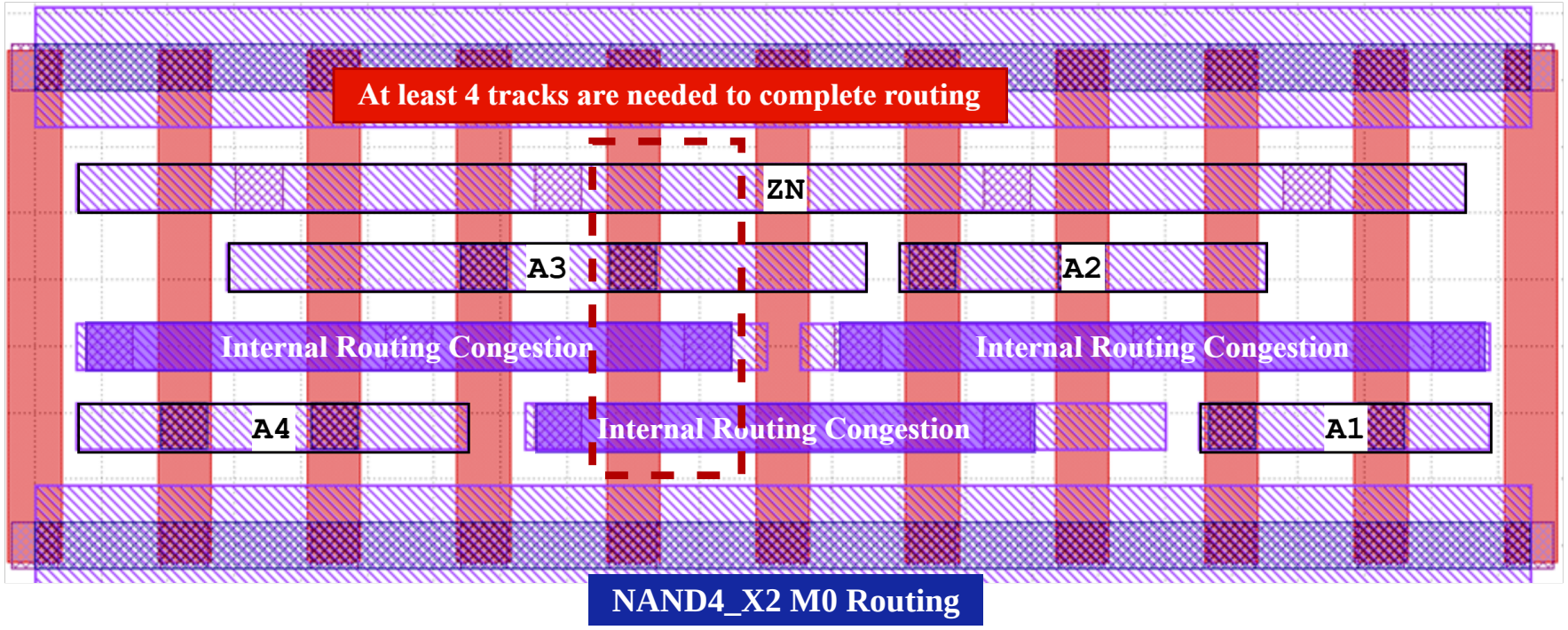
- Moore's Law: #transistors doubles every two years.
- IRDS roadmap shows
  - Contacted poly pitch (CPP) saturates at ~40nm. Thus, #CPPs dominate the cell width.
  - Metal (M0, M1, M2) pitches are smaller than CPP and saturate at around 16nm.
- We study layout area scaling
  - Track height compression
  - Gear Ratio for the layout area scaling
  - DTCO/STCO exploration



IEEE. 2020. IRDS International Roadmap for Devices and Systems: More-than-Moore White Paper. (2020).

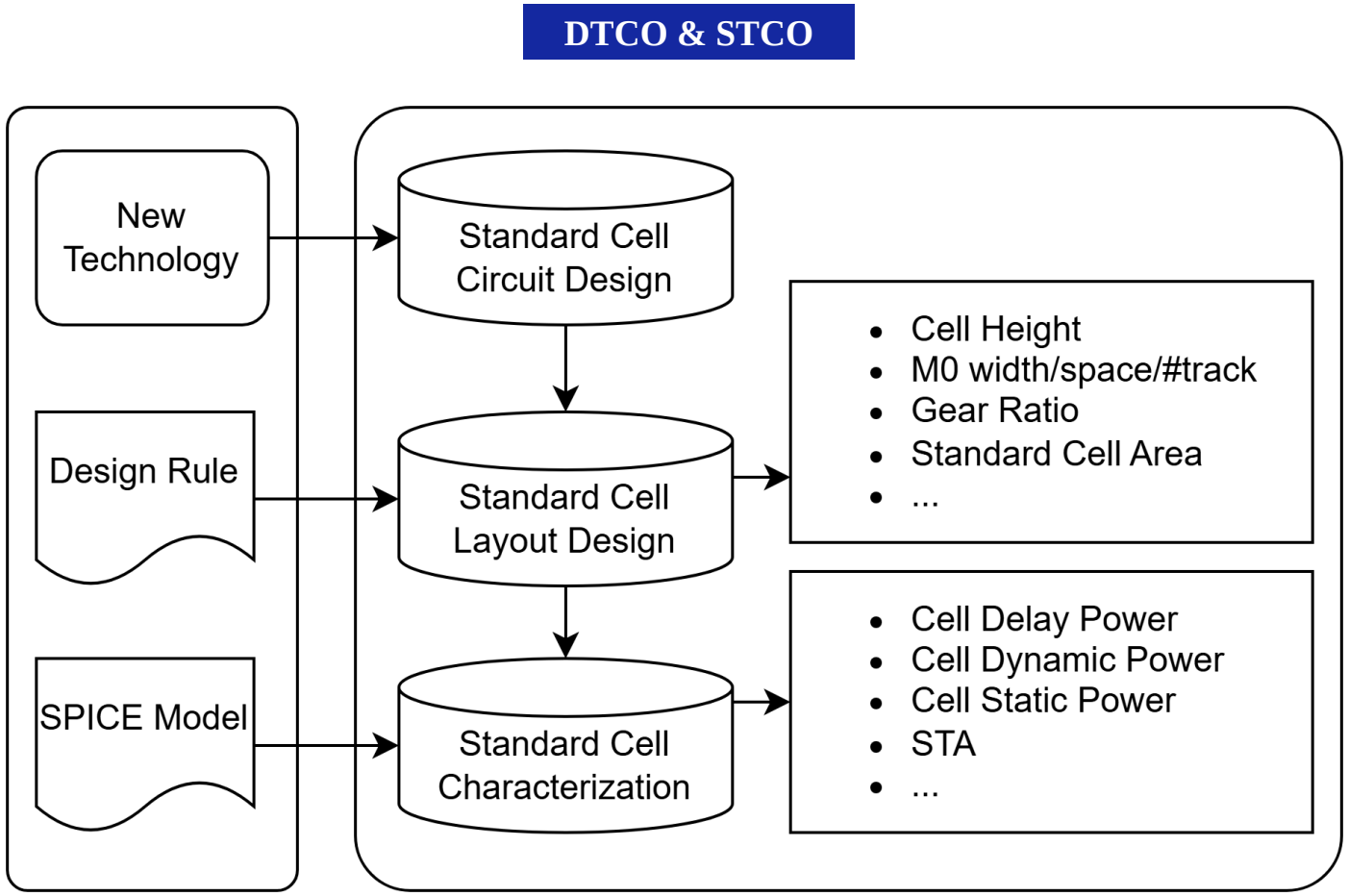
Preliminaries –Cell Height Compression

- When compressing cells, cells can:
  - Uses extra CPPs due to internal congestions;
  - Become *infeasible* due to the M0 routing congestions.



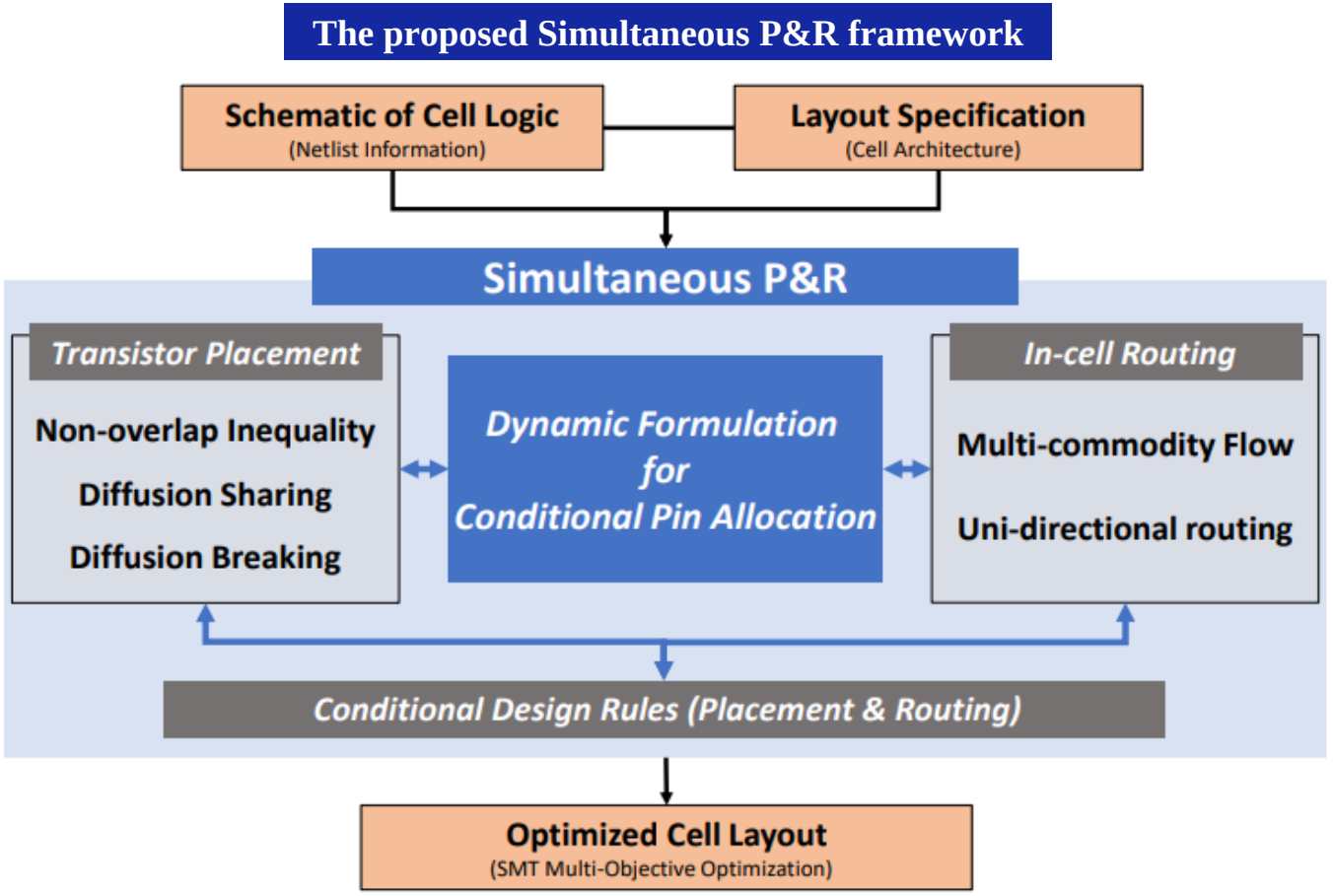
Preliminaries – DTCO/STCO-Design Flow

- **Design Technology Co-Optimization (DTCO)**: Layout/process engineers exchange feedback to address design challenges.
- **System Technology Co-optimization (STCO)**: Discover new design knobs and realize this technology through a system-level approach.
- The co-optimization effort promotes an efficient design workflow.



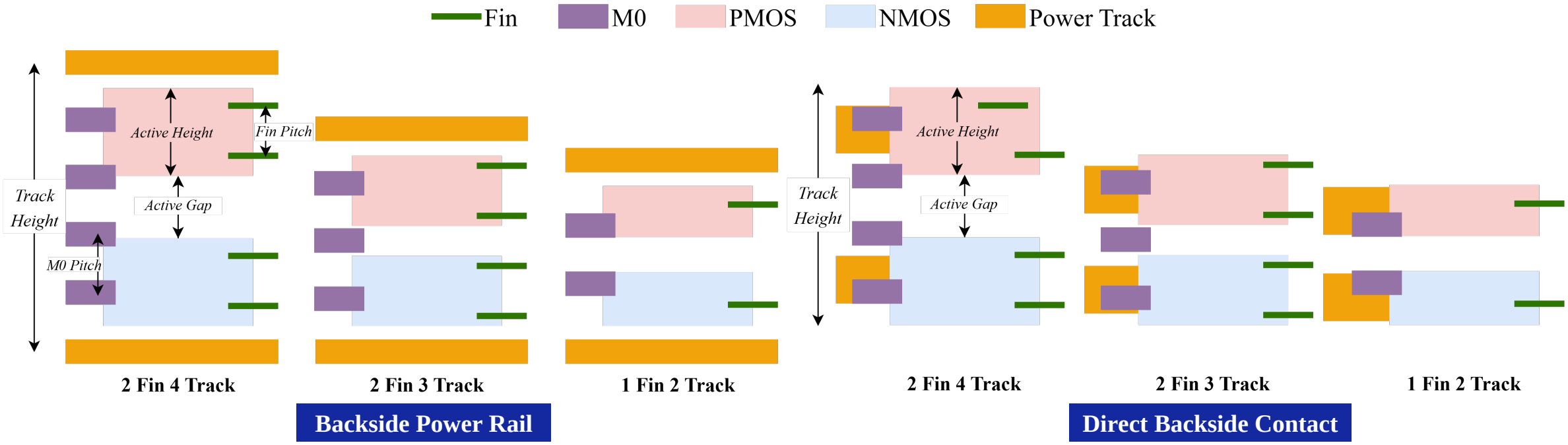
Preliminaries – DTCO/STCO-Design Automation Tool

- Handle conditional design rules and explore DTCO and STCO design parameters.
- Automate the layout with guaranteed solutions.
- Research and develop the framework: Satisfiability-Modulo-Theory (SMT) based cell layout tools:
  - SP&R - FinFET [Github]
  - SP&R - CFET
  - SP&R -VFET [Github]
  - SMTCell - Single-Height [Github]
  - SMTCell - Multi-Height [Github]



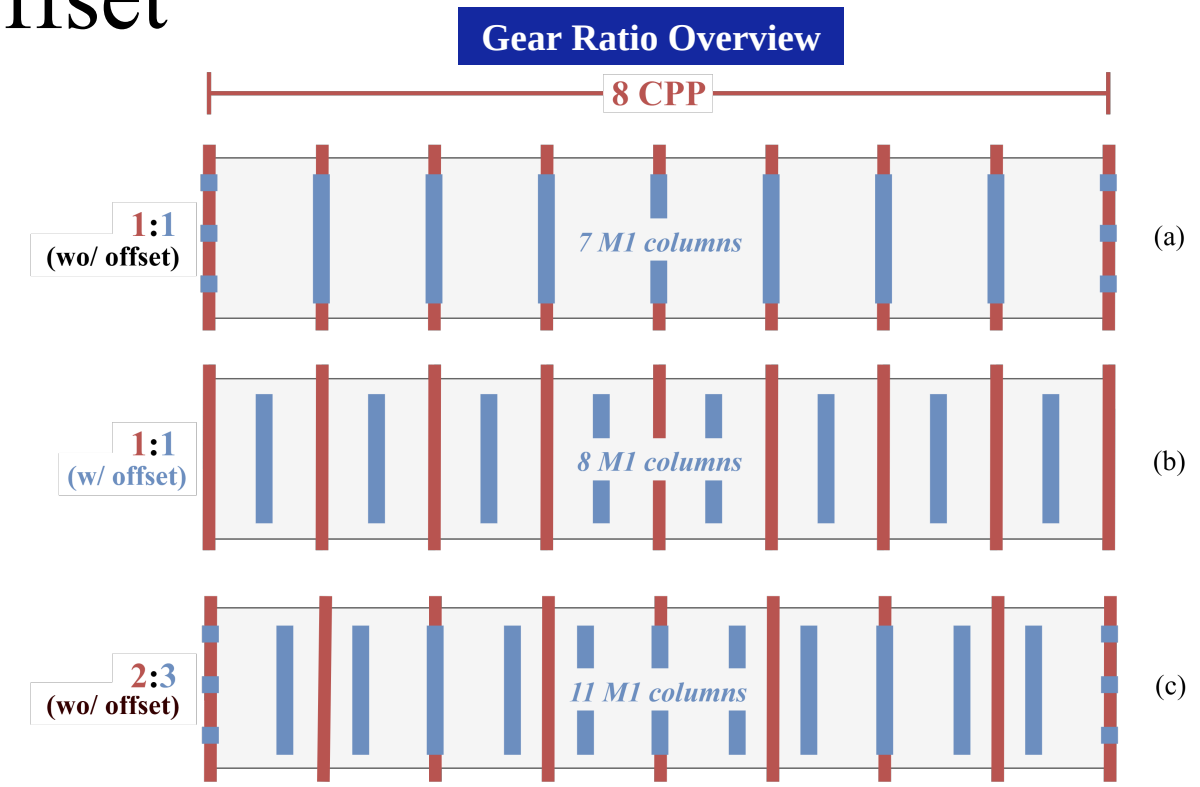
Design Knobs

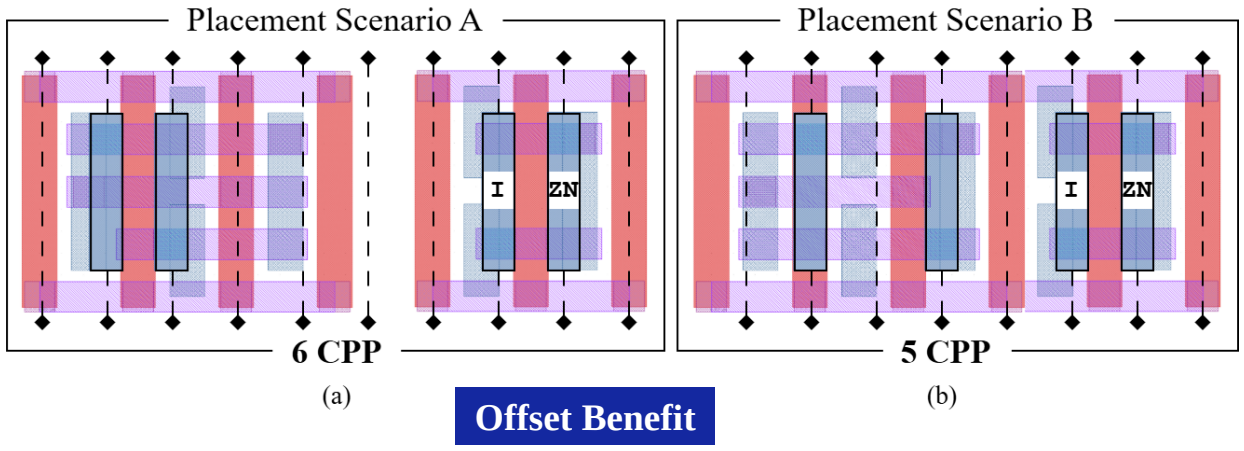
- Metal Pitch: Gear Ratio & Offset
- Gate Cut and LISD Technologies
- Double Height Architecture with Pass-Throughs
- Backside Power Delivery Approaches



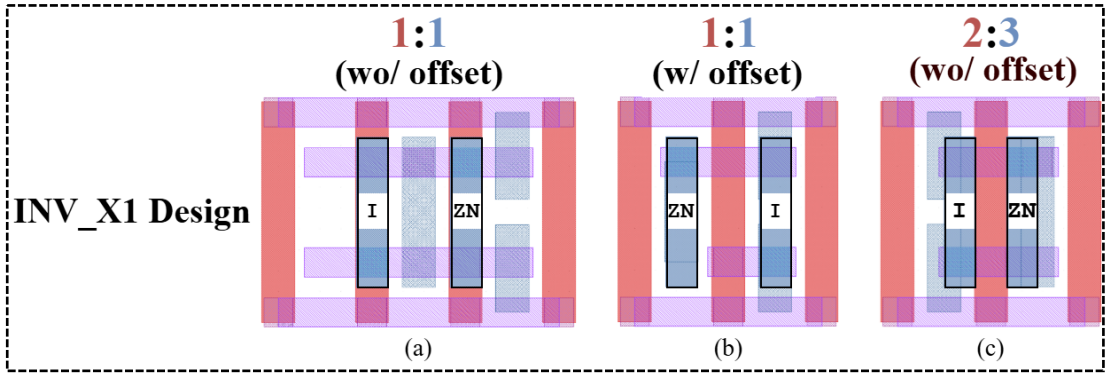
Design Knob – Gear Ratio & Offset

- We apply gear ratio between the contacted poly pitch and the M1 pitch.
- A lower M1 pitch offers benefit to routing resources and cell area.
- M1 offset offers more routing resources and improved cell abutment.





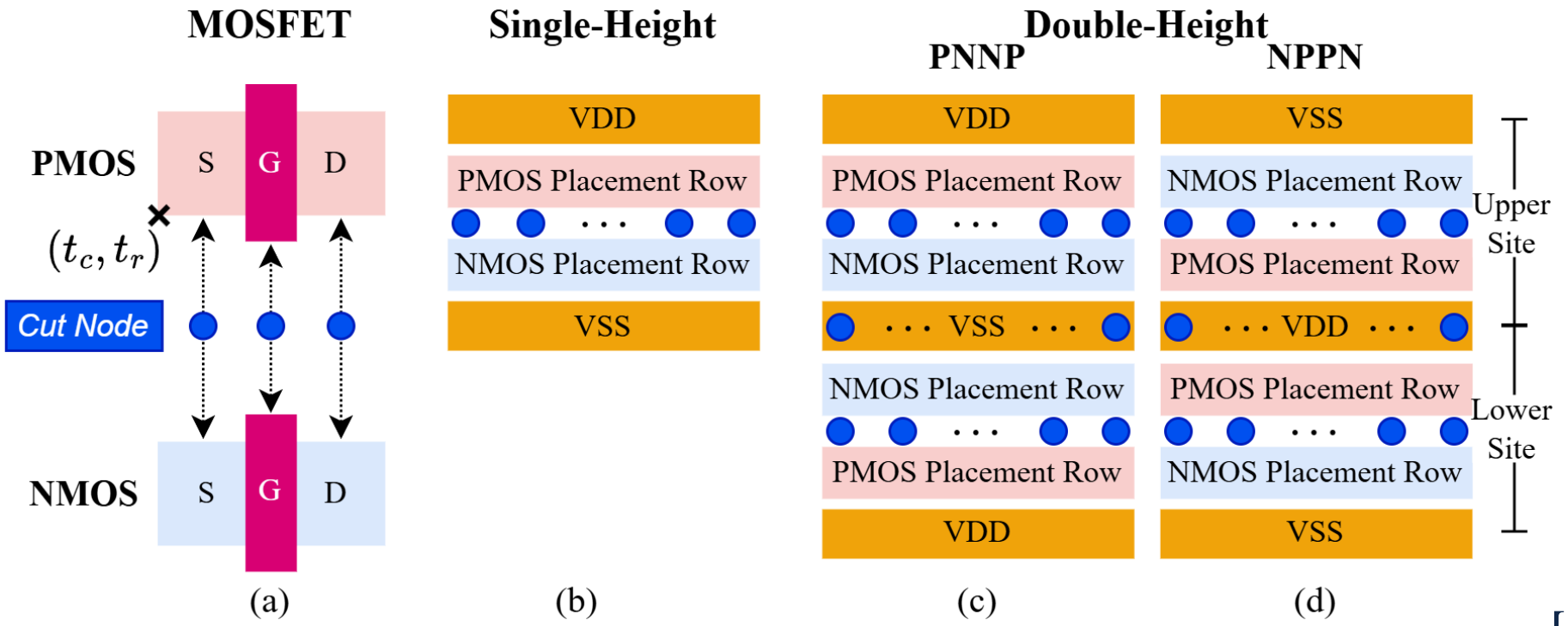
Offset Benefit



Gear Ratio & Offset Benefit

Design Knob – Gate Cut, LISD & Pass-Throughs

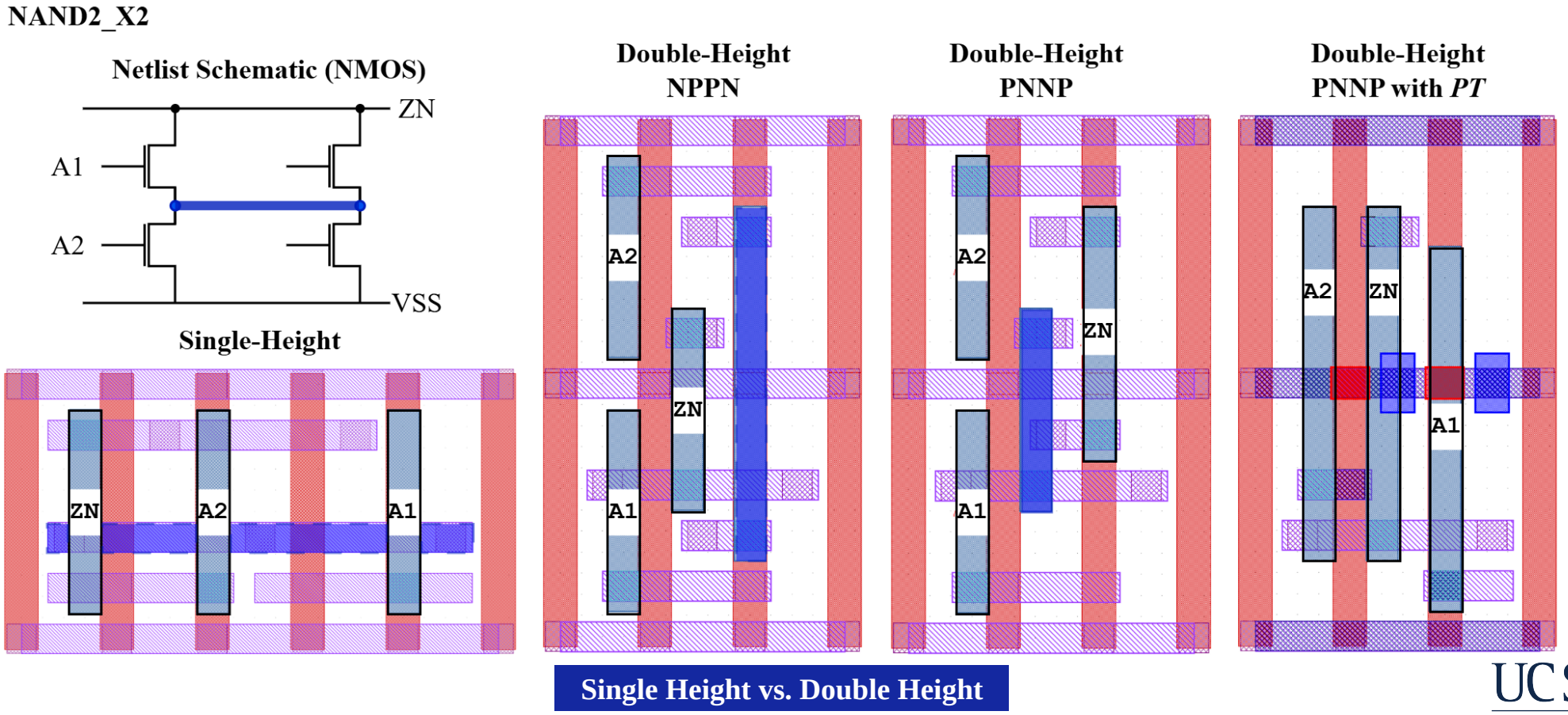
- Gate cut, LISD merging and pass-throughs allows source/gate/drain to connect or disconnect without the need for vertical routings.
- These three knobs are enabled by cut node formulations which are enabled or disabled based on the adjacently placed MOSFETs.



Cut Node & Pin Shapes

Design Knob: Double-Height with Pass-throughs

- Compared to a single-height cell, a double-height cell can lead to:
  - Less congested horizontal routing and better pin placement;
  - Pass-throughs enablement can reduce required metals.

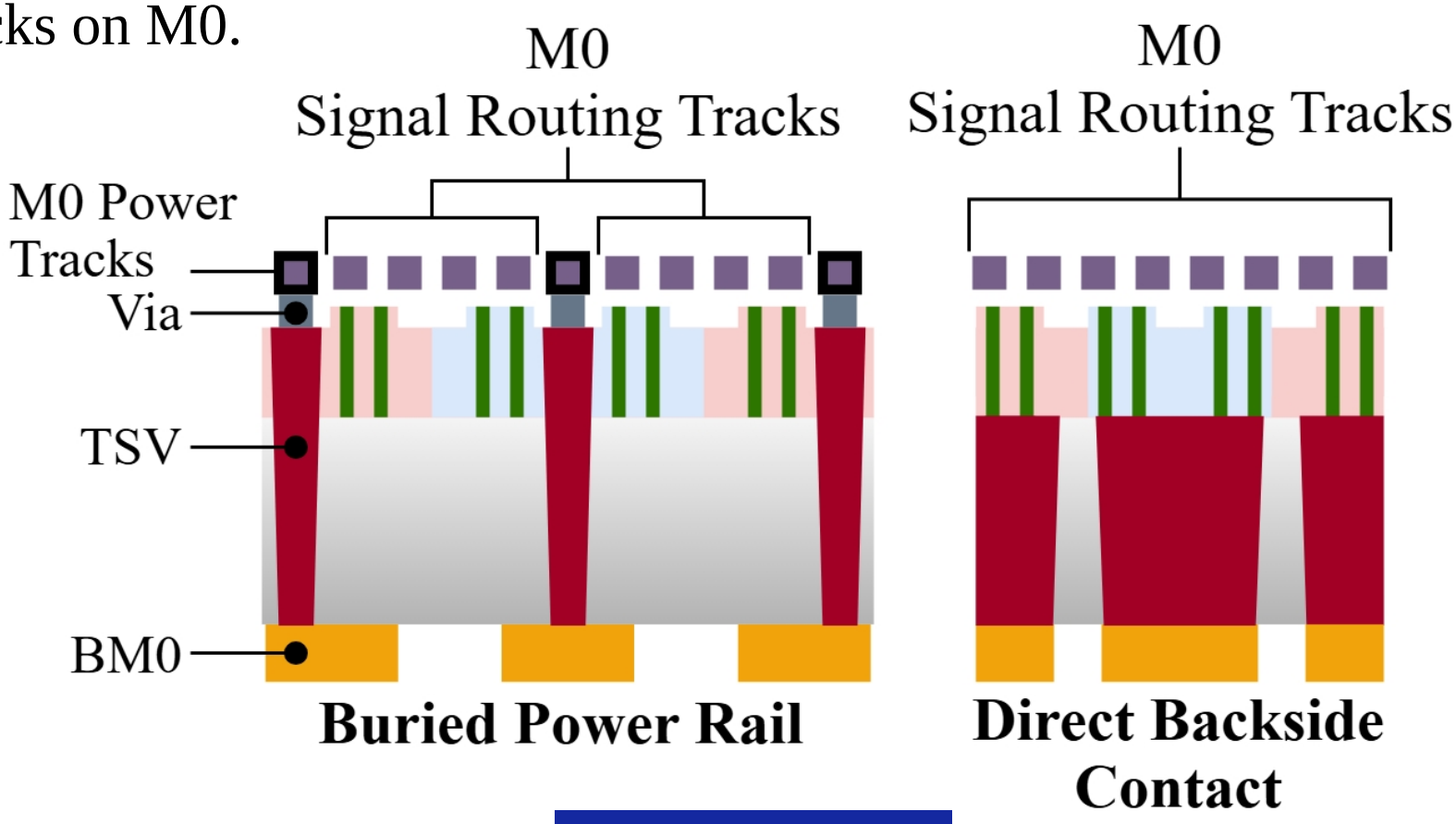


Single Height vs. Double Height

Design Knob – Backside Power Delivery Approaches

Two power delivery options.

- **Backside Power Rail (BPR)** backside power rails connect to the power track on M0.
- **Direct Backside Contact (DBC)** backside power rails make direct connection. No power tracks on M0.



Power Configuration

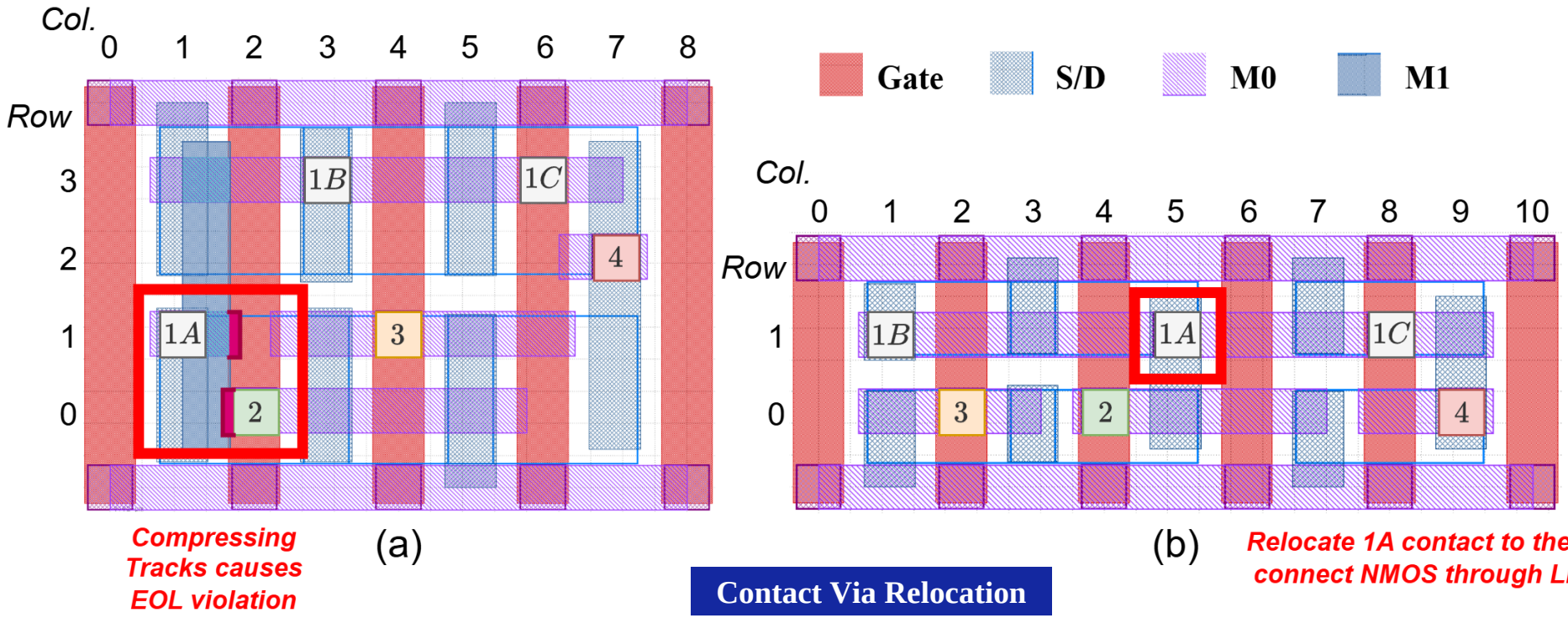
Experiments

- We run SMTCell iteratively with different design knobs to enable more feasible cells. Cell area and width are used to determine the area gain at cell level.
- We benchmark our cell libraries using the AES design at block level.
- The following experiments are carried out at cell-level:
  - Single-height architecture for 45:45 GR, 45:45(+22.5) GR, 45:30 GR in 4T/3T/2T.
  - **Double-height architecture** for 45:30 GR in 4T/3T/2T.
  - **Double-height architecture (w/ Pass-throughs)** for 45:30 GR in 4T/3T/2T.

We fix the contacted poly pitch to be 45nm. 45:45 GR corresponds to 1:1 GR; 45:45(+22.5) GR corresponds to 1:1(+1/2) GR; 45:30 GR corresponds to 3:2 GR.

Design Challenge – From 4T to 2T

Example: AND2_X1 layouts in 4T and 2T architectures. A problematic via pair in 2T layout is resolved by relocating a via through LISD merging, avoiding additional vias on the NMOS row. However, since adjacent columns are occupied by net 1 and the power net, diffusion sharing is not feasible, necessitating a diffusion break at column 6, which increases the cell width by one CPP.



Compressing Tracks causes EOL violation

(a)

(b)

Relocate 1A contact to the top row and connect NMOS through LISD merging

Contact Via Relocation

Single Row Height

- We shrink the track height from 4T to 2T.
  - Some cells increase width
  - 45:30 GR can enable more feasible cells in 2T
  - 2T is impossible to use in single-height architecture due to the lack of majority of the cells and sequential logic cells.

Cell Name	#FET	# Net	Cell Width (#CPP)								
			4T			3T			2T		
			45:45	45:45†	45:30	45:45	45:45†	45:30	45:45	45:45†	45:30
AND2_X2	8	7	5	5	5	5	5	5	7	6	6
AND3_X2	10	9	6	6	6	6	6	6	×	8	7
AOI21_X1	6	8	5	5	5	6	6	6	×	×	×
AOI21_X2	12	8	8	8	8	10	10	10	×	×	×
AOI22_X2	16	10	10	10	10	×	×	×	×	×	×
BUF_X4	4	5	7	7	7	7	7	7	7	7	7
BUF_X8	4	5	13	13	13	13	13	13	13	13	13
DFFHQN_X1	24	17	14	14	14	17	16	14	×	×	×
LHQ_X1	8	13	10	10	10	10	10	10	×	×	×
MUX2_X1	12	12	7	7	7	8	8	7	×	×	×
NAND2_X1	4	6	3	3	3	3	3	3	×	4	4
NAND2_X2	8	6	5	5	5	5	5	5	×	×	×
NAND3_X1	6	8	4	4	4	4	4	4	×	×	×
NAND3_X2	12	8	8	8	8	×	×	×	×	×	×
NAND4_X2	16	10	10	10	10	×	×	×	×	×	×
NOR2_X1	4	6	3	3	3	3	3	3	×	4	4
NOR2_X2	8	6	5	5	5	5	5	5	×	×	×
NOR3_X1	6	8	4	4	4	4	4	4	×	×	×
NOR3_X2	12	8	8	8	8	×	×	×	×	×	×
NOR4_X2	16	10	10	10	10	×	×	×	×	×	×
OAI21_X1	6	8	5	5	5	6	6	6	×	×	×
OAI21_X2	12	8	8	8	8	10	10	10	×	×	×
OAI22_X2	16	10	10	10	10	×	×	×	×	×	×
OR2_X2	8	7	5	5	5	5	5	5	7	6	6
OR3_X2	10	9	6	6	6	6	6	6	×	8	7
XOR2_X1	10	9	7	7	7	9	8	8	×	×	×

† Indicates the usage of offset cells.
× indicates infeasible cells.

Double Height

- Infeasibility issues can almost be resolved with double-height architecture.
- Double-height architecture favors different row orders in different netlists: PNNP vs. NPPN.
- However, DFFHQN remains to be infeasible for 2T architecture.

Cell Name	Architect. Config.			Cell Width (#CPP)			Cell Area (×1E3 nm^2)			Z3 Runtime (h::mm:ss)		
	4T	3T	2T	4T	3T	2T	4T	3T	2T	4T	3T	2T
AND2_X2	/	/	PNNP	3	3	4	32.4	25.9	25.9	0:00:52	0:00:17	0:00:42
AND3_X2	/	/	/	4	4	4	43.2	34.6	25.9	0:05:20	0:00:45	0:02:29
AOI21_X1	/	/	/	3	4	4	32.4	34.6	25.9	0:00:48	0:00:22	0:00:45
AOI21_X2	/	/	×	4	5	×	43.2	43.2	×	0:03:25	0:03:41	×
AOI22_X2	/	×	×	5	×	×	54.0	×	×	0:14:52	×	×
BUF_X4	/	/	/	4	4	4	43.2	34.6	25.9	0:00:18	0:00:05	0:00:12
BUF_X8	PNNP	PNNP	PNNP	7	7	7	75.6	60.5	45.4	0:02:30	0:00:51	0:07:34
DFFHQN_X1	NPPN	/	×	8	9	×	86.4	77.8	×	3:33:05	0:29:05	×
LHQ_X1	/	/	/	6	6	6	64.8	51.8	38.9	0:04:31	0:00:52	0:11:06
MUX2_X1	/	/	/	4	5	5	43.2	51.8	32.4	0:08:03	0:02:49	0:09:56
NAND2_X1	PNNP	PNNP	PNNP	2	3	4	21.6	25.9	25.9	0:00:16	0:00:05	0:00:17
NAND2_X2	/	/	/	3	4	5	32.4	34.6	32.4	0:00:24	0:00:12	0:00:27
NAND3_X1	/	/	/	3	4	4	32.4	34.6	25.9	0:00:49	0:00:14	0:01:01
NAND3_X2	/	/	×	4	5	×	43.2	43.2	×	0:06:36	0:01:00	×
NAND4_X2	/	/	×	5	7	×	54.0	60.5	×	0:07:47	0:18:39	×
NOR2_X1	NPPN	NPPN	NPPN	2	3	4	21.6	25.9	25.9	0:00:22	0:00:07	0:00:12
NOR2_X2	/	/	/	3	4	5	32.4	34.6	32.4	0:00:34	0:00:36	0:00:19
NOR3_X1	/	/	/	3	4	4	32.4	34.6	25.9	0:02:24	0:00:20	0:00:29
NOR3_X2	/	/	×	4	5	×	43.2	43.2	×	0:02:16	0:03:03	×
NOR4_X2	/	/	×	5	5	×	54.0	43.2	×	0:10:48	1:12:04	×
OAI21_X1	/	/	/	3	4	4	32.4	34.6	25.9	0:05:53	0:00:22	0:01:11
OAI21_X2	/	/	×	4	5	×	43.2	43.2	×	0:02:00	0:04:01	×
OAI22_X2	/	×	×	5	×	×	54.0	×	×	0:16:52	×	×
OR2_X2	/	/	NPPN	3	3	4	32.4	25.9	25.9	0:00:58	0:00:16	0:01:04
OR3_X2	/	/	/	4	4	4	43.2	34.6	25.9	0:03:17	0:00:41	0:01:33
XOR2_X1	/	/	/	4	4	5	43.2	34.6	32.4	0:03:14	0:00:34	0:05:14

/ indicates no area difference between PNNP and NPPN configuration.

× indicates infeasible cells.

Double Height (w/ PT)

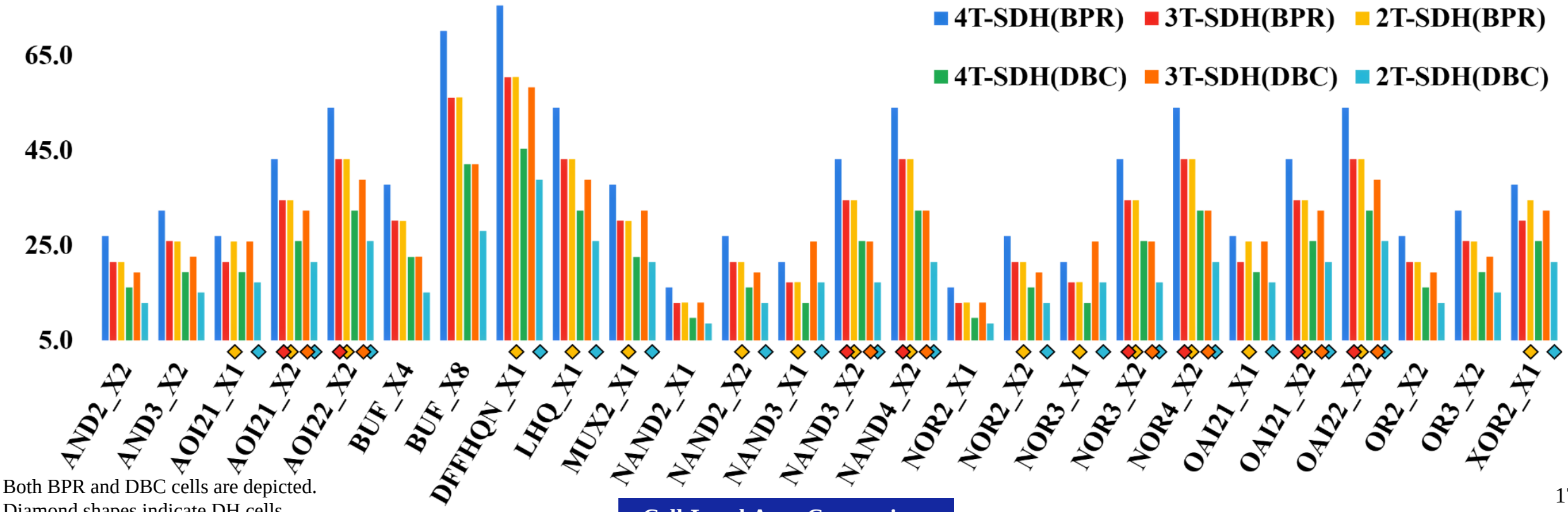
- All infeasibility issue is resolved. Notably, compared to 4T-DH, 3T-DH improves the cell area by 16.13%, and 2T-DH improves the cell area by 30.80%.
- 2T-DH and 4T-SH have the same number of horizontal routing tracks.
- An area reduction of 22.88% by using 2T-DH over 4T-SH.

Cell Name	Architect. Config.			Cell Width (#CPP)			Cell Area (×1E3 nm^2)			Z3 Runtime (h::mm:ss)		
	4T	3T	2T	4T	3T	2T	4T	3T	2T	4T	3T	2T
AND2_X2	/	/	PNNP	3	3	4	32.4	25.9	25.9	0:00:41	0:00:16	0:00:12
AND3_X2	/	/	/	4	4	4	43.2	34.6	25.9	0:03:29	0:00:43	0:00:15
AOI21_X1	/	NPPN	/	3	3	4	32.4	25.9	25.9	0:00:53	0:00:17	0:00:08
AOI21_X2	/	/	PNNP	4	4	5	43.2	34.6	32.4	0:01:54	0:00:43	0:00:22
AOI22_X2	/	/	PNNP	5	5	6	54.0	43.2	38.9	0:22:12	0:02:13	0:11:22
BUF_X4	/	/	/	4	4	4	43.2	34.6	25.9	0:00:22	0:00:05	0:00:02
BUF_X8	PNNP	PNNP	PNNP	7	7	7	75.6	60.5	45.4	0:02:42	0:00:57	0:00:11
DFFHQN_X1	/	/	/	8	8	9	86.4	69.1	58.3	3:56:47	0:28:46	0:01:00
LHQ_X1	/	/	/	6	6	6	64.8	51.8	38.9	0:05:55	0:01:00	0:04:13
MUX2_X1	/	/	NPPN	4	4	5	43.2	34.6	32.4	0:05:08	0:00:43	0:08:50
NAND2_X1	PNNP	PNNP	PNNP	2	3	3	21.6	25.9	19.4	0:00:15	0:00:05	0:00:02
NAND2_X2	/	PNNP	PNNP	3	3	3	32.4	25.9	19.4	0:00:57	0:00:08	0:00:04
NAND3_X1	/	/	/	3	4	4	32.4	34.6	25.9	0:00:50	0:00:39	0:00:06
NAND3_X2	/	/	/	4	4	4	43.2	34.6	25.9	0:00:50	0:06:00	0:00:17
NAND4_X2	/	PNNP	PNNP	5	5	5	54.0	43.2	32.4	0:02:35	0:01:31	0:02:28
NOR2_X1	NPPN	NPPN	NPPN	2	3	3	21.6	25.9	19.4	0:00:12	0:00:06	0:00:02
NOR2_X2	/	/	/	3	3	3	32.4	25.9	19.4	0:00:26	0:00:15	0:00:08
NOR3_X1	/	/	/	3	4	4	32.4	34.6	25.9	0:04:38	0:00:39	0:00:06
NOR3_X2	/	/	/	4	4	4	43.2	34.6	25.9	0:01:29	0:06:00	0:00:35
NOR4_X2	/	NPPN	NPPN	5	5	5	54.0	43.2	32.4	0:11:13	0:04:20	0:06:25
OAI21_X1	/	PNNP	/	3	3	4	32.4	25.9	25.9	0:02:01	0:00:16	0:00:09
OAI21_X2	/	/	NPPN	4	4	5	42.3	34.6	32.4	0:00:47	0:00:44	0:46:50
OAI22_X2	/	/	NPPN	5	5	6	54.0	43.2	38.9	0:04:53	0:03:00	0:30:56
OR2_X2	/	/	NPPN	3	3	4	32.4	25.9	25.9	0:03:30	0:00:18	0:00:14
OR3_X2	/	/	/	4	4	4	43.2	34.6	25.9	0:03:32	0:00:38	0:00:20
XOR2_X1	/	/	/	4	4	5	43.2	34.6	32.4	0:03:08	0:00:44	0:00:24

/ indicates no area difference between PNNP and NPPN configuration.

Experiment – Cell-Level Area Gain

- We combine SH and DH cells into a single library: 4T-SDH, 3T-SDH, and 2T-SDH cell libraries. We pick the best cell areas among each cell library and compare them using the figure below.
- Using 4T-SDH as the baseline:
  - 3T-SDH with BPR achieves 18.69% area reduction on average.
  - 2T-SDH with BPR achieves 26.46% area reduction on average.
  - 3T-SDH with DBC achieves 23.77% area reduction on average.
  - **2T-SDH with DBC achieves 38.72% area reduction on average.**

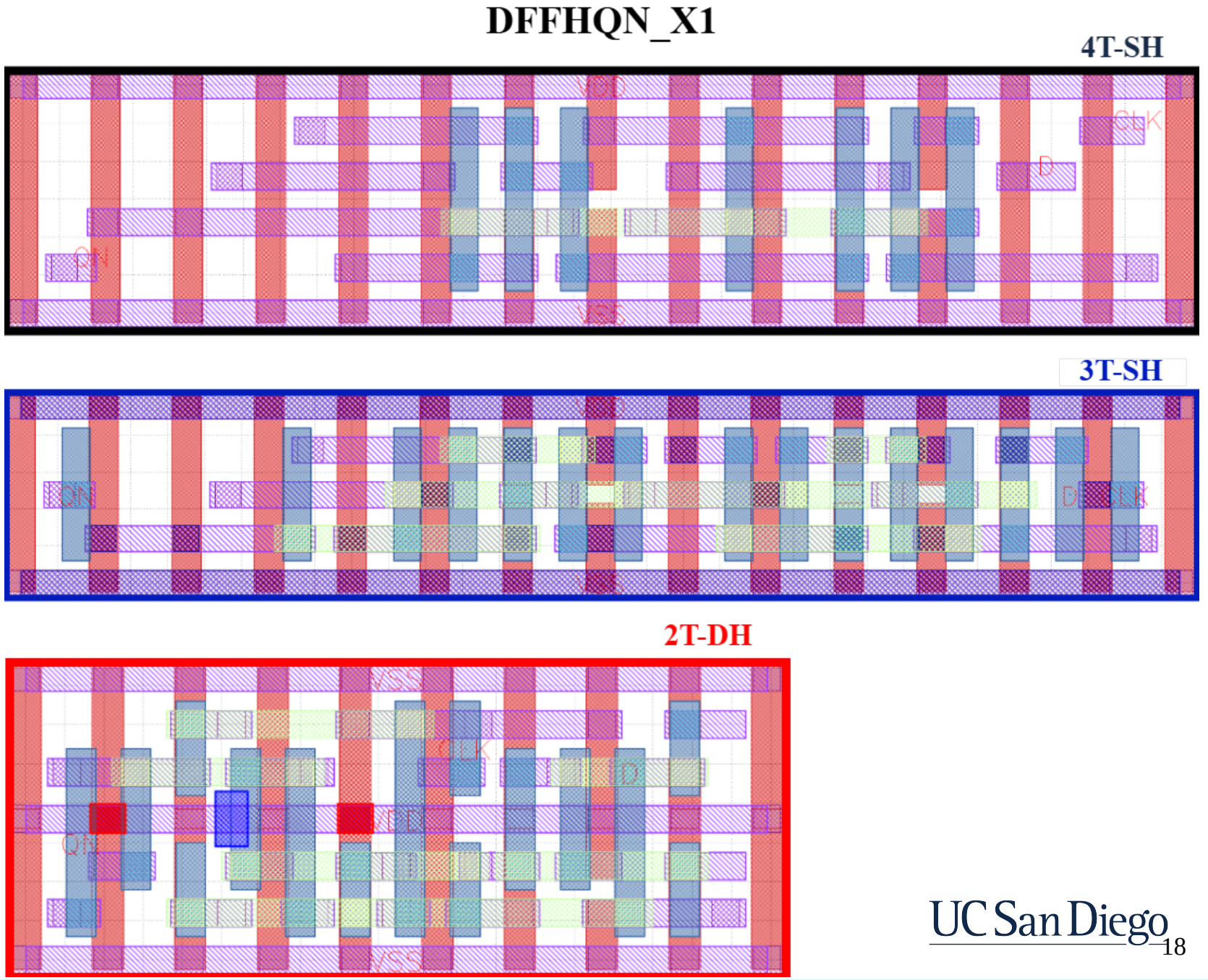


Both BPR and DBC cells are depicted.
Diamond shapes indicate DH cells.

Cell-Level Area Comparison

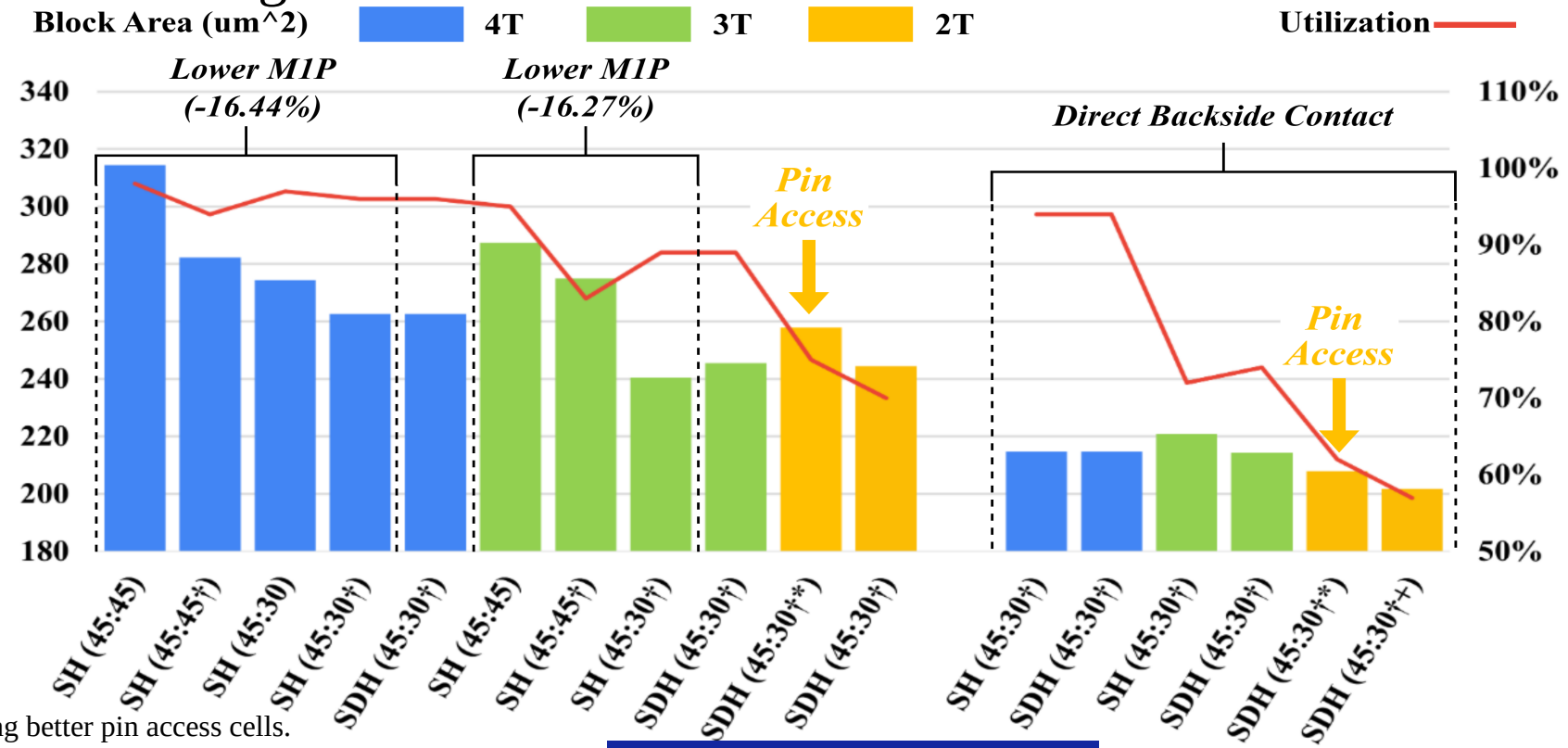
DFF Area Gain

- Cell area for the DFFHQN_X1:
  - 4T-SH 75.6E3nm^2.
  - 3T-SH 60.5E3nm^2.
  - 2T-DH 58.3E3nm^2.



Experiment – Block-Level Area Gain

- Our DTCO features achieved a block area reduction of **35.77%** overall.
- The best area achieved is **201.89um² by using 2T-SDH cells**.
- However, the overall utilization decreased from **98% to 57%.**
- If we prioritize pin accessibility ("Pin Access") cells, we can increase utilization to 62% with a slight block area increase to 207.85um².

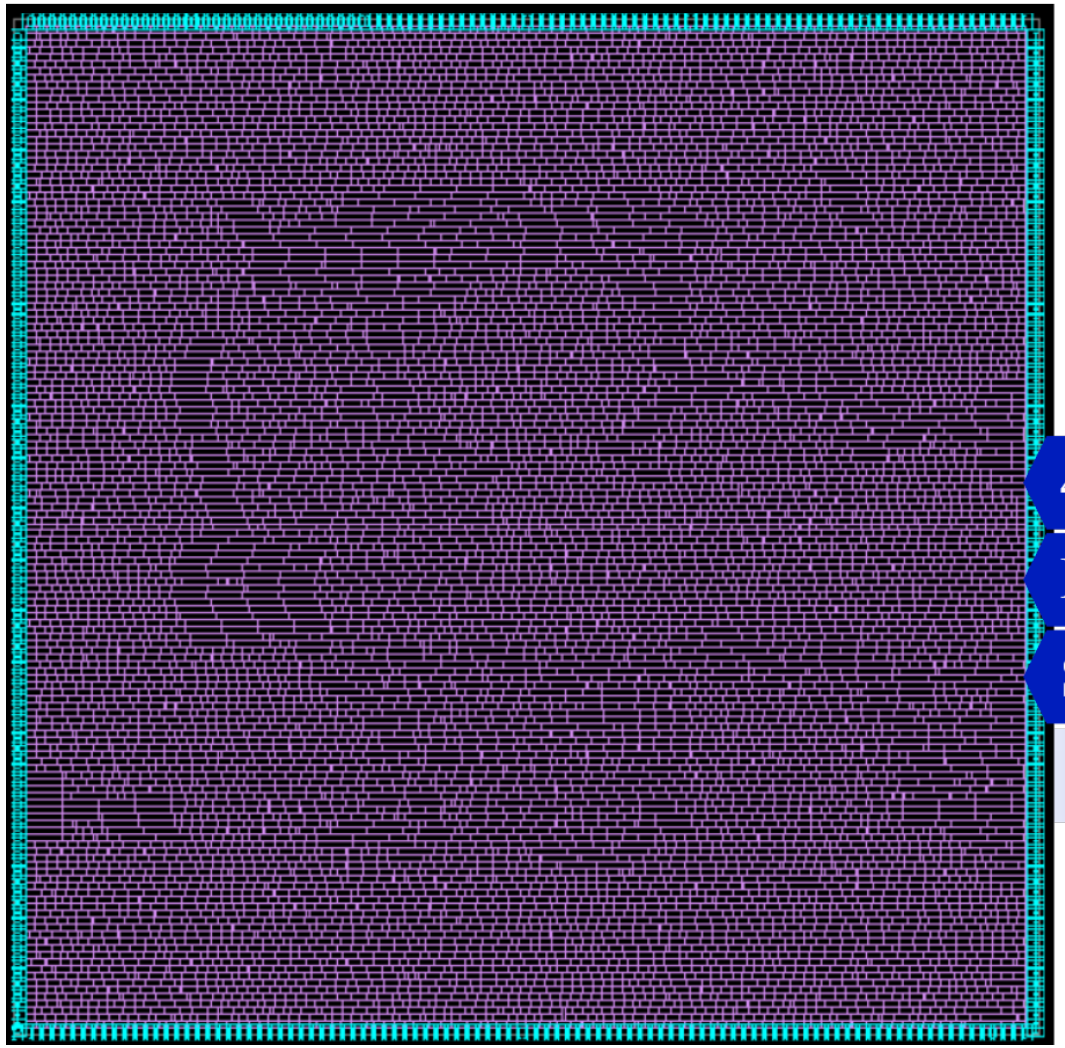


Block-Level Area Comparison

* Indicates the prioritizing better pin access cells.
† Indicates the usage of offset cells.

Experiment – Block-Level Area Gain

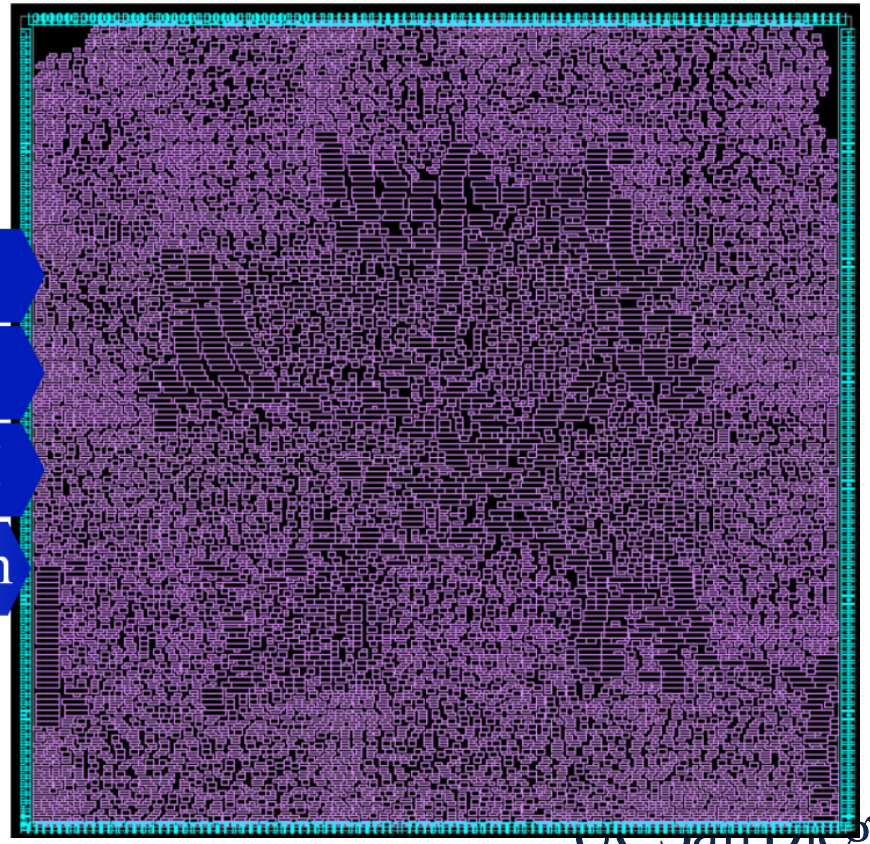
4T Architecture (314.35µm²)



DTCO Features

45:45	45:30
BPR	DBC
SH	SH + DH
	Passthrough

2T Architecture (201.89µm²)

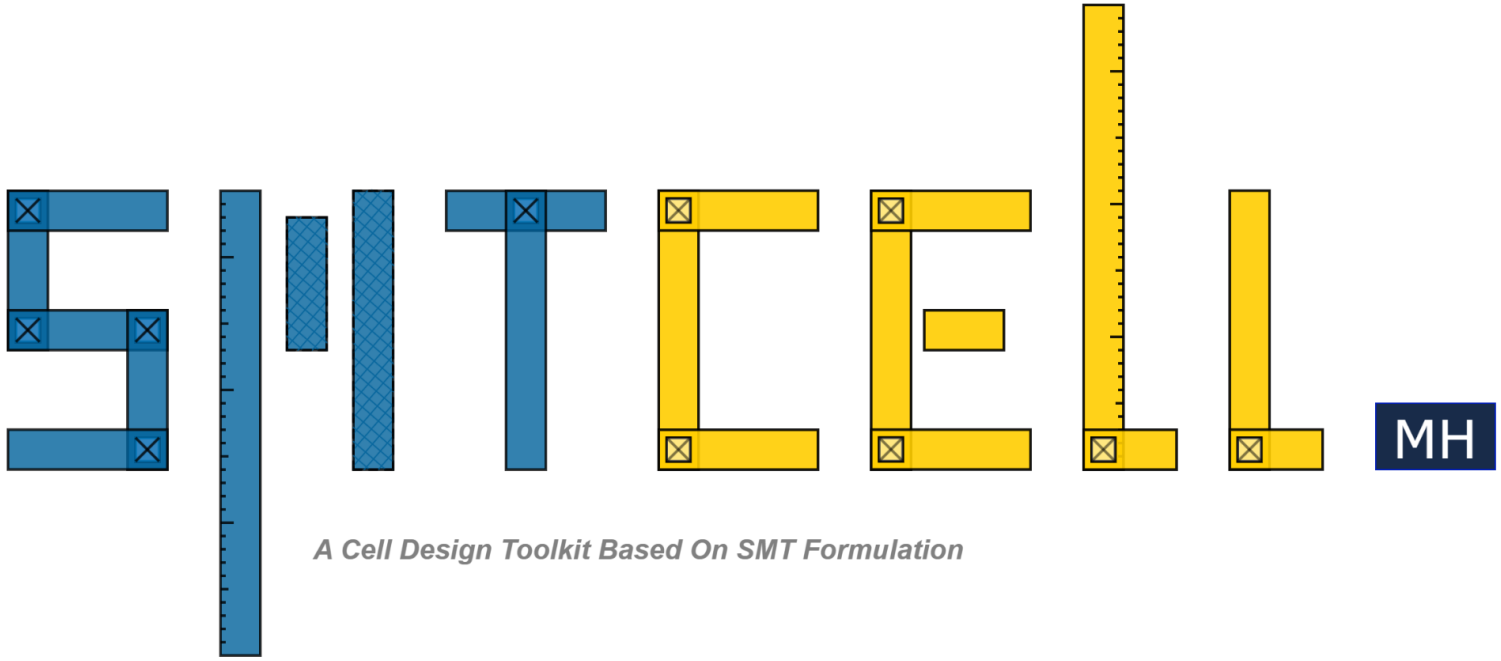


Conclusion

- Cell height compression from 4T to 2T is feasible with DTCO.
- Our DTCO features achieved an average cell area reduction of **38.72%** overall (DBC to DBC) and **50.98%** (BPR to DBC).
- Our DTCO features achieved a block area reduction of **35.77%** overall (BPC to DBC).
- Direct Backside Contact (DBC) plays a significant role in area reduction.
- Further work is needed to improve the utilization due to pin density wall.

GitHub Open Source

- Our SMTCell code is fully open sourced on GitHub:
  - Single-Height Version: https://github.com/ckchengucsd/SMTCellUCSD
  - Multi-Height Version: https://github.com/ckchengucsd/SMTCellUCSD-MH



Thank You!