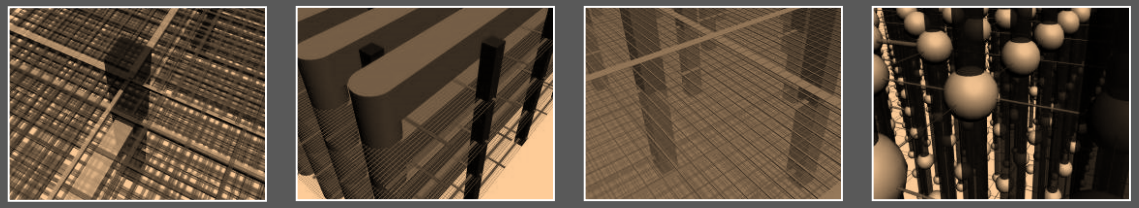
Routing Layer Sharing: An Opportunity for Routing Optimization in Monolithic 3D ICs



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Overview

- Motivation
  - Place and Route Flows for 3D ICs
  - Variations of different PnR stages
  - Types of 3D ICs
- Qualitative Analysis of Routing
  - Routing Trends in a 2D IC
  - Types of Nets in 3D IC
  - Routing types in 3D IC
- Prevalence of Metal Layer Sharing
  - Bonding Orientations
  - Partitioning Type
- Cost and PPA Saving & Analysis

Motivation

RTL-to-GDSII Design Flows for 3D ICs

Two types of 3D RTL-to-GDSII flows:

Partitioning-middle:

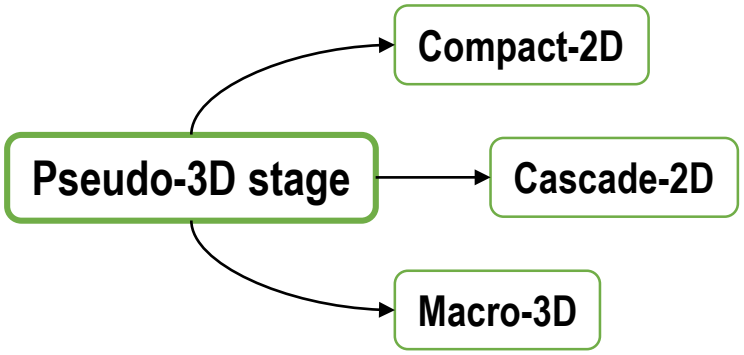
- Pseudo-3D stage
- Placement Transformation
- Tier Partitioning
- Via planning
- 3D Place and Route
- 3D optimization

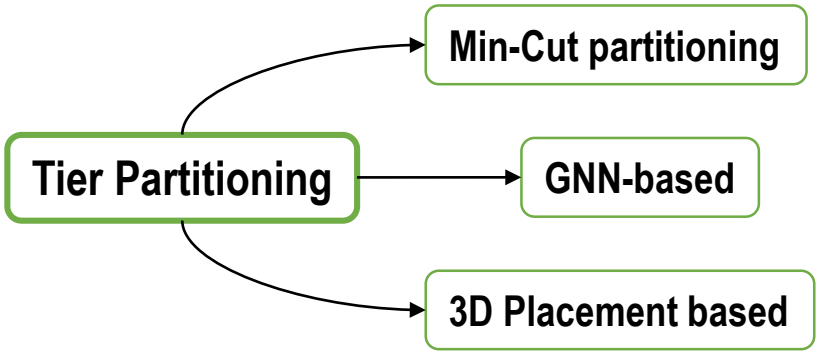
Partitioning-first:

- Tier Partitioning
- Via planning
- Accurate Pseudo-3D representation
- 3D Place and Route
- 3D optimization

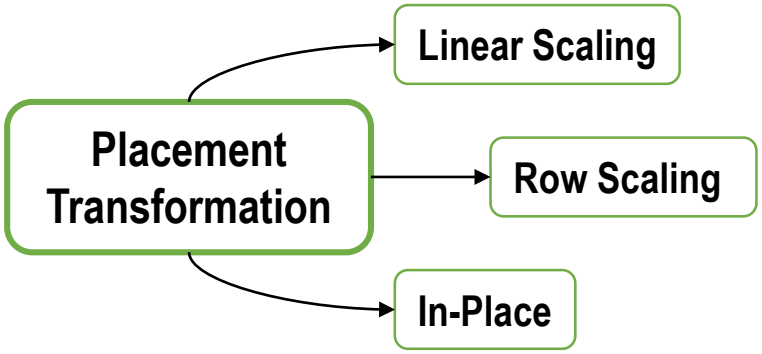
Motivation

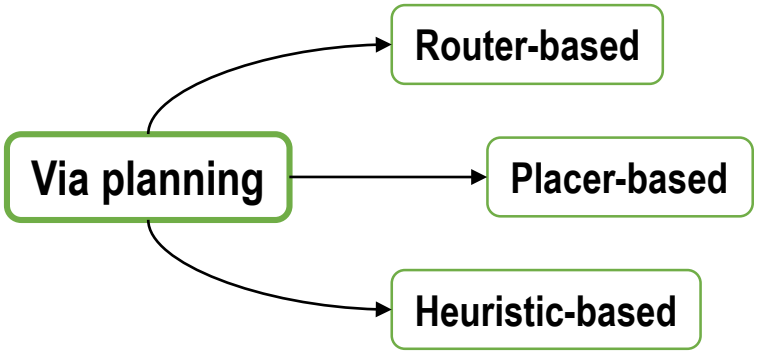
Design Stages





Different Pseudo-3D stages for various partitioning types



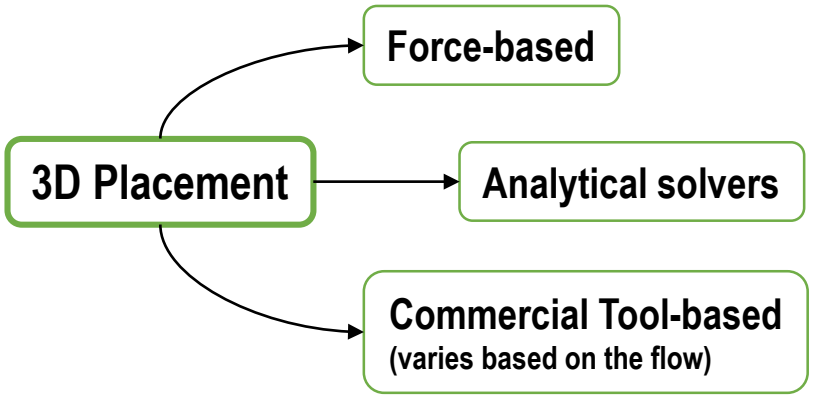


Different transformations have different benefits. Specific to the pseudo-3D flows

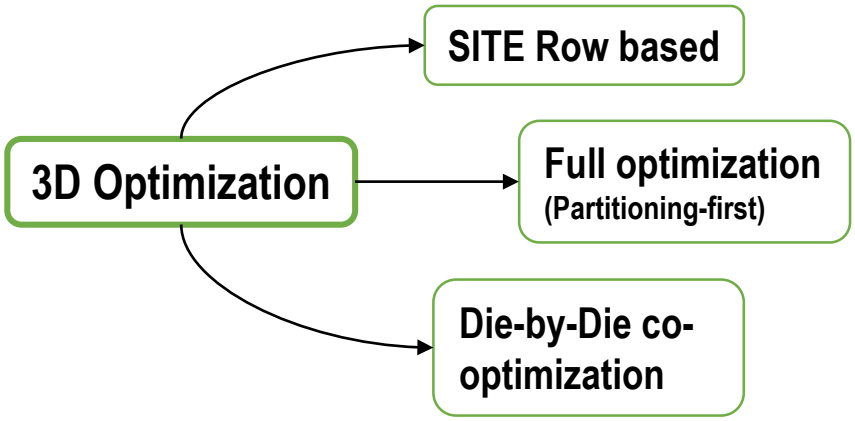
Different bond types are legalized differently, and also vary based on the flow

Motivation

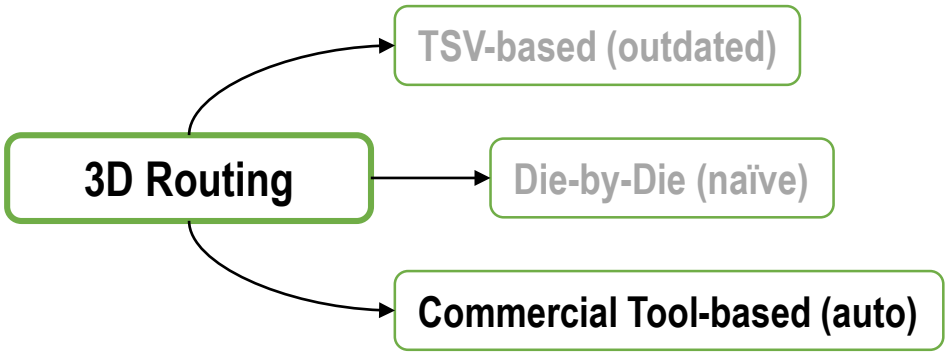
Design Stages



Different 3D placement options exist, also changes based on the flow



Different flows handle optimization differently

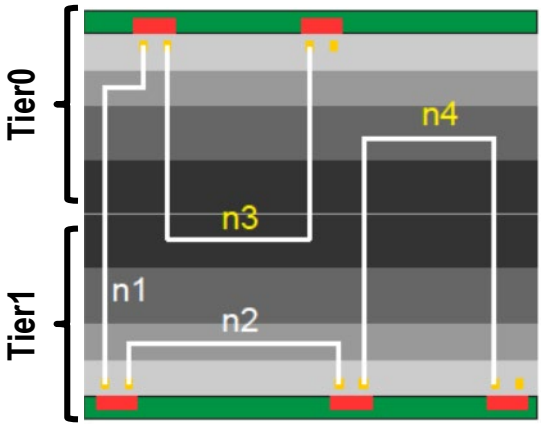


Routing is pretty similar for all the different bonding and partitioning types

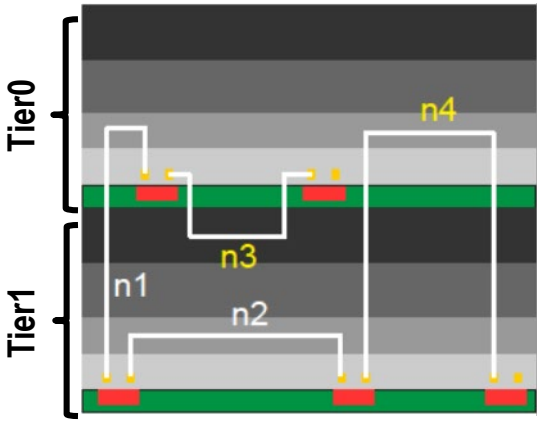
Motivation

Types of 3D ICs

Bonding Orientation



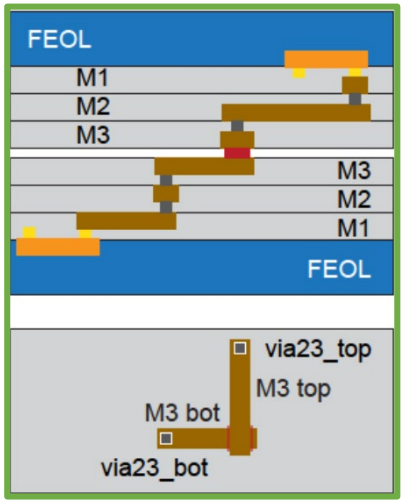
Face-To-Face



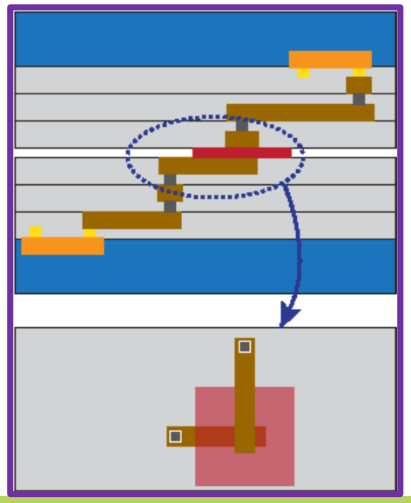
Face-To-Back

Bonding Pitch

Fine Pitch

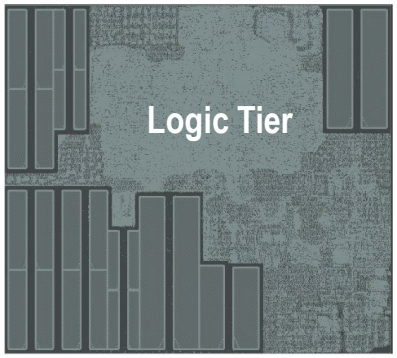


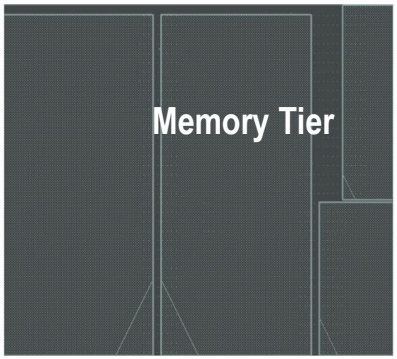
Coarse Pitch



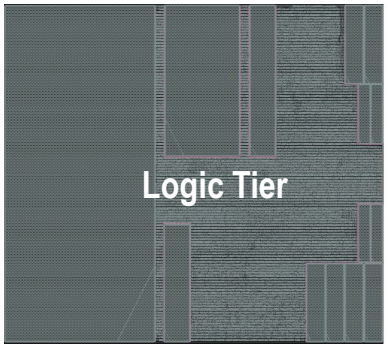
Partitioning Type

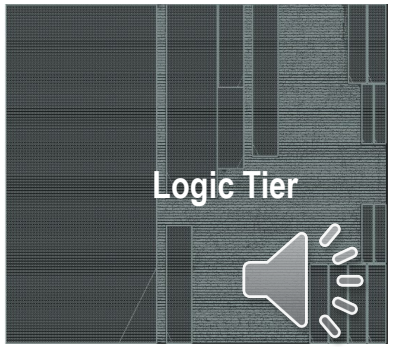
Logic on Memory Partitioning





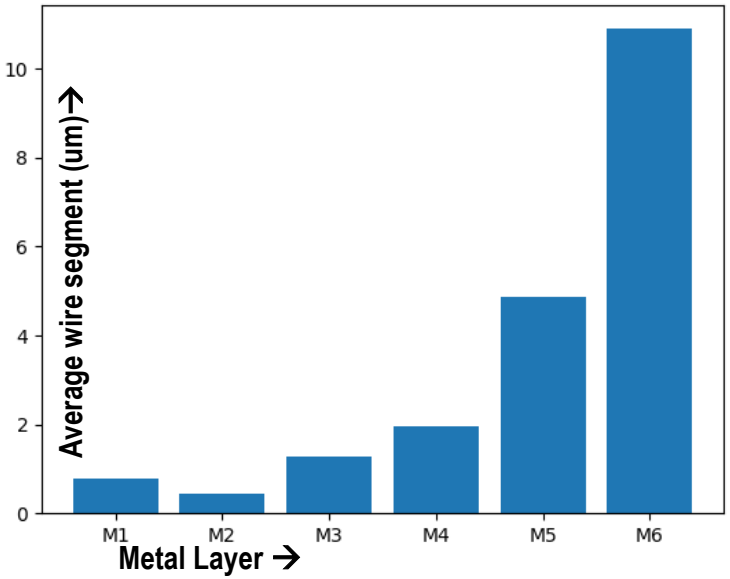
Logic on Logic Partitioning

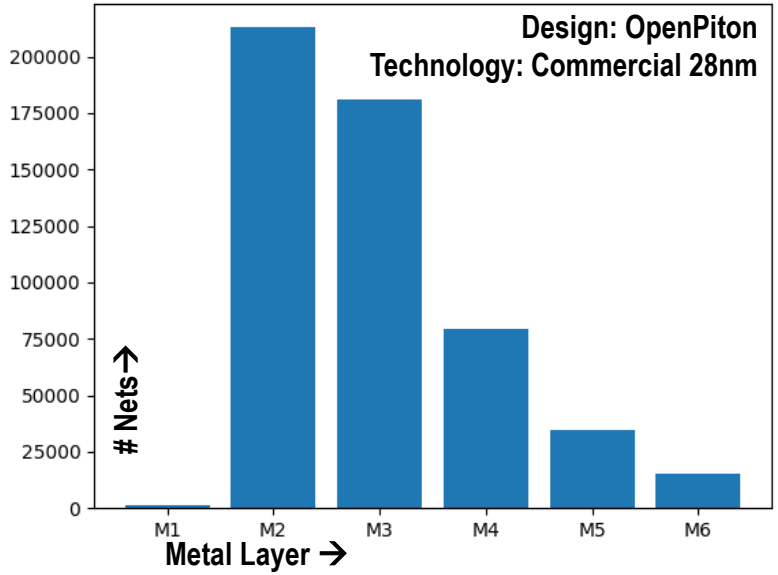


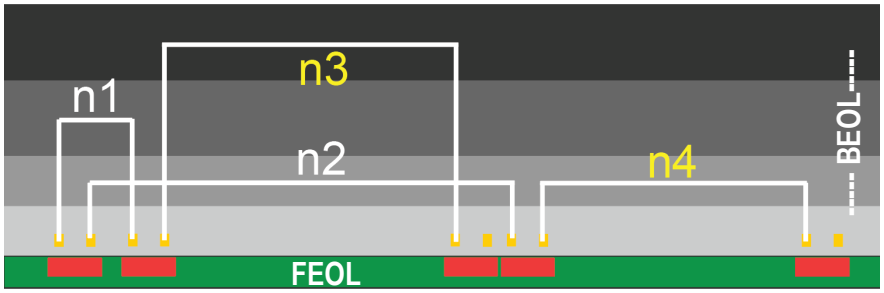


Routing Analysis

Traditional 2D IC: Layer Distribution







As we go up in the metal stack (M1 – M6):

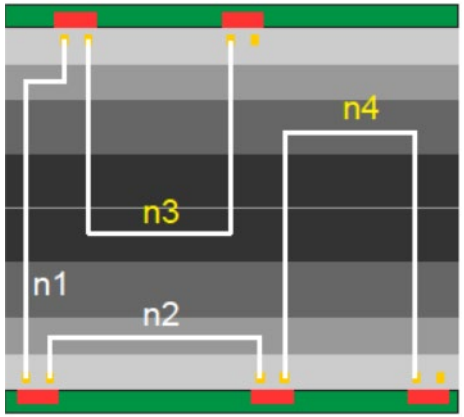
- #Nets routed *decrease*
- The average length of the wires *increase*

Number of long nets decrease

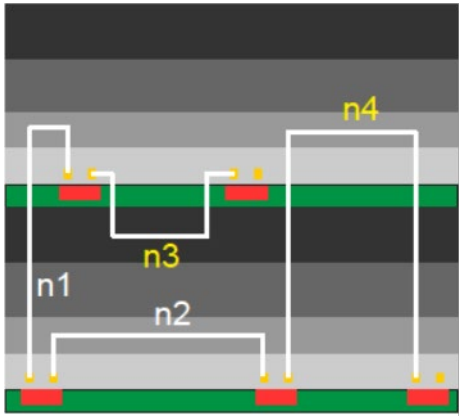
Pitch increases monotonically => # Routing tracks reduce

Routing Scenarios

3D ICs: Different Types of Nets



Face-To-Face Bonding Style
Stack: FEOL – M1 – Mx – Mx – M1– FEOL

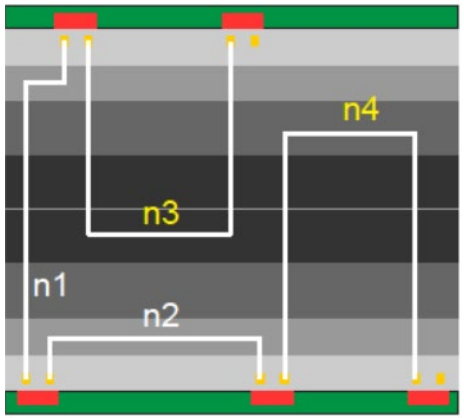


Face-To-Back Bonding Style
Stack: FEOL – M1 – Mx – FEOL – M1 – Mx

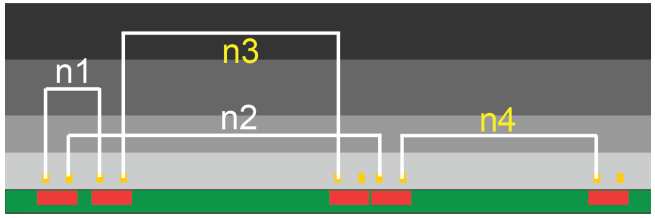
- ***n1***: 3D net
- ***n2***: 2D net routed in a traditional fashion
- ***n3, n4***: 2D nets routed with metal layer sharing
  - ***n3***: Connects cells in the top FEOL
  - ***n4***: Connects cells in the bottom FEOL

Qualitative Routing Analysis

Face-To-Face 3D ICs



Face-To-Face Bonding Style
Stack: FEOL – M1 – Mx – Mx – M1– FEOL

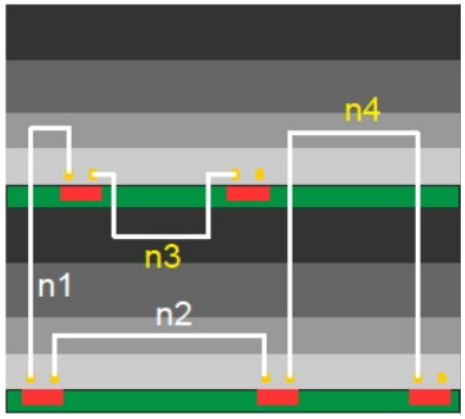


Example 2D reference
Stack: FEOL – M1 – Mx (larger footprint)

- *n1*: Routed over 2 BEOLs
  - "3D Overhead"
- *n2:* Similar to 2D routing
  - has fewer obstructions
- *n3, n4*: Borrowed tracks located beyond their respective BEOLs
  - Frees up tracks in the lower metals

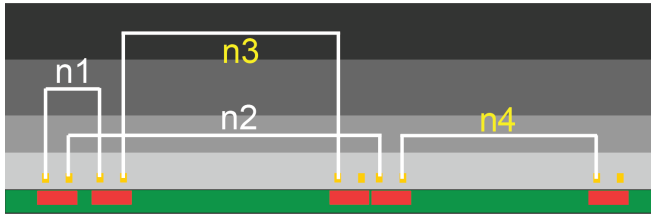
Qualitative Routing Analysis

Face-To-Back 3D ICs



Face-To-Back Bonding Style

Stack: FEOL – M1 – Mx – FEOL – M1 – Mx



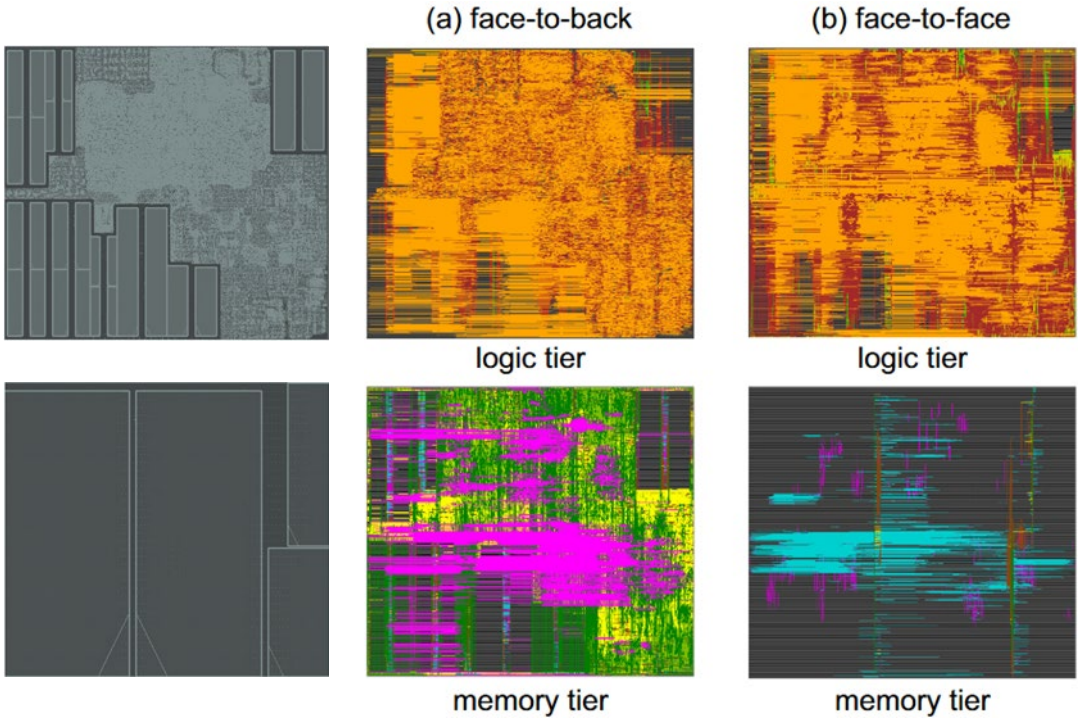
Example 2D reference

Stack: FEOL – M1 – Mx (larger footprint)

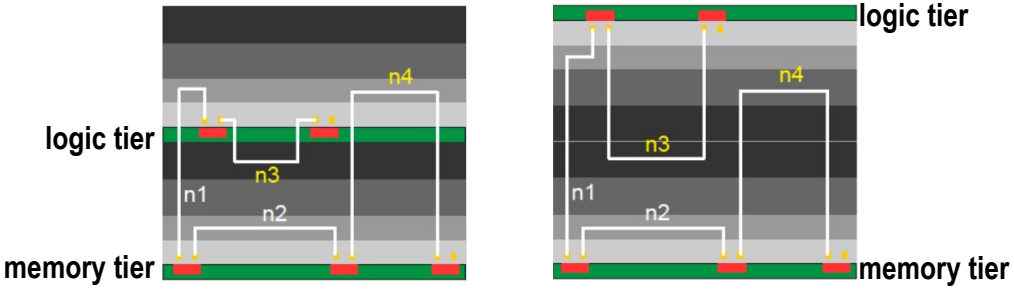
- *n1*: Routed over 1 BEOL
  - A new kind of "3D Overhead" occurs as MIVs drill through the top FEOL
- *n2:* Similar to 2D routing
  - has fewer obstructions
- *n3*: Borrowed tracks close to the FEOL
  - Simplified Routing, frees up top BEOL
- *n4*: Borrowed tracks located beyond its own BEOL
  - frees up bottom BEOL. No inherent advantage

Quantitative Routing Analysis

In Different Bonding Orientations



	F2B	F2F
Frequency (MHz)	1000	1000
# MIVs	120351	3112
On 2D nets	119317	2293
On 3D nets	1034	819
Wirelength (m)	6.36	5.81
Worst Slack (ns)	-0.38	-0.44

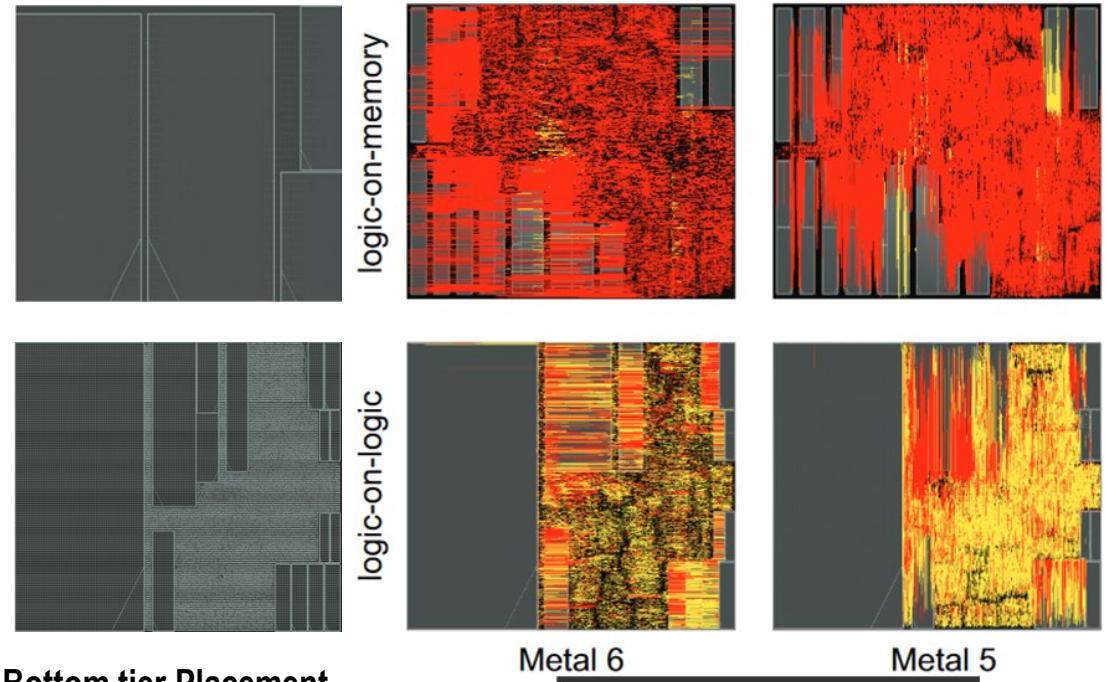


Design: OpenPiton
Technology: Commercial 28nm

Quantitative Routing Analysis

In Different Partitioning Types

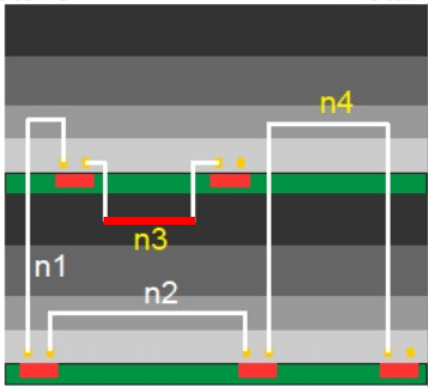
Fig: Routing in M5, M6 of the bottom tier. Red: Borrowed tracks from top BEOL



Bottom tier Placement

	L+M	L+L
Frequency (MHz)	1000	1000
#MIVs	120351	104606
On 2D Nets	119317	17575
Borrow from bottom	119317	17421
Borrow from top	0	154
WL (m)	6.36	4.66
% WL on shared tracks	25.1	6.4
Worst Slack (ns)	-0.38	-0.40

Example Cross-section



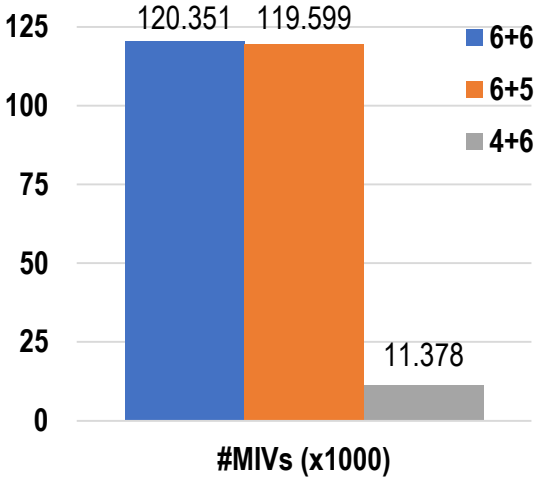
Design: OpenPiton
Technology: Commercial 28nm

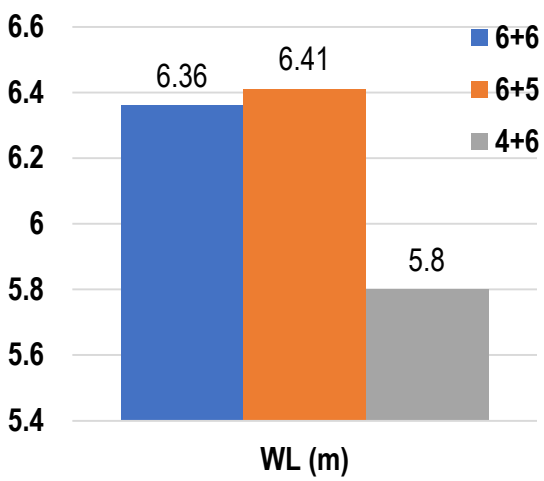
Benefits of Metal Layer Sharing

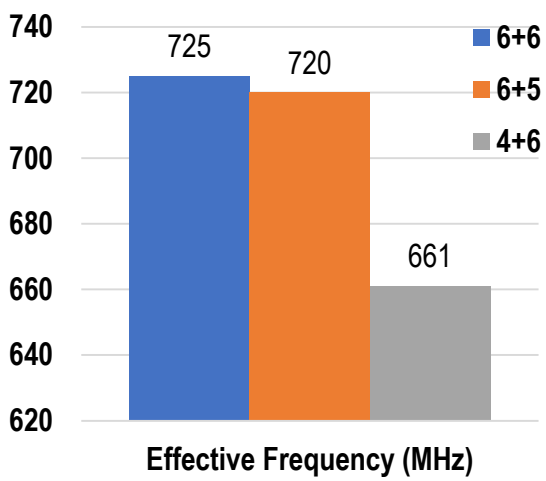
Metal Cost Saving

Three BEOL options:
Default: 6 metals in memory tier + 6 metals in logic tier
Case1: 6 metals in memory tier + 5 metals in logic tier
Case2: 4 metals in memory tier + 6 metals in logic tier

Design: OpenPiton
Technology: Commercial 28nm





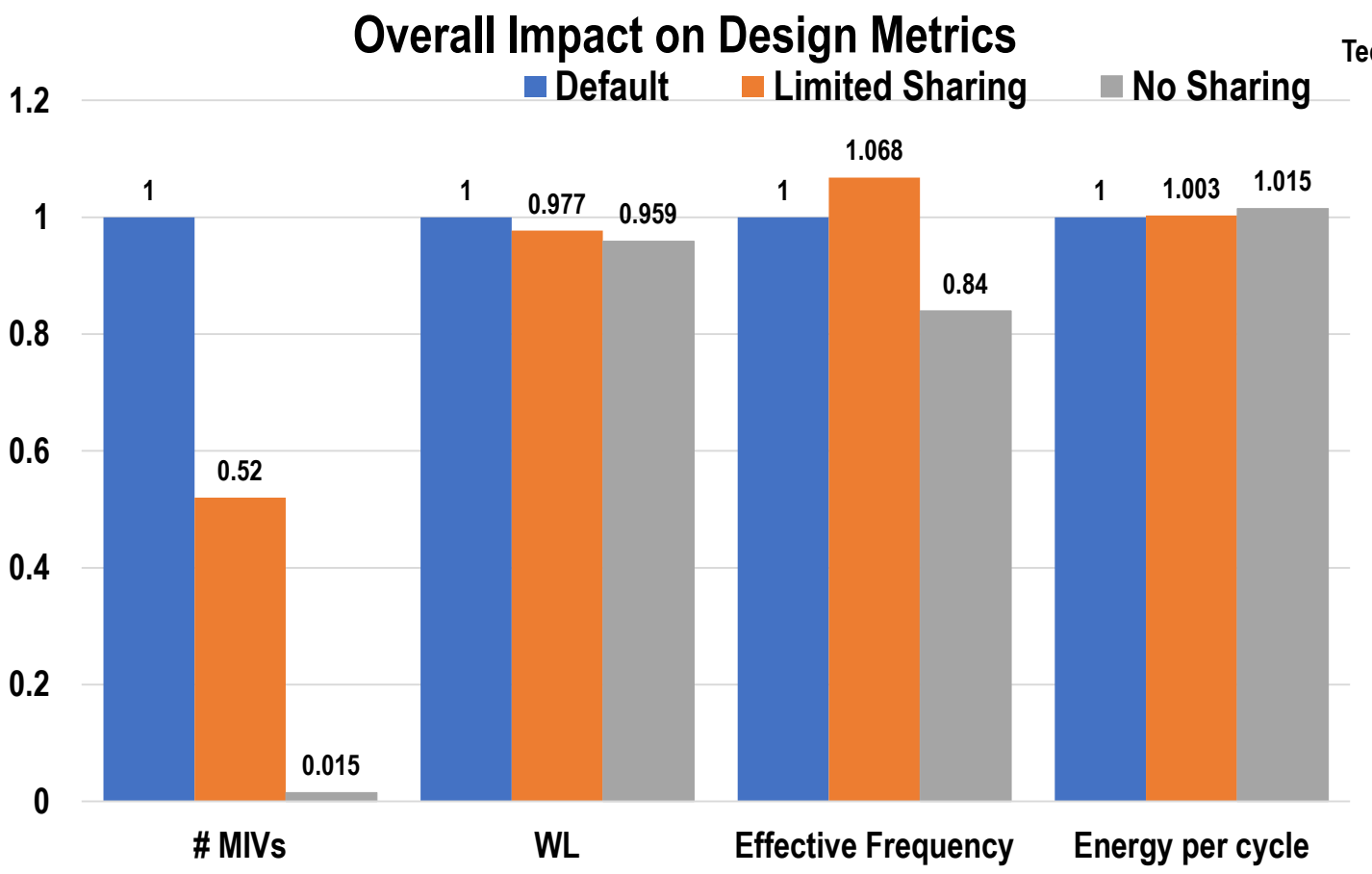


#MIVs reduces with 4+6 option due to the lack of available tracks in the bottom (memory) tier

Frequency goes down by ~9% in the 4+6 option.
With 6+5, we do not see a decrease in the effective frequency

Metal Layer Sharing

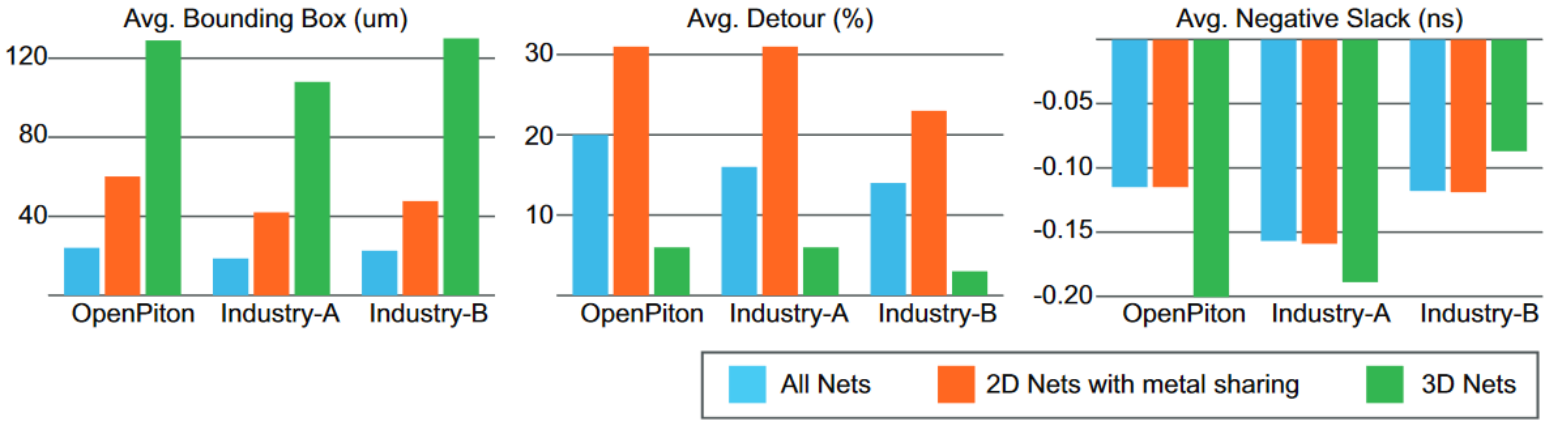
Overall PPA Improvement

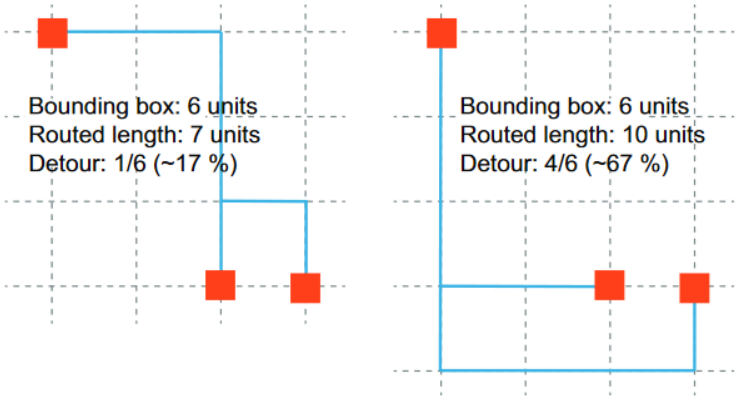


Design: Industry-A
Technology: Commercial 28nm

Without metal sharing: effective frequency drops 16%
Limited sharing (only wires > 50um): frequency increases 7%

Analysis of Different Net Types

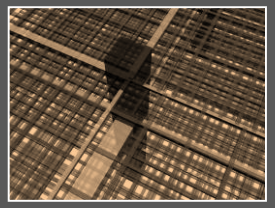
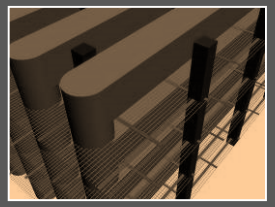
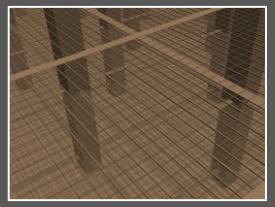
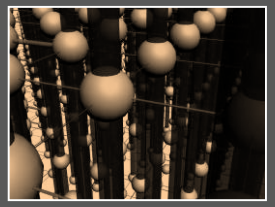




Summary

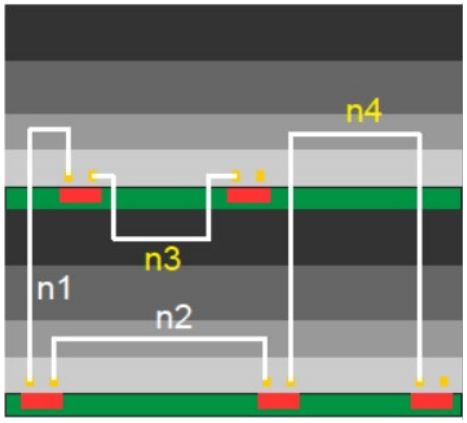
- No variety in routing flows for different 3D IC configurations
- Different 3D ICs affect routing in different ways
- Face-To-Back 3D ICs with memory-on-logic partitioning show highest amount of metal sharing
- Sharing allows for effective BEOL usage and show metal layer cost savings (upto 1-2 fewer layers)
- No sharing negatively impact PPA, but controlled sharing can be better than the auto routing
- Shared nets usually have higher detour due to the BEOL and FEOL configurations

Thank You

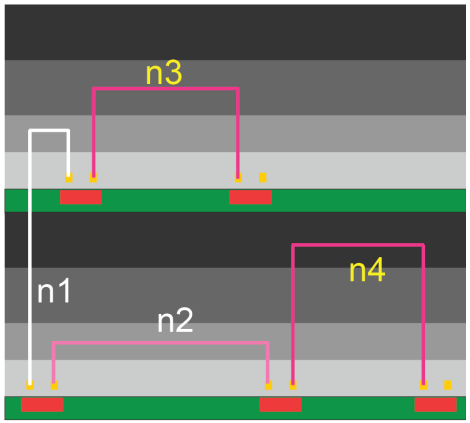





Controlling Metal Layer Sharing

- **To study the impact of the Routing Sharing**
  - **We restrict routing of the nets to their own BEOL**
  - **Router constraints of min, max layer for all 2D nets**



F2B with no restrictions



F2B with restrictions on all 2D nets (n2, n3, n4)

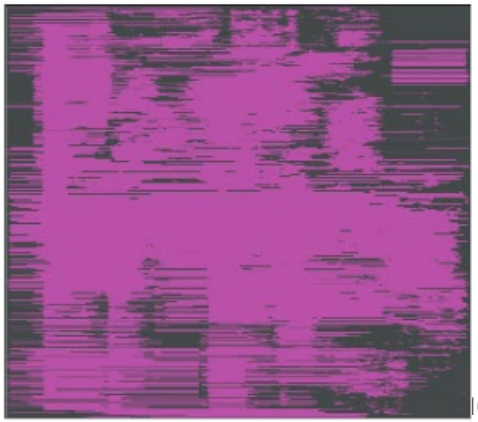
- **Limited Sharing:**
  - **Only constrain nets with wire length > threshold to use metal layer sharing**

Metal Layer Sharing

Effect on Routing

Logic M6 with sharing

Logic M6 without sharing



Wirelengths in logic tier are well distributed

Legend:

With Metal Layer Sharing; and no logic tier M6

Without Metal Layer Sharing (6 metals per tier)