Challenges and Solutions for 3D Fabric™:
A Foundry Perspective

Sandeep K Goel, TSMC

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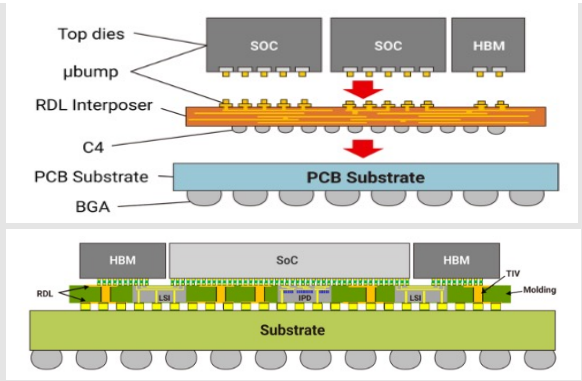
Outline

- **Advanced Packaging Paradigm**
- **Challenges and Solutions**
  - Thermal
  - Interface Design
  - APR
  - DFT and Testing
- **Conclusion**

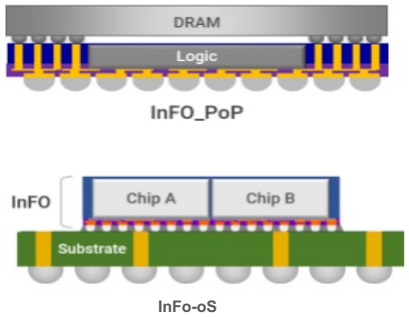
Advanced Packaging Paradigm: 3D Fabric™

- **Continues to advance much like process technology**



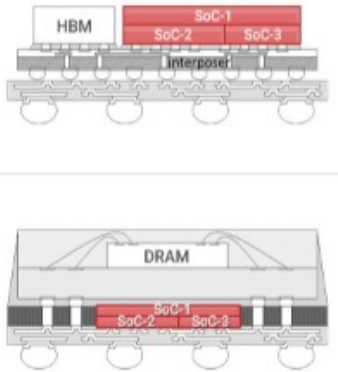
CoWoS

Best in breed performance for high performance computing applications



InFO

Best cost/performance for high density, high performance mobile, network applications



TSMC-SoIC

Chiplets stacking with exceptional performance, form factor, and power saving

Production Milestone

More than 60 product tape-outs are in production or in development as of Aug. 2019

Production Milestone

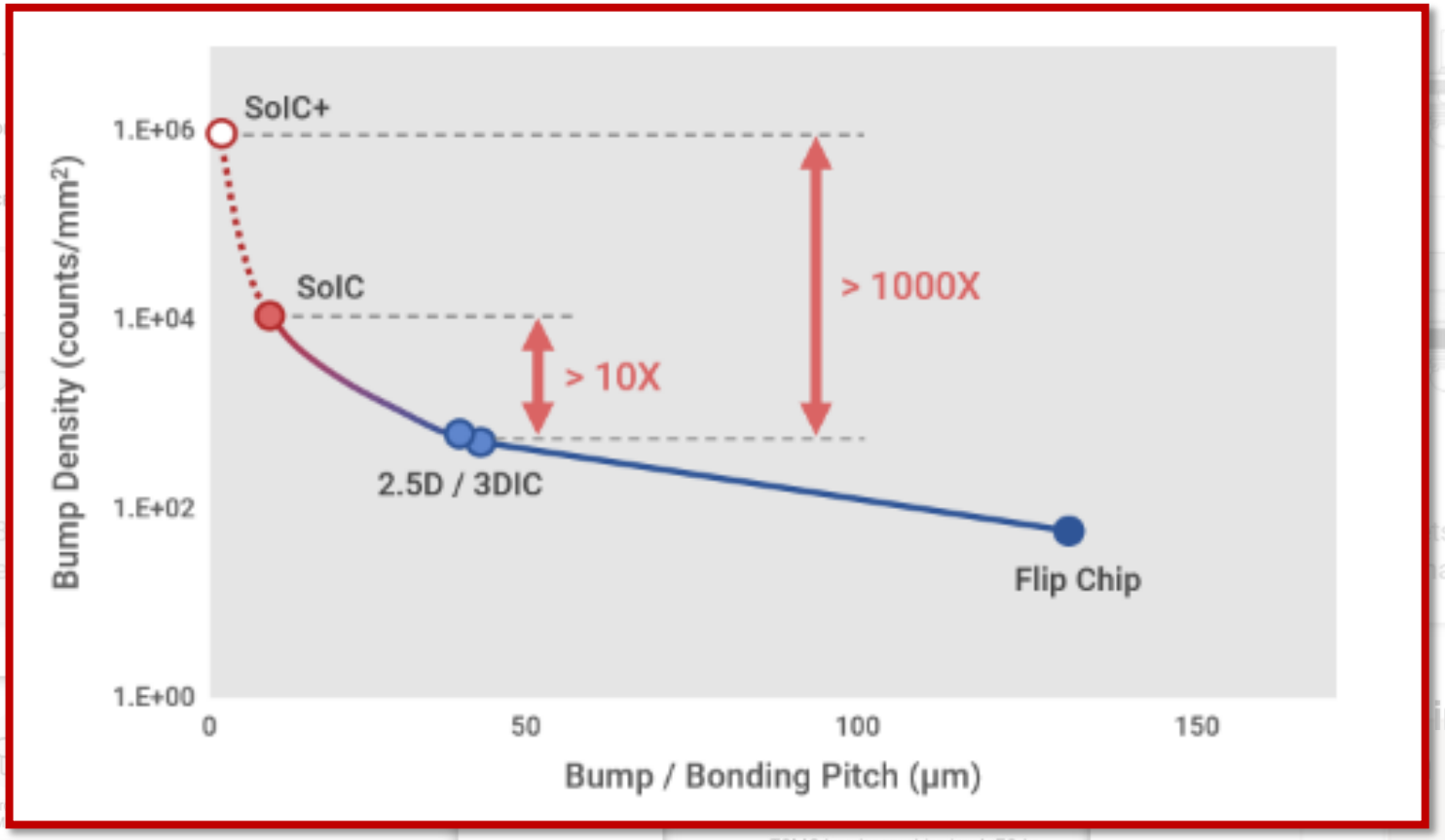
More than 20 product tape-outs are in production or in development as of Aug. 2019

TSMC has been shipping InFO in high volume since 2016

Chiplet integration combined with CoWoS/InFO-Pop

D2D Connections and Bump Density

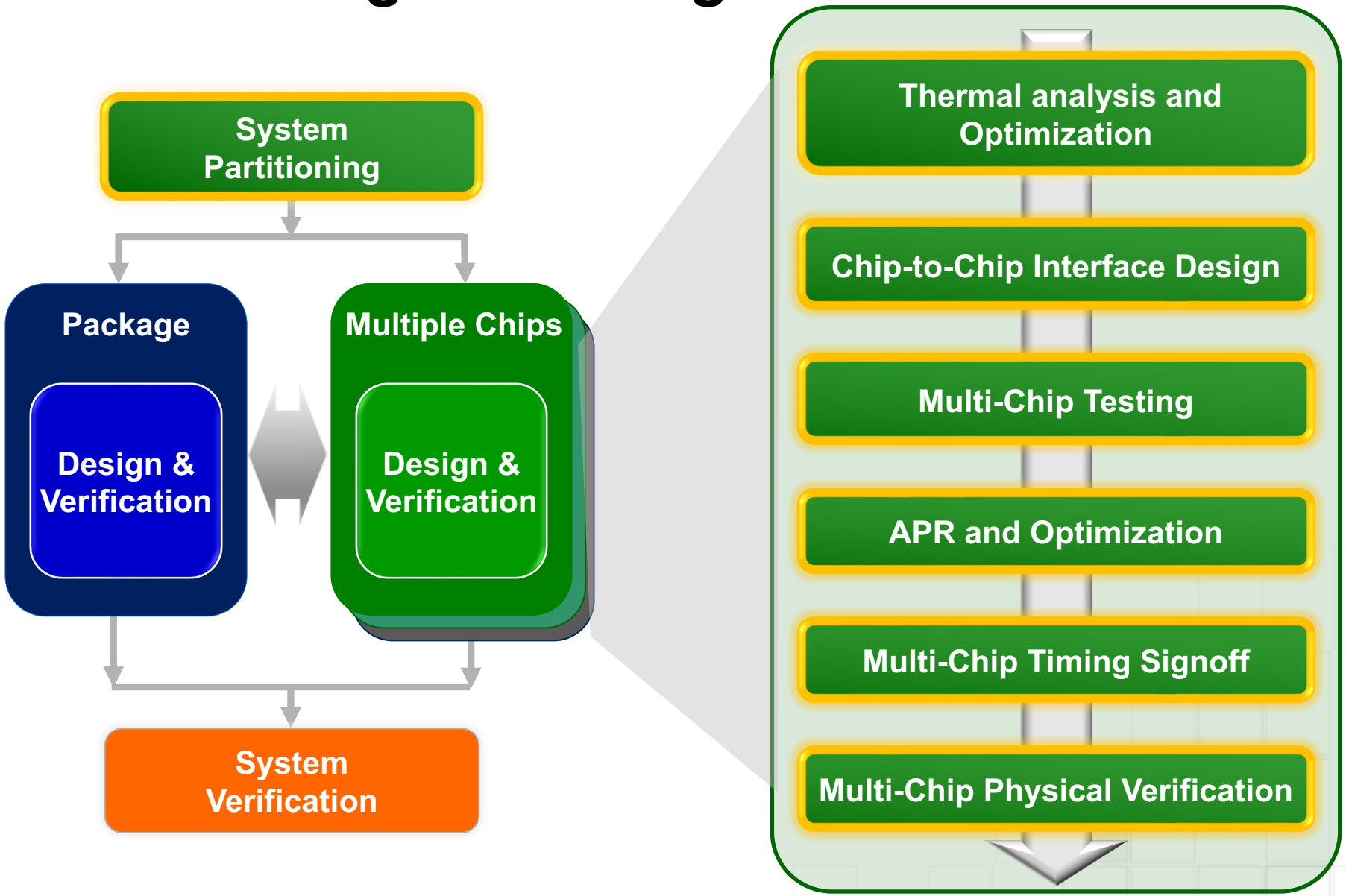
- Number of D2D connections can range in millions (not hundreds)



Selection of packaging technology depends on application's PPA-C

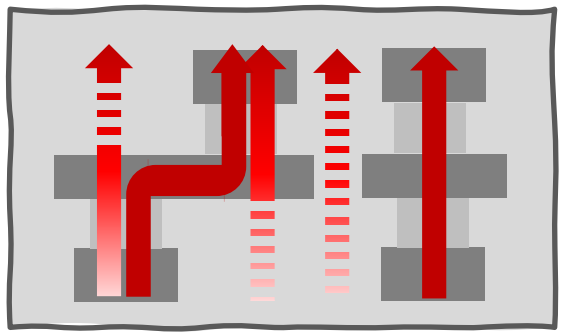
Different set of challenges for each technology

3DFabric™ Design Challenges

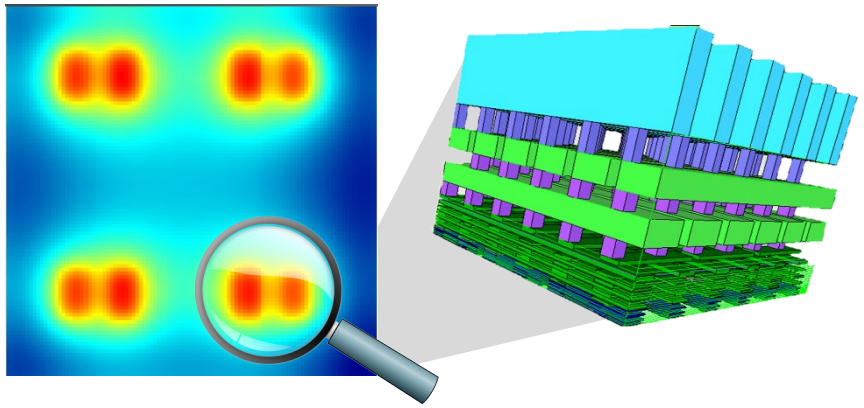


Thermal Analysis Challenge

- **BEOL metal has higher conductivity than dielectric**
  - PDN network behaves like Chimney where heat flux follows connected metal shapes
- **Conventional thermal analysis divides BEOL into coarse grids due to # of shapes**
  - Improves run time at expense of accuracy ➔ ~10% optimism at hot spots
- **Divide-n-Conquer for detailed BEOL modeling through EDA partner collaboration**
  - Coarse-grained hotspot identification followed by fine-grained detailed hotspot analysis

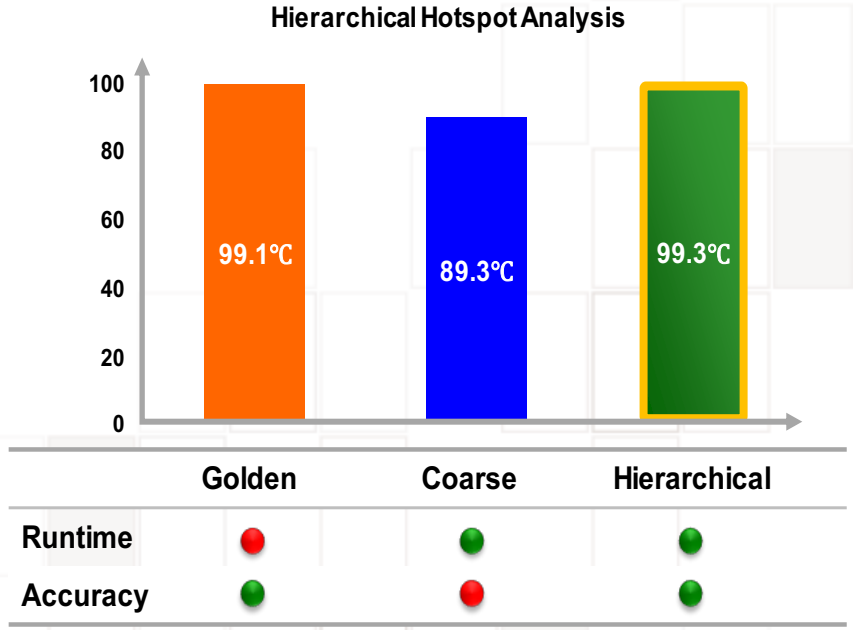


Thermal conduction paths
(metal (398) vs. dielectric (0.25)
=~ 1600X difference!)



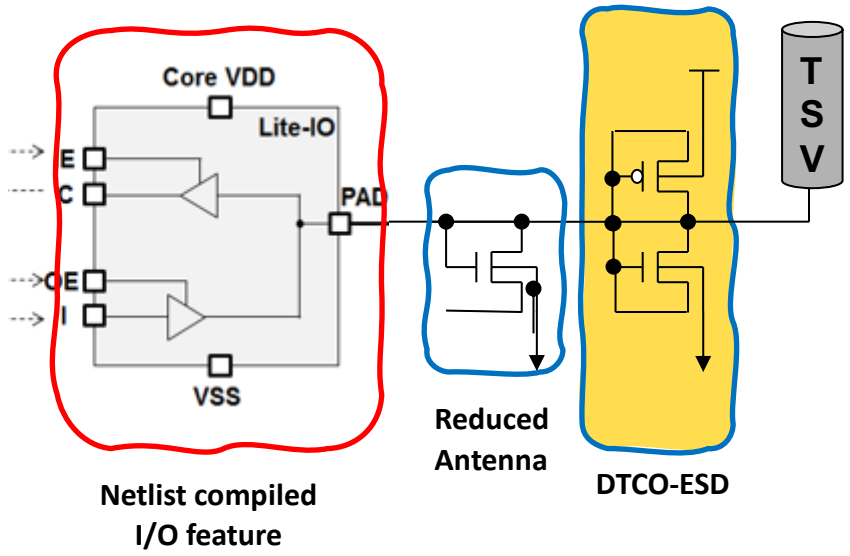
Coarse-grained (Hotspot Identification)

Fine-grained (Detained Analysis)

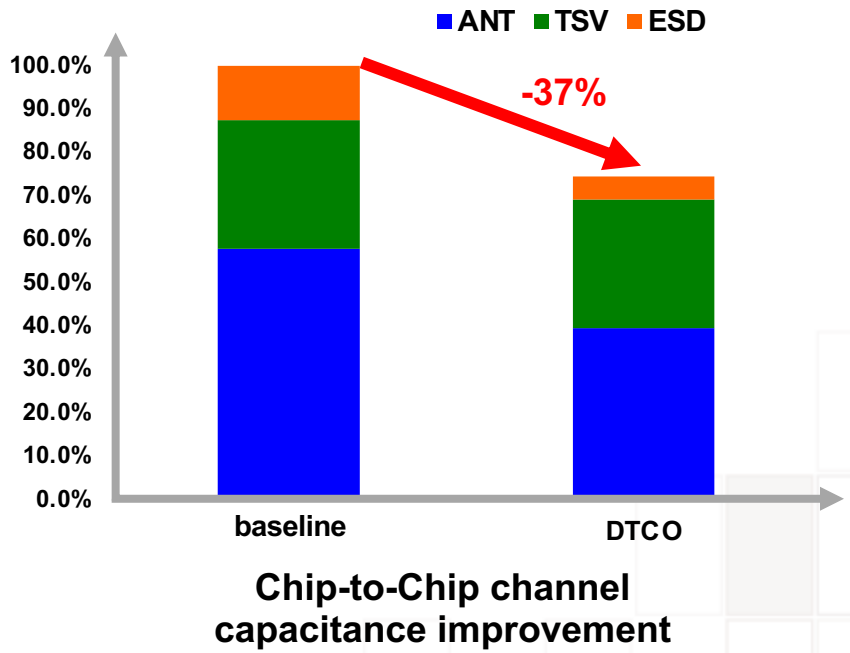


Innovative Chip-to-Chip Interface Design

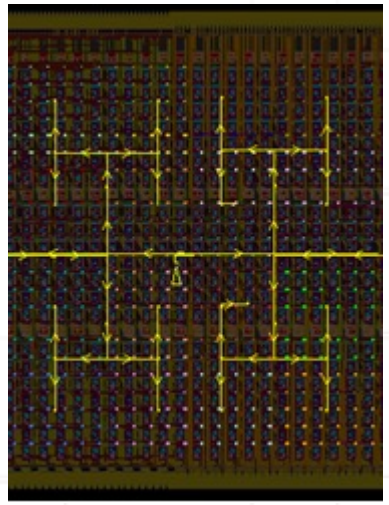
- **Design and Technology Co-Optimization is must for D2D interface**
  - Holistic approach to combine layout and design rule optimization leads to 37% reduction in channel capacitance
  - Customized clock tree for variation-aware design; reduces 6-sigma clock skew by >100ps
  - Improve Lite-IO bitrate from 2Gbps to 4Gbps



Lite-IO/ESD/ANT DTCO



Chip-to-Chip channel capacitance improvement

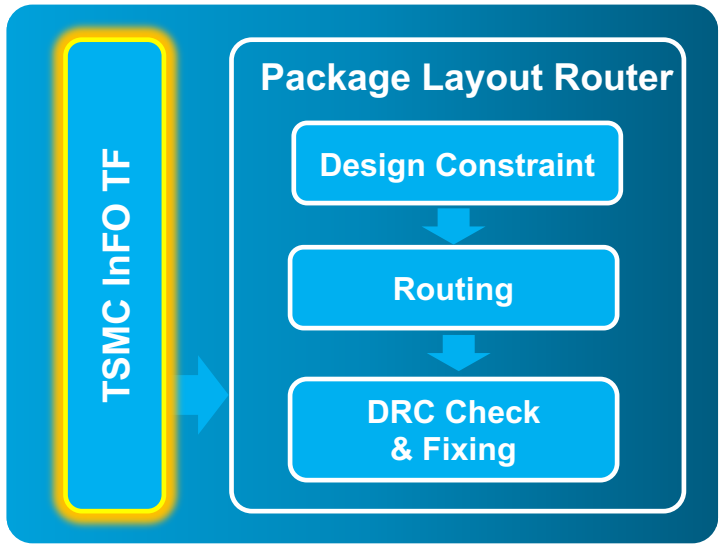


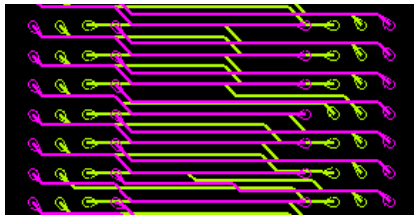
Chip-to-Chip variation-aware design

Bringing APR into Package Routing

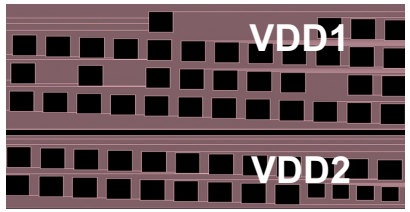
- **Connections to substrate requires careful design of metal connections and becomes challenging with increase in number of signals**
  - To bring layout automation similar to APR, TSMC has developed InFO Tech File
  - Package layout tool can do routing and produce DRC-clean design like real routing engine

Example: InFO 3D Fabric™

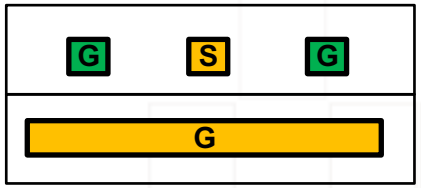




Ultra dense auto routing
- Uniform bus routing patterns
- Chip-to-Chip/to-Substrate

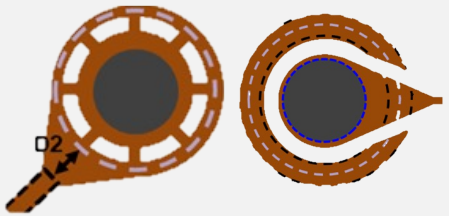


Auo PG plane creation
- Multiple power domains
- Degassing hole auto insertion



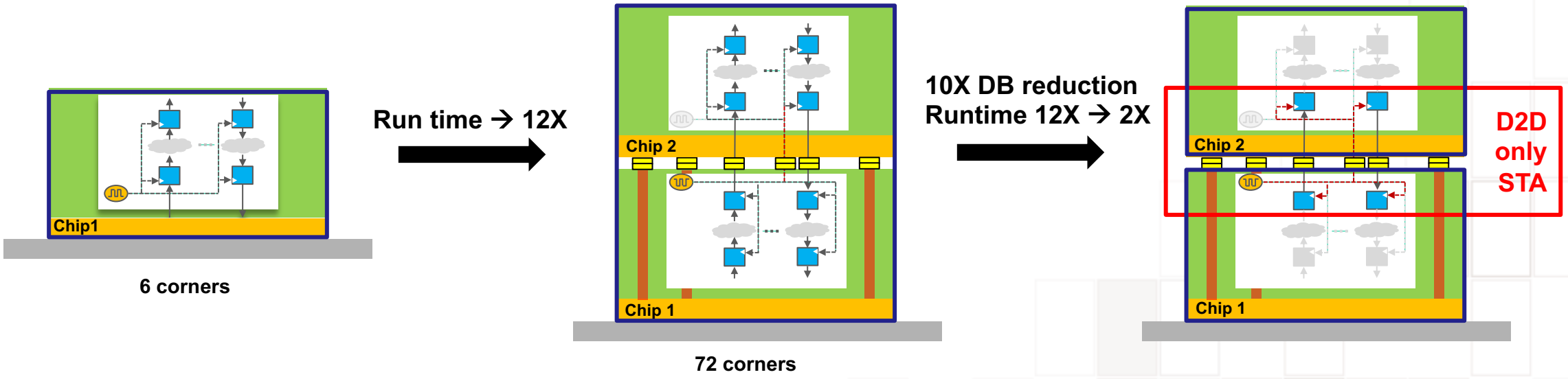
SI-driven routing constraint
- Guard trace pattern definition

Special pattern creation
- Mesh hole pad
- C-ring pad
- Teardrop



Multi-Chip Timing Sign-off

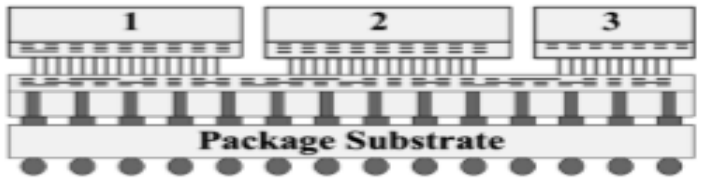
- **Corner combination grows as products of corners from each chips**
  - Chip 1: 6 corners, Chip 2: 6 corners
  - Combinations: 6 x 6 x 2 {TSV_worst, TSV_best} = 72 corner combinations (12X !)
- **Enabled efficient hierarchical STA focuses on interface checks**
  - Interface model reduced the design size by 10X
  - Overall runtime reduced from 12X down to 2X



DFT: Physical vs Electrical View

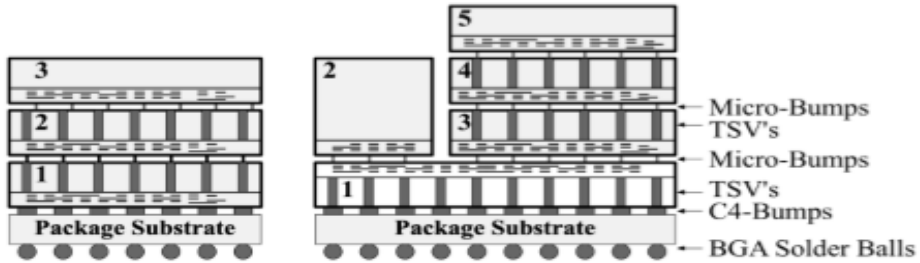
- **DFT considers electrical view while test application is dependent on physical view**
  - Independent of packaging technology, electrical view can be defined in two ways

Type 1



Each Die has access to package pins

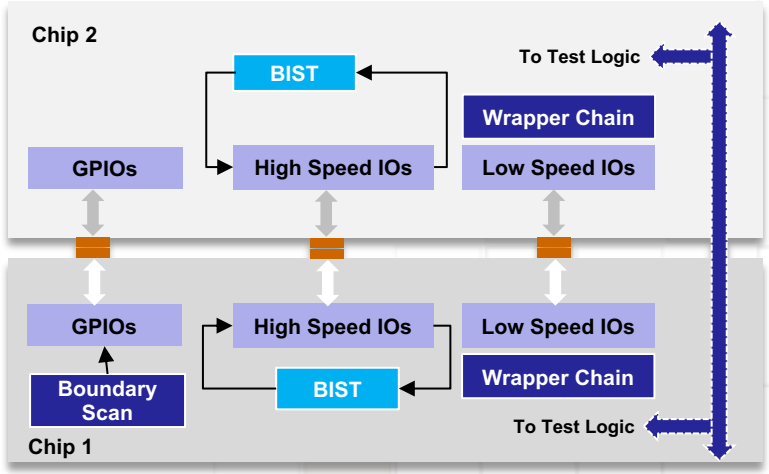
Type 2



Only Bottom (or Top) die has access to package pins

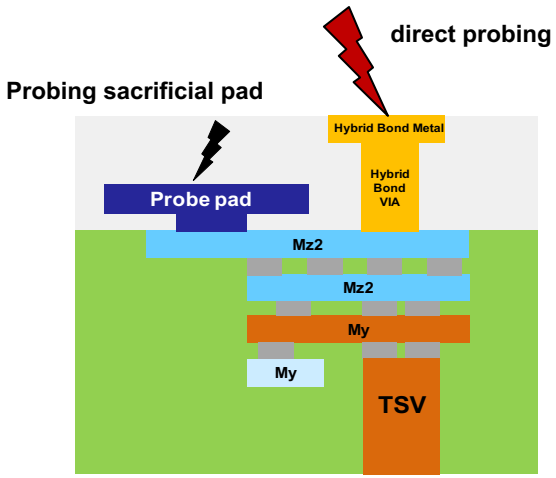
DFT Solutions

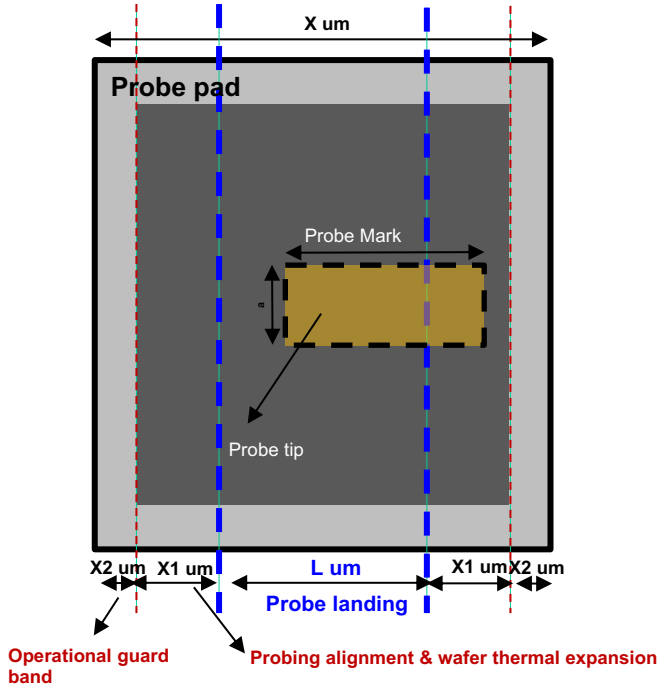
- **Access and Interface**: IEEE 1838 Std. Compliant access for pre/post-stack testing and minimize # of test pins
- **Chip-2-Chip interconnect**: BIST for high-speed IOs and 1838 Wrapper for low speed IOs supporting AC/DC test

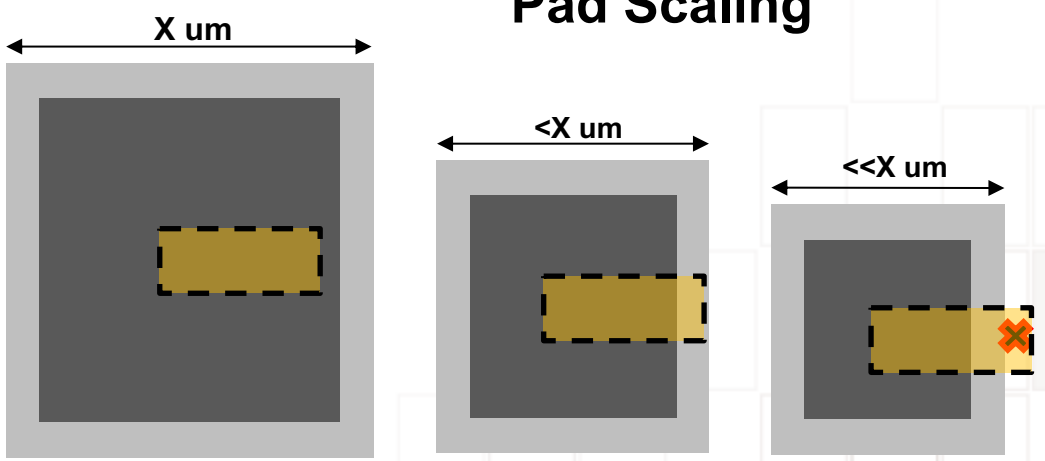


Probe Pads and Physical Consideration

- **Testing is done via probing of probe pads or ubumps/hybrid bonds**
- **Sacrificial pads are usually large in size and only limited number of signals can be probed**
  - Impacts bump assignment, routing and PG connections
  - Scaling of probe pad is not trivial and limited by various testing issues







Three Phenomena affecting probing results

a. Probe Mark size
b. Probing accuracy
c. Wafer thermal radial expansion

Conclusion

- 3D advanced packaging continues to scale and provides more effective and efficient solutions for different applications
- Innovative hierarchical solutions are required to deal with the complexity of the problem without sacrificing accuracy
- Close collaboration between foundry and EDA partners has enabled many of the solutions for industry-wide usage
- We need to continue to drive industry wide standardization to make sure solutions are plug-n-play