Novel methodology for assessing chip-package interaction effects on chip performance

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Outline

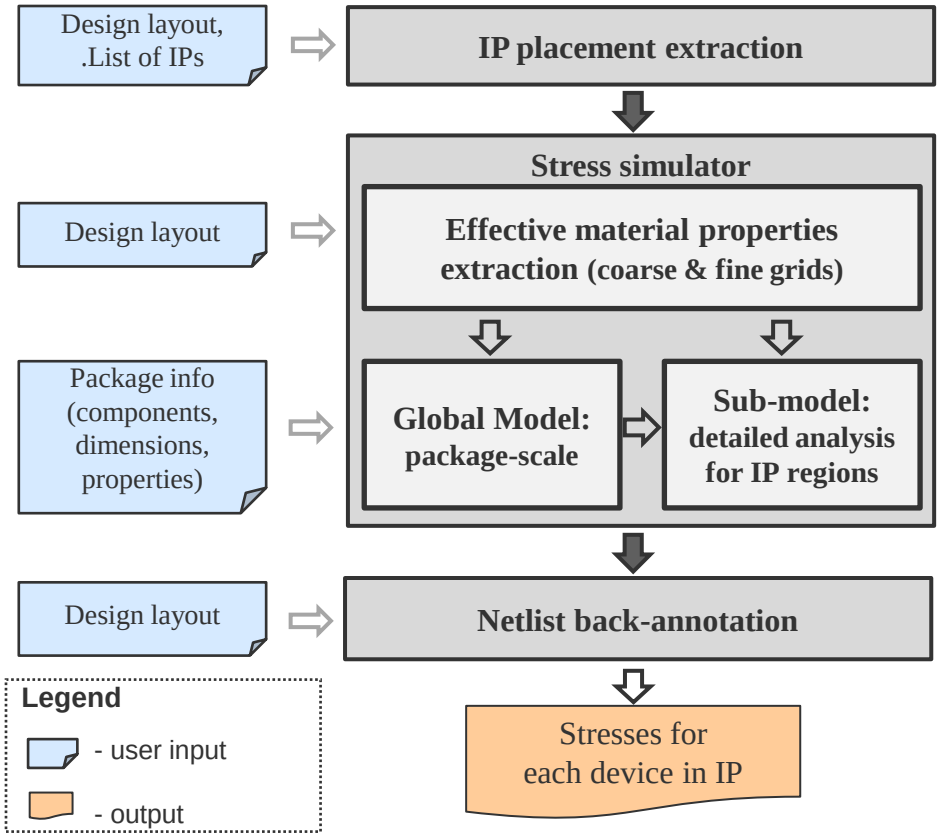
- A novel multi-scale simulation methodology (EDA tool) that assesses the effect of assembly-induced thermal mechanical stresses on chip performance.
- Employed methodology of anisotropic effective thermomechanical material properties (EMP) is bin-based, and scalable with simulation grid size. With feature-scale resolution, the tool accurately calculates stress components in the active region of a device.
- The tool back-annotates the hierarchic SPICE netlist with the stress values, and enables a user to perform number of simulations on IP block that is placed multiple times in different stress environment.
- Both schematic and post-layout netlists can be employed for finding optimal floorplan that minimizes the stress impact at early design stages, as well as for the final design sign-off.
- Electrical measurements on a test-package: good agreement between measured and simulated variations of device characteristics has been demonstrated.

Introduction

- Chip-package interaction (CPI) generates mechanical stress in silicon die, and contributes to parametric failure of circuits through carrier mobility degradation.
- Even in the most advanced traditional finite element (FE) modeling, a die is treated as a pair of homogeneous isotropic material blocks: silicon and BEoL interconnect, which cannot describe CPI stress distribution coming from non-uniformity of metal layer geometries.
- We present an advanced methodology of assessment of CPI stress impact on circuits performance for,
  (1) avoiding placement of the stress-sensitive circuits in the highly stressed locations, and,
  (2) performing accurate circuit simulations that account for the stress-induced variations in device characteristics.

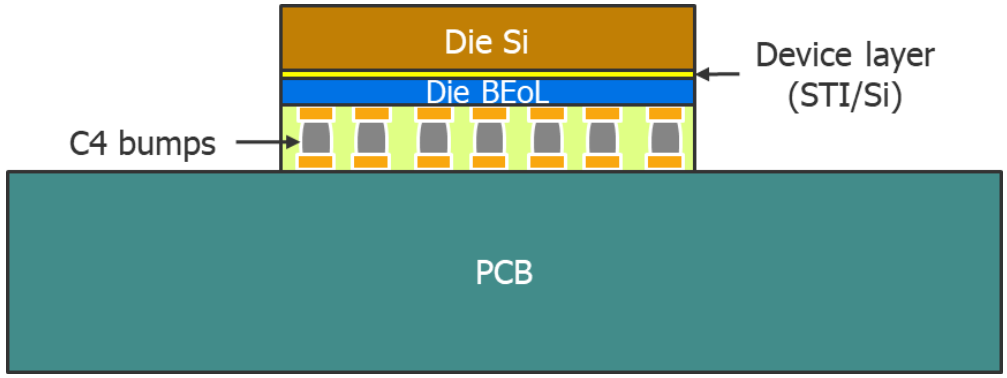
Simulation and Tool operational flow

- Automated sign-off flow for analyzing the performance of various circuits under the influence of CPI-induced stress.
- Flow enables the performance analysis of circuits that are placed in different stress environment inside layout.



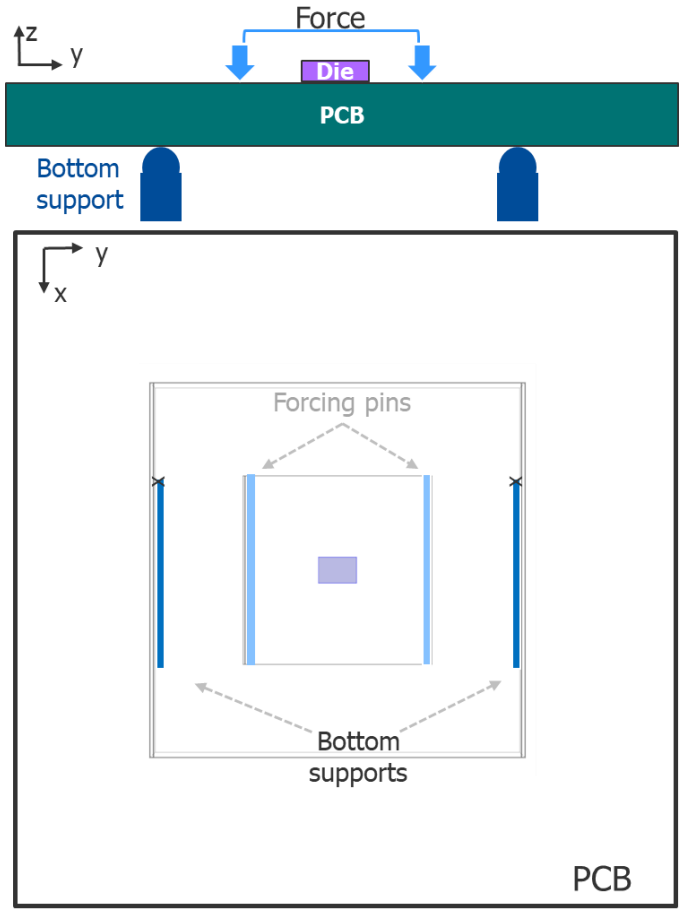
Package setup for simulation

- A sample package structure: face-down die, C4 bump/underfill, and a printed circuit board (PCB).
- A separate block for C4 bumps, die BEoL, STI (device) layers.
- For each of these blocks, coordinate-dependent EMP describes the properties.



Package bending setup for simulation

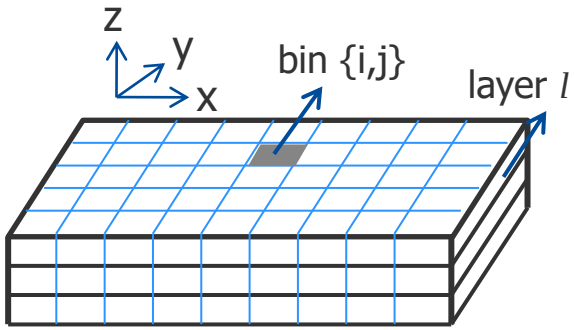
- Four-point bending test represents a standard approach for the device model calibration and validation by measurements of stress-induced variations in device characteristics.



Anisotropic Effective thermomechanical Material Properties (EMP)

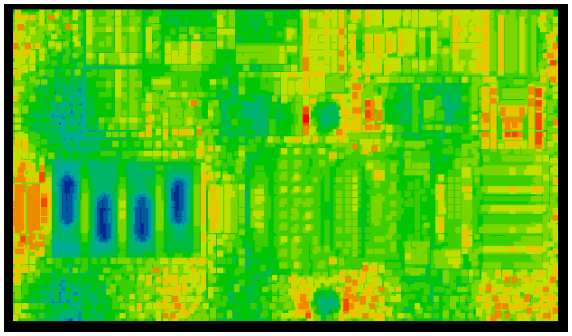
- Employs rules of mixtures from the theory of anisotropic composite materials.
- Bin-based approach: each bin consists of parallel metal "fibers" embedded in a dielectric "matrix".
- For each metal layer, metal density (ρ_M) is extracted by layout processing tool. Knowledge of preferential routing direction enables to calculate properties for each bin, in directions parallel ($\parallel$), and normal ($\perp$) to the routing direction of metal wires:

$$E_{\parallel} = E_M\rho_M + E_D(1-\rho_M),$$
$$E_{\perp} = E_M E_D/\big(E_D\rho_M + E_M(1-\rho_M)\big)$$
$$\alpha_{\parallel} = \frac{\alpha_M E_M\rho_M + \alpha_D E_D(1-\rho_M)}{E_M\rho_M + E_D(1-\rho_M)}$$
$$\alpha_{\perp} = \alpha_M\rho_M + \alpha_D(1-\rho_M)$$
$$\nu = \nu_M\rho_M + \nu_D(1-\rho_M)$$

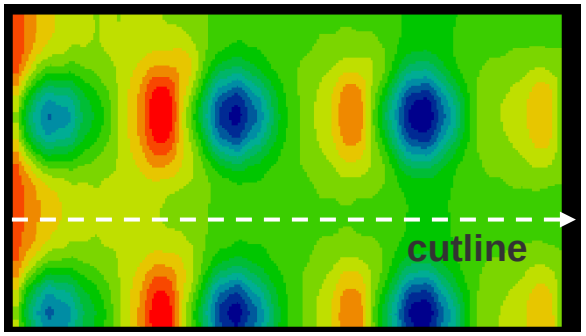


Anisotropic Effective thermomechanical Material Properties (EMP)

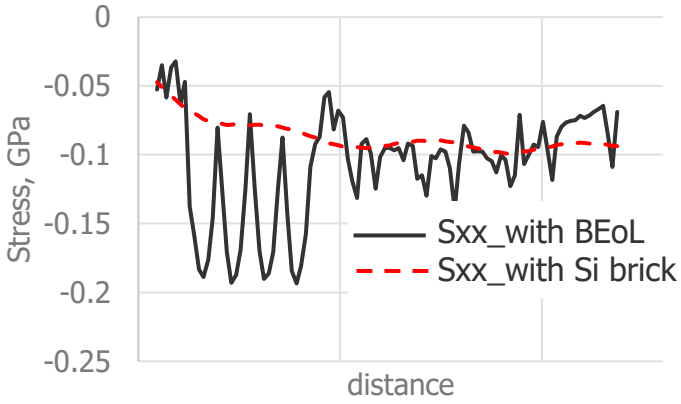
- Simulated stress(Sxx) distributions in an IP block. Die BEoL is represented by two different methods.
- Large stress variation caused by local layout geometries is missing when the entire die is represented by a silicon brick.



(a) interconnect layers are resolved by EMP



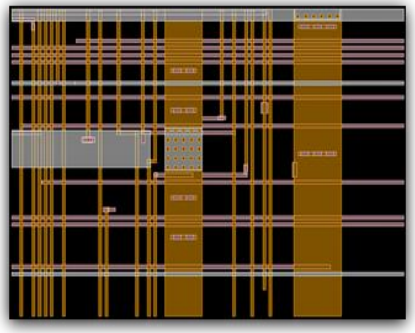
(b) Entire die as a silicon brick.



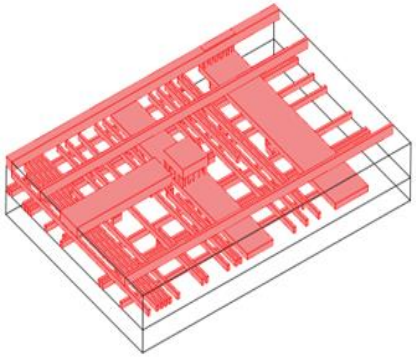
(c) Comparison of stress (Sxx) for the two cases along cutline.

Anisotropic Effective thermomechanical Material Properties (EMP)

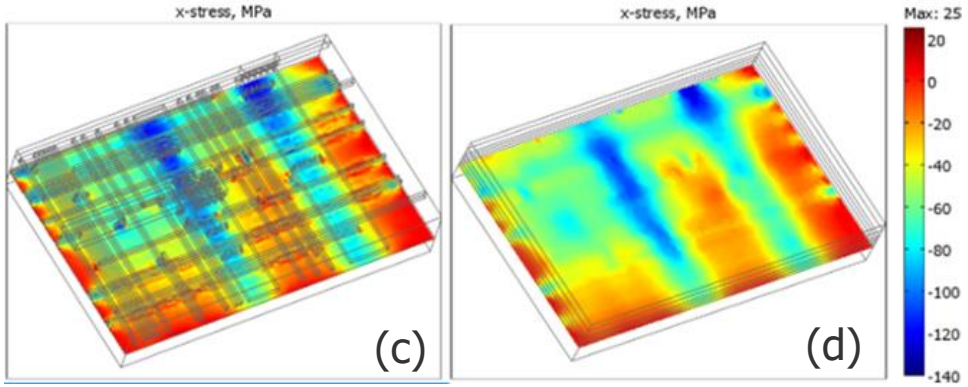
- Validating EMP methodology that replaces sharp boundary geometry/mesh model was done by FEM thermal stresses simulation.
- The same stress distributions are obtained for the two setups: employing (c) sharp boundaries, and (d) EMP, for representing interconnects.



(a) Layout showing metal layers.



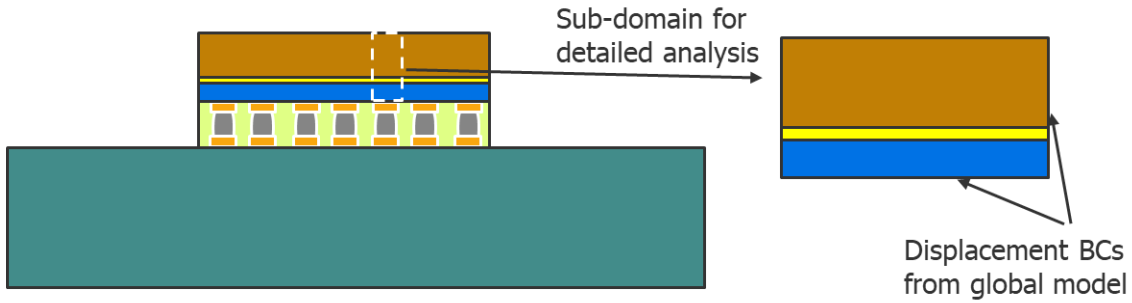
(b) 3D geometry of silicon/interconnect.



FEM simulations showing thermal stress on silicon / interconnect interface by employing
(c) sharp boundary model, and,
(d) EMP for interconnects.

Multi-Scale Simulation

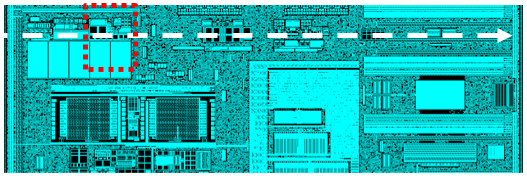
- Multi-scale in dimension: thickness varies from “mm” (PCB) to “sub-micron” (device layer).
- Very fine lateral mesh is required for device and BEoL, in order to obtain stress with accuracy required by feature-scale modeling.
- Highly non-uniform mesh should be avoided for simulation accuracy and performance.
- The desirable solution is multi-step simulation with displacement boundary conditions that transfers the obtained global-scale stress distribution on surfaces to successive sub-modeling.

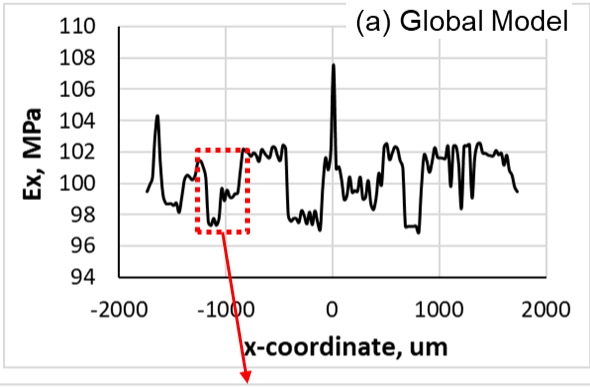


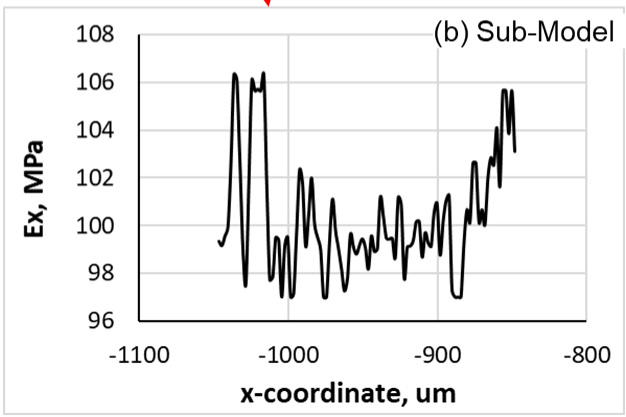
Two-step (global and sub-modeling) simulation schematic.

Multi-Scale Simulation

- At each step simulation, the granularities of EMP grid and FEA mesh should be determined by the smallest scale of stress sources that need to be resolved.
- Global-scale discretization size is normally smaller than C4 bump size.
- Very fine granularities can be used for sub-modeling that is performed on a very small region.
- Effective properties (Ex) extracted for two different modeling scales.

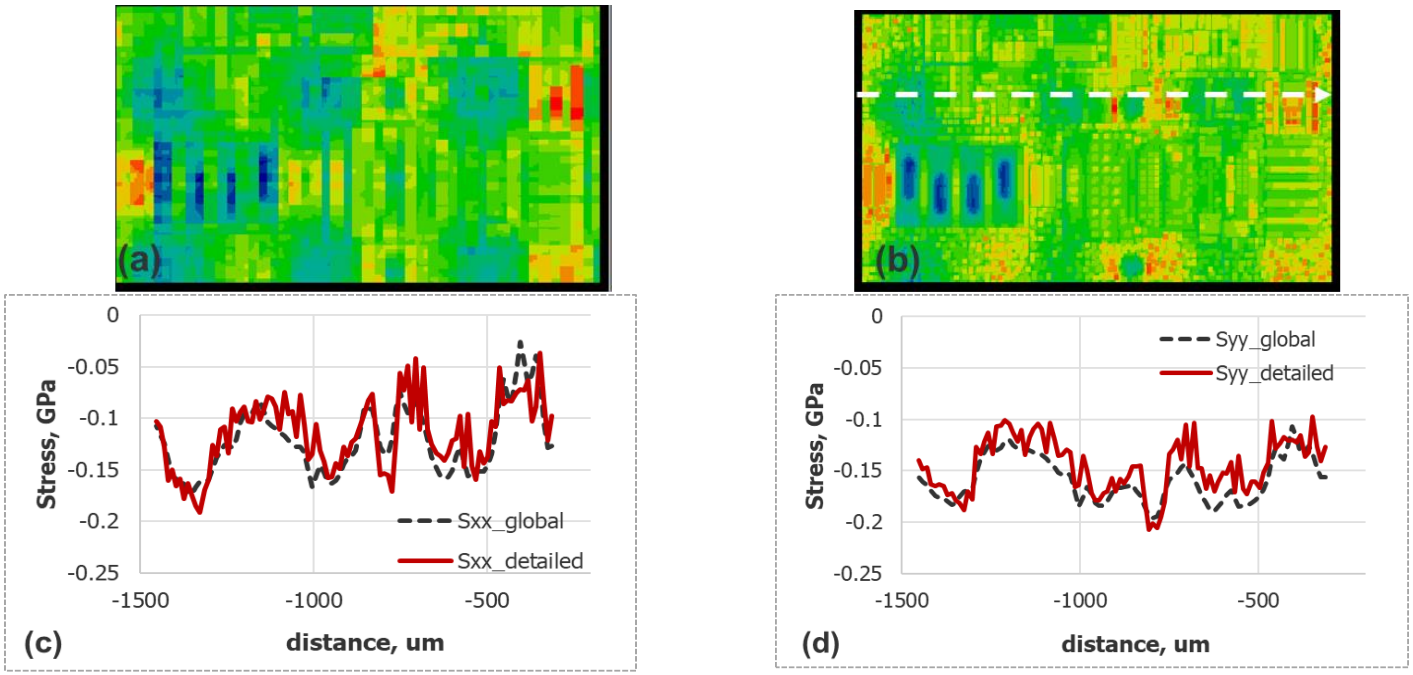






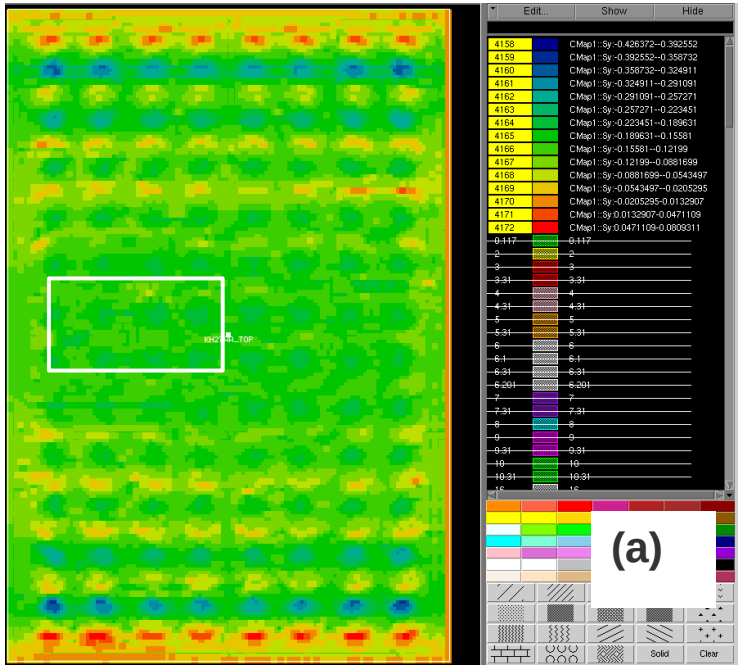
Multi-Scale Simulation

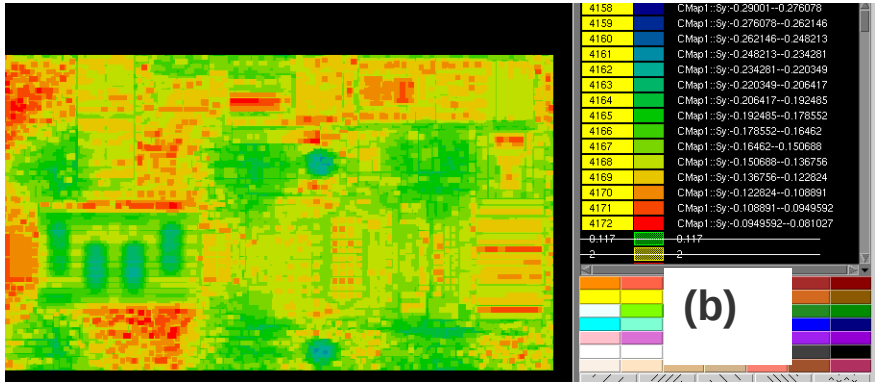
- Distribution of thermal stress component (Sxx) inside an IP block obtained from (a) global-scale, and (b) sub-modeling.
- 1D profiles of Sxx and Syy reveal the difference of the order of tens of *MPa* in stress components for the two scales.
- Performing only global-scale modeling can lead to inaccuracy in predicting device characteristics.



Multi-Scale Simulation

- Results of multi-scale stress (Syy) simulations for obtaining bending-induced stresses in (a) a die, and (b) IP block.





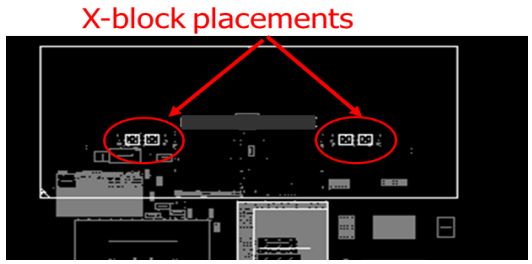
Hierarchic Spice netlist annotation with local stress

- An identical device can exhibit very different electrical performance when placed in different locations, each characterized by own stress environment.
- Tool's sub-modeling results accurately describe each stress environment, and enable a user to perform accurate circuit simulation, and obtain a correct performance.
- At each device location, the layout analysis tool finds absolute coordinate, and defines the stresses using the calculated CPI stress distributions.
- Eldo circuit simulator input is populated with externally defined stresses of any device, which will be used for circuit simulations.
- An example Eldo hierarchic netlist annotation for a device (*M*) in circuits (*X_i*):

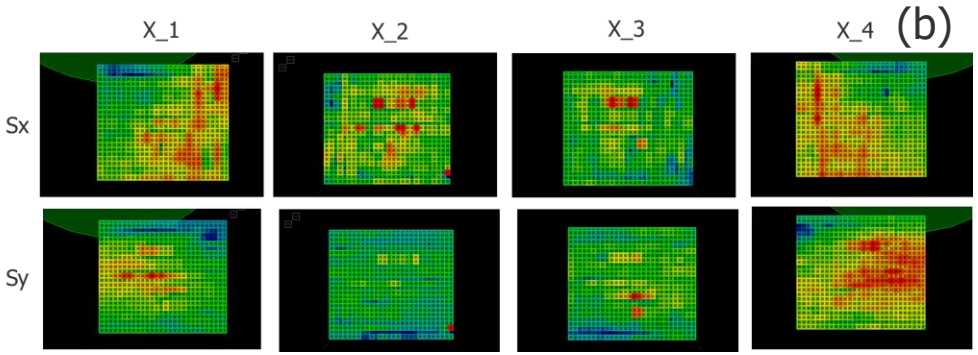
X_Top/X_1/X_2/M.sx=-85.7306
X_Top/X_1/X_2/M.sy=-69.0353
X_Top/X_1/X_2/M.sz=16.3638

What-if Analysis for Circuit Block Placement

- Performed during the design floor planning step, for optimization of the IP-block placement in terms of stress effects.
- Global-scale simulation results are used as an input.
- A user-supplied average metal density can be used for extracting BEoL EMP when routing is not available: stress variation due to C4 bumps, die edges.
- Designers define several different locations for the studied block, and obtain SPICE netlist annotated with stress components for each placement instance.
- Four instances of the same X-block in different layout environment exhibit different distributions of the X- and Y-stress components.



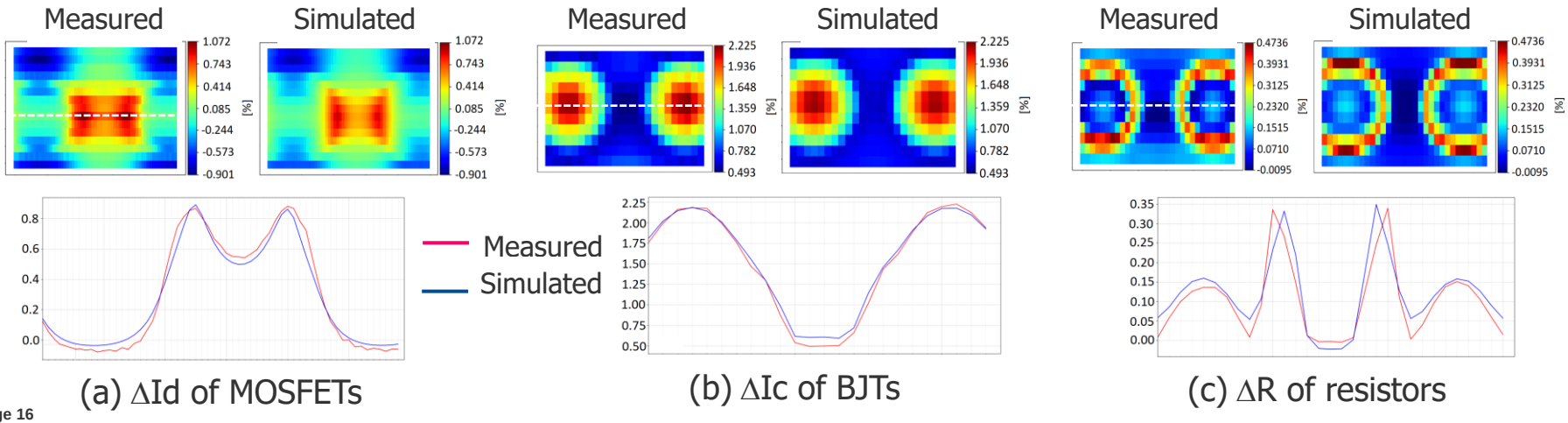
(a)



(b)

Experimental Validation

- WLCSP die contains matrices of MOS, resistors and BJT devices. Multiple placements of each matrix across die.
- Measurements of electrical characteristics of all device instances enable to separate out stress impact on electrical performance of devices.
- Simulated stresses were transformed to current variations: $\Delta I = \pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp} + \pi_{out}\sigma_{out}$ ("∥", "⊥" along and across electric current flow, and "out" for out-of-device plane)
- Measured and simulated device chacteristics agree within 5%.



(a) ΔId of MOSFETs (b) ΔIc of BJTs (c) ΔR of resistors

Summary

- We present a novel methodology for assessment of the performance variation of on-chip electric circuits due to CPI induced stress.
- Employed EMP methodology allows to perform a multiscale simulation of accurate stress distributions across the package and inside small IP-blocks.
- Stress components simulated in device channels can be immediately supplied to the linked Spice simulator for performing stress-aware analysis of circuits performance. The tool offers “what-if” analysis at the early floor planning step and for final design sign-off.
- Good fit between simulated and measured stress-induced shifts of device characteristics can be considered as the experimental validation of the proposed simulation methodology.

Thank you !