

3DIC Design: Challenges and Opportunities in System-of-Chips Integration

SYNOPSYS®

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Making System-of-chips for the SysMoore Era

Manufacturing Trends

Why “System of Chips”

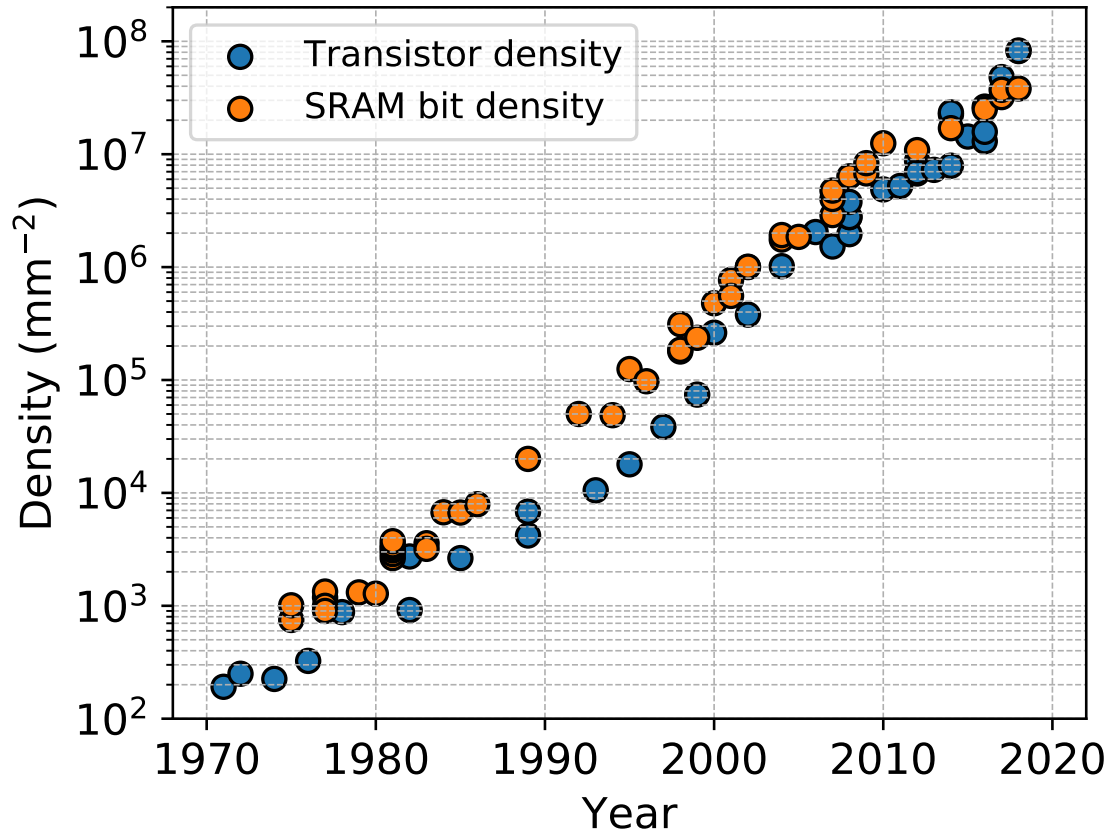
EDA as an Innovation Catalyst

SysMoore Journey Ahead

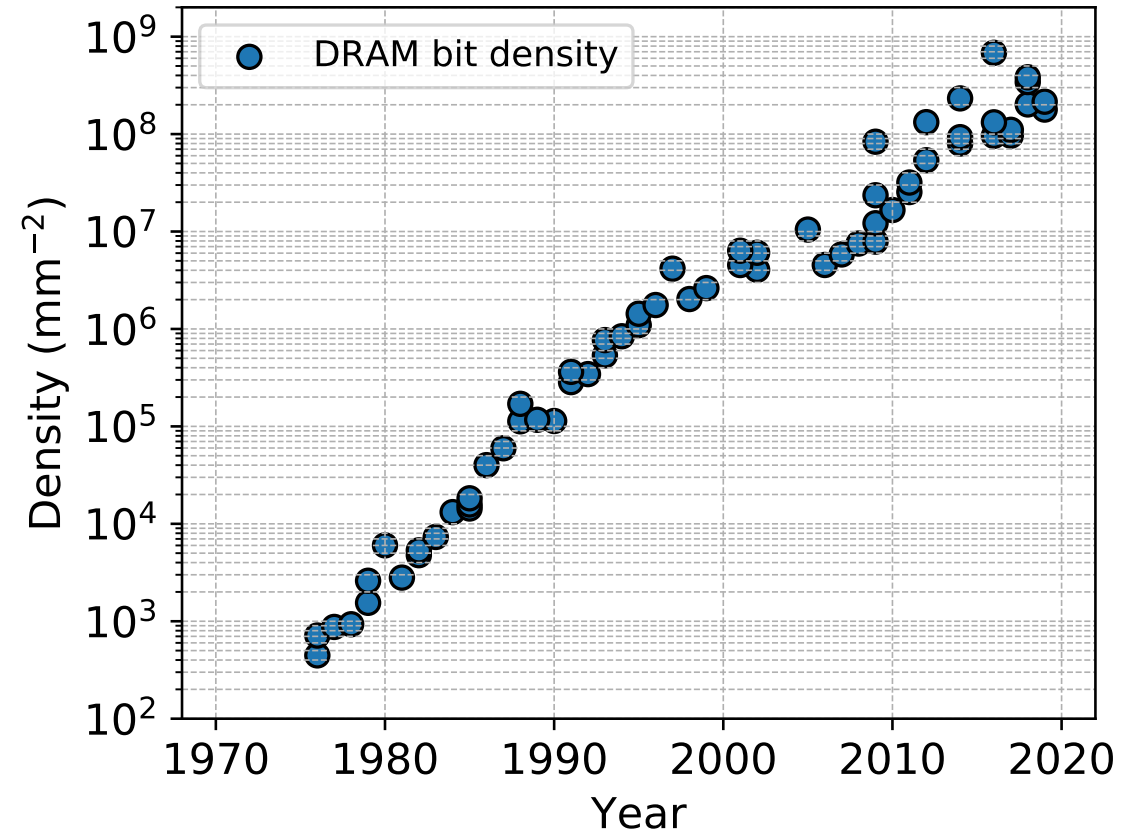
2D Scaling

The Last 50 Years

Logic density



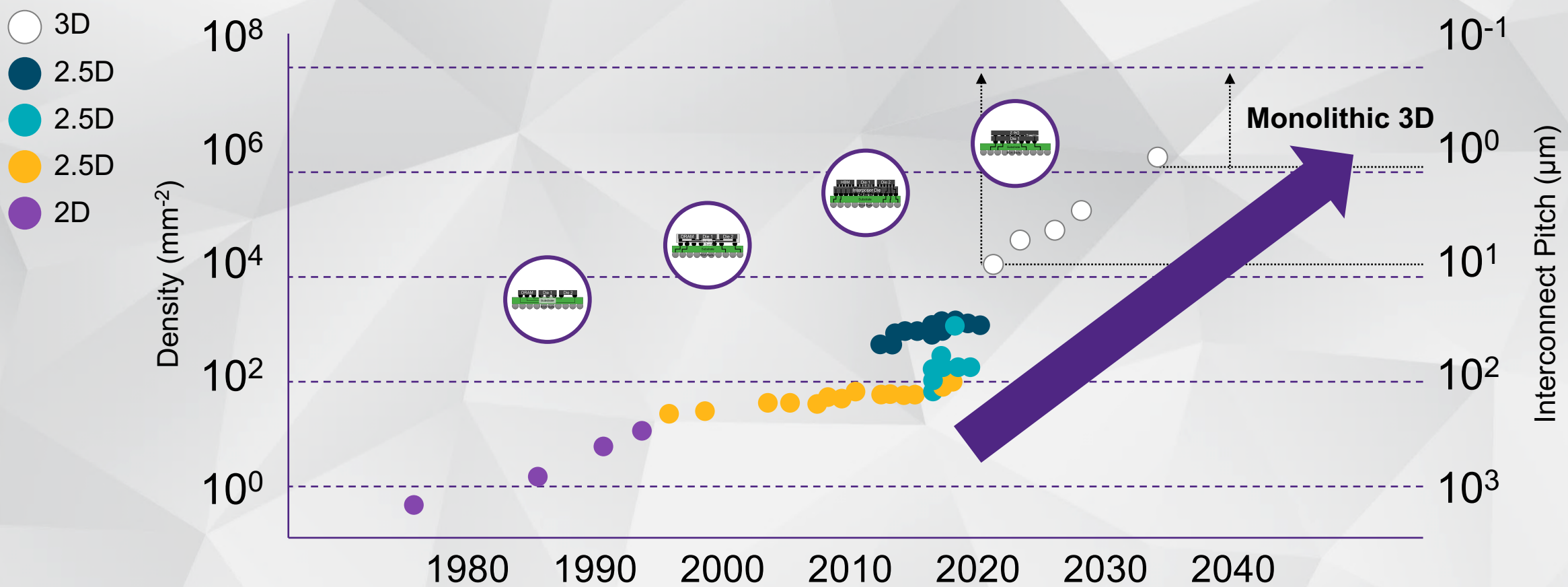
Memory density



Wong et al., Stanford, IEEE Proc., 2020

3D Interconnects

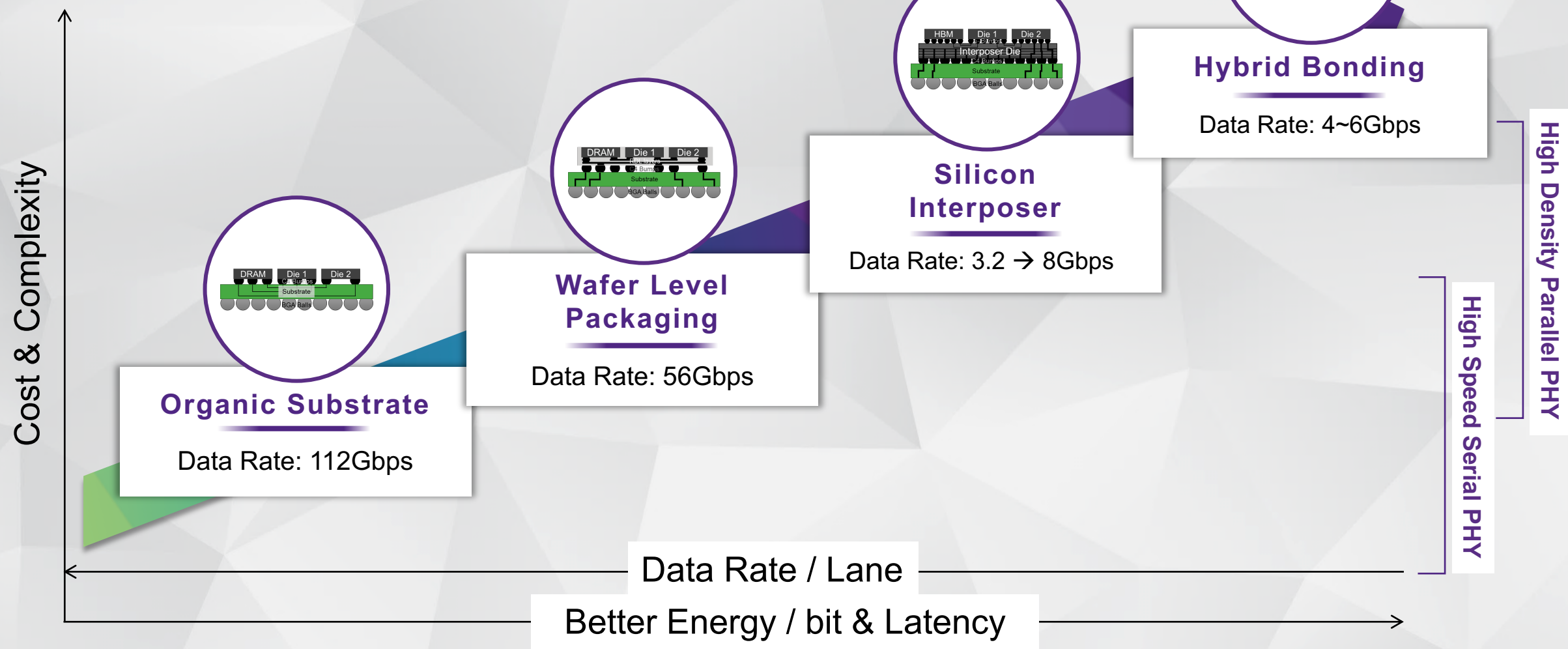
Scaling Beyond Miniaturization Barrier



TSMC, ISSCC, 2021

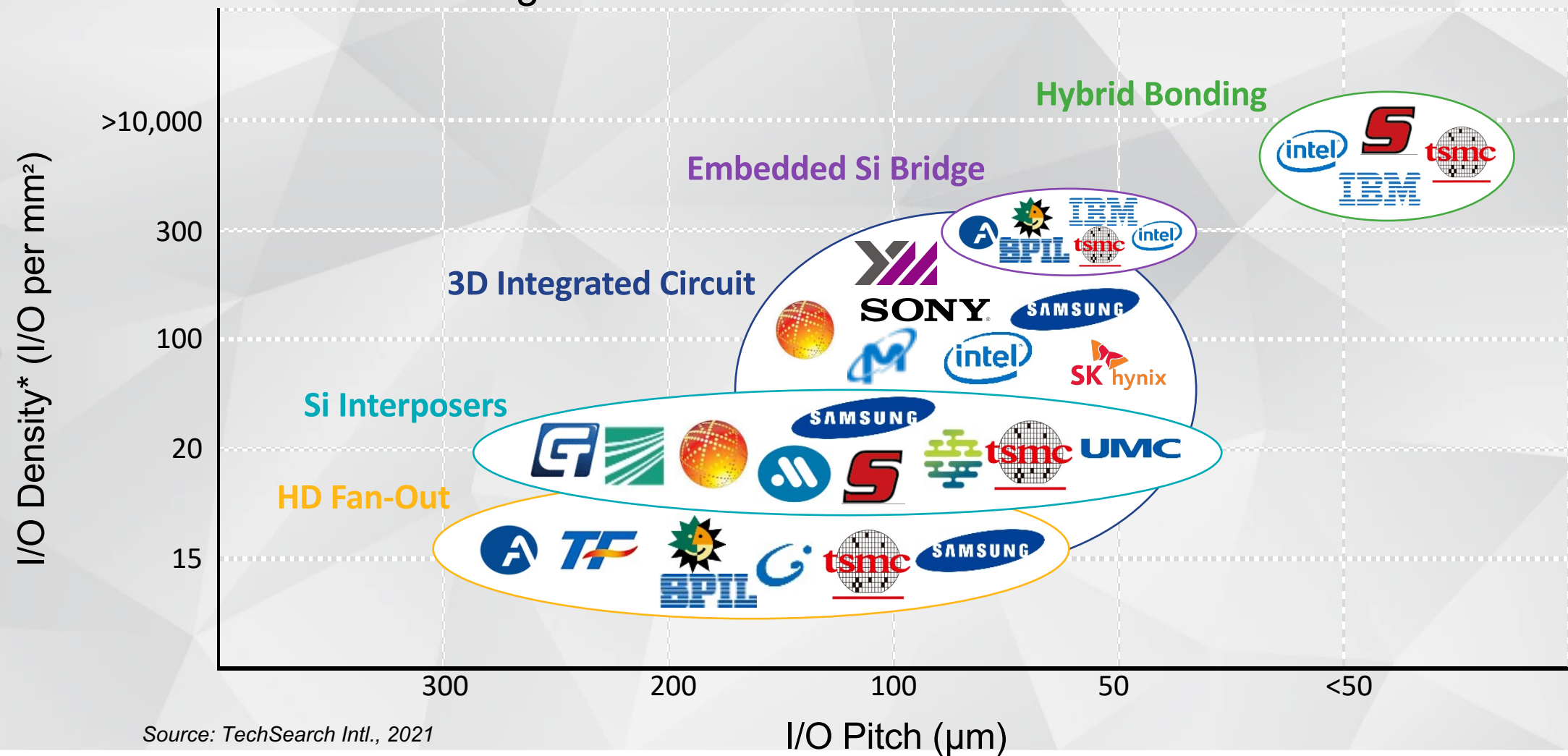
Advanced Packaging

Packaging & IC Now a Continuum



Many Manufacturers

Endless Possibilities for Design Innovation



Making System-of-chips for the SysMoore Era

Manufacturing Trends

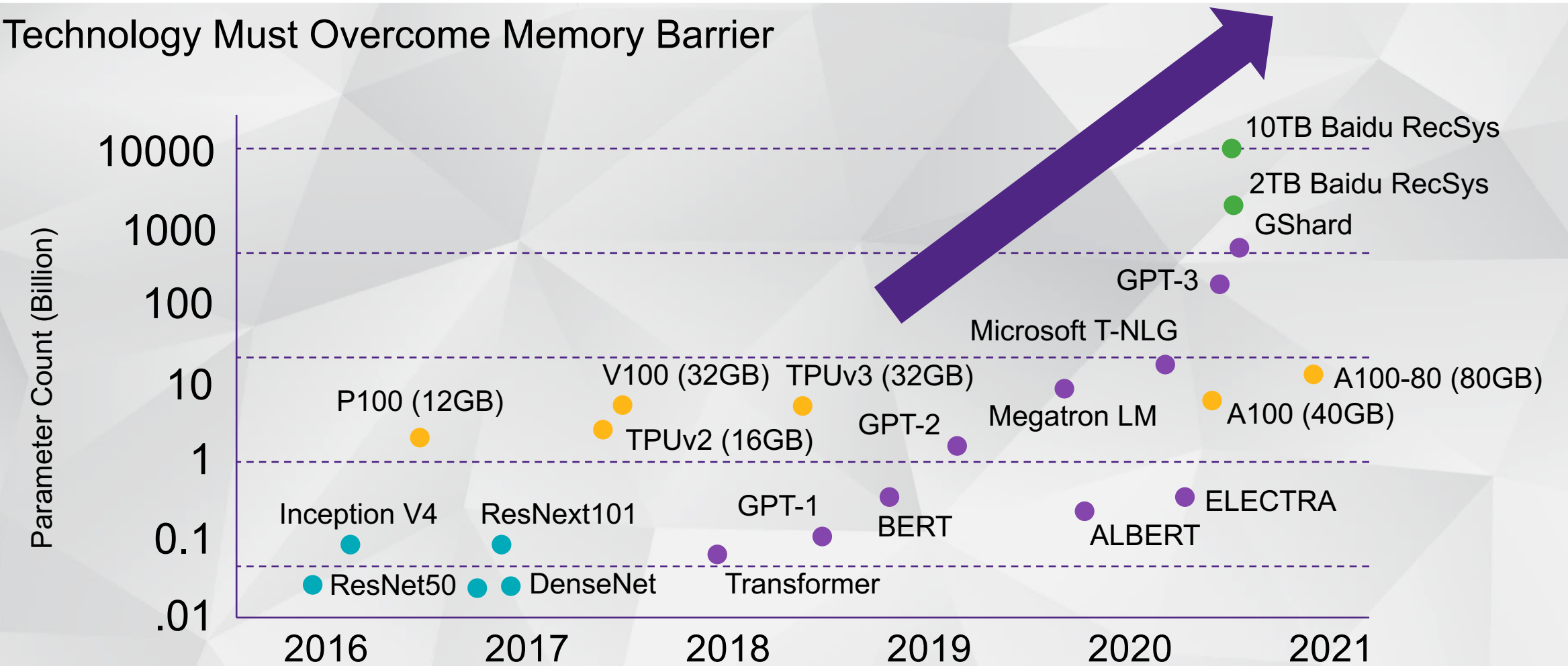
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AI Pushing the Limit

Technology Must Overcome Memory Barrier



He et al., Microsoft, Hot Chips, 2021

Tech

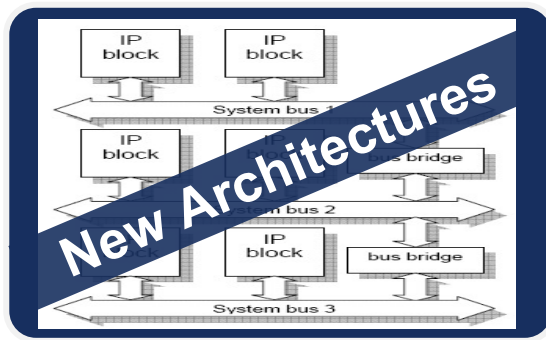
Onomics

Push

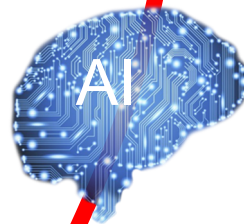
Pull

Scale Complexity

Systems of Chips



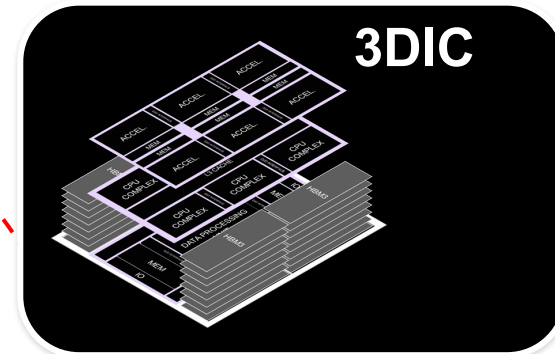
SoCs



AI

Classic Moore

SysMoore



3DIC

SoCs
System on Chip

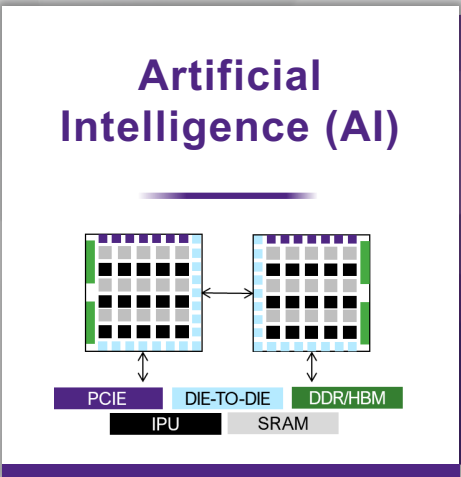
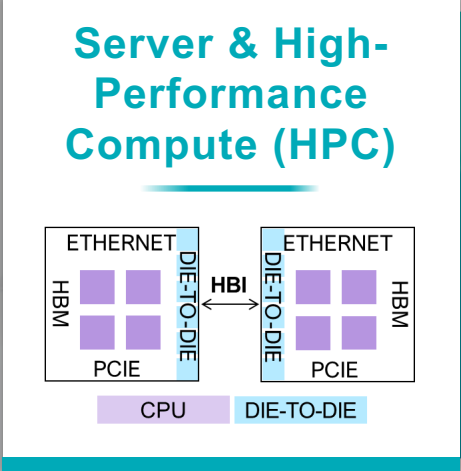
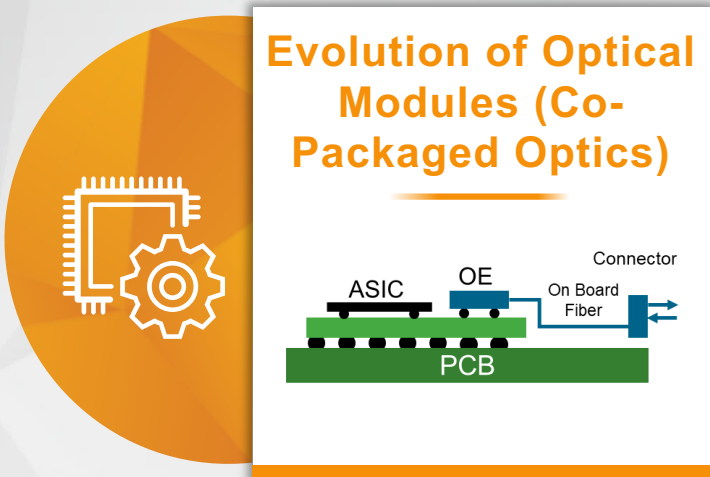
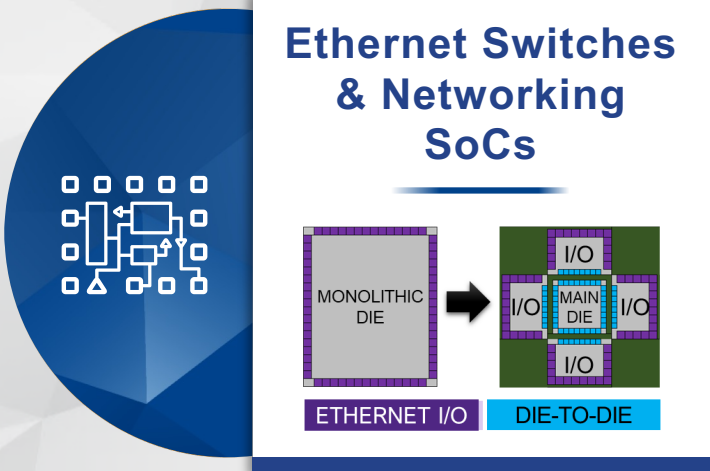
7nm 5nm 3nm 2nm...

Why System of Chips?



Common Commercial Use Cases

INTEGRATION



DISAGGREGATION

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SysMoore Journey Ahead

Journey of Creation

SoC Solution

Manufacturing &
Deployment

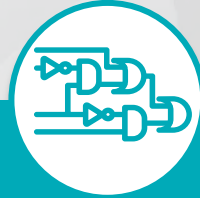
EDA (Electronic Design Automation)

Enabling Journey of Creation



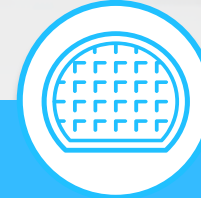
EXPLORE THOROUGHLY

- Substrate choice
- Chiplet / IP choice
- Early PPA / Reliability / Cost



DESIGN RAPIDLY

- Design IP, RTL to GDS
- Optimization
- SKU Variation



MANUFACTURE ROBUSTLY

- Cost (Yield)
- Time to Volume
- In-field Safety, Security & Reliability

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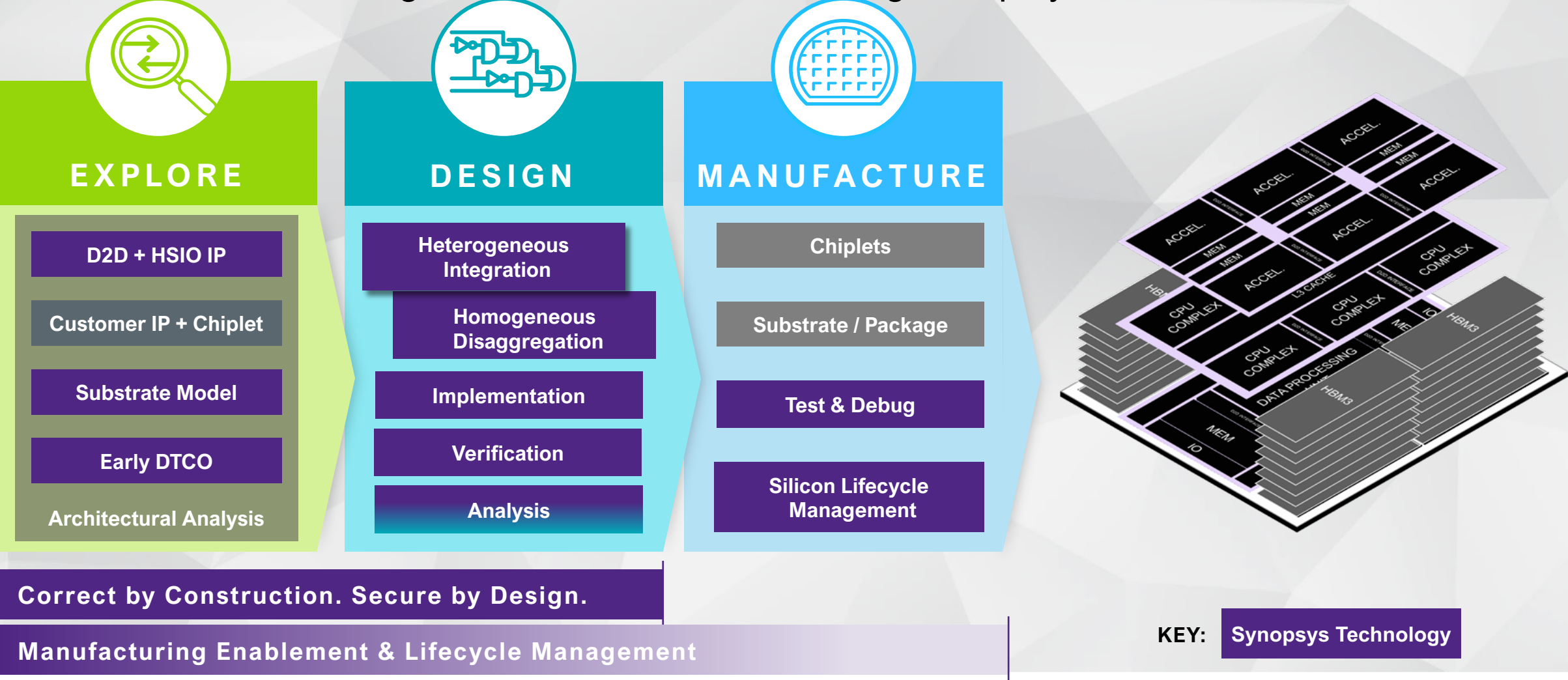
Journey of Creation

SoC Solution

Manufacturing &
Deployment

System-of-Chips (SoC) Solution =

1. Interface IP + 2. Design Platform + 3. Manufacturing & Deployment



SoC Solution =

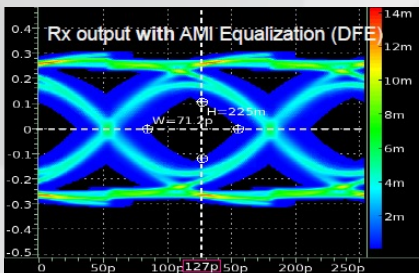
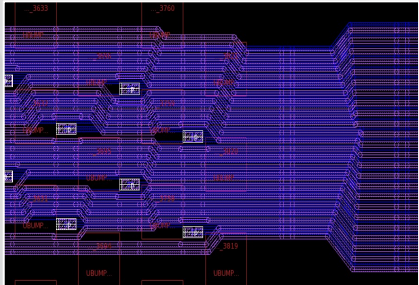
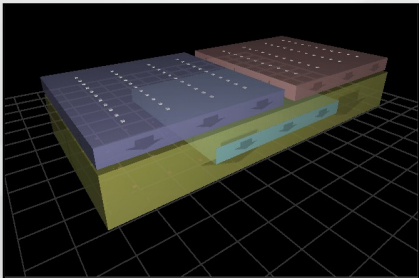
1. Interface IP + 2. Design Platform + 3. Manufacturing & Deployment

Assembly Density / Optimal Integration

Packaging technology	2D – Substrate	2.5D – RDL Fanout	2.5D – Si-Interposer / Bridge	3D – Die Stacking
D2D architecture	SerDes	SerDes / Parallel	Parallel	Bumpless (Parallel)
Reach	Range			
Bump Pitch				
Data rate / lane				
Power efficiency				
Latency				
Standards	OIF: CEI-112G-XSR/USR JEDEC: JESD204x		OCP: OpenHBI, BoW ChipsAlliance: AIB	Emerging
Use Cases	- Heterogenous integration: 5G, ADC, Sensors - SiPhotonics/CPO - Low-cost Server/AI	- High radix Switches - Mid-range/Edge compute - Servers/AI - Automotive	- High-end HPC - AI training, Servers - HBM memory	- High End HPC - SRAM, memory access - Mobile compute

SoC Solution =

1. Interface IP + **2. Design Platform** + 3. Manufacturing & Deployment



3D Pathfinding

3D Design Architecture

Place & Route

Test

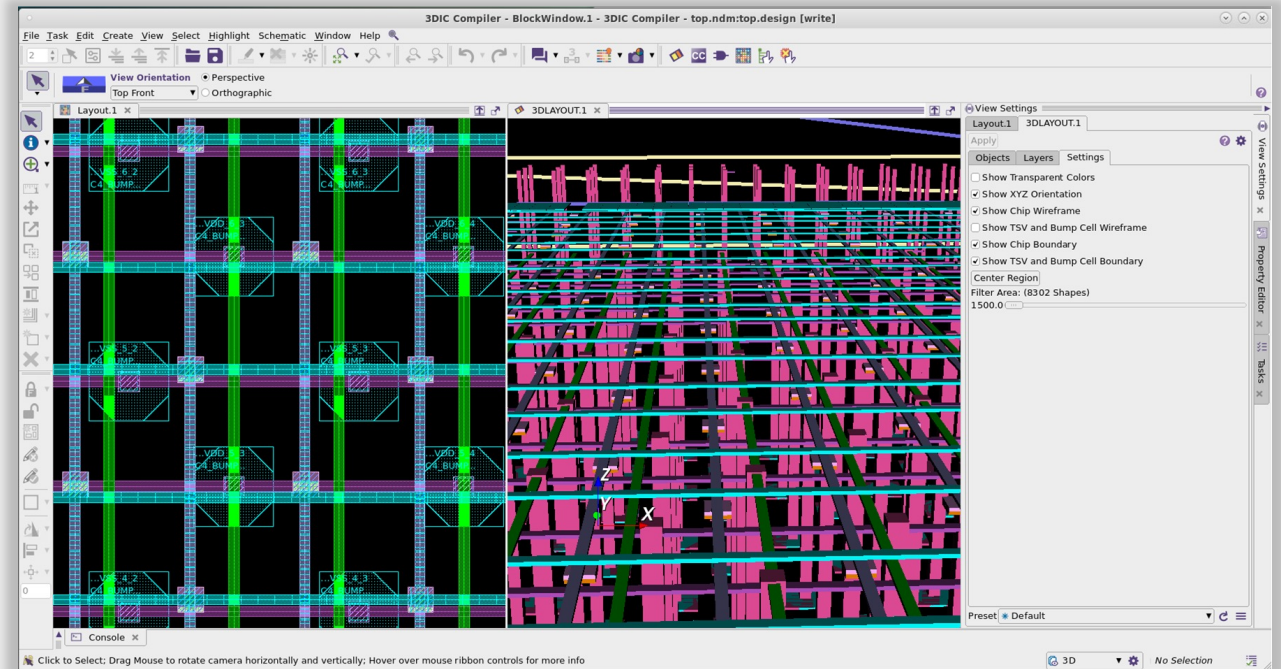
Extraction

Signal & Power Integrity

Thermal Integrity

Timing Analysis

Physical Verification



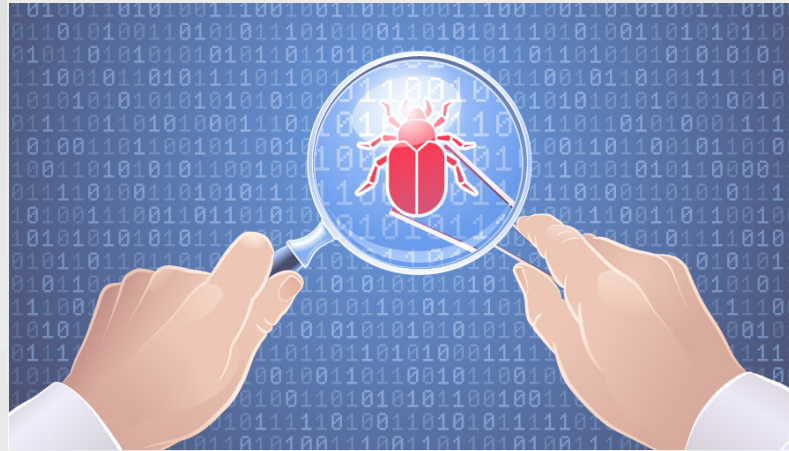
3D Chip Solution =

1. Interface IP + 2. Design Platform + **3. Manufacturing & Deployment**

PRODUCT QUALITY



PRODUCT DEBUG & TRACEABILITY



IN-FIELD OPTIMIZATION



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Journey of Creation

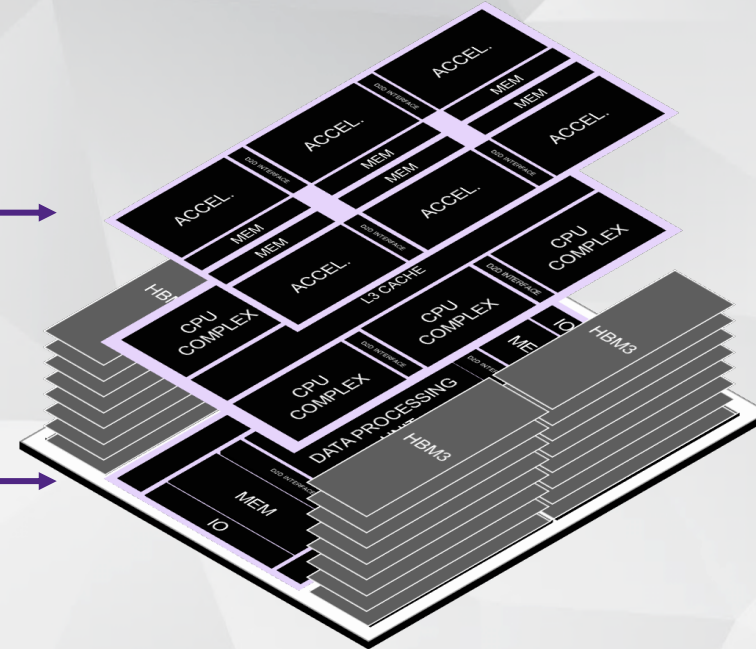
SoC Solution

Manufacturing &
Deployment

Enabling Manufacturing & Deployment

Product Quality

- Known Good Die (KGD) quality
- Interconnect test, diagnosis, & repair
- System test



Enabling Manufacturing & Deployment

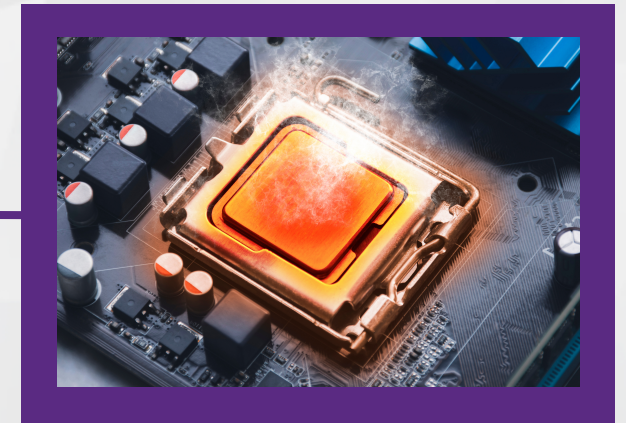
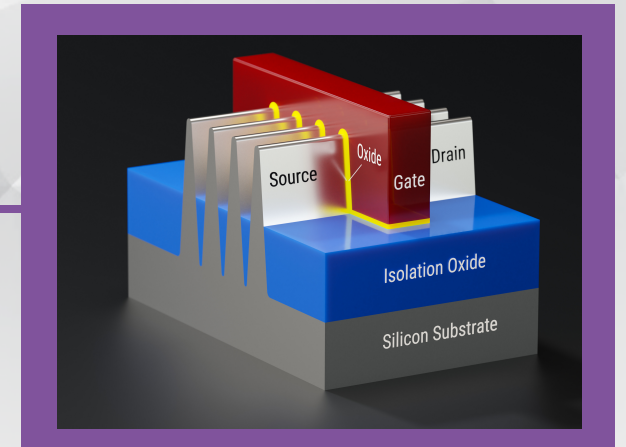
Product Quality

- KGD quality

Tech

Circuits

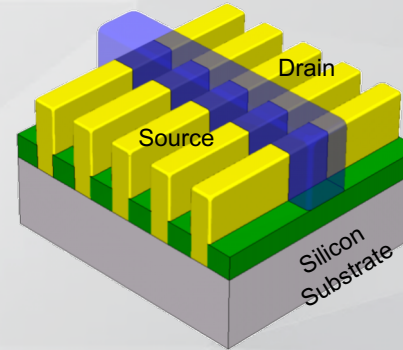
Product Use Cases



Enabling Manufacturing & Deployment

Product Quality

- **KGD quality**
 - Process-aware DFT
 - Cell-aware DFT
 - At-speed / at-temperature / power-aware testing

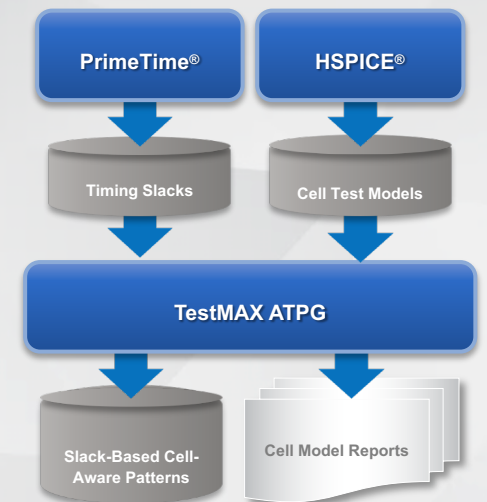
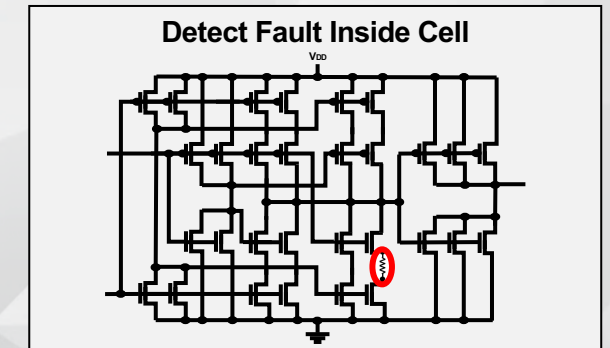
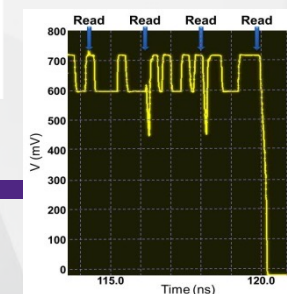
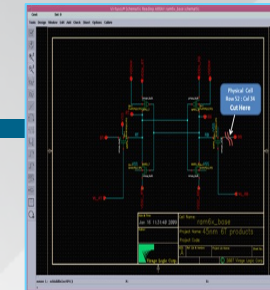
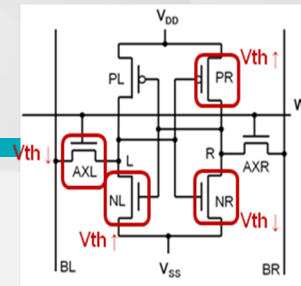


Resistive shorts between Fins

Resistive
Open/Short
Static/Dynamic Fault

Process
Variation
Faults

Random
Telegraph
Noise



Enabling Manufacturing & Deployment

Product Quality

- KGD quality
 - **Interconnect test, diagnosis, repair**
- **Logic to logic, low speed**

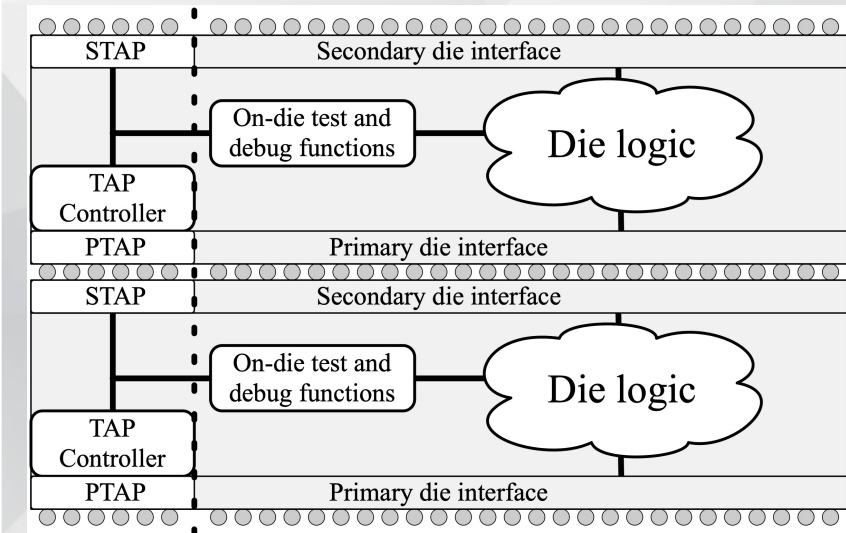
TSV / RDL based low speed interconnects

Scan Based Testing

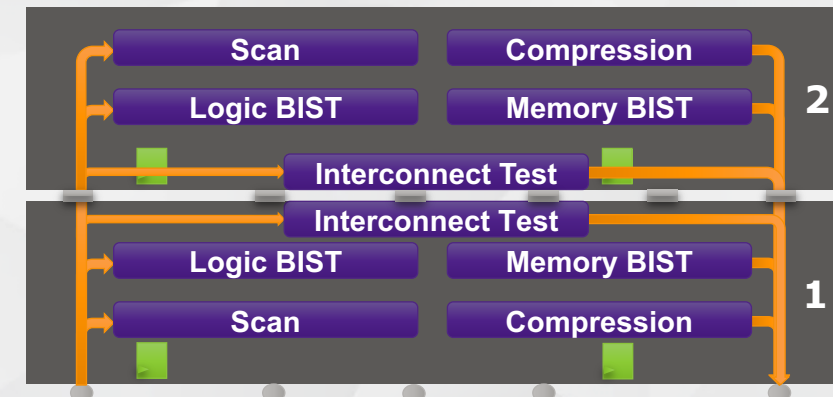
- Test access needs to be plug-and-play between dies
- Support by IEEE test standards - 1149.1 (PCB), 1500 (Core/IP), 1687 (instruments) and 1838 (3D Test)

Post-Assembly Access

- Test die-to-die, through micro bumps and TSV interconnects
- Static testing - for shorts and opens, similar to boundary scan testing
- Transition test for far-end loopbacks using PHY protocols, or registered loopbacks



Source: IEEE Std 1838™-2019



Enabling Manufacturing & Deployment

Product Quality

- KGD quality
- **Interconnect test, diagnosis, repair**
 - Logic to logic, low speed
 - **PHY to PHY, high speed**

IP test & diagnostic features

- BIST, loopback, at-speed probing, overriding calibration

Link test & repair capability for PHY to PHY

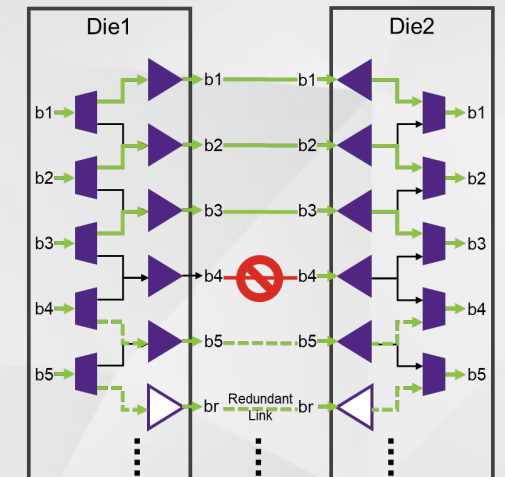
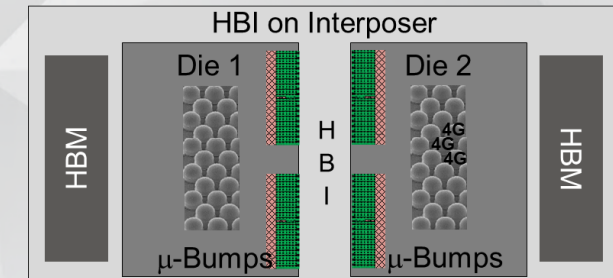
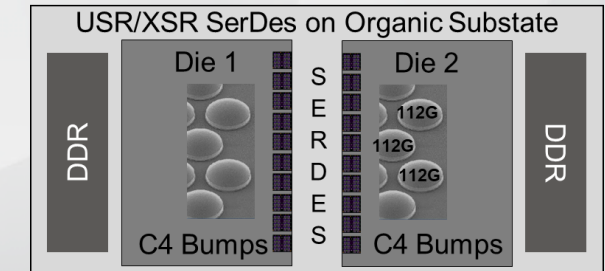
- Redundant lanes (two per channel) for repair

Embedded calibration

- Calibration handshake
- I/O driving strength calibration
- TX duty cycle correction
- RX DLL-based phase alignment

Built-in Self-Test (BIST) for at-speed production testing

- Internal loopback test (pre- and post- driver)
- External PHY-to-PHY link test for HBI+ ↔ HBI+ connections
- DLL BIST, Boundary scan, Scan ATPG and On-chip clock controller (OCC)



Enabling Manufacturing & Deployment

Product Quality

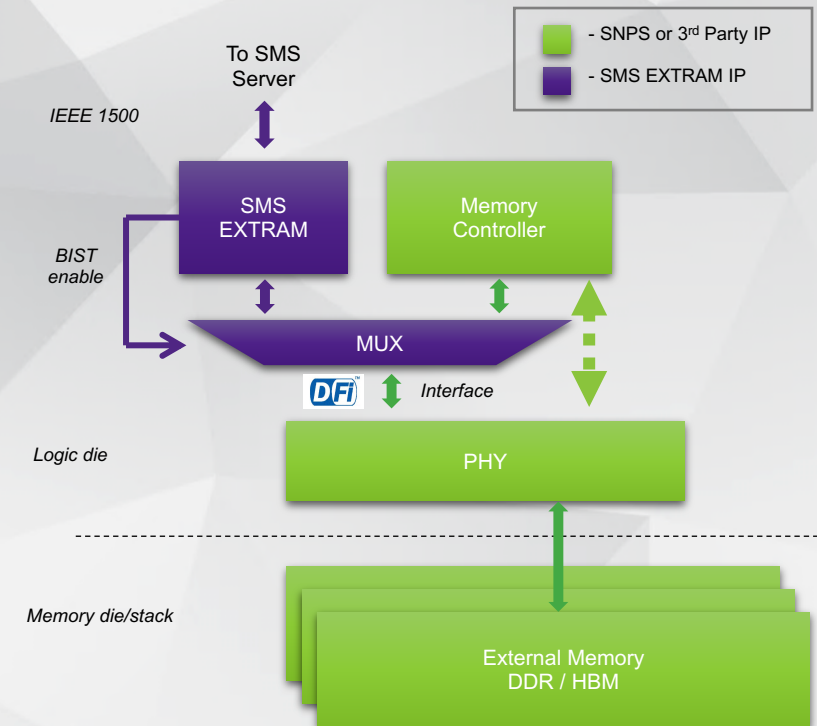
- KGD quality
- **Interconnect test, diagnosis, repair**
 - Logic to logic, low speed
 - PHY to PHY, high speed
- **Logic to memory, high speed**

PHY IP Test

- Scan for stuck-at fault and transition-delay fault test
- Test access to PHY CSRs through TDR interface
- I/O Bypass for die wrapper registers
- Interface Test (loopback, simple BIST)
- Redundant lane repair per channel for yield maximization

Memory Test

- Broad DFT support (DFI 3.1, 4.0, 5.0)
- Comprehensive March based BIST
- Extensive programmability and debug
 - Configurable addressing, timing operations, rank select, full data pattern, bus trimming, and diagnosis to bit cell

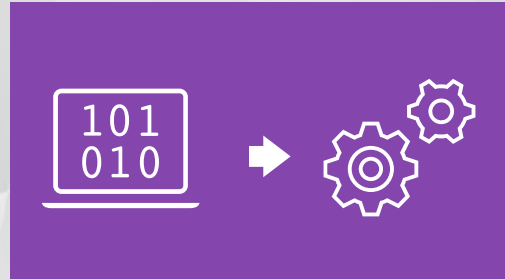


Enabling Manufacturing & Deployment

Product Quality

- KGD quality
- Interconnect test, diagnosis, repair
- **System test**

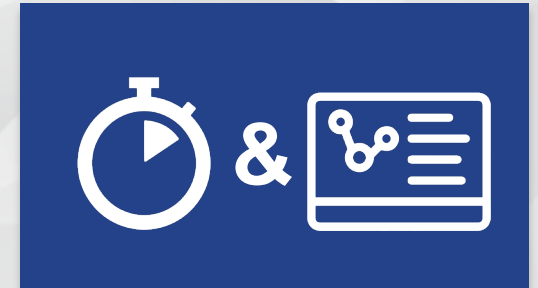
TRADEOFFS



Test time/cost
vs.
package yield lost



Simple pass/fail
vs.
System binning



Time-zero test
vs.
in-field monitoring

Enabling Manufacturing & Deployment

PRODUCT QUALITY

- KGD quality
- Interconnect test, diagnosis, & repair
- System test

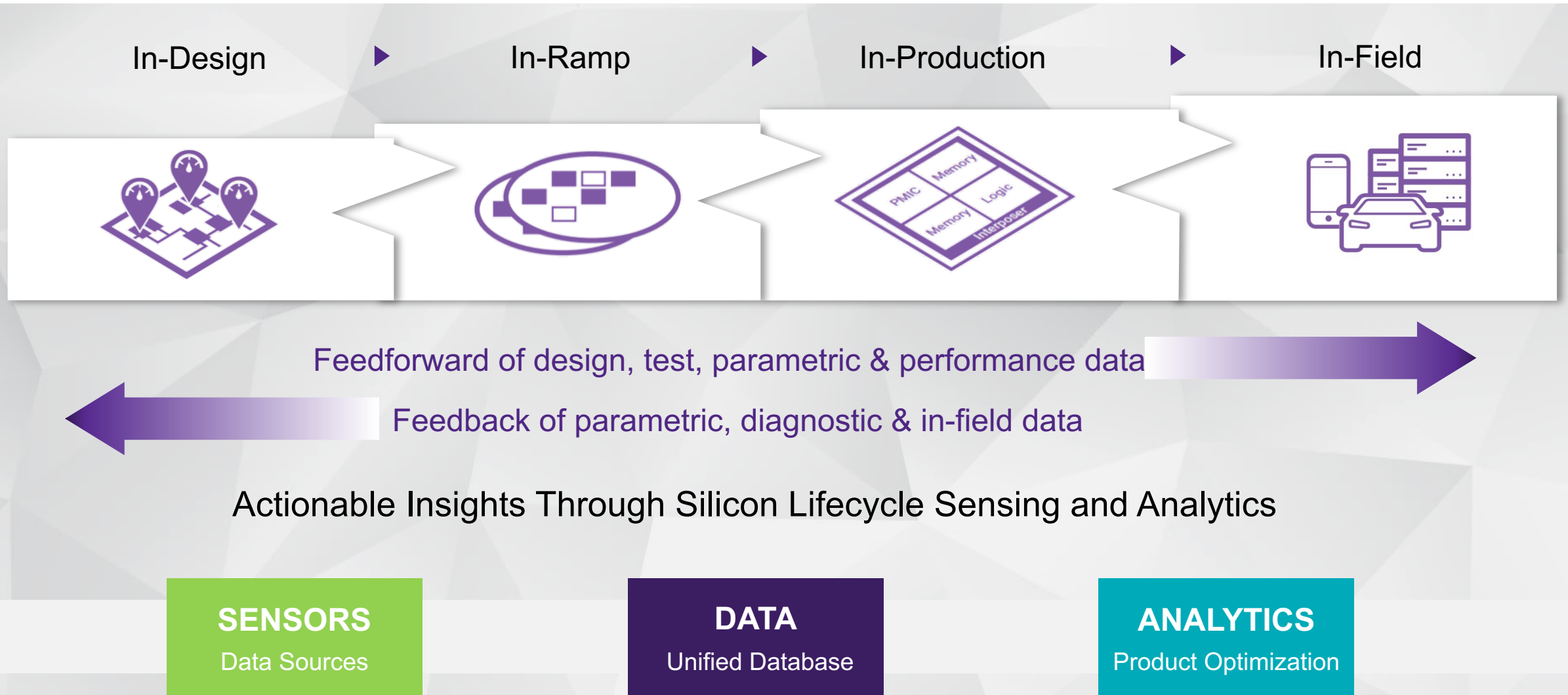
PRODUCT DEBUG & TRACEABILITY

- In-design sensors
- In-ramp volume diagnosis
- In-production quality & traceability

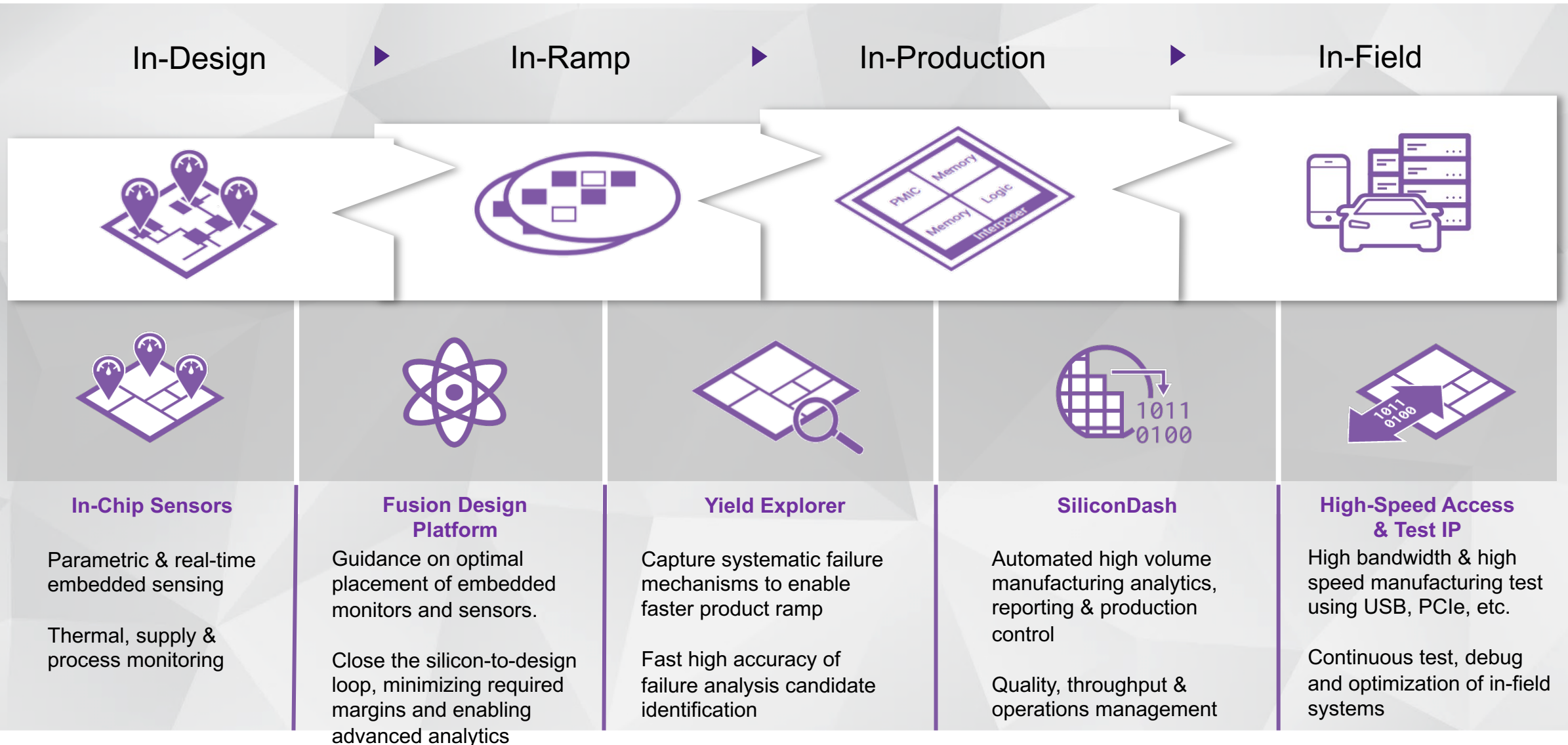
IN-FIELD OPTIMIZATION

- Performance optimization
- Functional safety & security
- Predictive maintenance

Silicon Lifecycle Management



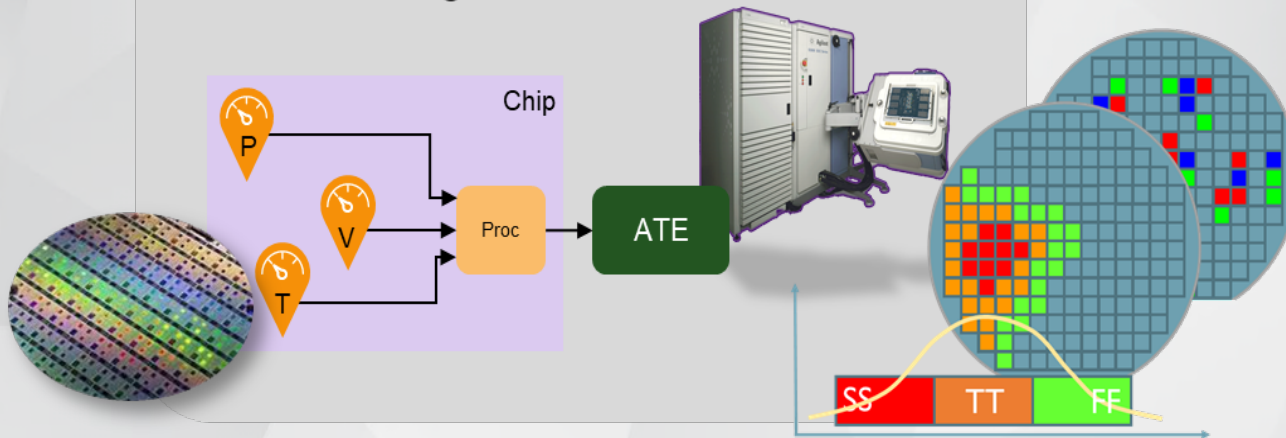
SiliconMAX Established Tool Solutions



SiliconMAX Use Case - Design Optimization

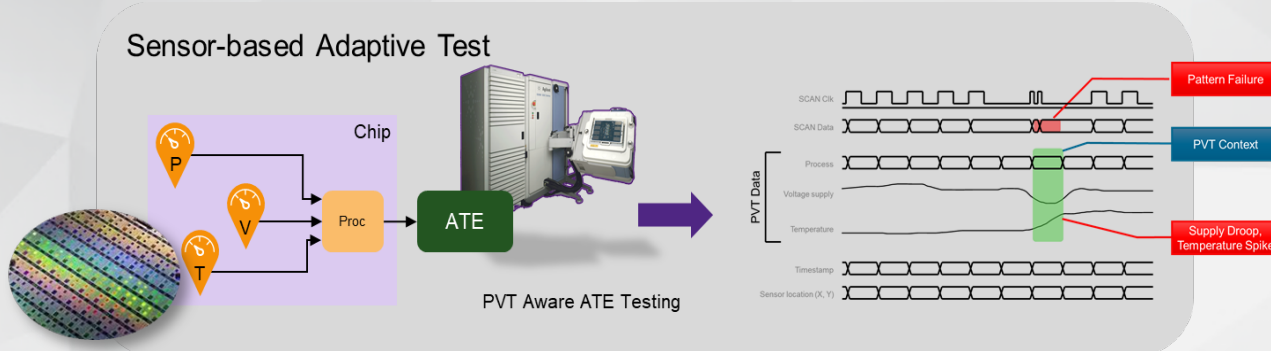
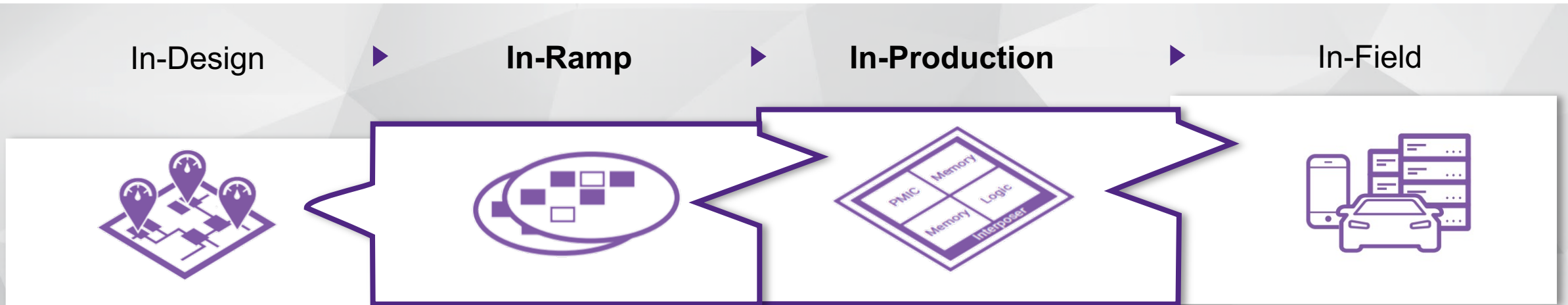


Silicon to Design Calibration



- Comparing measured silicon delay data to modeled cell and slack delay parameters
- Enabling the adoption of tighter timing margins resulting in faster and more robust designs

SiliconMAX Use Case - Test Optimization

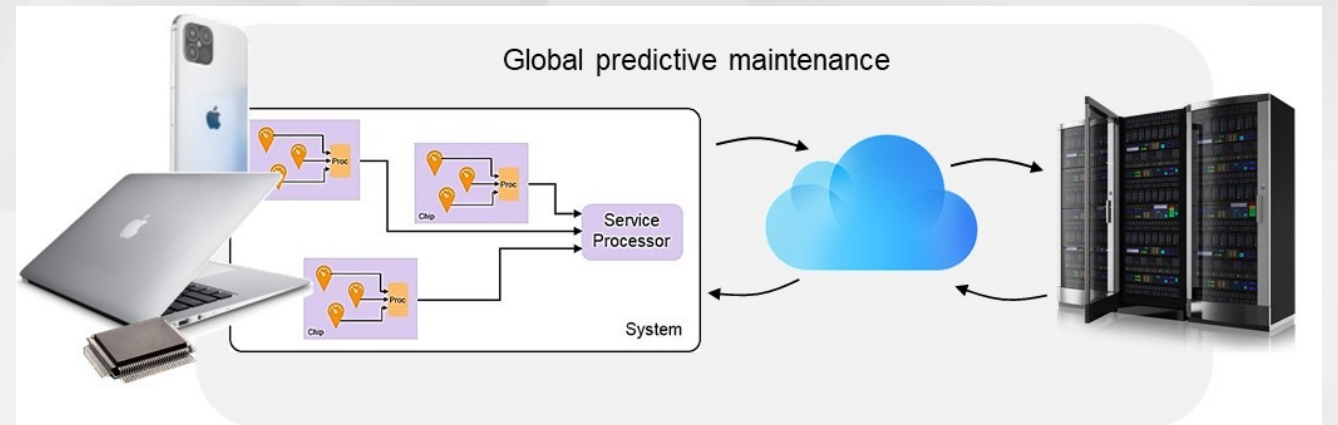


- Correlating PVT sensor data with test result data
- Enabling better outlier detection, more accurate failure diagnosis and improved test throughput through scan clock throttling
- Either Synopsys or customer-supplied sensors could be used

SiliconMAX Use Case - In-Field Performance Optimization

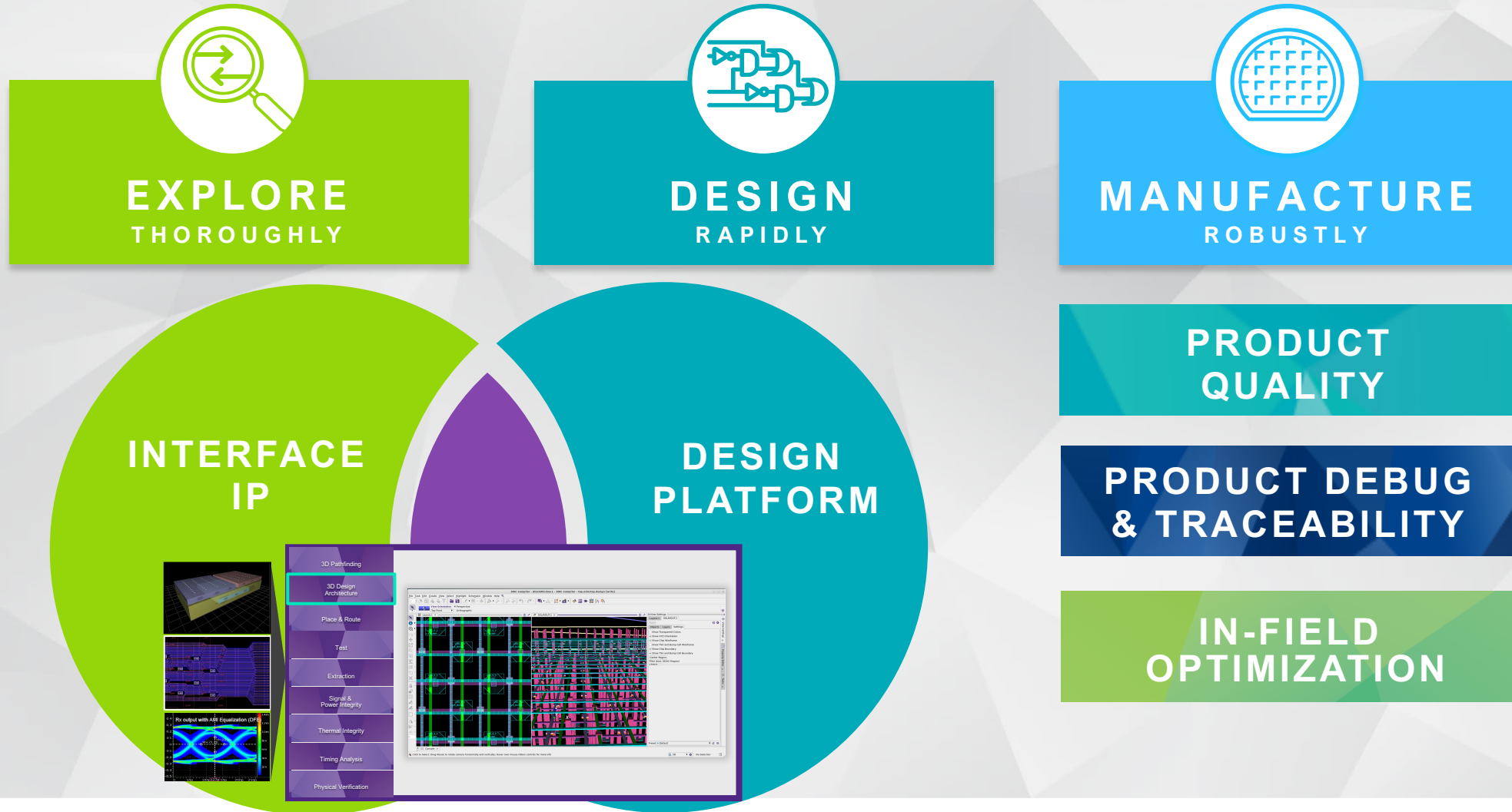


- Predictive system maintenance and performance optimization through the on-going analysis of on-chip sensor data
- Data sent securely through the cloud to centralized data analytics



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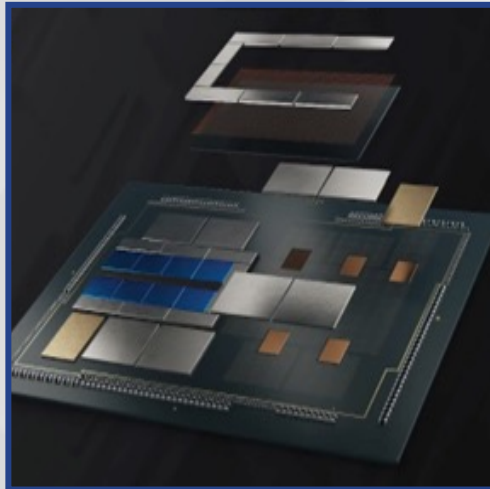
SysMoore Journey Ahead

Remaining Challenges

- Assembly Design Kits including mechanical, electrical, photonic, and thermal properties
- Industry standards for ensuring supply chain security
- Proliferation of inline process control for advanced packaging / 3DIC
- Proliferation of both data feedback and feedforward during complete product life cycle, with trust among vendors and OEMs

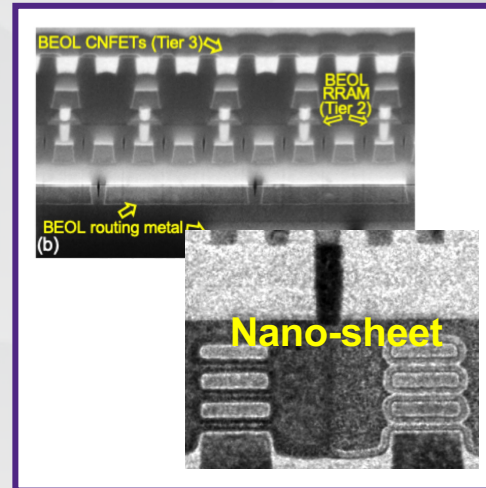
Technology Gives Us Wings

Heterogeneous Dense Interconnects/ Chiplets



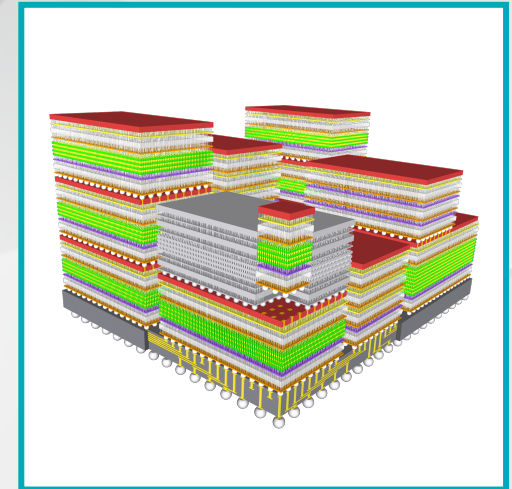
Intel, 2021

Super-monolithic Emerging Devices



Srimani, VLSI, 2020; TSMC, ISSCC, 2021

Hybrid Architecture Heterogenous + Monolithic



Radway, IEDM, 2021

Better Chips, Done Faster, by More People



EDA will catalyze the next 1000X

Transistors per
SoC

Reduction of
energy-delay product

Number of chip
innovators