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Machine-Learning Enabled PPA Closure for Next-Generation Designs

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Outline

- Introduction to Advanced Node PPA Challenges
- Evolution of Physical Design and AI/ML Inside-the-tool
- ML-Driven Synopsys Digital Implementation and Signoff
- Summary

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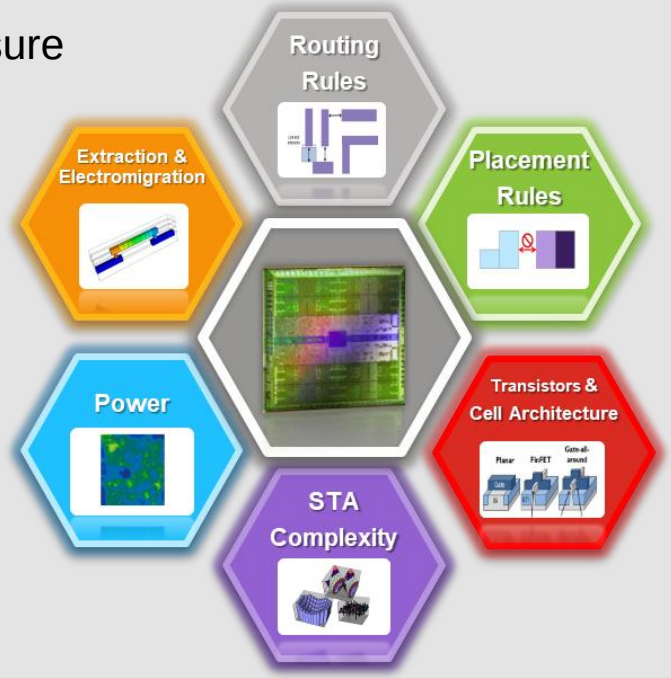
Accelerating Complexity of Physical Design

Introduction

- Physical design tools dealing with a myriad of challenges
  - Semi-conductor design companies under time-to-market and quality-of-results pressure
  - Foundries pushing strong DTCO to deliver Moore's law at new nodes
  - Technical requirements from each new node are increasingly complex
- Design size and constraints are growing rapidly
  - Block sizes are 2-10M instances
  - 10-20 timing and power scenarios
- Robust Power, Performance and Area closure requires AI/ML augmented tool flows



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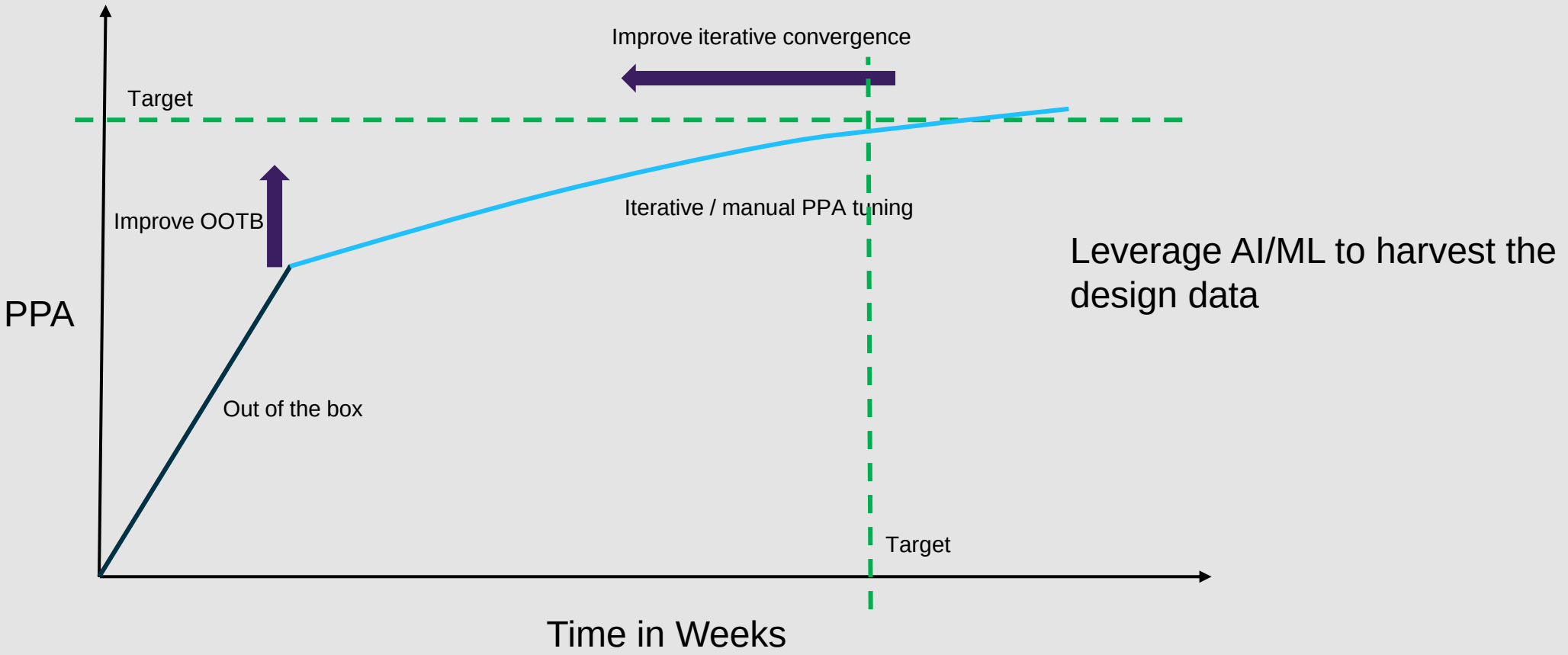
Power, Performance, Area Closure

Definition



Leverage AI/ML to harvest the design data

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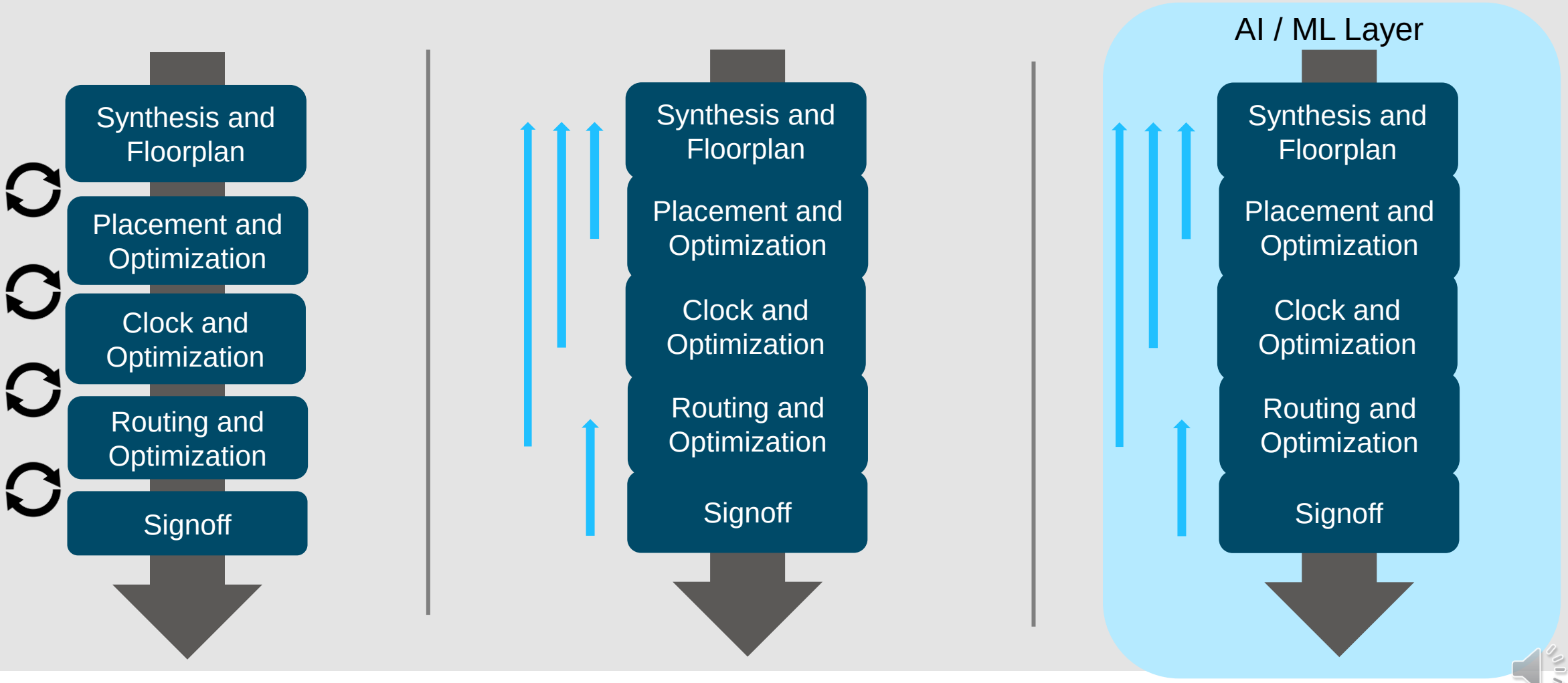
Evolution of Physical Design Flows

Shift-Left push



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AI / ML Driven PPA Closure

Current status

- Significant focus from EDA community to develop AI/ML-enabled algorithms and tool flows
- Majority of published work is centered around “tuning tool knobs” to improve PPA closure
  - FlowTuner, STS, FlowTune, OpenTuner etc.
  - Techniques like Multi-armed bandit, Bayesian optimization, Genetic Algorithms, Reinforcement Learning, Deep Learning, ….
- Two big EDA vendors are offering AI/ML powered Chip Design Closure capabilities
  - Good success in delivering PPA gains on leading-edge designs

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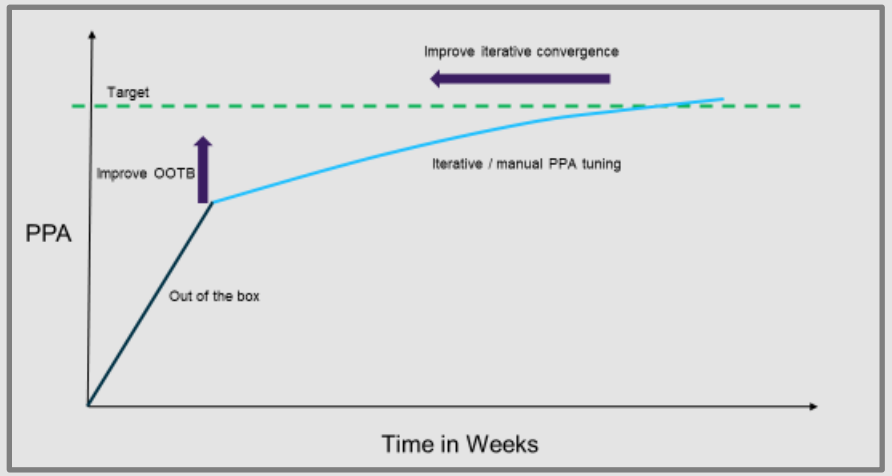
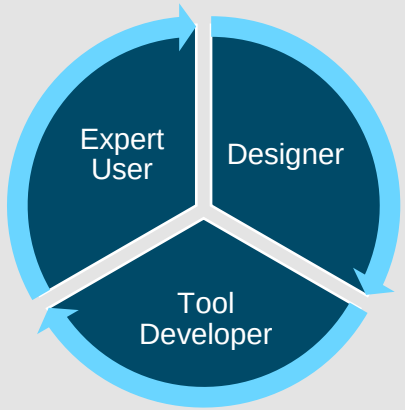
AI / ML Driven PPA Closure

Learnings as we look back

- Change in designer mindset to accept
  - Increase in compute resource to enable auto-exploration
  - Increase in tool runtime to accelerate PPA closure



- Harness knowledge/AI from different sources to deliver full PPA potential
  - Expert user (tool behavior)
  - Designer (design intent)
  - **Tool developer (New algorithmic approaches “Inside-the-tool”)**



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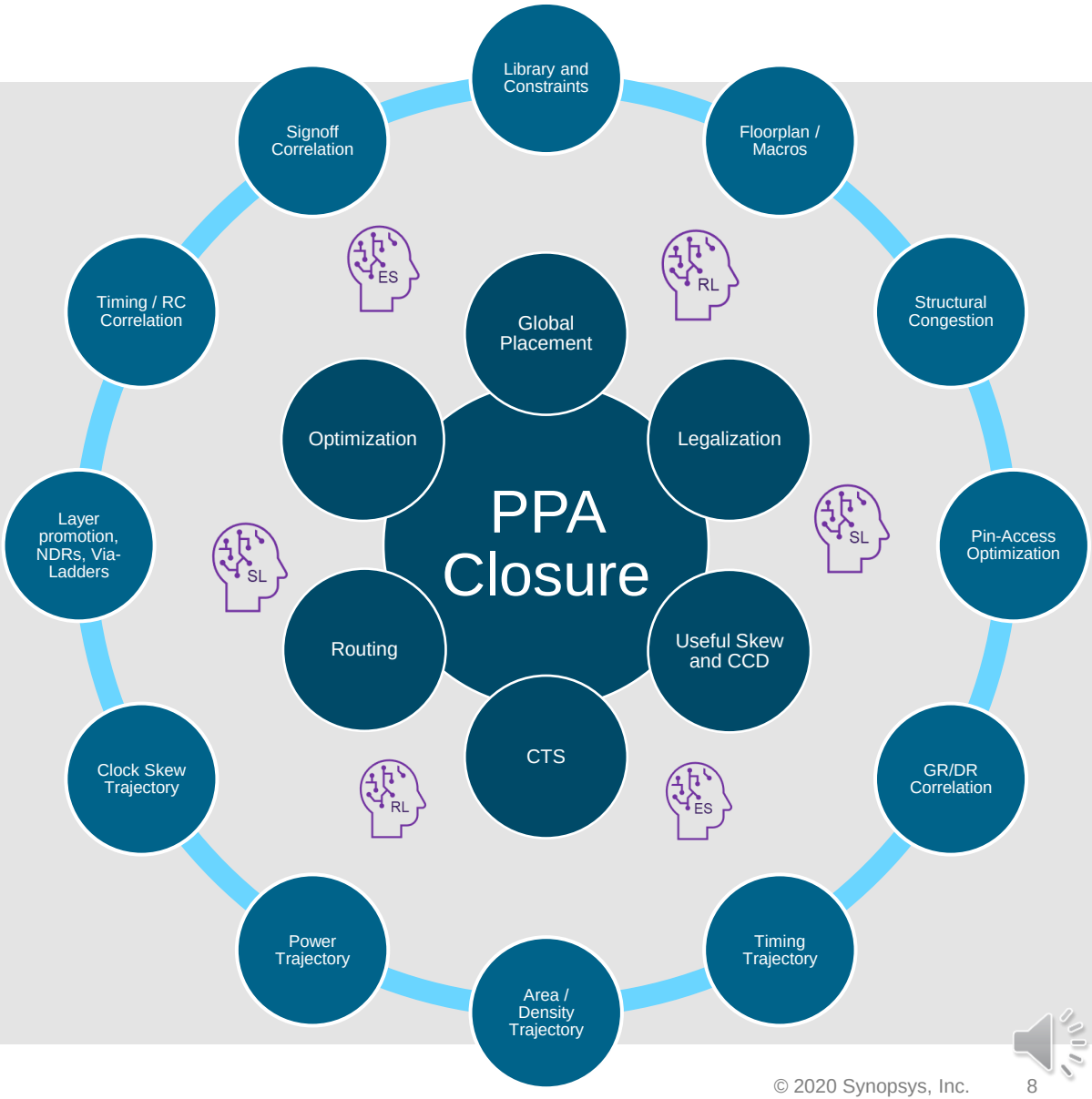
Engine vs. Sub-System

It is all about the sub-system

- Exponential complexity, intractable to formulate “global” solutions
- Algorithms need to be developed at the resolution of sub-systems
  - PPA Closure (QoR + Runtime)
  - Robust, Predictable and Scalable
- Leverage a combination of
  - Traditional algorithms and estimation strategies
  - AI/ML predictive modeling (Pre-trained, In-Design, Transfer Learning, Context Embedding)
  - Exploratory sub-flows (Look-Ahead)
- Popular AI/ML Paradigms
  - Supervised Learning
    - Pre-trained models
    - In-Design learning models
  - Reinforcement Learning
    - Transfer learning across runs



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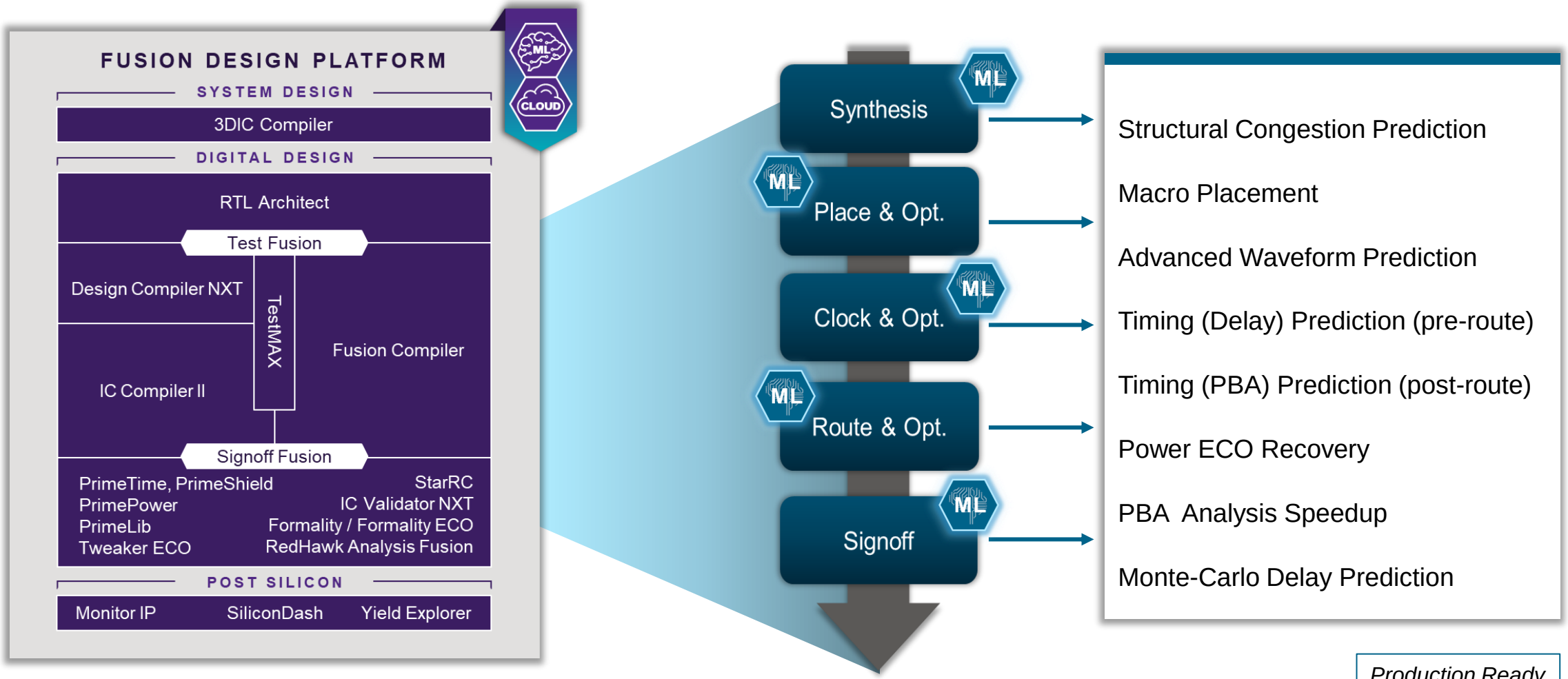
Machine-Learning Driven Digital Design and Signoff

"ML-*everywhere*" delivering better PPA, predictable flow convergence and faster TTR



Production Ready

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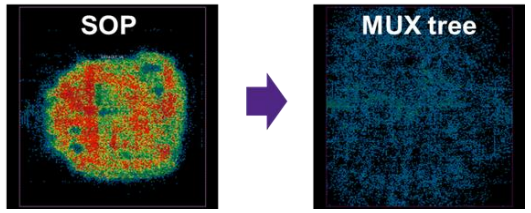
ML-Driven Implementation for Better PPA, Faster TTR

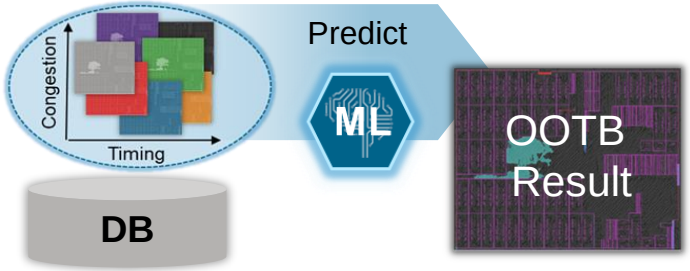
Key Features in IC Compiler II and Fusion Compiler

Structural Congestion Prediction



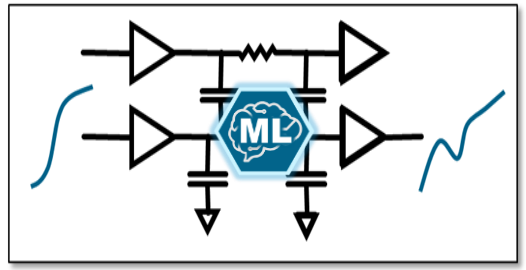
Better SELECT-OPs Architecture

ML-Driven Macro Placement



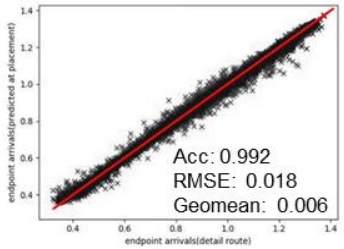
Accelerate Design Exploration

Waveform Prediction



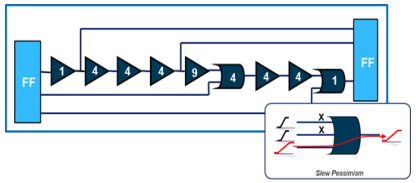
Fast Timer for Adv. Delay Compute

Timing Delay Prediction



Better Post-Route R2R Timing

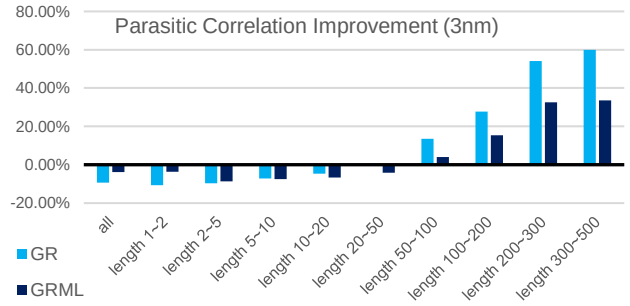
Timing (PBA) Prediction



Predict GBA vs. PBA gap

Reduced Total Power

Global Route Extraction Prediction



Accurate RC prediction

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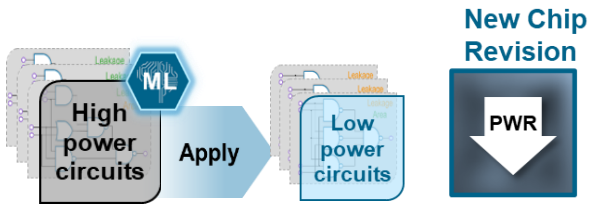
ML-Driven Signoff Technologies for Faster TTR

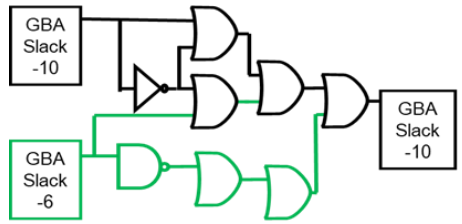
Key Features in Signoff Engines

PrimeECO : ML Power Recovery



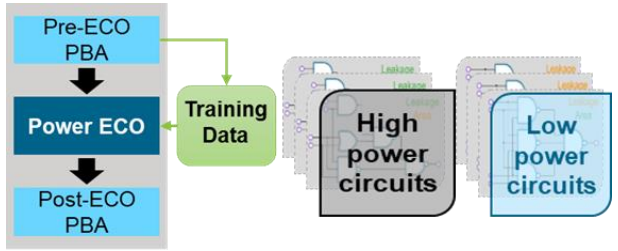
Highly Correlated, 10X Faster

PrimeTime : ML PBA Analysis



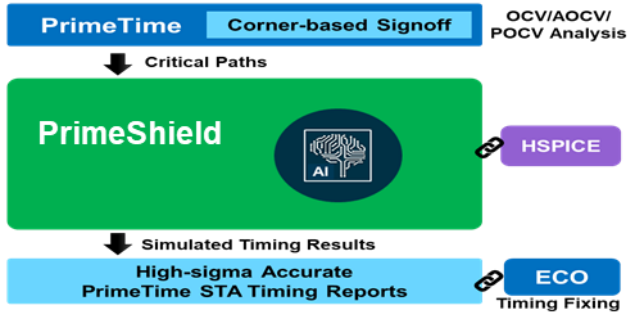
Signoff Accuracy, 5X Faster

PrimeECO : ML PBA Driven ECO



Similar Timing & Power, 5X Faster

PrimeShield : ML MC Simulation



> 100X Faster w/ HSPICE Accuracy

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Significant Benefits using ML Technologies in All Verticals

Customer Success with Digital Implementation and Signoff Tools

FC / ICC II : ML Timing Prediction

5nm
68% TNS
4.5% Leakage

5nm
20%-60% TNS
50% NVP

6nm
60% TNS, WNS
1.7X TTR

7nm
15%-30% WNS
25%-50% TNS
2%-10% Leakage

PrimeTime : ML PBA + HyperTrace

14nm
51M instances

10X Speedup
Similar QoR

7nm
6.5M instances

6X Speedup
99.97% NVP Accuracy
98.5% TNS Accuracy

PrimeShield : ML Monte-Carlo Sim

5nm
155X-495X Speedup
Days to mins

5nm
100X-500X Speedup
< 2hrs, < 1% error

5nm
156X Speedup
99% HSPICE MC accuracy

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Summary

- Reviewed PPA closure challenges on advanced node designs
- Presented the need for sub-system driven PPA closure using new algorithms leveraging AI/ML techniques
- Presented a snapshot of successful AI/ML features in Synopsys Digital Implementation and Signoff tools
- Synergistic benefits possible from AI/ML technique Inside and Outside the tool.

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