ISPD 2022 Panel – PCB routing

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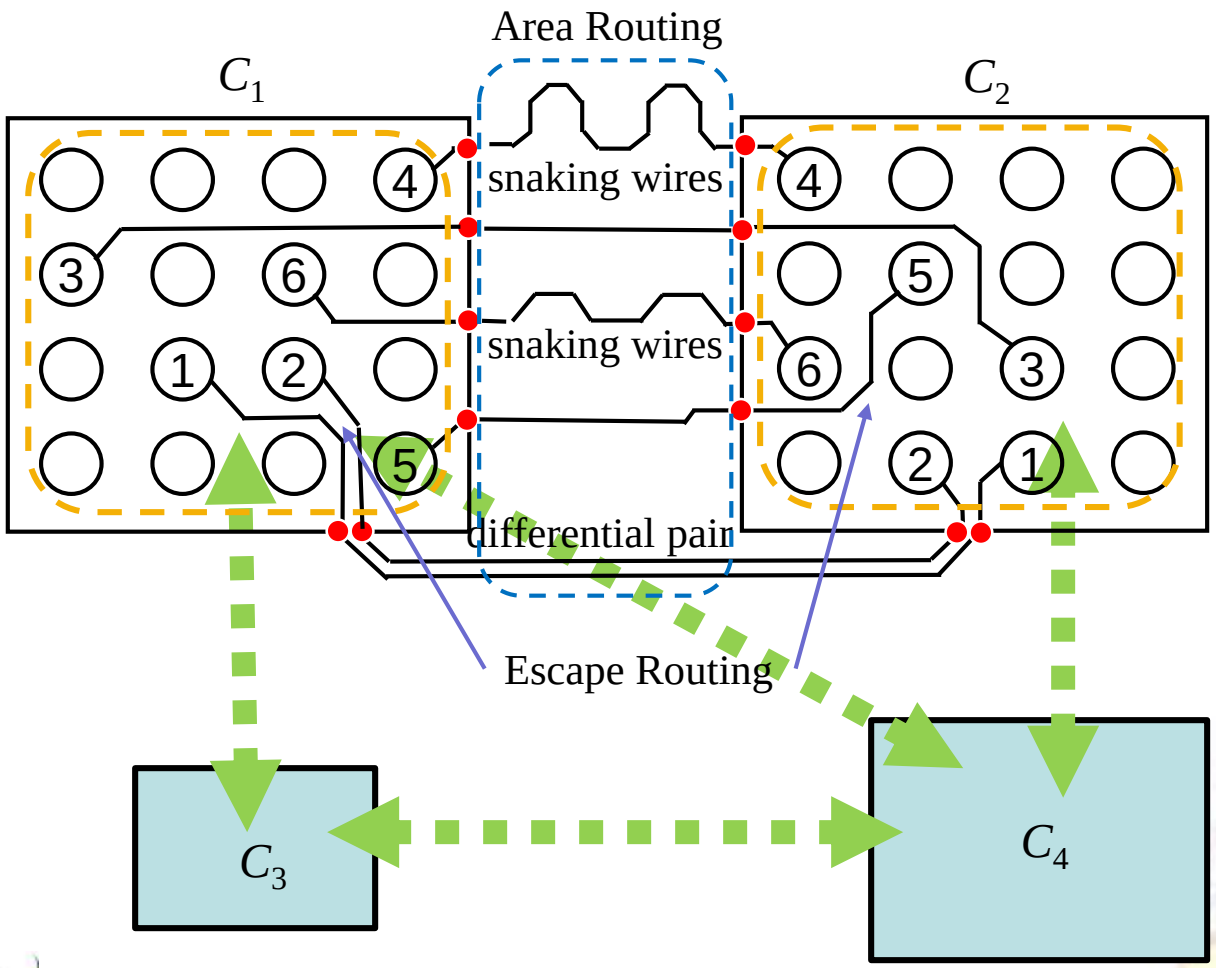
PCB Routing


Area Routing
C_1
C_2
snaking wires
snaking wires
differential pair
Escape Routing
C_3
C_4

Previous Works

- Escape routing
  - ✓ Unordered escape routing (UER)
  - ✓ Ordered escape routing (OER)
    - ➢ SAT [08, 09] & ILP [09, 16, 20] approaches
    - ➢ Monotonic path with via assignment for 2-layer BGA [06]
  - ✓ Simultaneous escape routing (SER)
    - ➢ Pattern routing [06, 08]
    - ➢ Boundary routing [11]
    - ➢ Hierarchical multi-layer SAT [21]
- Area Routing – length matching
  - ✓ Lagrangian relaxation [03]
  - ✓ Bounded-sliceline grid [08]

Previous Works

- Escape and area routing considering length matching constraints
  - ✓ Hierarchical multi-layer SAT for escape routing and layer assignment together with crossing-free area snaked routing [21]

Challenges

- Total solution rather than separate works
  - ✓ Length-matching aware PCB routing flow
- No benchmark
  - ✓ DAC 2021 test cases from the industry