

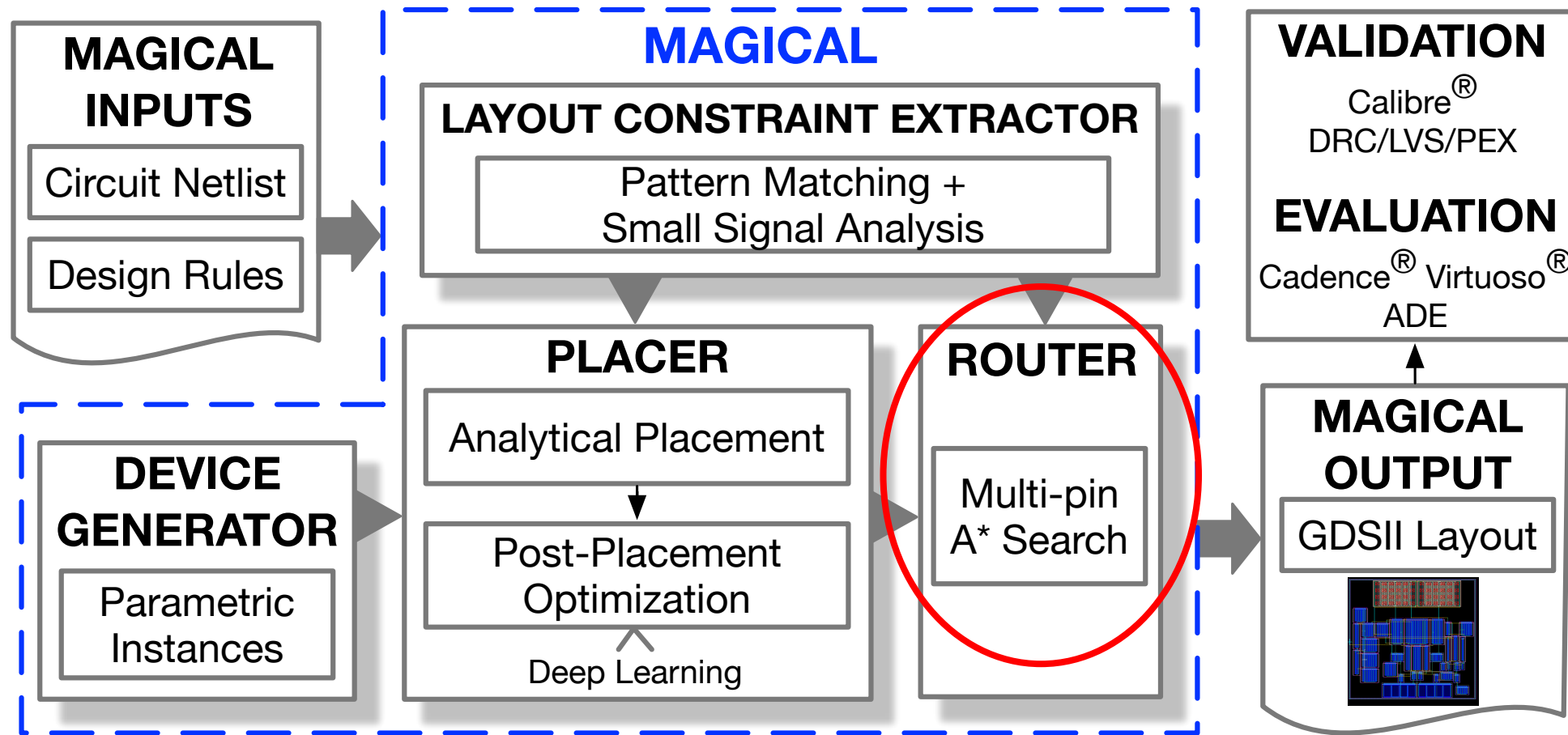
Integrating Human and Machine Intelligence into Analog Routing

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MAGICAL: Machine Generated Analog IC Layout

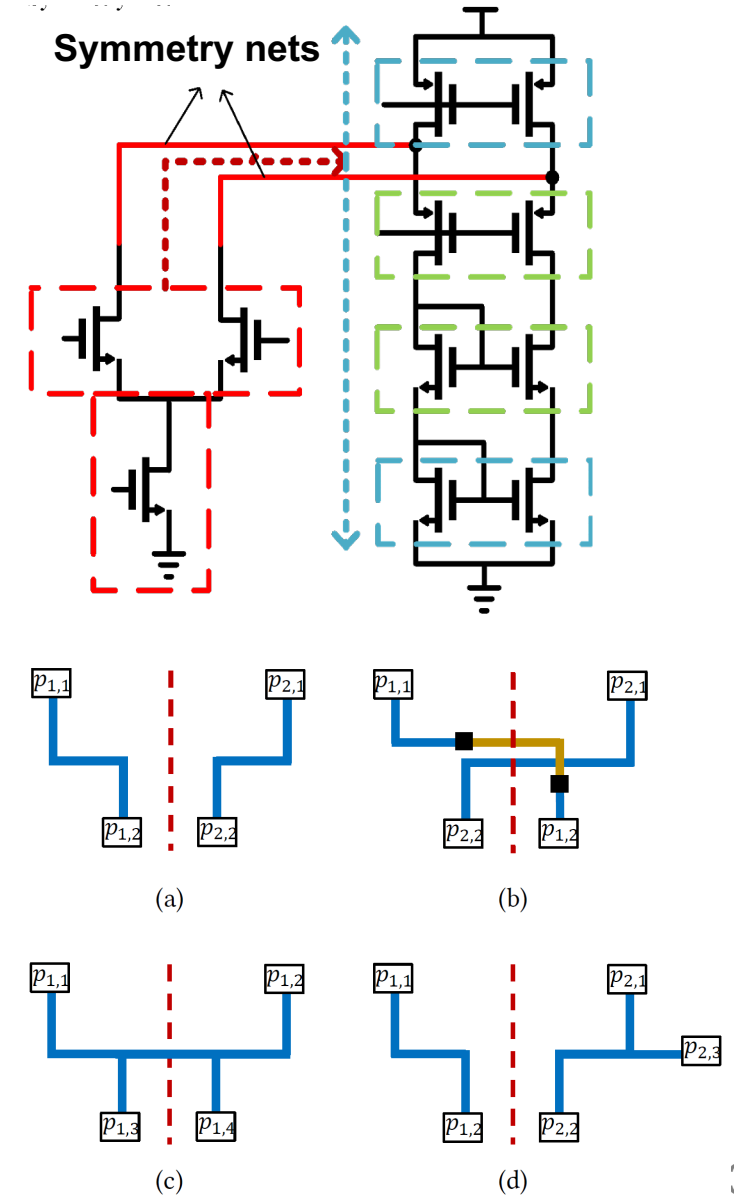


- Fully-automated analog layout, leveraging human and machine intelligence

[ISPD'19; DAC'19; ICCAD'19; ASPDAC'20; DATE'20; DAC'20; ICCAD'20;
D&T'20; JoS'20; CICC'21; DAC'21; ICCAD'21; ASPDAC'22; DATE'22; DAC'22]

Automating Analog Constraint Generation

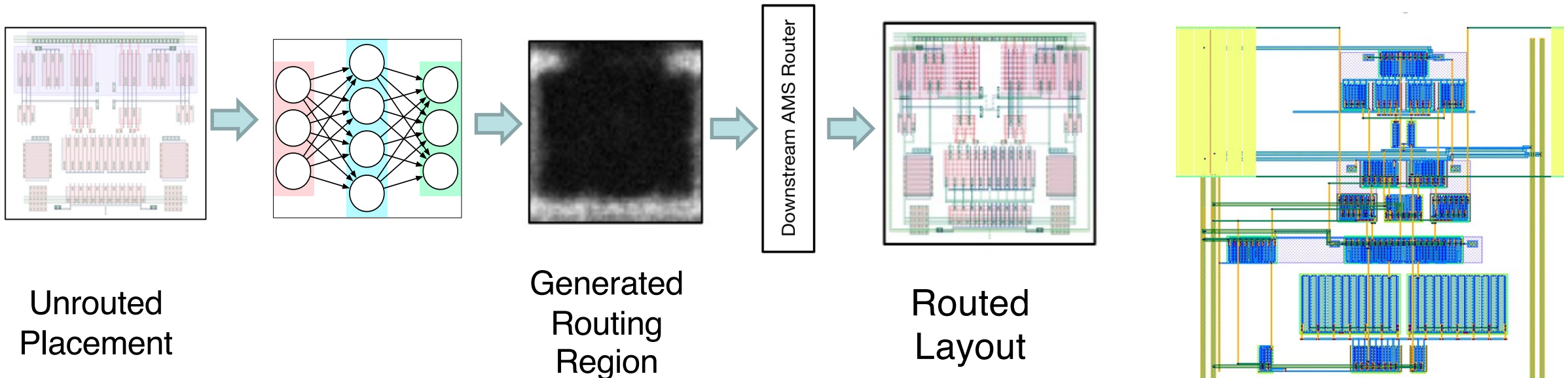
- ◆ Block-level and system-level symmetry
- ◆ Signal flow analysis [Xu+, ICCAD'19]
- ◆ Pattern matching [Xu+, 2019]
- ◆ Graph similarity S^3 DET [Liu+, ASPDAC'20]
- ◆ Supervised graph learning [Gao+, ASPDAC'21]
- ◆ Unsupervised graph learning [Chen+, DAC'21]



ML-Guided Analog Routing [Zhu+, ICCAD'19]

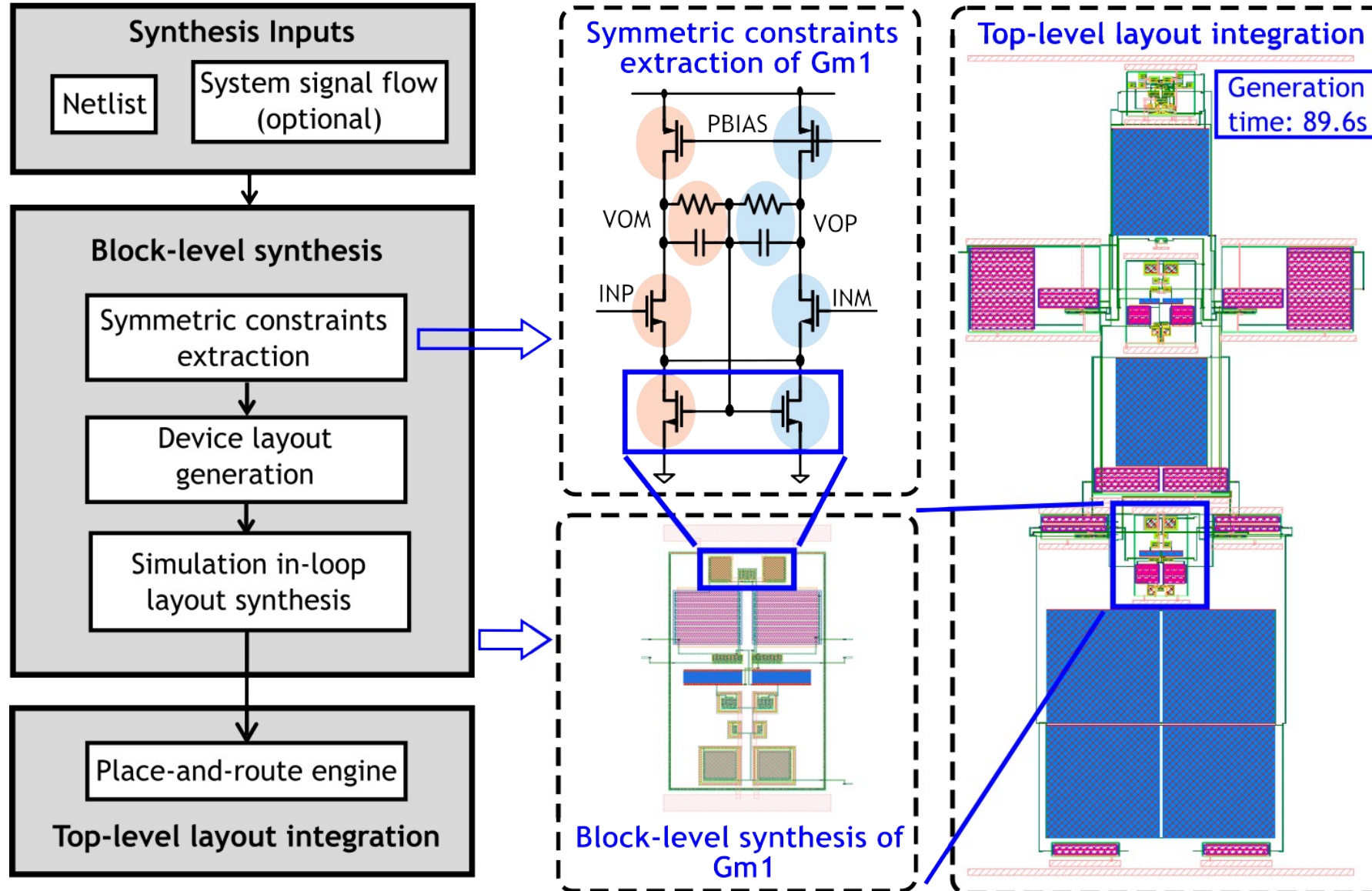
- ◆ Learn from manual layouts
- ◆ Encode designer expertise into neural networks
- ◆ Incorporate ML into automatic routing

	Manual	Baseline	Genius Route
Offset (uV)	480	2530	830
Delay (ps)	170	164	163
Power (uW)	16.98	16.82	16.8

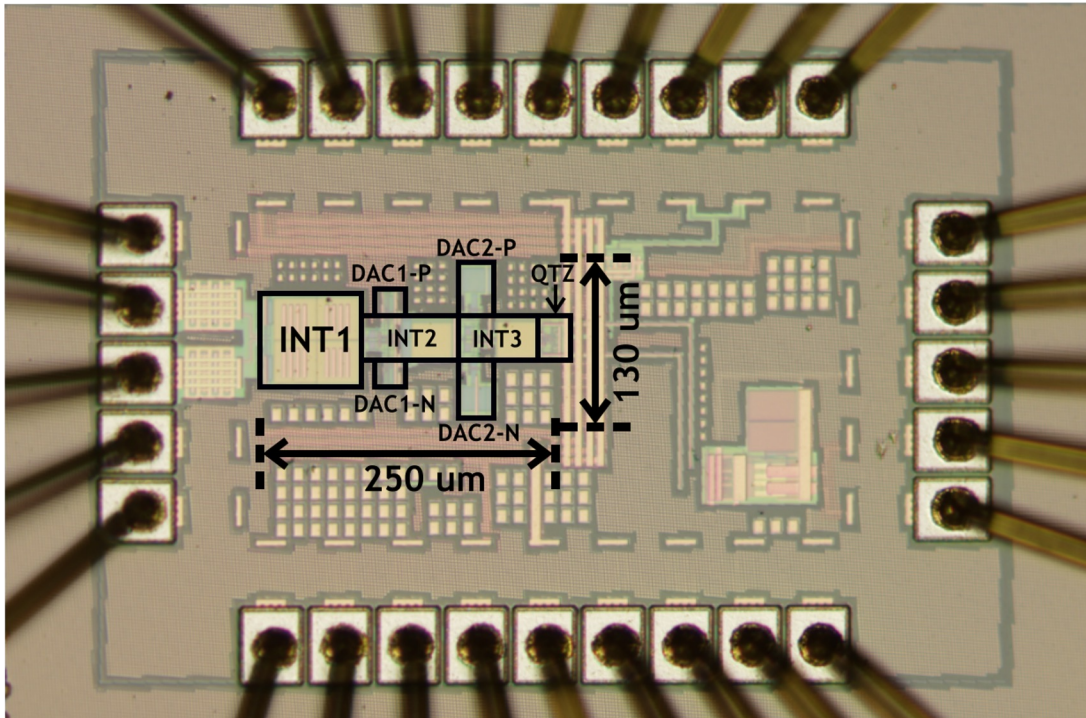


MAGICAL 1.0 Hierarchical Framework [Chen+, CICC'21]

Hierarchical layout synthesis framework



- ◆ 1GS/s 3rd-order high-performance continuous time $\Delta\Sigma$ modulator



- ◆ MAGICAL 1.0 layout outperforms manual layout (SSCL'20) in terms of power, performance, and area
- ◆ MAGICAL O(min) vs. Manual O(month)
- ◆ Comparable results with other SOTA CTDSM ADCs

Core: 22,000 μm^2

Chip: 800 μm x 550 μm

TSMC 40nm

Open Research Directions

- ◆ How to obtain generalized analog constraints?
- ◆ How to generalize to very diverse analog circuits?
- ◆ Supervised learning vs. unsupervised learning
- ◆ Reinforcement learning
- ◆ Go beyond GNN
- ◆ Using layout feedbacks to improve constraint generation
- ◆ ...