Challenges for Automating Package Routing

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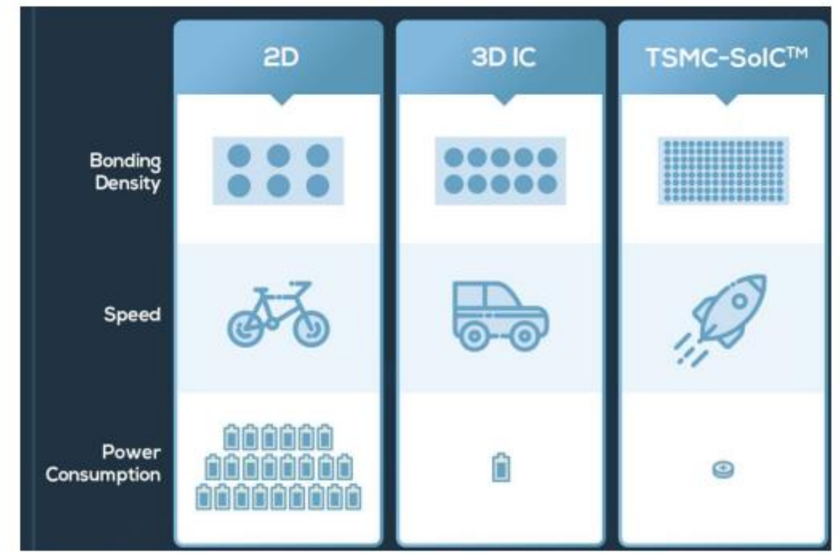
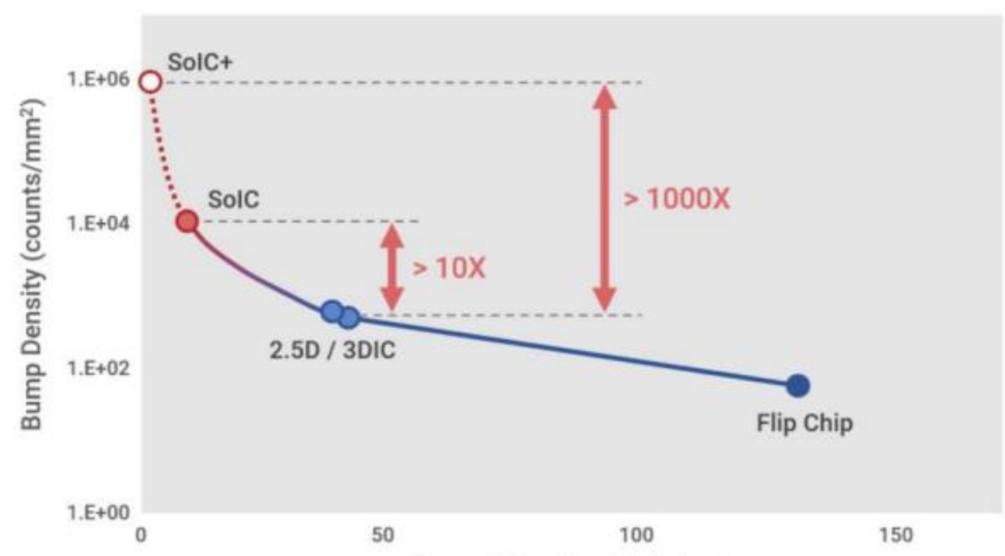
Introduction to Fully Automatic Package Routing

- Typically done manually or semi-automatically
- Important and laborious component of 3D-IC implementation flow
- The size of package designs is rapidly increasing, with complex routing rules, requiring fully-automatic package routing solution.
  - Past: hundreds of nets
  - Now: ten thousands of nets
  - Future: millions of nets ?

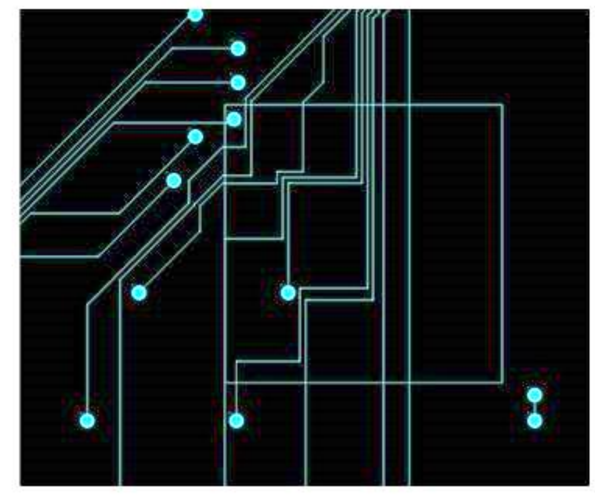




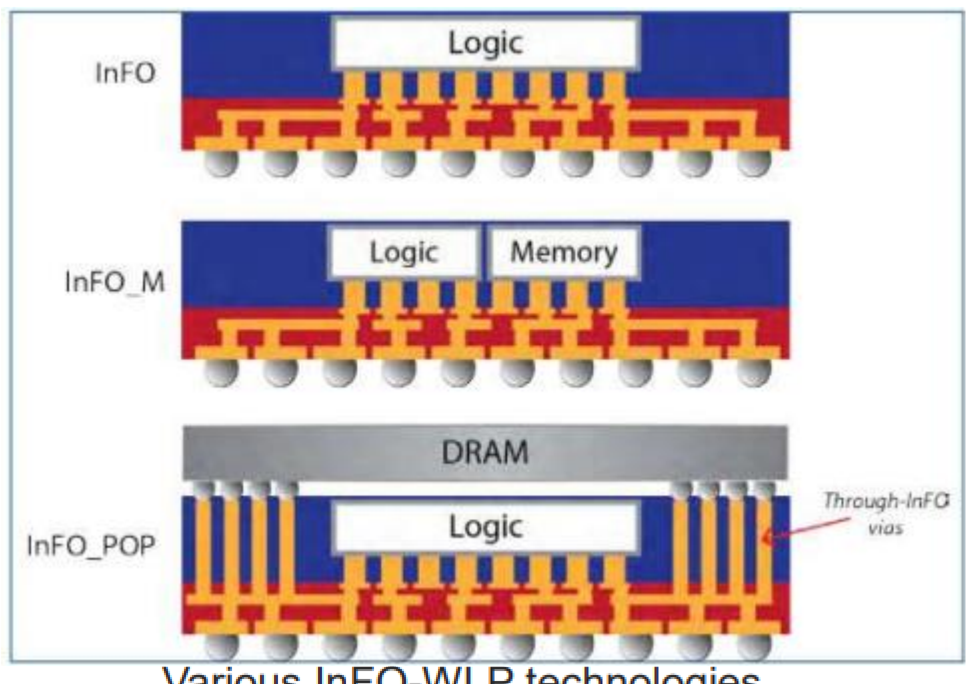
Source: TSMC publication on System on Integrated Chips

Package Routing Problem

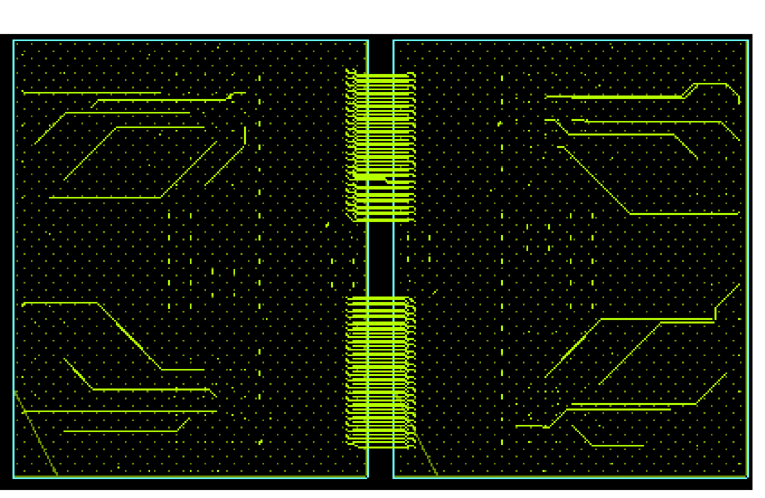
- Gridless routing (i.e., no routing tracks)
- Routing direction: Any-angle, octagonal, orthogonal, or hybrid
- Multiple routing layers, but layer switching is non-preferred
- Supporting many different design styles



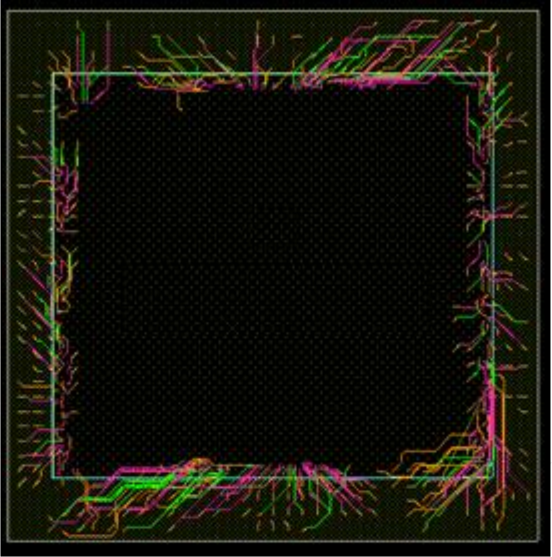
Routing direction control



Various InFO-WLP technologies
Source semiwiki.com



Die-to-die style



fanout style

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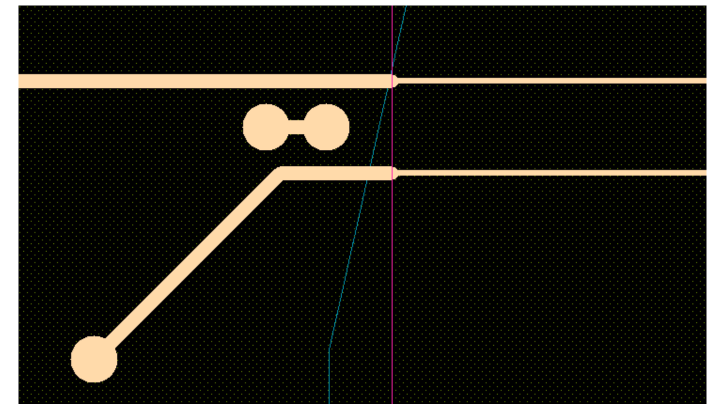
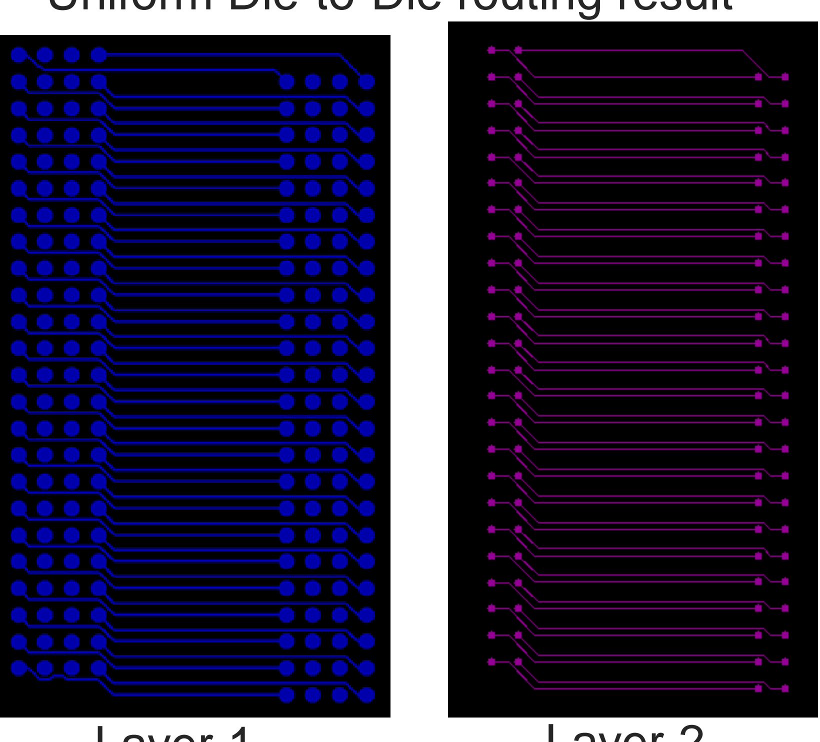
Package Routing Challenges

- Uniform Die-to-Die routing
- Supporting various shielding styles
- Complex non-default rules

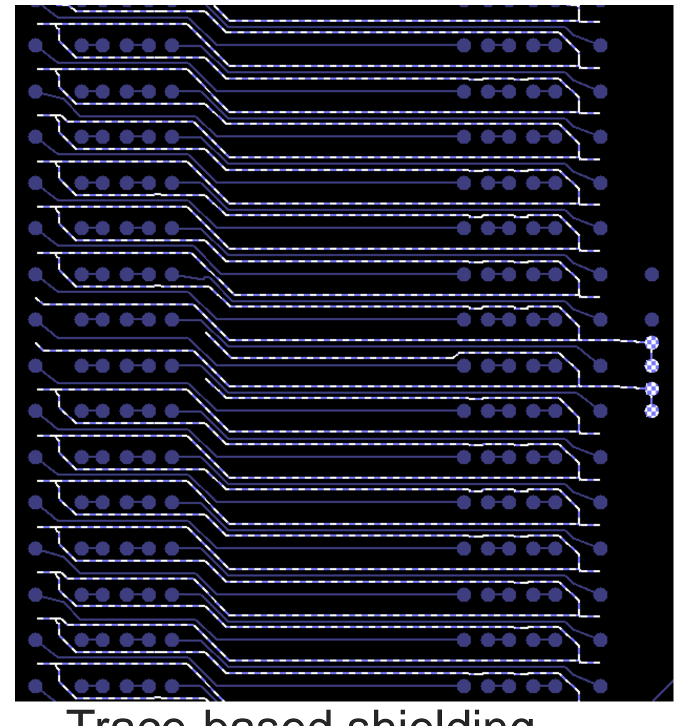


Wire width and spacing may vary for different nets in different regions

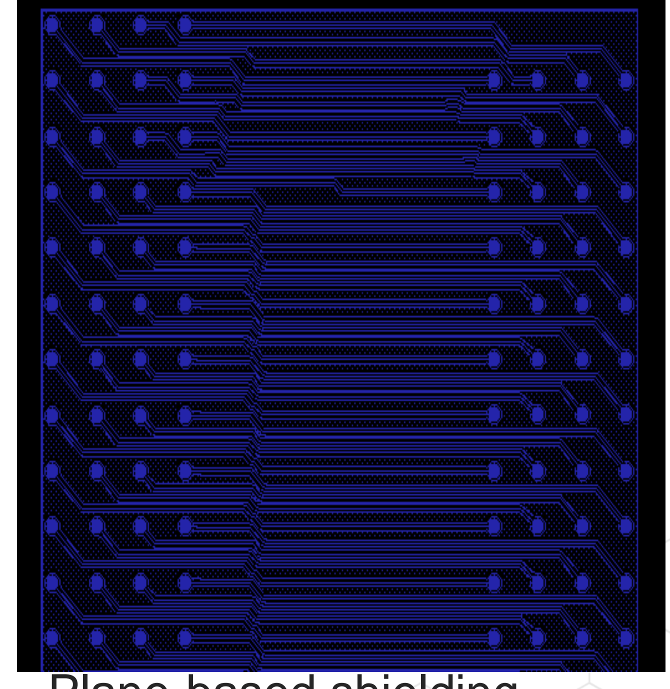
Uniform Die-to-Die routing result



Layer 1 Layer 2



Trace-based shielding



Plane-based shielding

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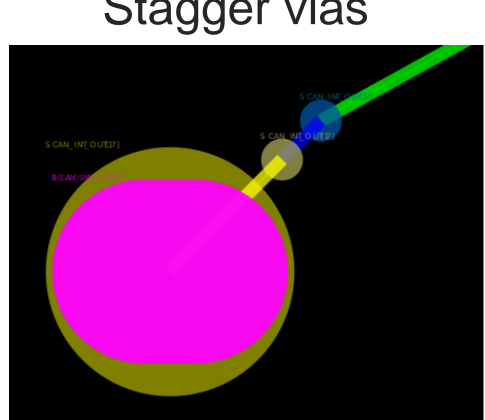
Package Routing Challenges

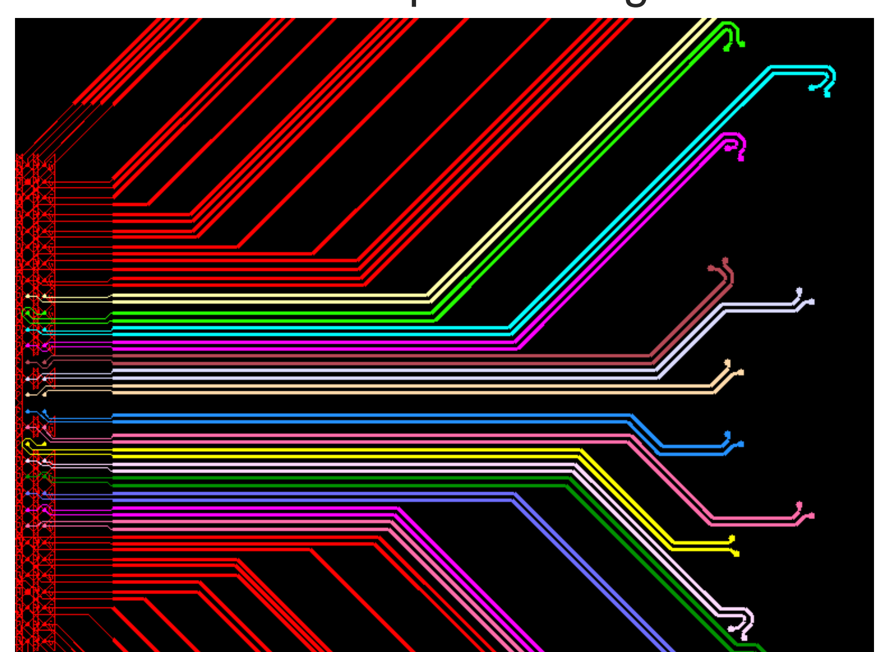
- Complex via stacking rules
- Differential-pair routing / bus routing
- Teardrop connections for yield concerns
- Multithreading for large-scale designs

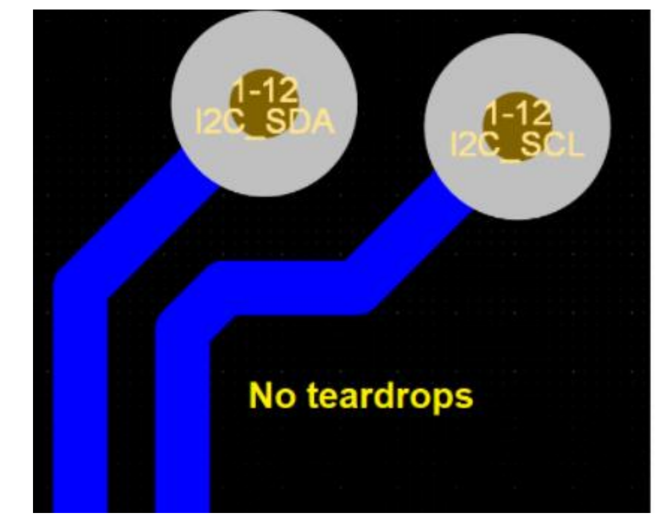
Stacking vias

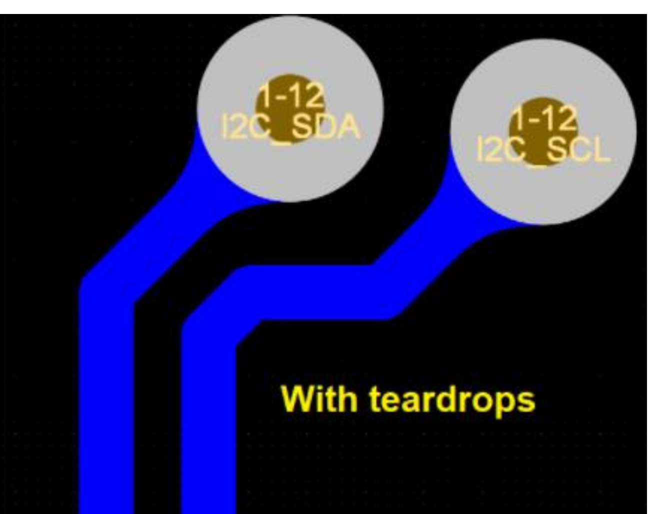
Stagger vias



Differential-pair routing







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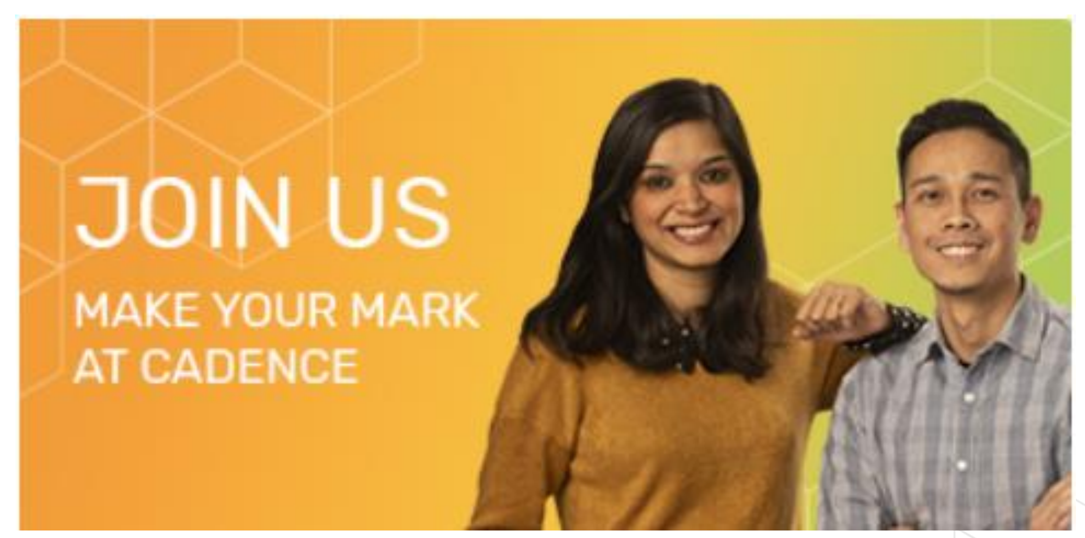
Takeaway

- Fully-Auto solution is a requirement for advanced package routing
- Cadence has world class 3D-IC solution ”Integrity”. Fully-automatic package routing engine is a key component in 3D-IC solution.
  - https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/3dicinteg
- Cadence is hiring. If you are interested to address the modern 3D-IC challenges, please email me.
  - Wen-Hao Liu (whliu@cadence.com)



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