Analog Synthesis – The Deterministic Way

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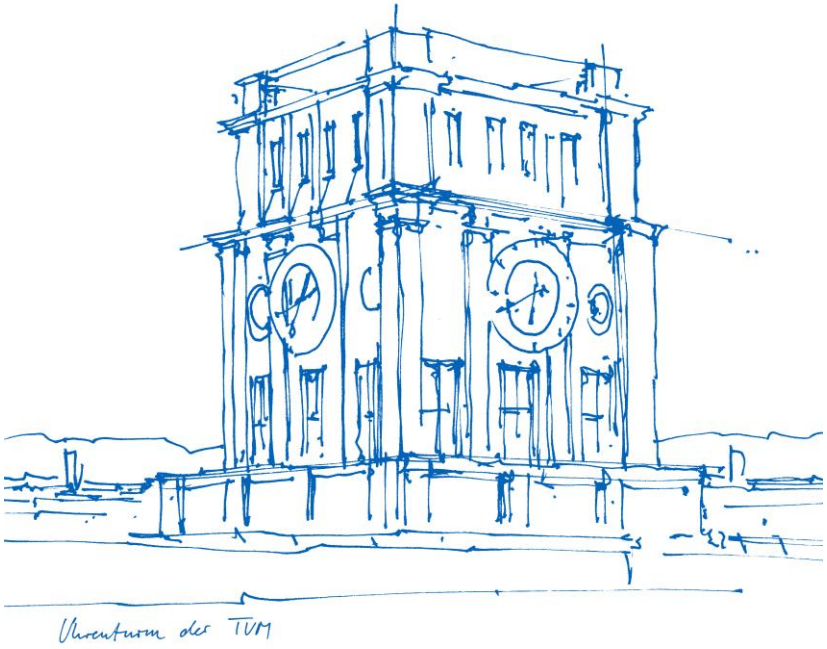
ISPD‘22 - invited

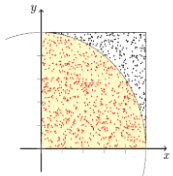


Two Main Issues in Analog Design

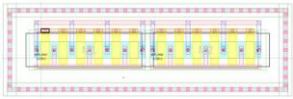
- Circuit simulation is extremely expensive
  - Several minutes for one simulation, e.g., ~5 min per simulation → ~80 hours per 1000 simulations
- Design knowledge is ubiquitous (physics!) and implicit
  - Symmetry, matching, transistor operating region, alignment, common centroid, …
- How many simulations does a design tool need?
- How comprehensively and fast are constraints set up?

Analog EDA Types of Focus

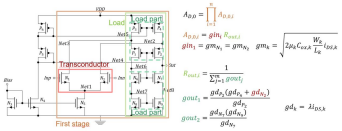
- Statistical focus („machine learning“)
  - Learning inherent in algorithm
  - Learned knowledge stays hidden (brain -> neural net)
  - Huge simulation cost (natural evolution)
- Module focus
  - „Silicon compiler“
  - Implementation slow, execution fast
  - Does not scale, low reusability (just one circuit)
- Deterministic focus
  - White-box knowledge in analog cell library
  - Automatic set-up of design objectives/constraints
  - Guided/bounded optimization/construction/enumeration
  - Low simulation cost

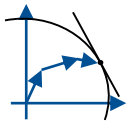


https://de.wikipedia.org/wiki/Monte-Carlo-Simulation#/media/Datei:PI_statistisch.png



© IEEE Elshawy, Dessouky et al. Multi-device layout templates for nanometer analog design, IDG 2014

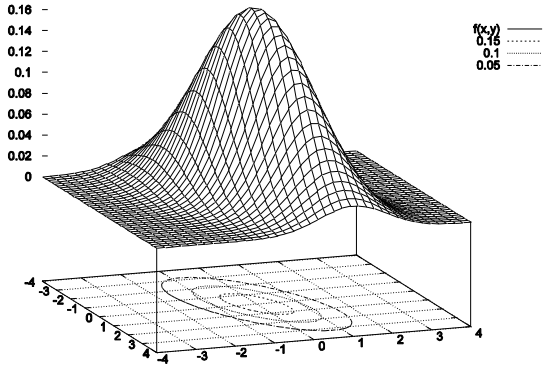


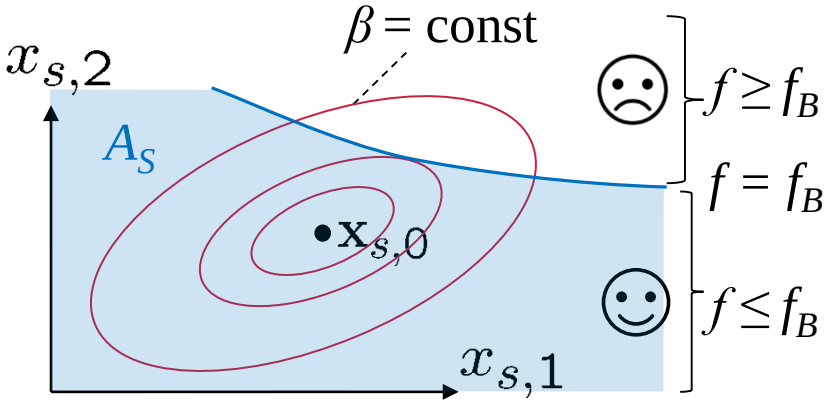


Two Deterministic-Focus Approaches

- Statistical design
- Functional building block library

Statistical Design

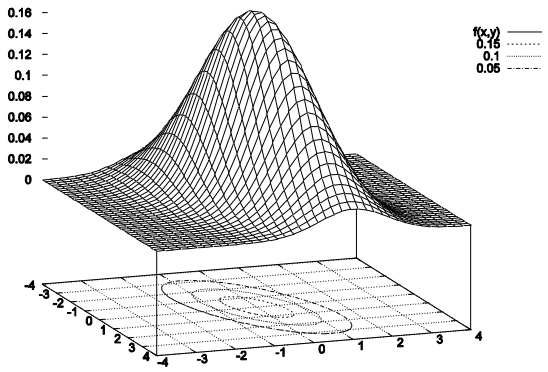


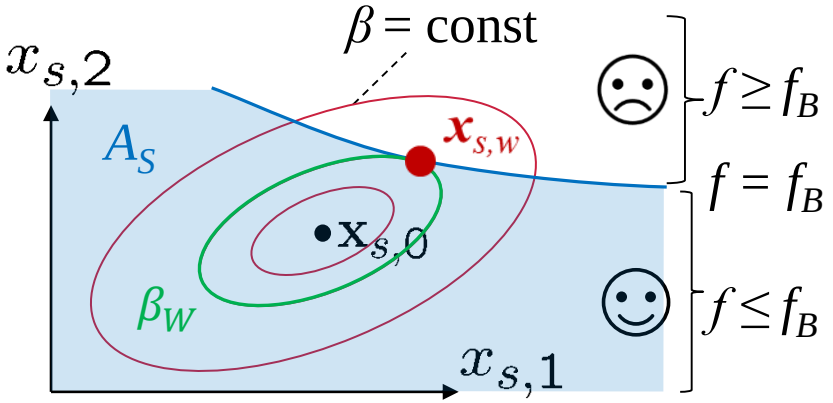


$$pdf(\mathbf{x}_s) = \frac{1}{\sqrt{2\pi}^{nxs}\sqrt{\det \mathbf{C}}} \exp(-\frac{1}{2}\beta^2(\mathbf{x}_s)) \qquad \beta^2(\mathbf{x}_s) = (\mathbf{x}_s - \mathbf{x}_{s,0})^T \mathbf{C}^{-1} (\mathbf{x}_s - \mathbf{x}_{s,0})$$

- Yield Y: percentage of circuits satisfying performance spec
- Integral of probability density *pdf* over acceptance region A_S
- Statistical approach: Monte Carlo analysis
- Huge number of simulations (rare event analysis task)

Deterministic characterization of rare event problem





$$pdf(\mathbf{x}_s) = \frac{1}{\sqrt{2\pi}^{nxs}\sqrt{\det \mathbf{C}}} \exp(-\frac{1}{2}\beta^2(\mathbf{x}_s)) \qquad \beta^2(\mathbf{x}_s) = (\mathbf{x}_s - \mathbf{x}_{s,0})^T \mathbf{C}^{-1} (\mathbf{x}_s - \mathbf{x}_{s,0})$$

- Point of highest probability (density) to violate the spec
- Nonlinear optimization problem
- Immediate yield value: $Y' = \int_{-\infty}^{\beta_W} (1/\sqrt{2\pi}) exp(-t^2/2) dt$
- Gradient for optimization, tool

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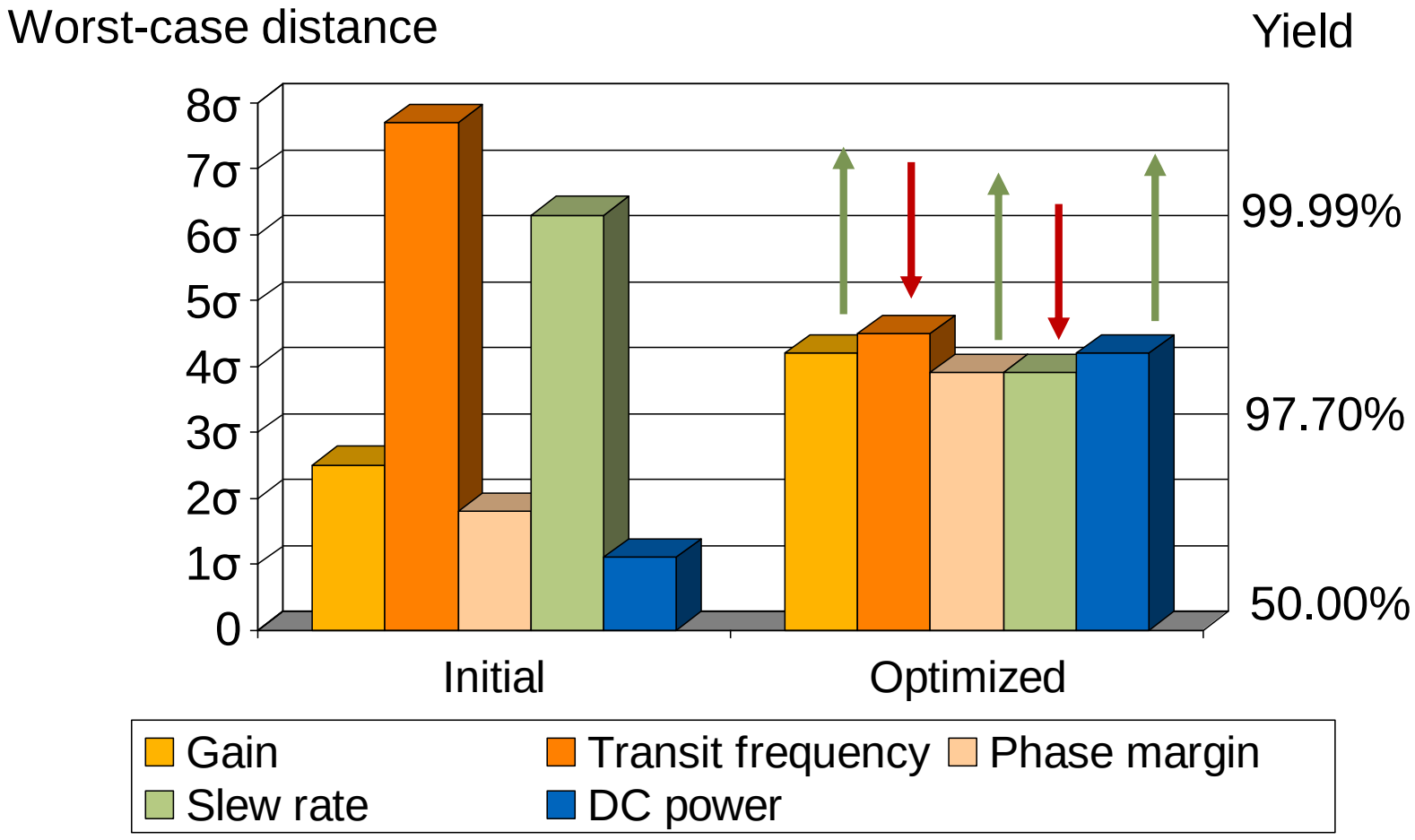
Design Centering



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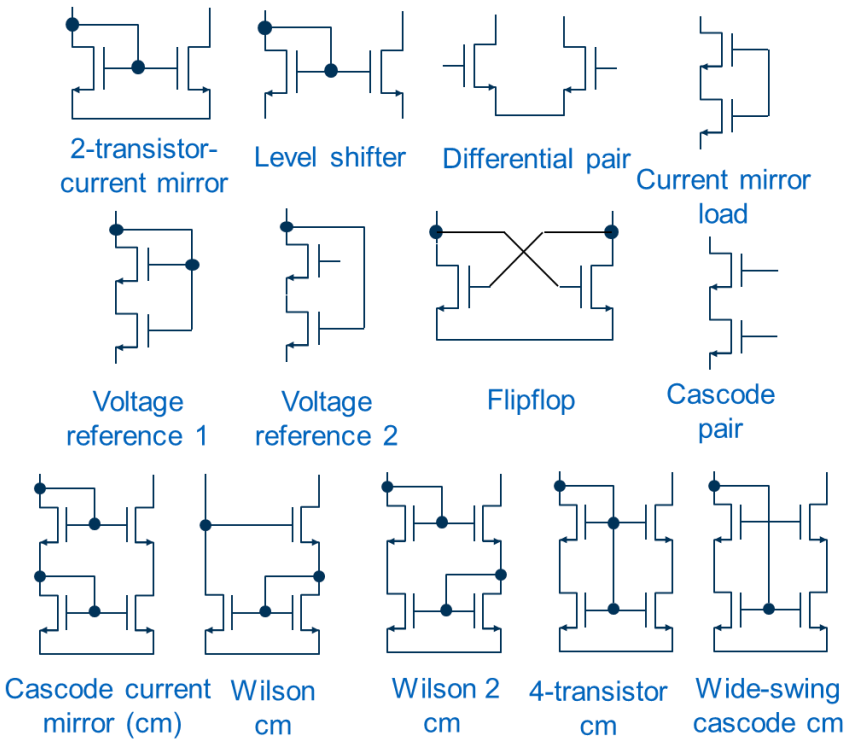
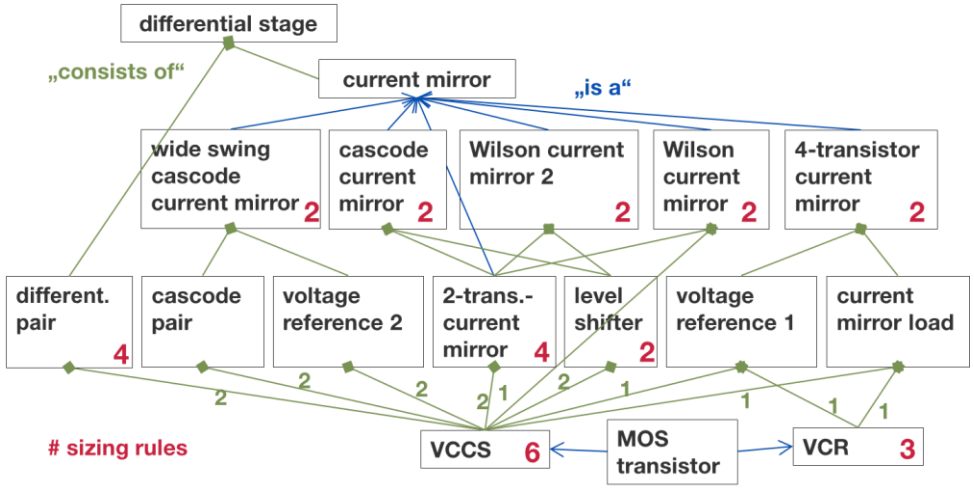
Two Deterministic-Focus Approaches

- Statistical design
- Functional building block library

Structural Block Library

- Basic current mirrors, differential stage, sizing constraints
- Automatic netlist analysis (subgraph isomorphism search)
- Automatic sizing





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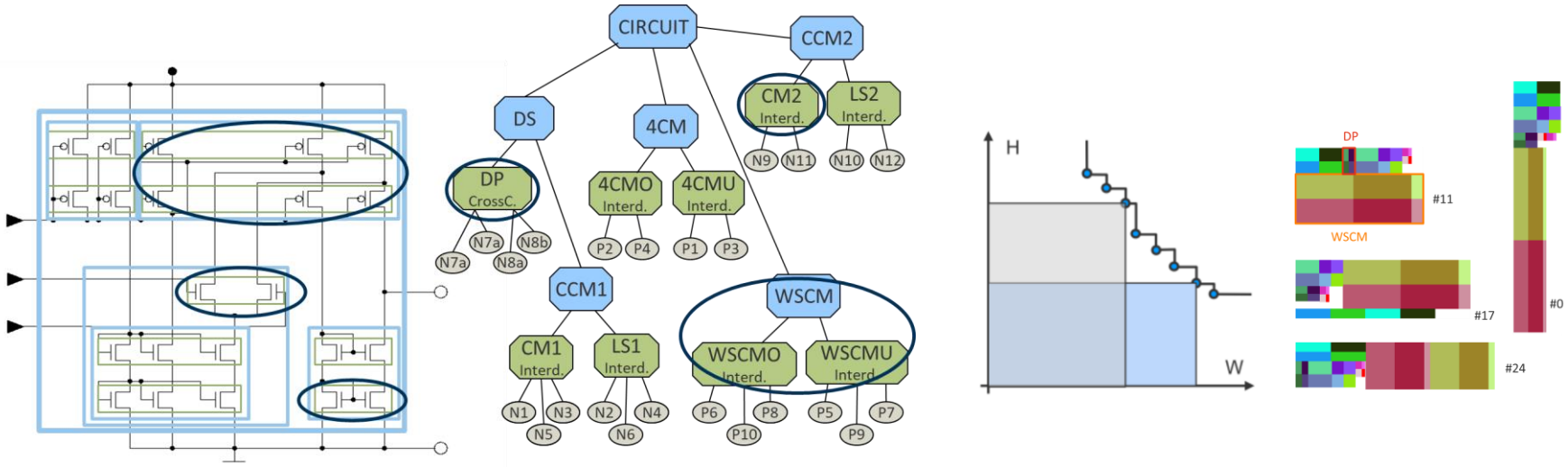
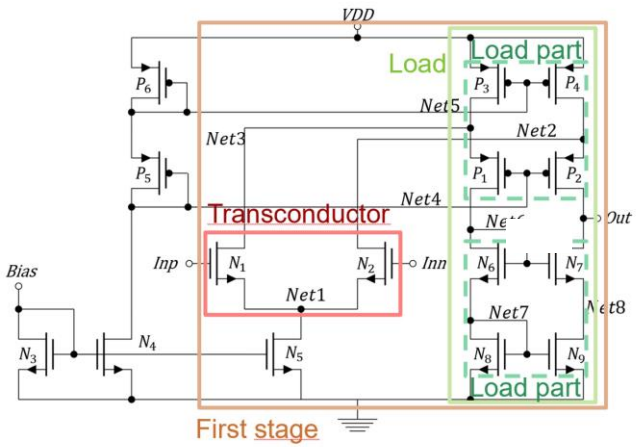
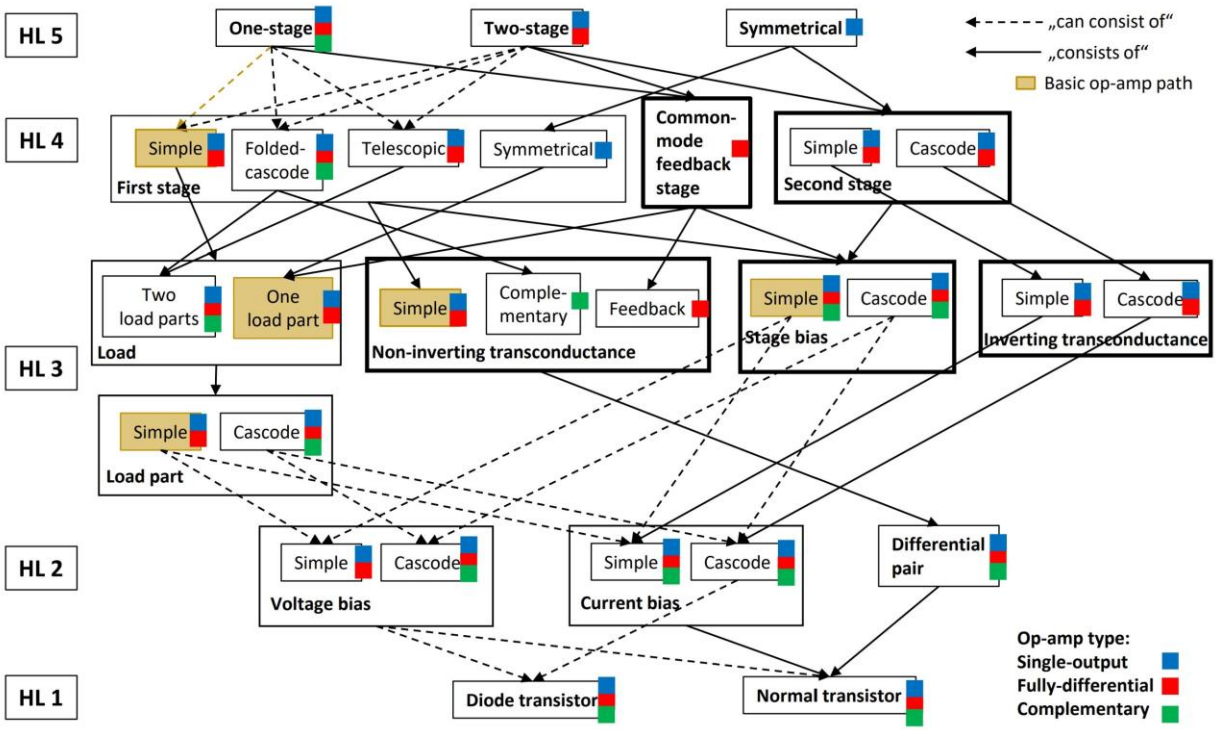
Deterministic Placement Approach



- Automatic placement constraints and placement plan
- Placement enumeration of small transistor groups
- Constraint-compliant vertical and horizontal merging of B*-trees bottom-up according to hierarchical placement plan
- B*-tree → horizontal/vertical constraint graph → ILP → x-/y-coordinates

Functional Block Library for Opamp Design





- Functional block ←→ structural block == one ←→ many
- Initial sizing by interlinkable hierarchical equations
- Structural synthesis

Conclusion: Do‘s and Don‘ts for Analog EDA

- Don‘t hide analog design knowledge in (human or machine) neural networks
- Don‘t code the design of every analog circuit type from scratch

- Do capture the design knowledge of small building blocks with disseminator capacity in analog cell libraries
- Do tools for library- and netlist-driven automatic set up of constraints and objectives
- Do design tools based on guided optimization, construction and bounded enumeration

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Structural Synthesis

Specification of performance constraints and opamp type

Specs #	1	2	3	4	5	6	7
Op-amp type	Single-output			Fully-differential		Complementary	
Bias current (μA)	10	100	10	100	100	100	100
Load Capacitance (pF)	20	20	20	20	20	20	20
Supply voltage (V)	5	5	5	5	5	5	5
Gate-area ($10^3 \mu m^2$)	≤ 15	≤ 5	≤ 5	≤ 50	≤ 20	≤ 15	≤ 5
Quiescent power (mW)	≤ 15	≤ 8	≤ 5	≤ 25	≤ 15	≤ 10	≤ 5
Phase Margin (°)	≥ 60	≥ 60	≥ 80	≥ 60	≥ 60	≥ 60	≥ 60
CMRR (dB)	≥ 70	≥ 70	≥ 70	≥ 80	≥ 80	≥ 80	≥ 80
CMIR (V)	2-3	1.5-3.5	1.5-3.5	2-3	2-3	-	-
Open-loop gain (dB)	≥ 80	≥ 70	≥ 45	≥ 70	≥ 60	≥ 70	≥ 70
Unity-gain bandwidth (MHz)	≥ 2.5	≥ 10	≥ 10	≥ 2.5	≥ 10	≥ 2.5	≥ 10
Slew rate ($\frac{V}{\mu s}$)	≥ 3.5	≥ 20	≥ 20	≥ 3.5	≥ 15	≥ 3.5	≥ 15
Output voltage swing (V)	1.5-3.5	1.5-3.5	1-4	2-3	1.5-3.5	1.5-3.5	1-4

*

Topology type

 # Topologies

First stage type	simple a_s		folded-cascode a_{fc}		telescopic a_{tel}		symmetrical a_{sym}	# topologies fulfilling
# stages	1	2	1	2	1	2	-	*Specs* / all topologies)
Specs 1	0	40	30	68	30	0	60	228 / 2940
Specs 2	0	5	18	0	20	0	28	71 /2940
Specs 3	24	0	0	0	3	0	27	54 /2940
Specs 4	0	0	11	22	1	0	-	34 / 936
Specs 5	0	0	2	0	0	0	-	2 / 936
Specs 6	-	-	10	-	-	0	-	10 / 36
Specs 7	-	-	6	-	-	-	-	6 / 36

e.g., more stages only considered if these* performances good enough

Specs fulfilled

Search space