Analog/Mixed-Signal Layout Optimization using Optimal Well Taps

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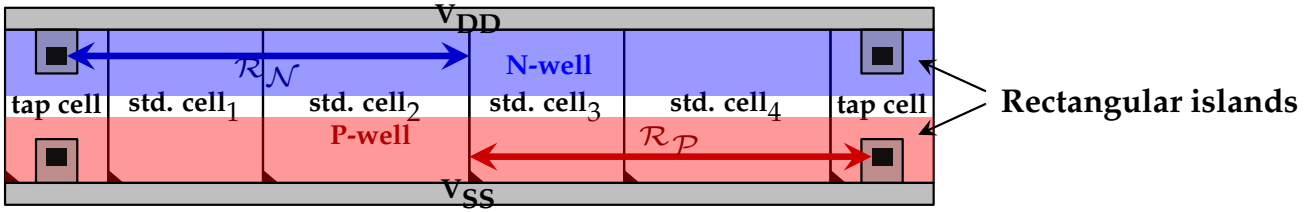
[*]Intel Labs, Hillsboro, OR, USA.

Overview

DEFINITIONS AND MOTIVATING EXAMPLE

Abstract digital layout: Rectangular well islands



- Well layers – channel types in MOSFET devices
- Well island – continuous region of the same well layer

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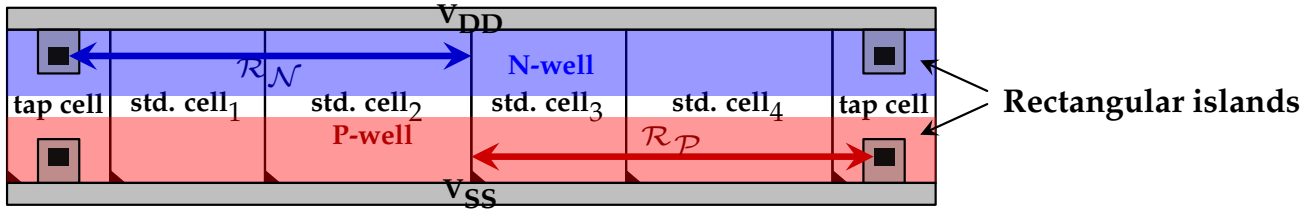
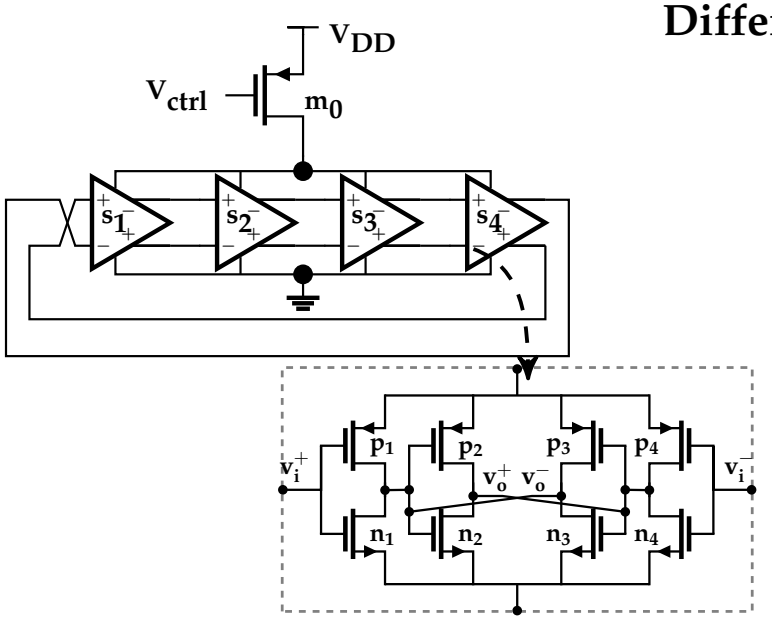
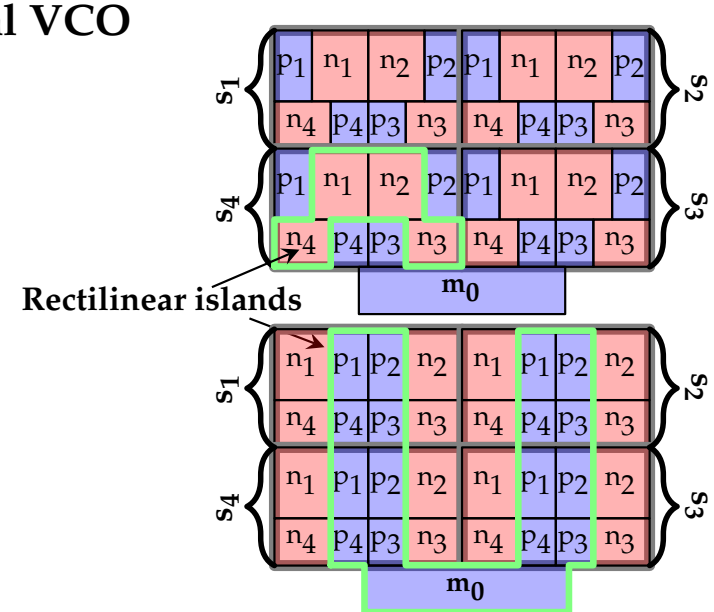


- Well layers – channel types in MOSFET devices
- Well island – continuous region of the same well layer

Analog/Mixed-Signal (AMS) circuits : Rectilinear well islands.

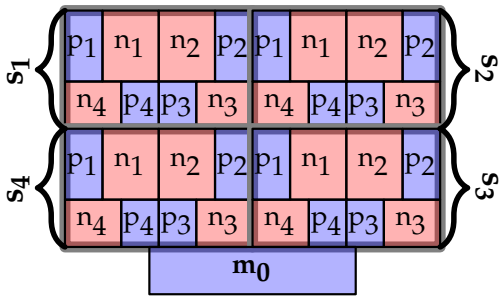
Differential VCO





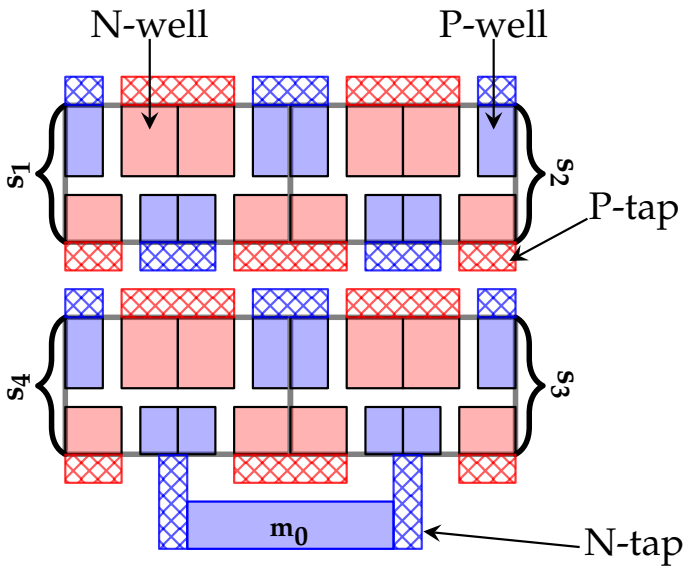
VCO LAYOUTS WITH WELL ISLANDS AND WELL TAPS

After placement:



After well island and well tap insertion:

$> 2\times$ area



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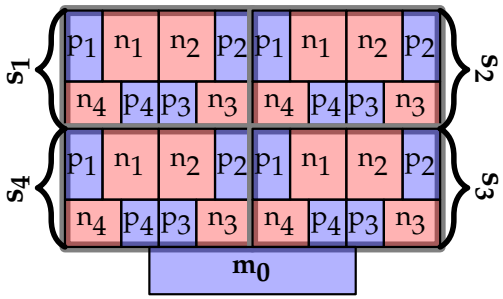

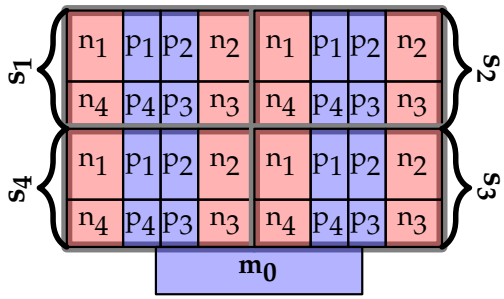

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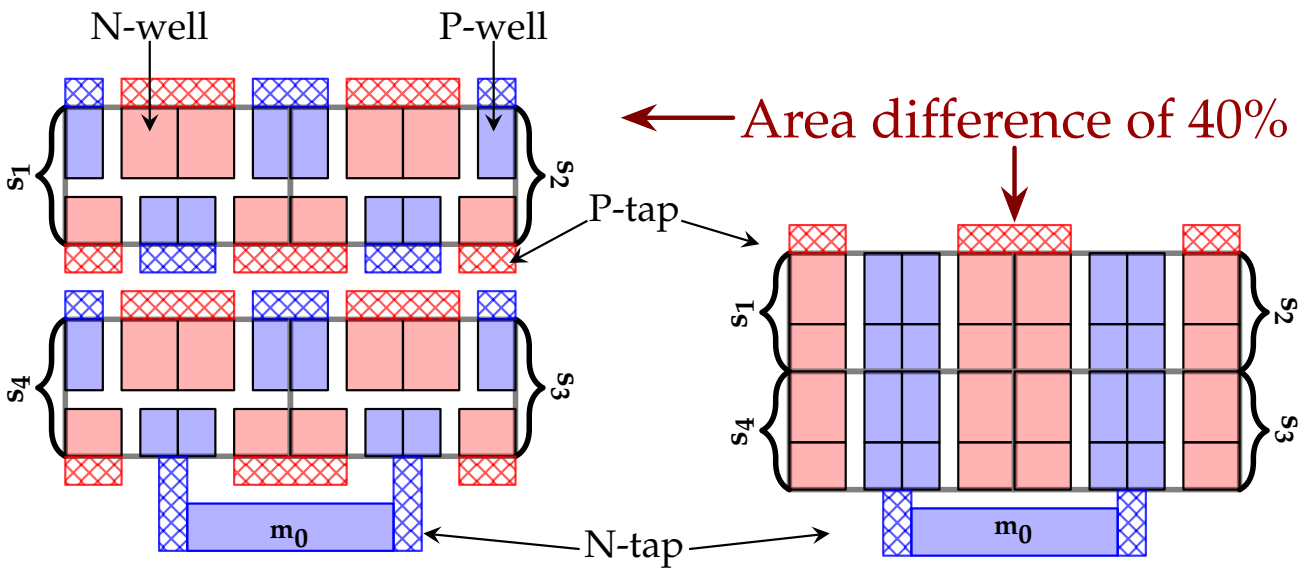
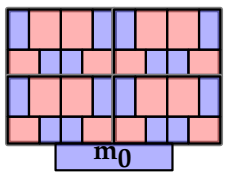


EXISTING TECHNIQUES

- Geometric operations
  [COHN, J., ET AL., JSSC'91]
- Generative Adversarial Networks (GANs) [XU, B., ET AL. DAC'19]

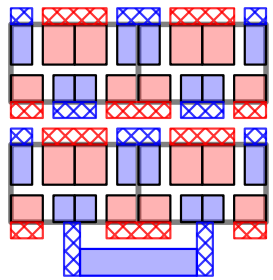


Post placement well island gen.

Input layout

Layout with well islands

Tap insertion



Layout with well islands and taps

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[XU, B., ET AL. DAC'19] – WellGAN: Generative-adversarial-network-guided well generation for analog/mixed-signal circuit layout.

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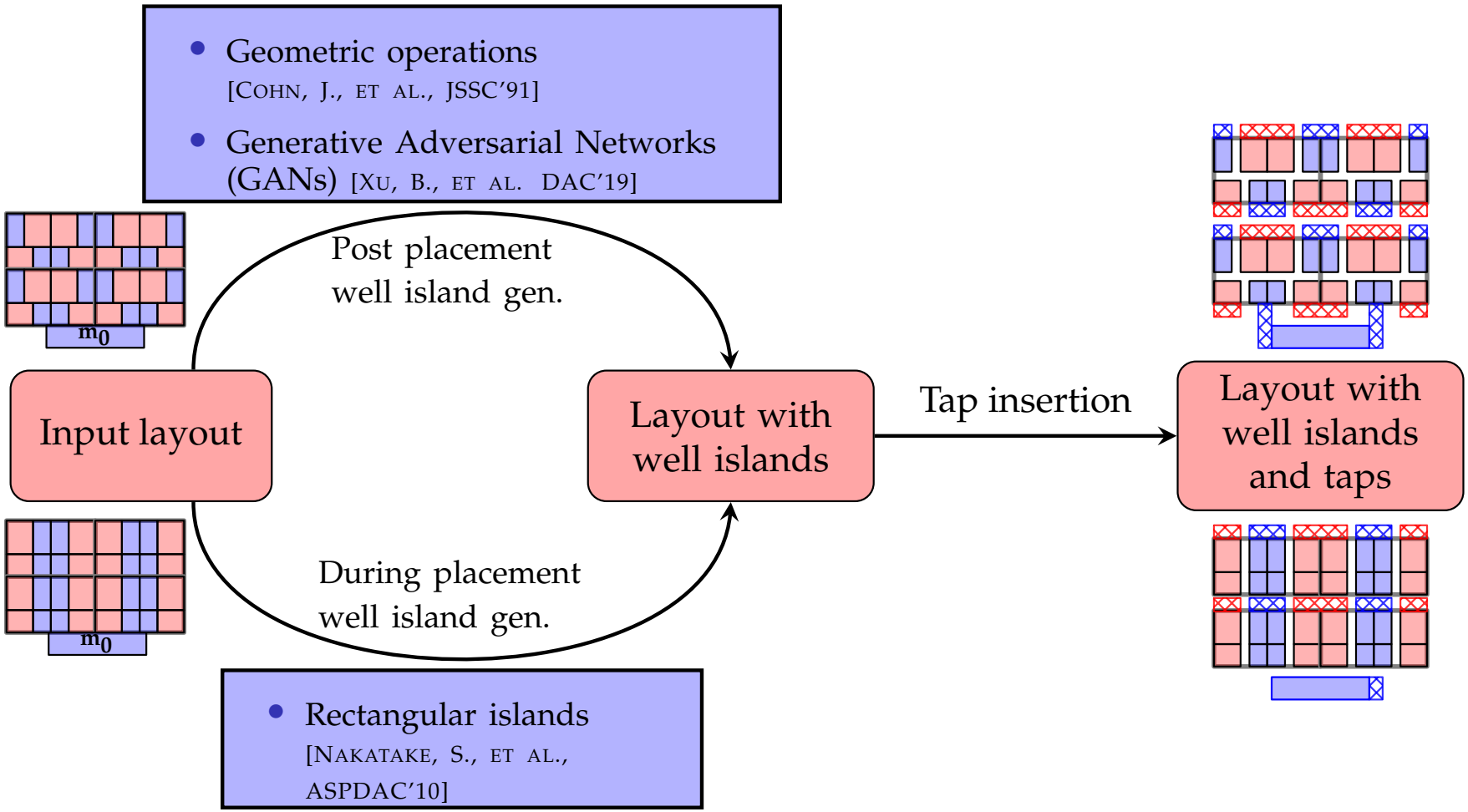

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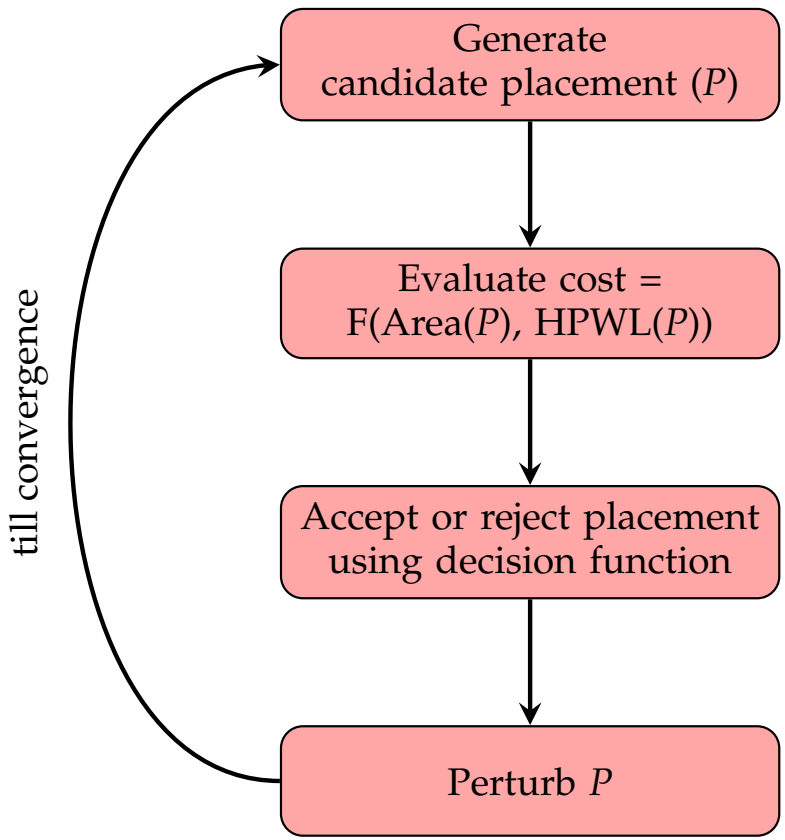
PROPOSED APPROACH

- Mainstream analog and mixed signal placers use stochastic placement algorithms like simulated annealing: [BALASA, F., ET AL., ASPDAC'03], [COHN, J., ET AL., JSSC'91], [KODA, S., ET AL., TCAD'07], [MA, Q., ET AL., TCAD'11]



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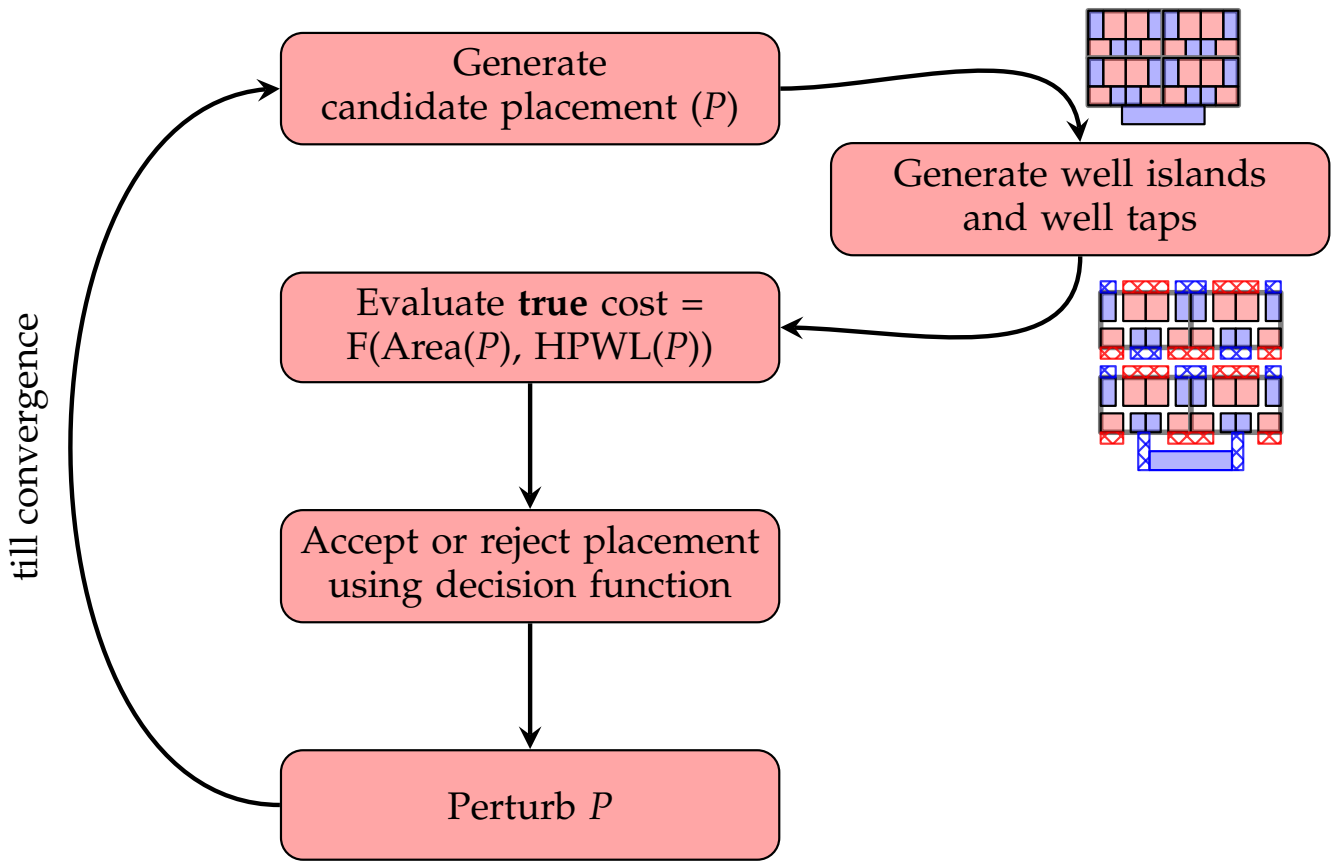

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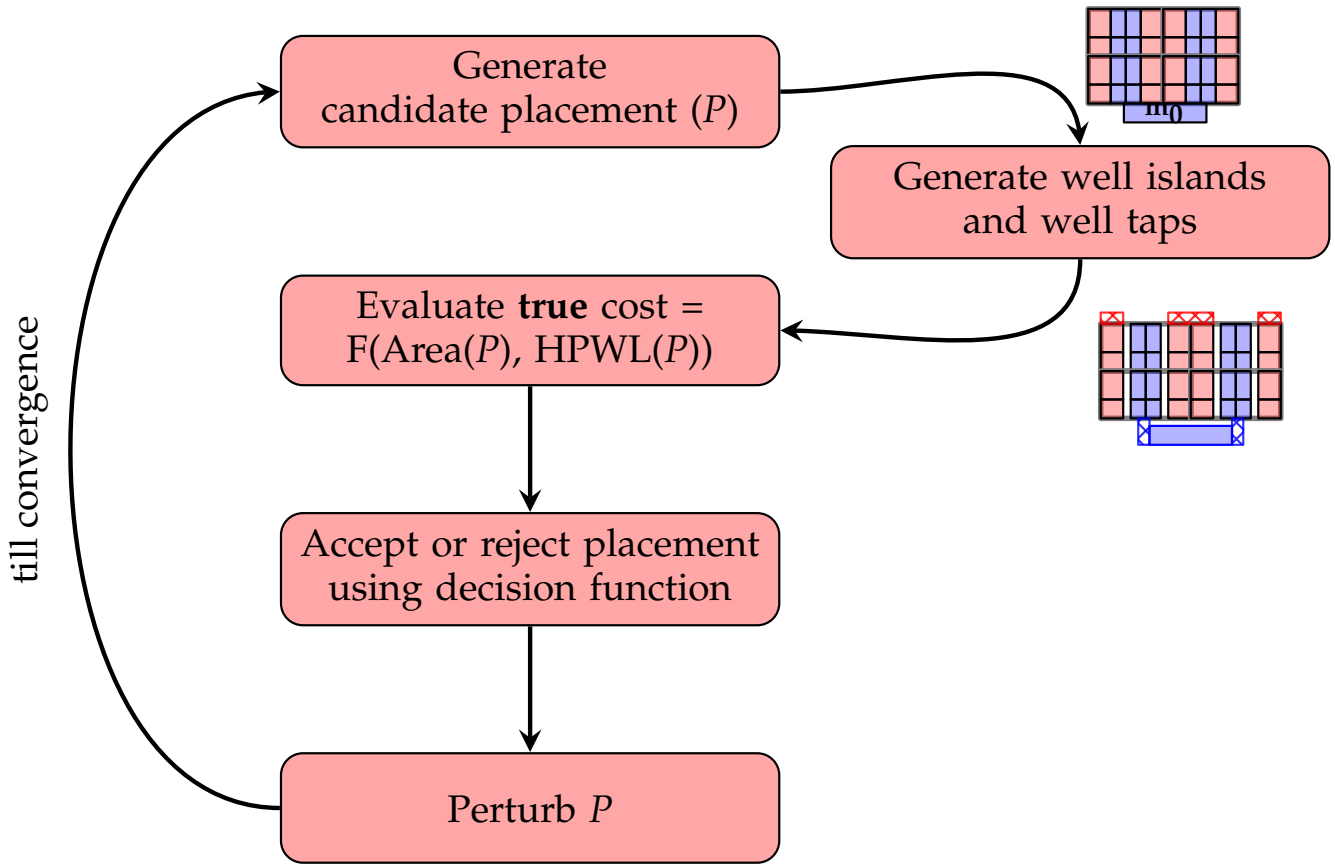

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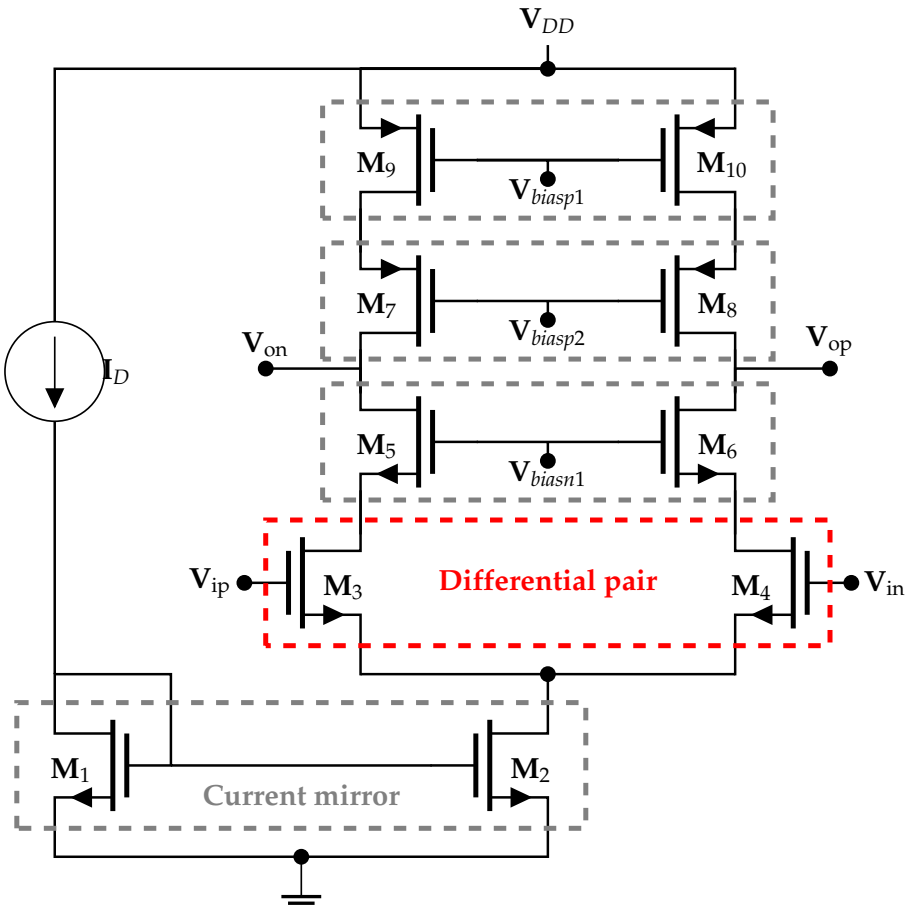
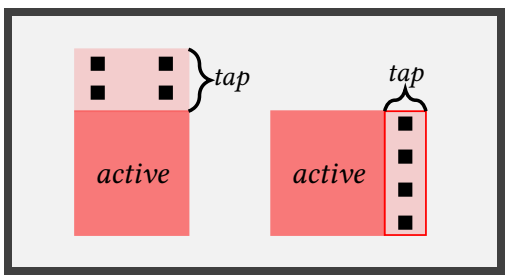
PRIMITIVES AND CELL LAYOUTS [DHAR, T., ET AL., DESIGN & TEST'20]

Telescopic Operational Transconductance Amplifier



M_3-M_4 layout variants

Tapped

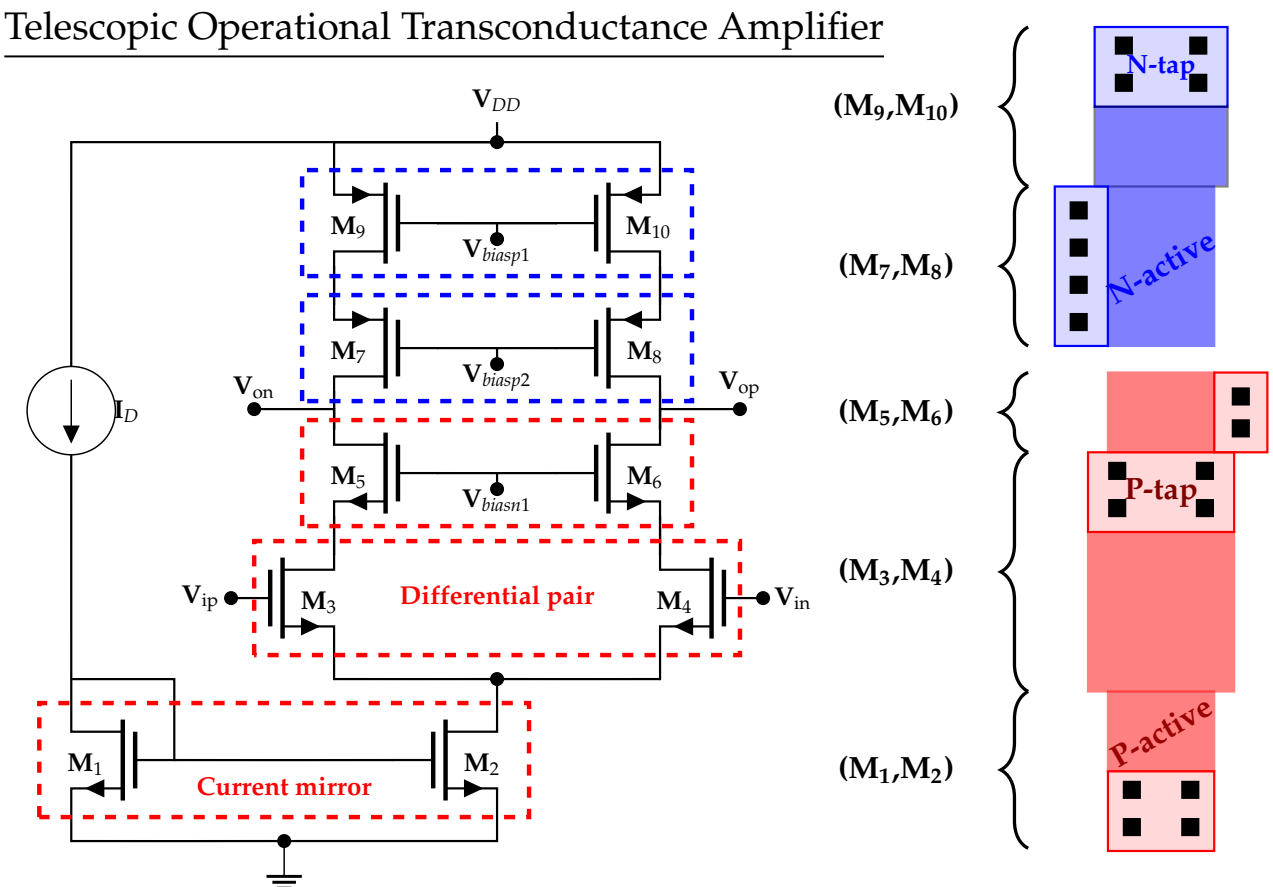


Tapless

[DHAR, T., ET AL., DESIGN & TEST'20] ALIGN: A system for automating analog layout.

REDUNDANT TAP REMOVAL

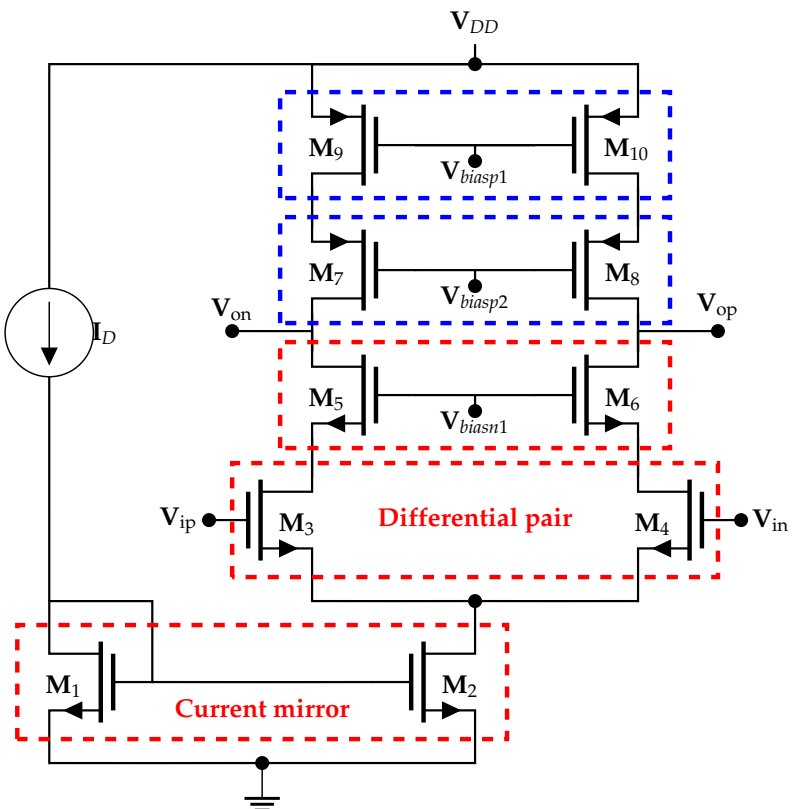
- Candidate input layout with all cells using *tapped* variant.

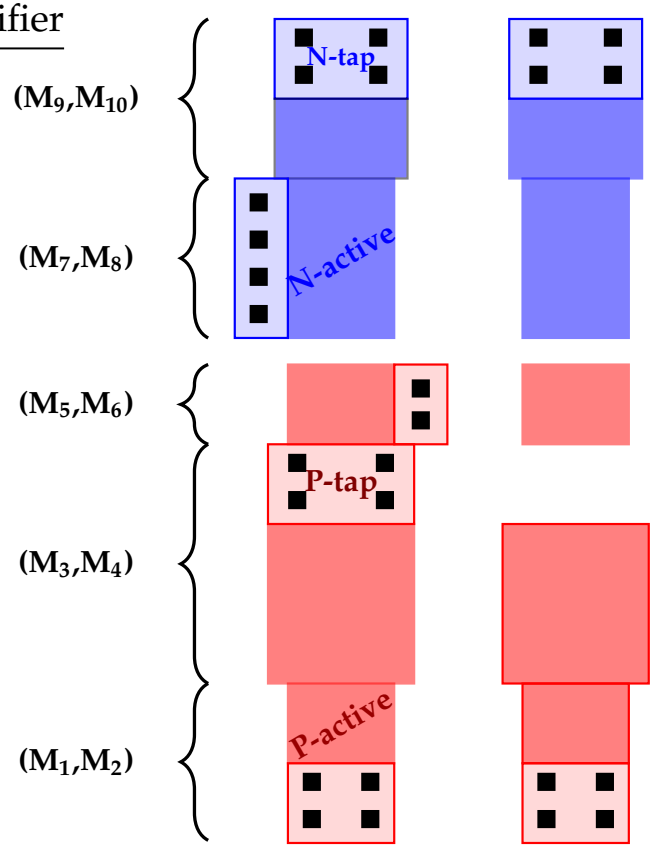


REDUNDANT TAP REMOVAL

- Candidate input layout with all cells using *tapped* variant.
- Detect redundant taps and replace tapped cells with *tapless* variant.

Telescopic Operational Transconductance Amplifier

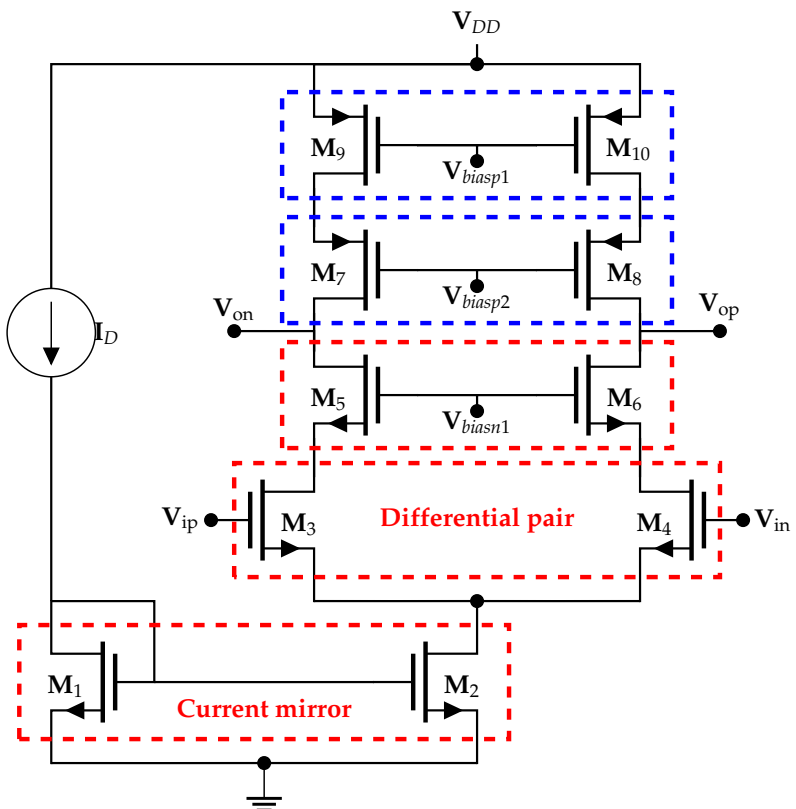


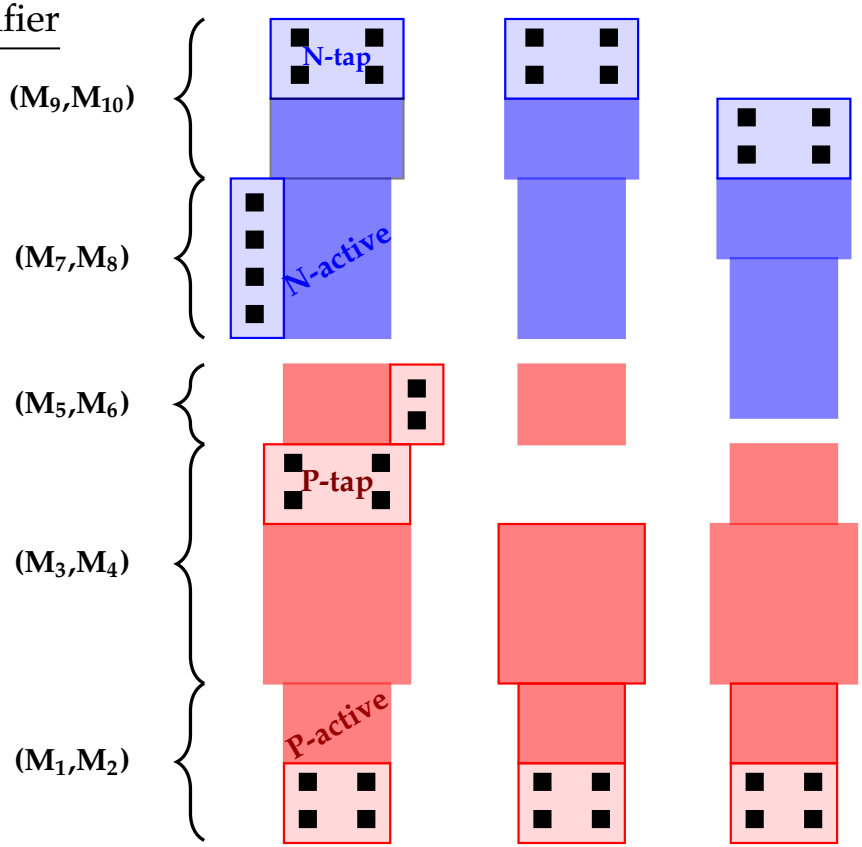


REDUNDANT TAP REMOVAL

- Candidate input layout with all cells using *tapped* variant.
- Detect redundant taps and replace tapped cells with *tapless* variant.
- Compact layout.

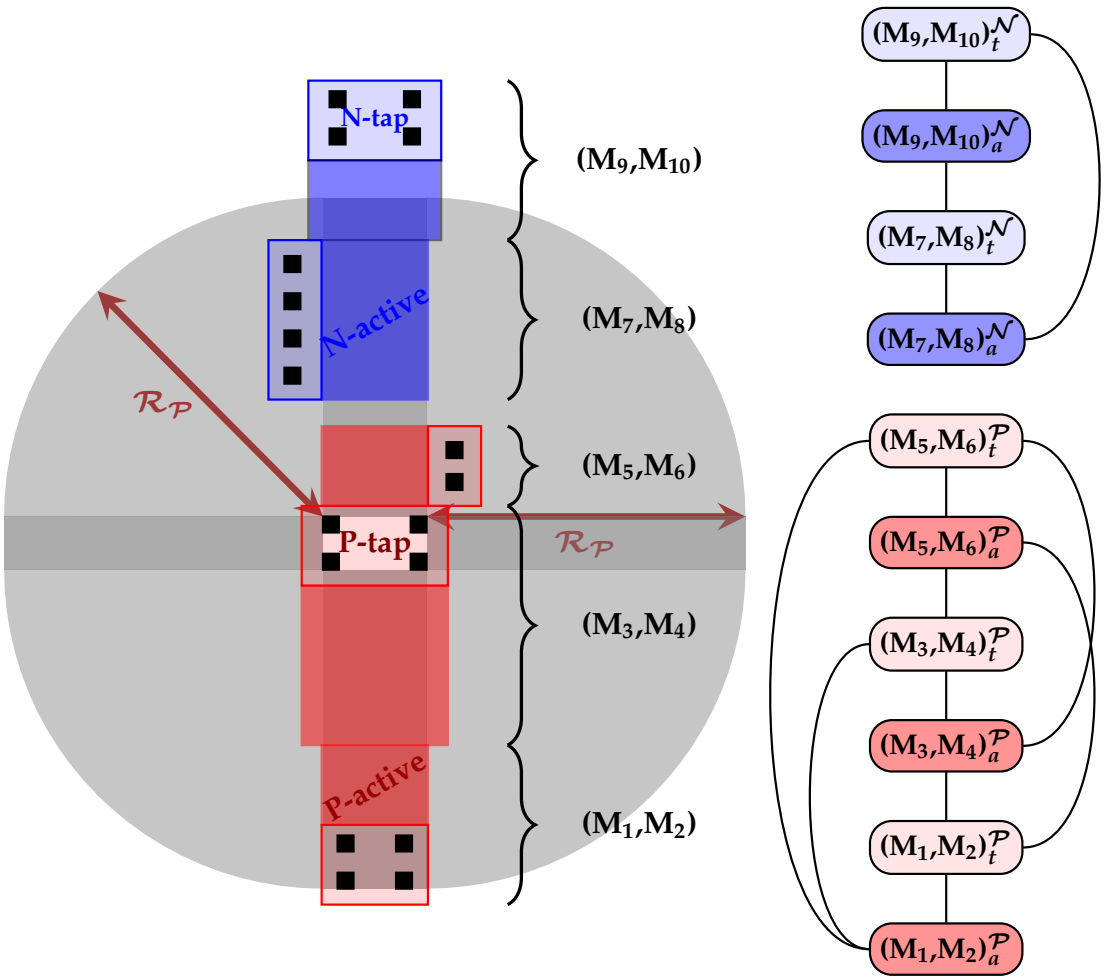
Telescopic Operational Transconductance Amplifier





WELL TAP GRAPH

Well tap graph



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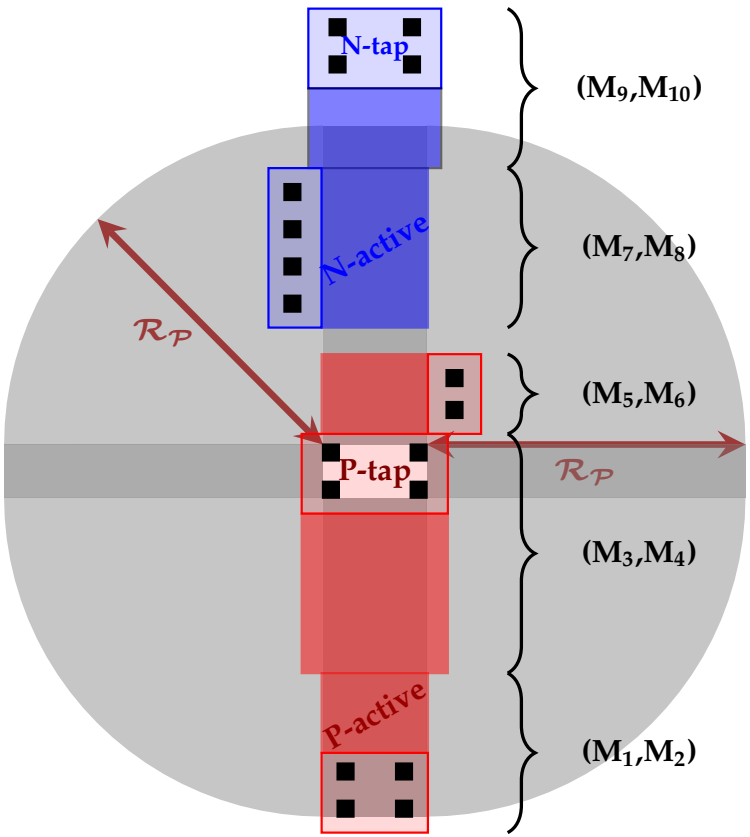

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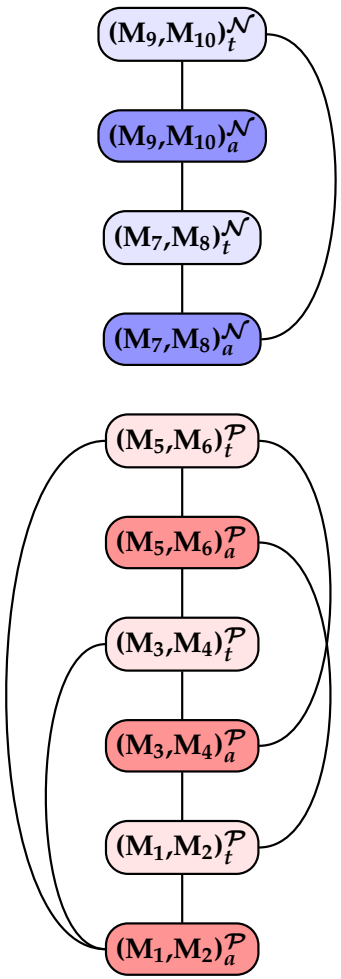
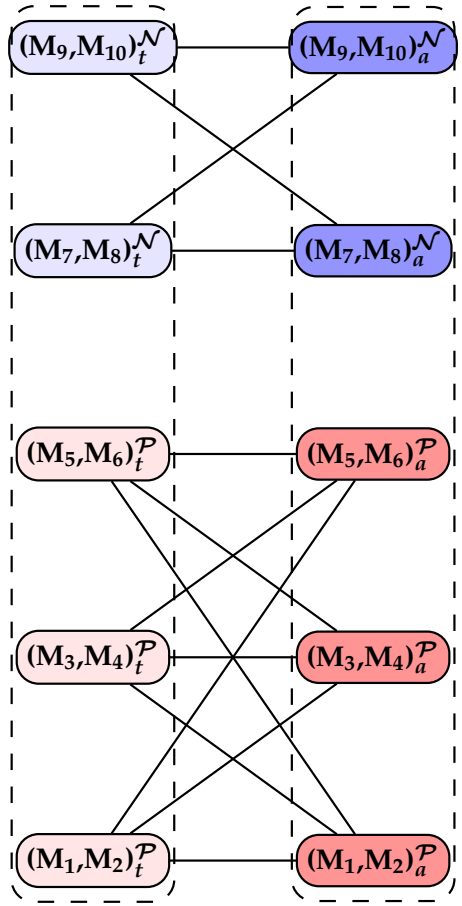
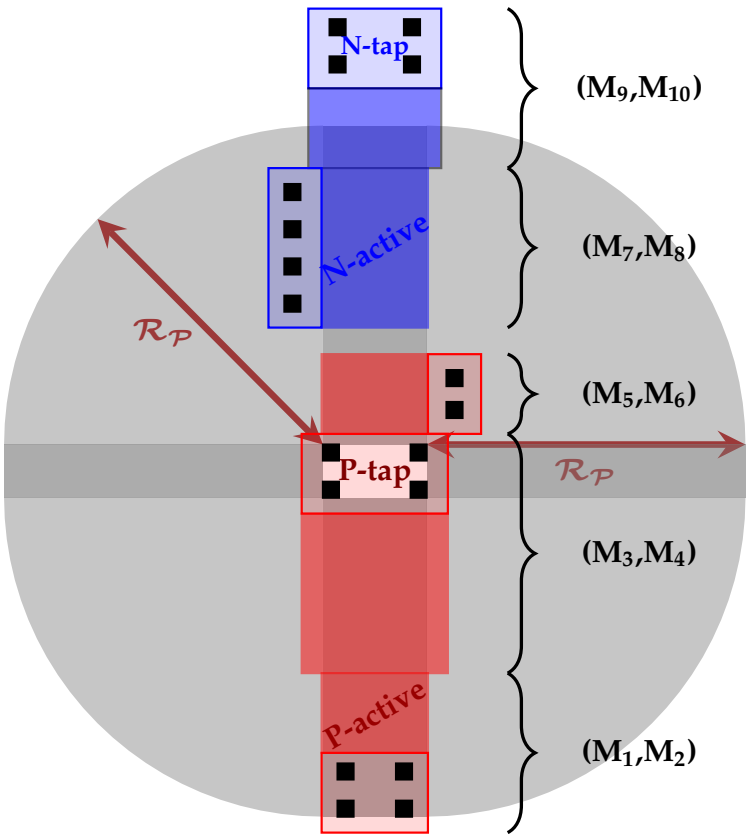




Tap cells - T Active cells - A

Bipartite

WELL TAP GRAPH



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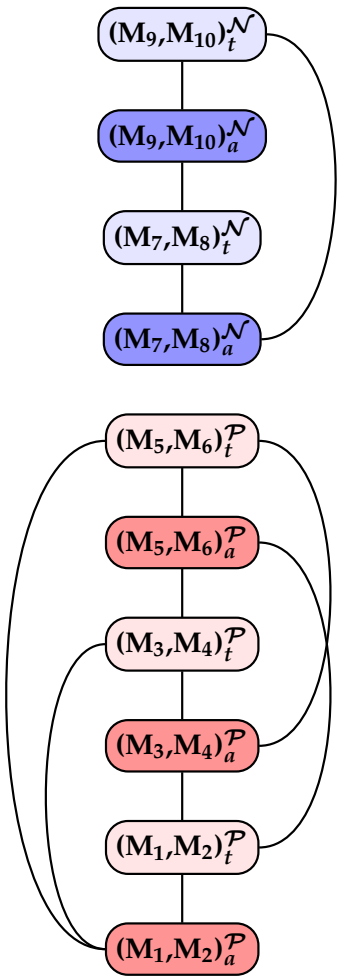

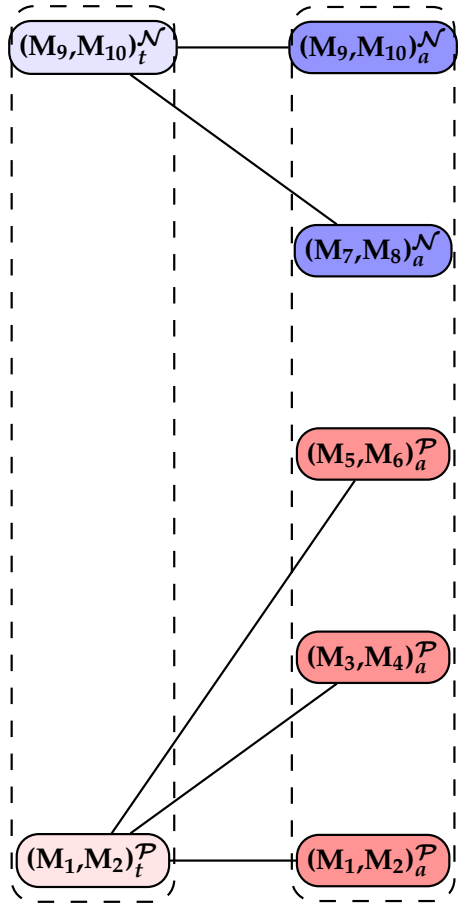

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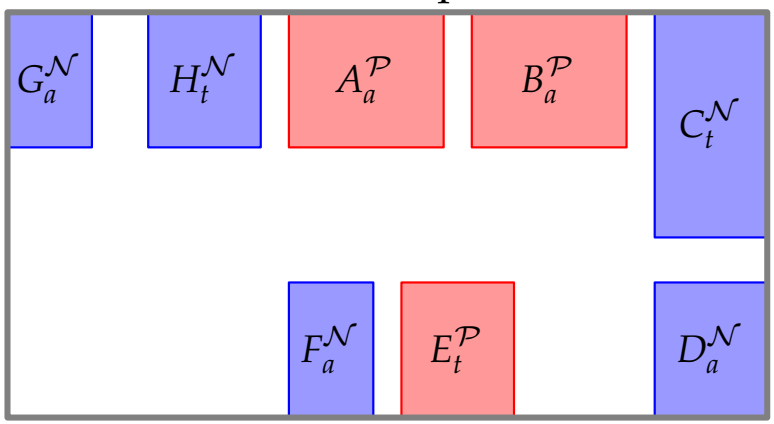
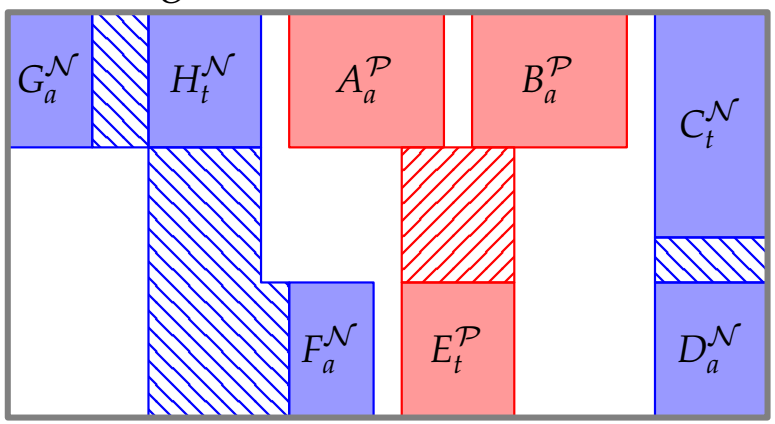
WELL ISLAND GENERATION
WELL TAP GRAPH EDGES : WHICH DEVICES CAN FORM A WELL ISLAND?

Consider active and tap vertices:



How to generate these well islands?

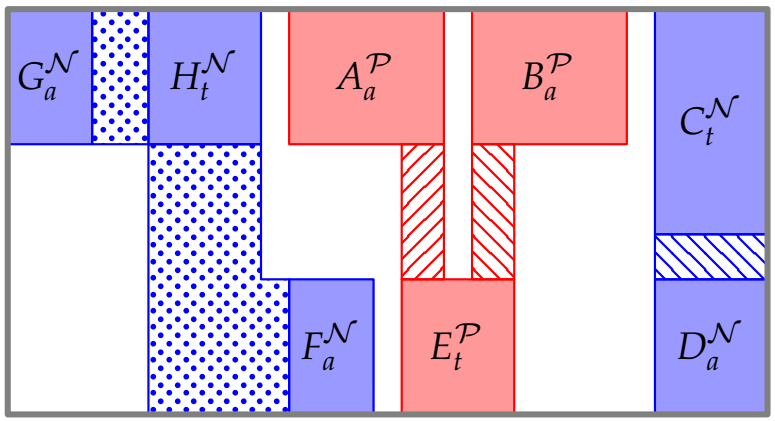


- Problem of finding well islands : similar to multi-pin single layer routing.
  - Active/Tap vertices are pins and rectilinear well layer shapes are the routes.
  - Multi-pin routing problem shown as NP-complete. [LIM, A., ET AL., TCAD'97]
- Additional complexity : Pins have to be grouped into partitions (nets) for routing.

[LIM, A., ET AL., TCAD'97] Planar topological routing.

WELL ISLAND GENERATION

- Approximate multi-pin net as multiple two pin nets.
  - Nets between active vertex and tap vertex that are within radius.
- Nets can only be connected using :
  - Straight-lined routes : line-of-sight.
  - L-shaped routes : no line-of-sight.



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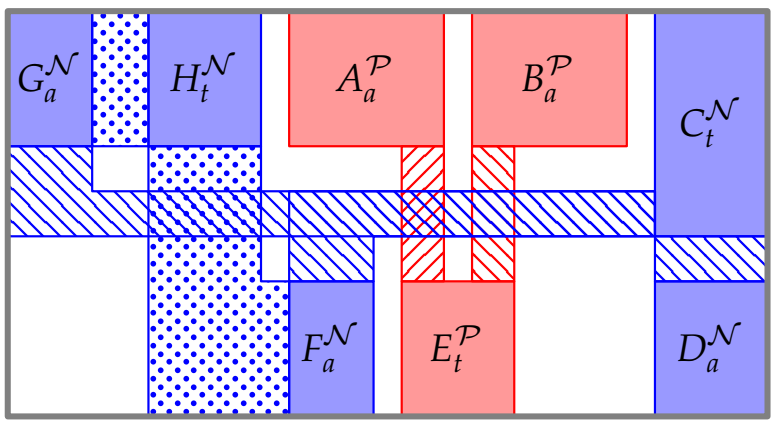
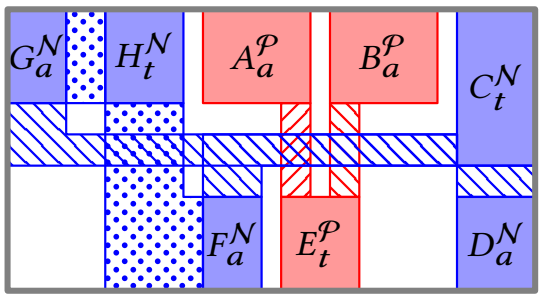
  - Straight-lined routes : line-of-sight.
  - L-shaped routes : no line-of-sight.
- Connecting all nets leads to illegal *shorts*.
  - Well islands of different types (e.g., $\mathcal{P}$ & $\mathcal{N}$) lying within a min. spacing form a *short*.



GENERATION OF LEGAL WELL ISLANDS

Find minimum number of legal well islands $\equiv$ Maximal planar topological routing of two-pin nets [MAREK-SADOWSKA, M., ET AL., TCAD'83]



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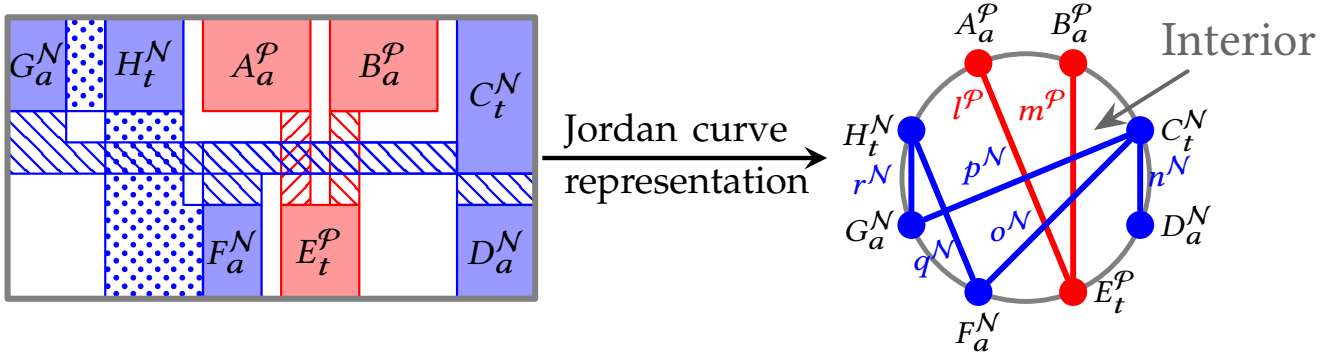

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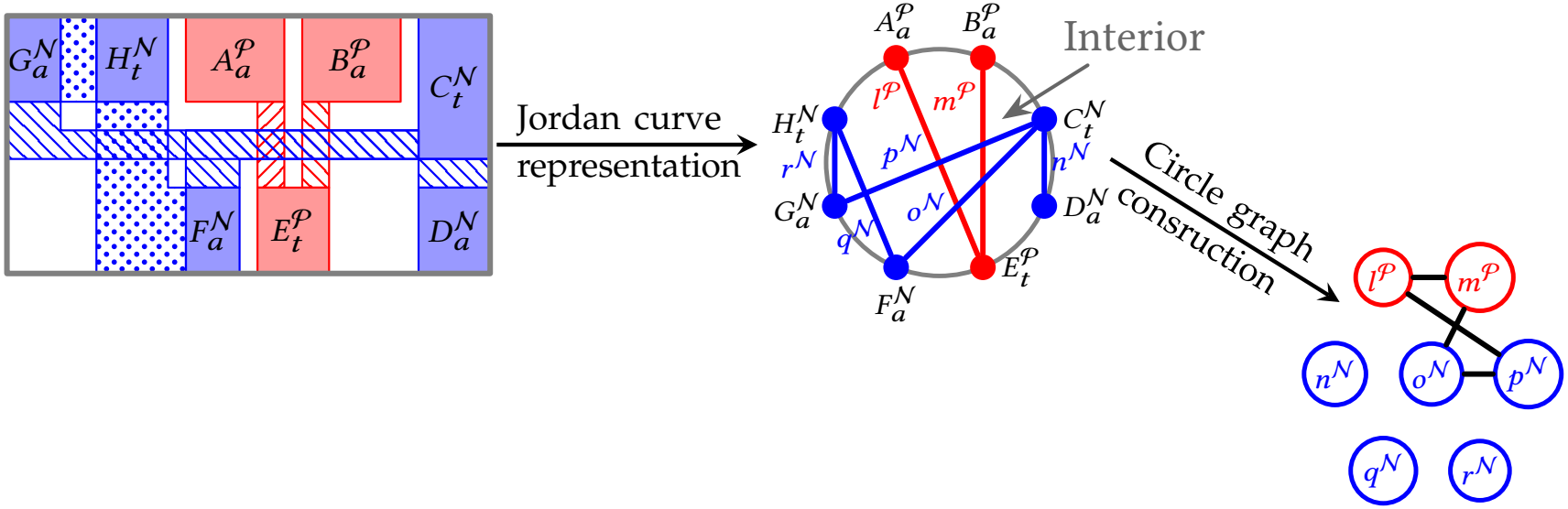

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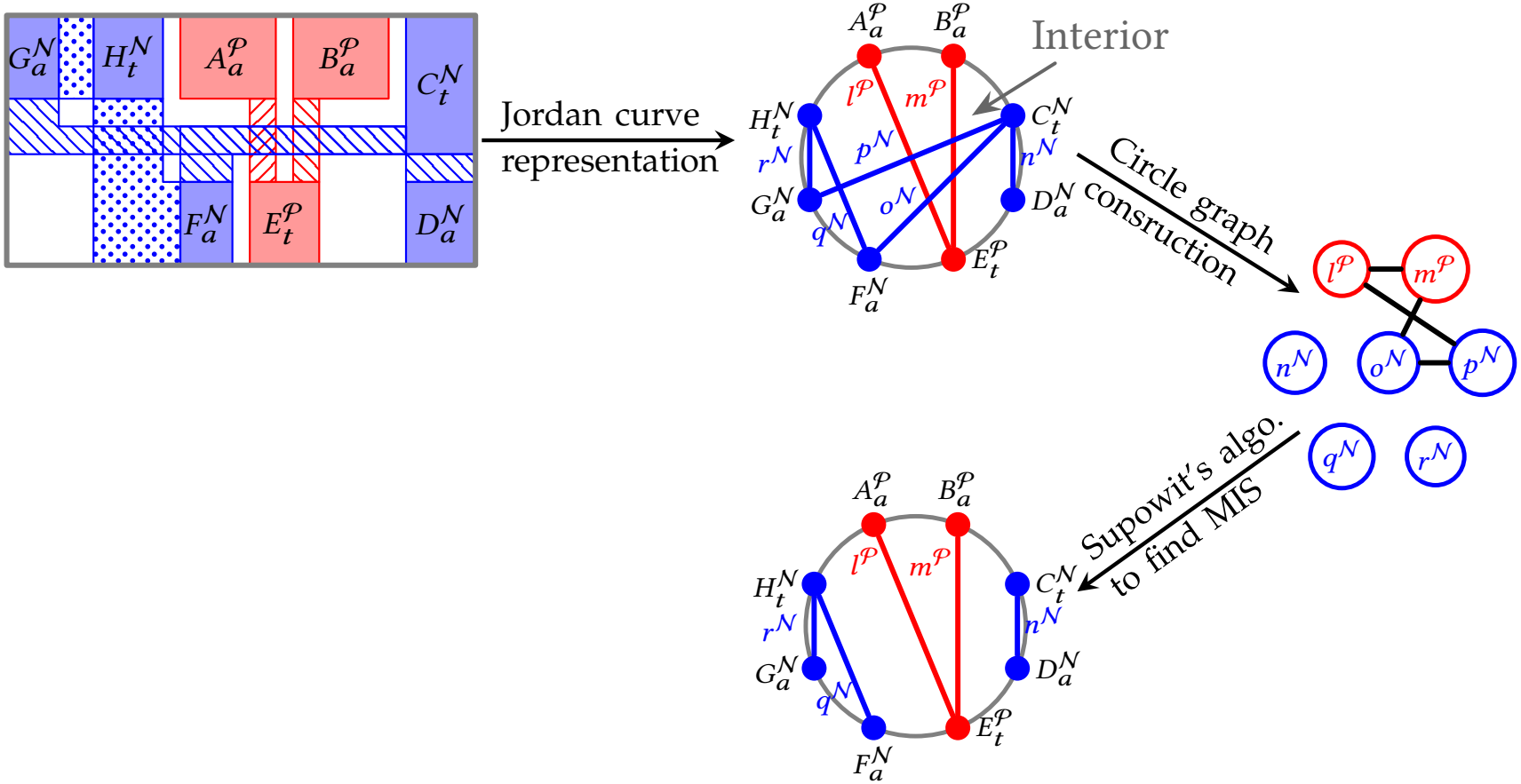

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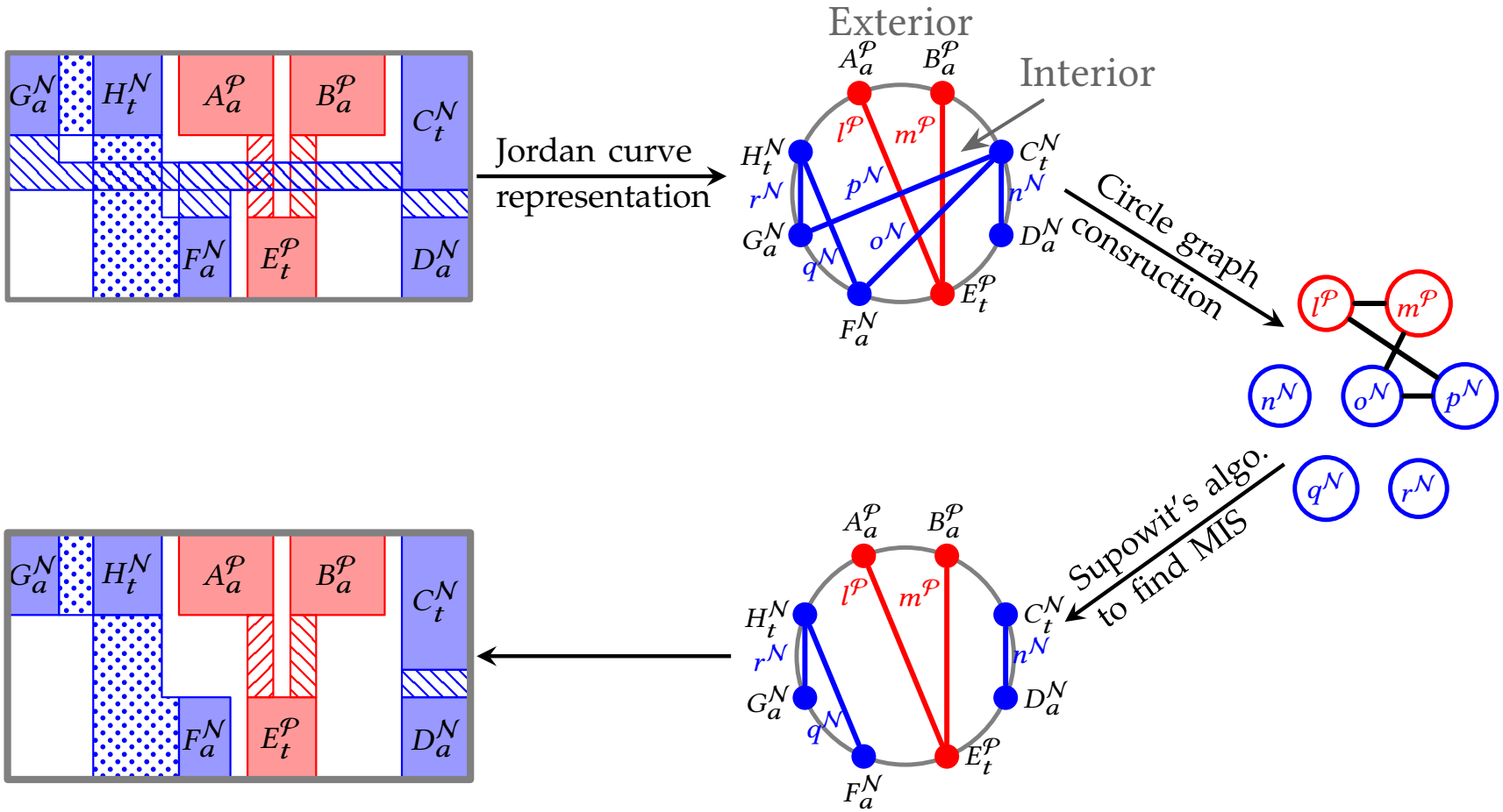

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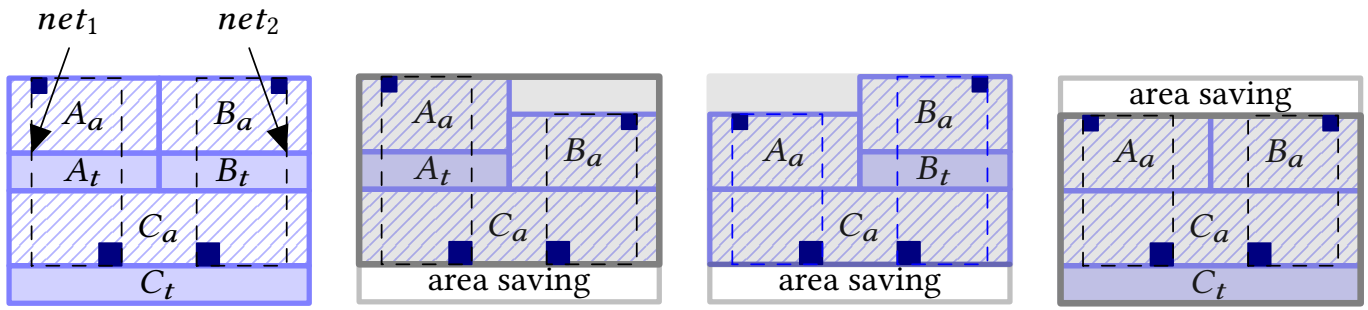
WELL TAP OPTIMIZATION

Goal is to remove redundant taps while taking into account:

- Cost function used by AMS placers : $F(P) = \lambda_1 \cdot f_1(Area(P)) + \lambda_2 \cdot f_2(HPWL(P))$



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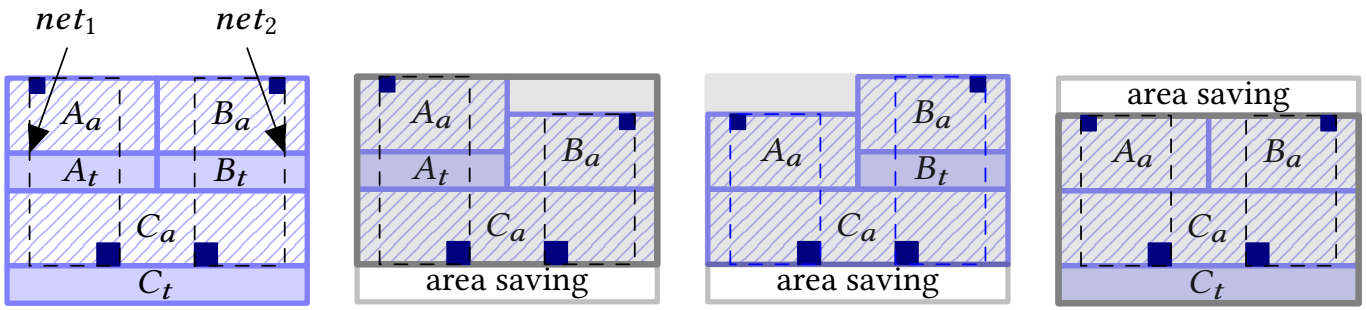
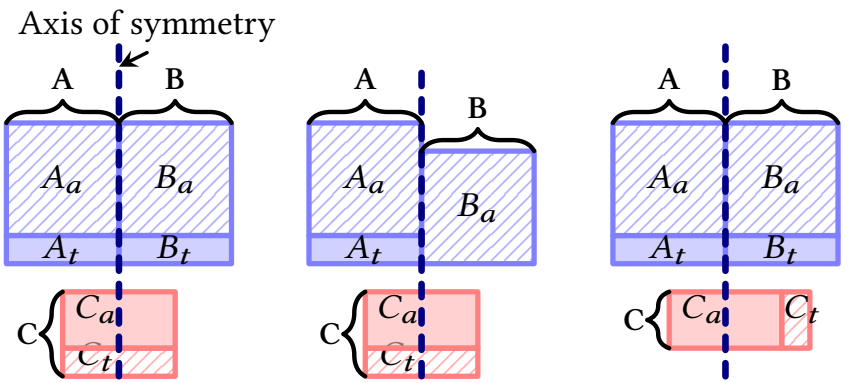


- Symmetry constraint:



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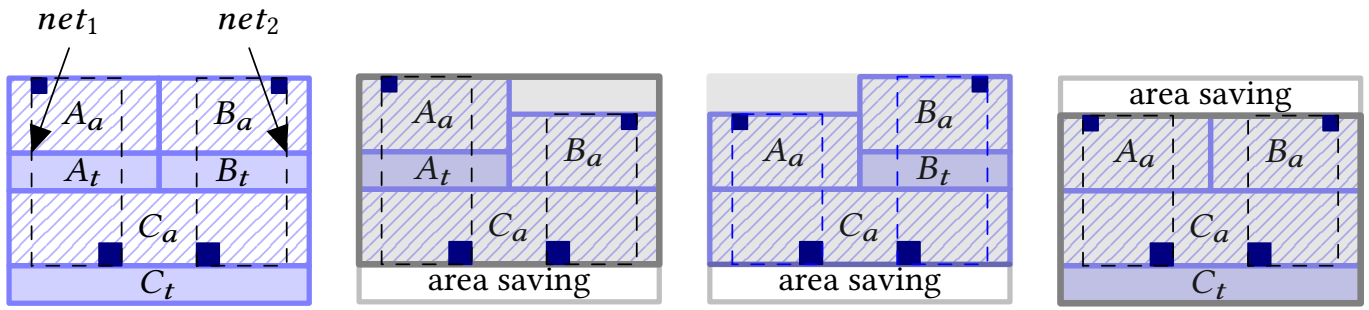
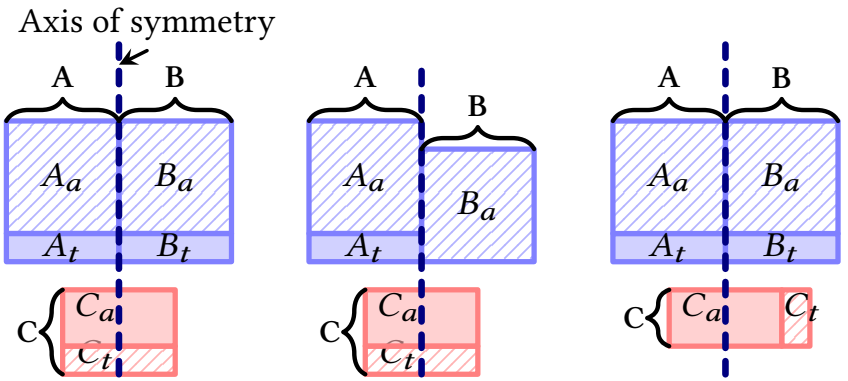
Goal is to remove redundant taps while taking into account:

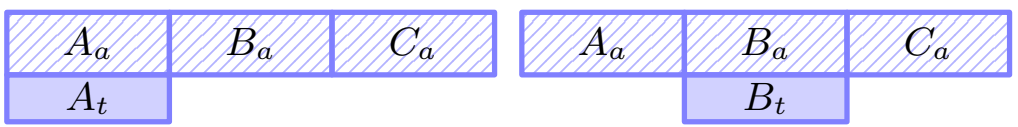
- Cost function used by AMS placers : $F(P) = \lambda_1 \cdot f_1(Area(P)) + \lambda_2 \cdot f_2(HPWL(P))$



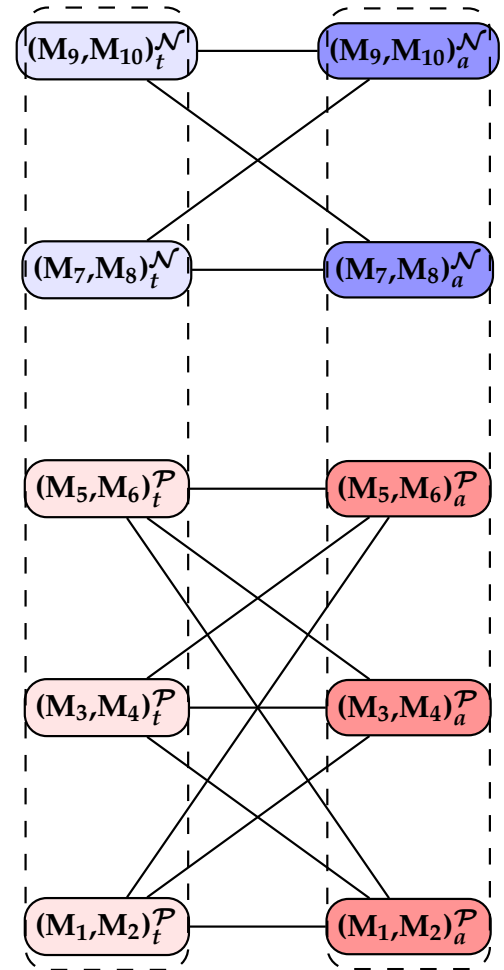
- Symmetry constraint:



- Centering:

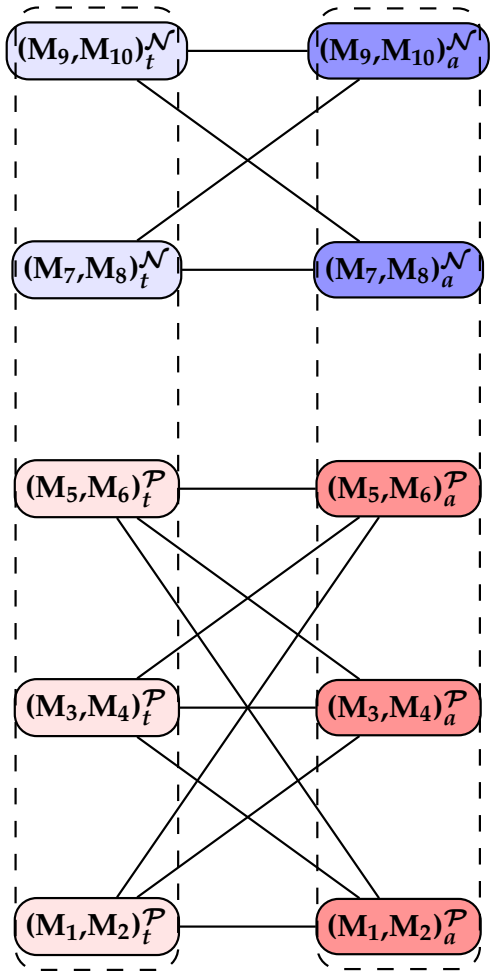


ILP FORMULATION



- $x_i \in \{0, 1\}$: indicator variable to retain tap vertex $i \in T$.
- r_i – largest distance between a tap vertex i and its adjacent active vertices.

ILP FORMULATION



Tap cells - T **Active cells - A**

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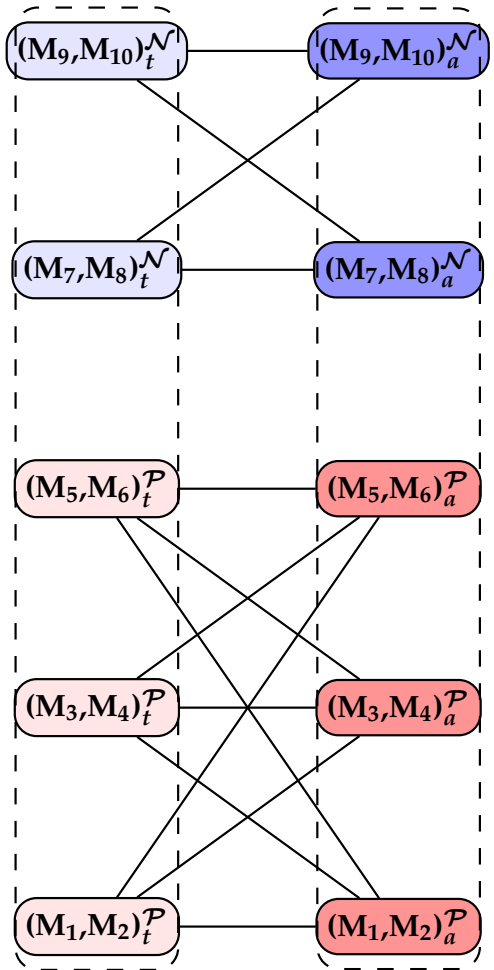
- r_i – largest distance between a tap vertex i and its adjacent active vertices.

$$\arg\max_{x_i} \overbrace{\sum_{i \in T} (1 - x_i)(\lambda_1 \Delta Area_i + \lambda_2 \Delta L_i)}^{\text{Area \& HPWL saving}} - \underbrace{\sum_{i \in T} \lambda_3 x_i r_i}_{\text{centering}}$$

ILP FORMULATION



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such that,

$$\underbrace{\sum_{\forall e_{i,j} \in E} x_i \geq 1, \forall j \in A, i \in T}_{\text{All actives should connect to at least one tap}}$$

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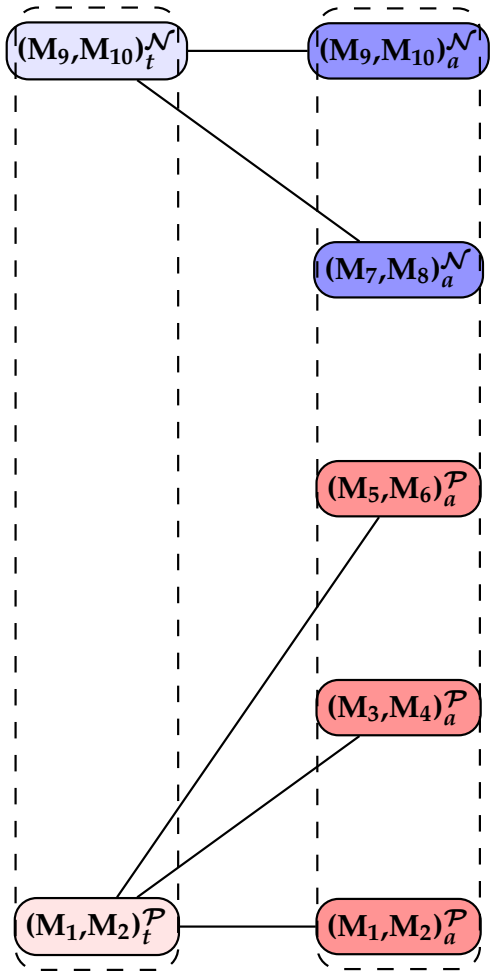

- $x_i \in \{0,1\}$: indicator variable to retain tap vertex $i \in T$.
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$$\arg\max_{x_i} \overbrace{\sum_{i \in T}(1-x_i)(\lambda_1 \Delta Area_i + \lambda_2 \Delta L_i)}^{\text{Area \& HPWL saving}} - \underbrace{\sum_{i \in T} \lambda_3 x_i r_i}_{\text{centering}}$$

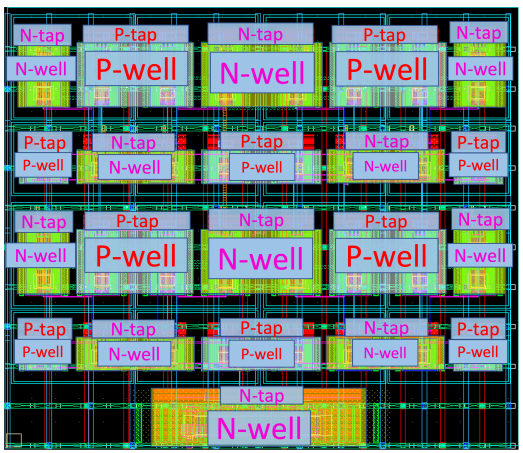
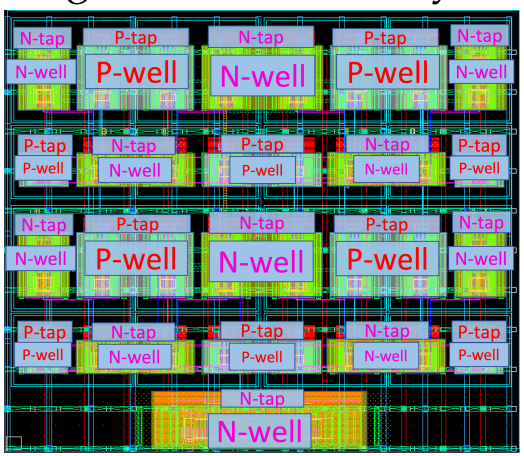
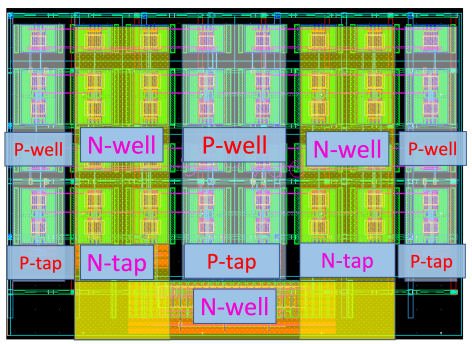
such that,

$$\underbrace{\sum_{\forall e_{i,j} \in E} x_i \geq 1, \forall j \in A, i \in T}_{\text{All actives should connect to at least one tap}}$$

$$\underbrace{x_i = x_j, \forall (i,j) \in \text{symm. pairs}}_{\text{Symmetry constraint}}$$

Results

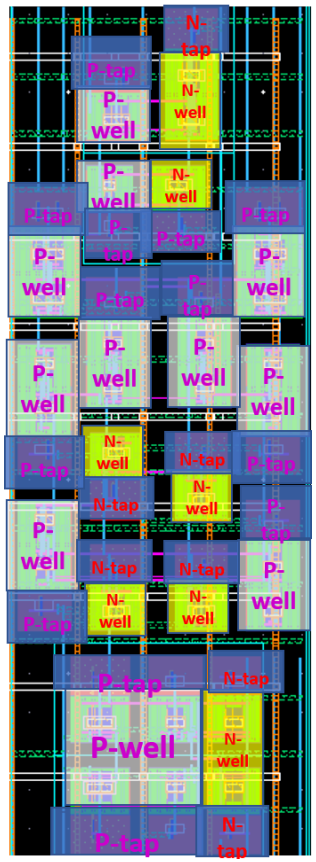
Differential VCO layouts : All layouts are generated using a stochastic placer.

Taps for all cells	Taps inserted and islands generated manually	Taps and islands generated automatically
		
Max. frequency : 3.16 GHz	Max. frequency : 3.16 GHz	Max. frequency : **4.71 GHz**
30% larger area	**30%** larger area	
12% larger HPWL	**12%** larger HPWL	

Results

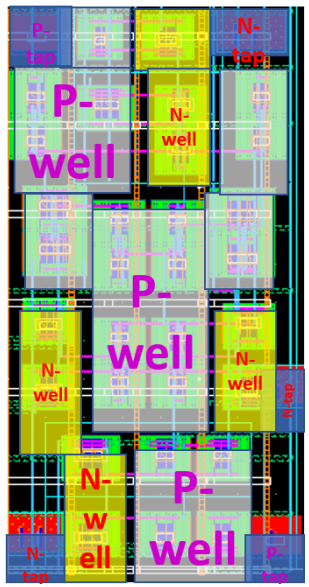
Comparator layouts : All layouts are generated using a stochastic placer.

Taps for all cells



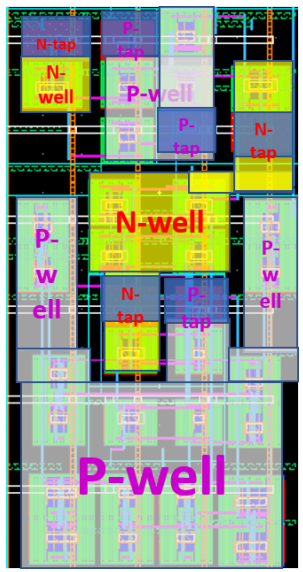
Eval. delay : 192 ps
Precharge delay : 149 ps
48% larger area
39% larger HPWL

Taps inserted and islands generated manually



Eval. delay : 153 ps
Precharge delay : 119 ps
5% larger area
12% larger HPWL

Taps and islands generated automatically



Eval. delay : **151 ps**
Precharge delay : **116 ps**

RESULTS

Circuit	Performance metric	Taps for all cells	Manual tap insertion	Proposed approach
High-speed comparator	Evaluation delay (ps)	64	60	60
	Precharge delay (ps)	48	47	47
Five-transistor high-frequency OTA	DC gain (dB)	22.13	22.13	22.13
	3-dB freq. (MHz)	335	343	343
	UGF (GHz)	4.08	4.18	4.18
Folded cascode OTA	DC gain (dB)	13.40	13.75	**14.80**
	3-dB freq(GHz)	2.39	2.68	2.64
	UGF(GHz)	7.60	7.77	**8.05**
Two-stage differential OTA	DC gain (dB)	44.4	45.0	44.7
	3-dB freq(MHz)	4.04	3.52	**4.41**
	UGF(MHz)	685	810	798

CONCLUSION

- Demonstrated the impact of ignoring well-islands and well-taps during placement in automatic AMS layout generation flow.
- Showed that the generation of optimal layout in terms of area/HPWL with well taps and islands for a given input layout is NP-complete.
  - Posed the well island generation as a multi-pin planar topological routing problem.
  - Approximated the problem as multiple two-pin routing problem that can be solved in polynomial time.
- Optimal well taps are chosen using an ILP formulation.
  - Considers the impact of taps on Area & HPWL.
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- Optimal well taps are chosen using an ILP formulation.
  - Considers the impact of taps on Area & HPWL.
  - Takes into account AMS layout constraints like symmetry and tap centering.
- Inclusion of well islands/well taps during placement generates layouts that are better in terms of area (20% vs ALIGN and 5% vs manual), HPWL (9% vs ALIGN and 4% vs manual) and performance.