

Physical Design Optimization

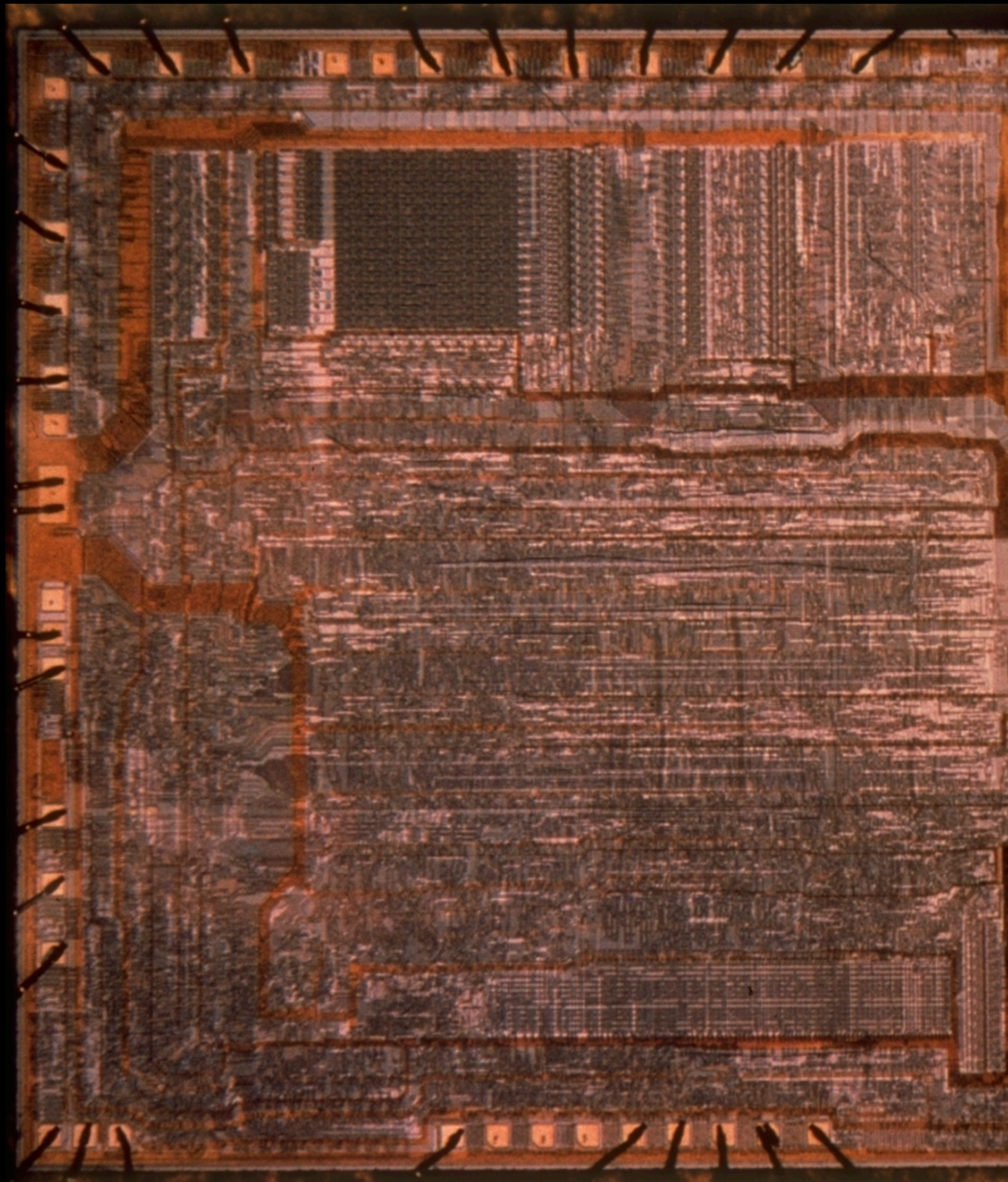
From Past to Future

Remembering the Past

Reverse Engineering of the Z8000 (Zilog)

done in 1979/1980

NMOS 3.5 μ
1 metal layer



Data Path

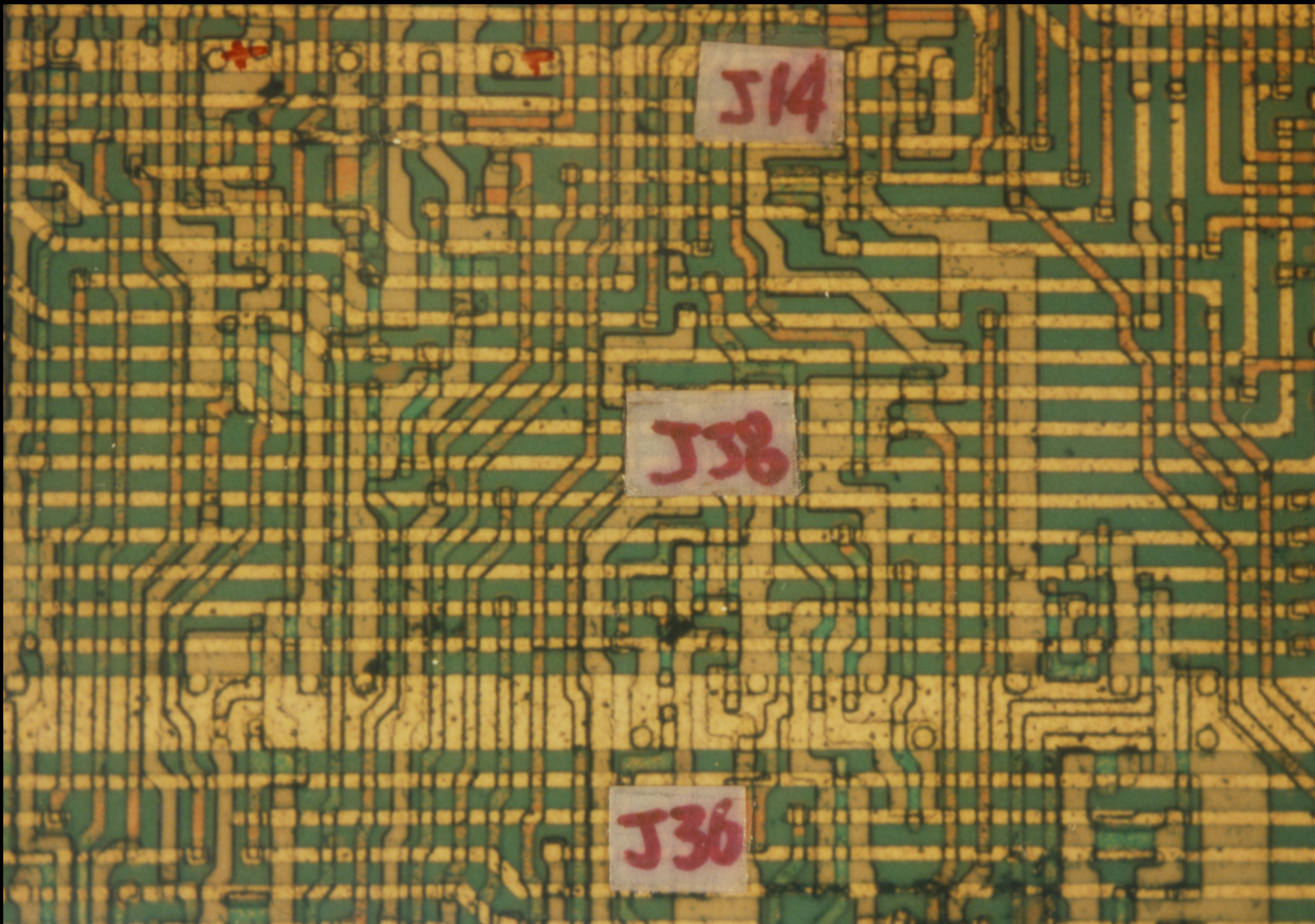
Control Part

The designers of the Z8000 identified that four instructions were responsible for about 40% of instruction use. Then the Control Part was divided into 2 parts.

One to take care of these four instructions and other to take care of the other more than 100 instructions.

Z8001 and Z8002 microprocessors

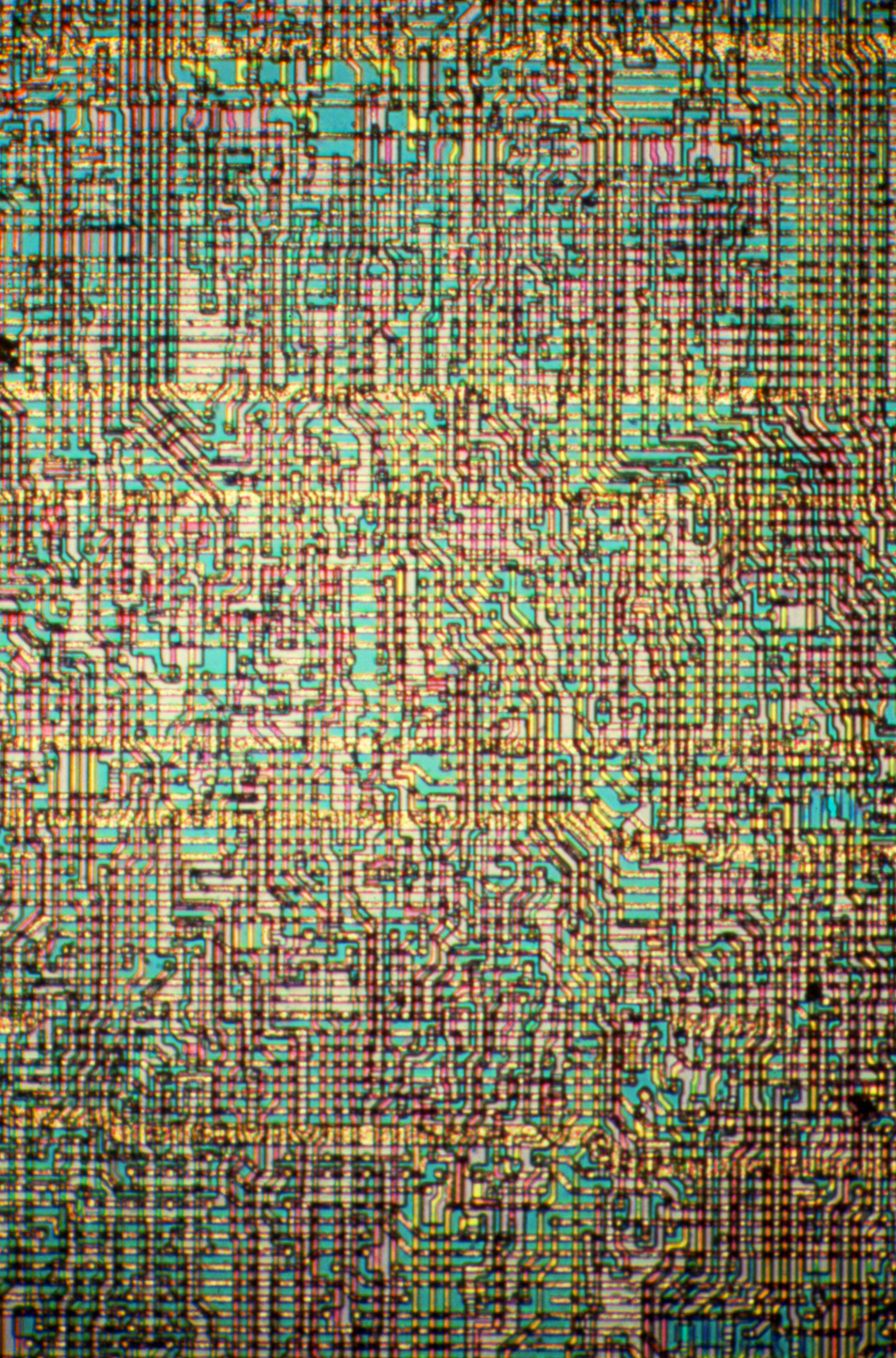
Reverse Engineering of the Z8000



A set of photos were done using an optical microscope and a polaroid camera, attached to it. The photos were assembled generating a mosaic with about 2x2 m.

Each time a poly was crossing over a diffusion, the transistor was recognized and labeled. Then it was observed the connections between transistors, letting the identification of the logic gates.

Then it was observed the connections between logic gates to identify functions...



VDD

Z8000

GND

Detail of the Z8000 control part in random logic.

High density of gates, some with till 23 inputs

Layout optimization by using supergates

Use of lines in 45°

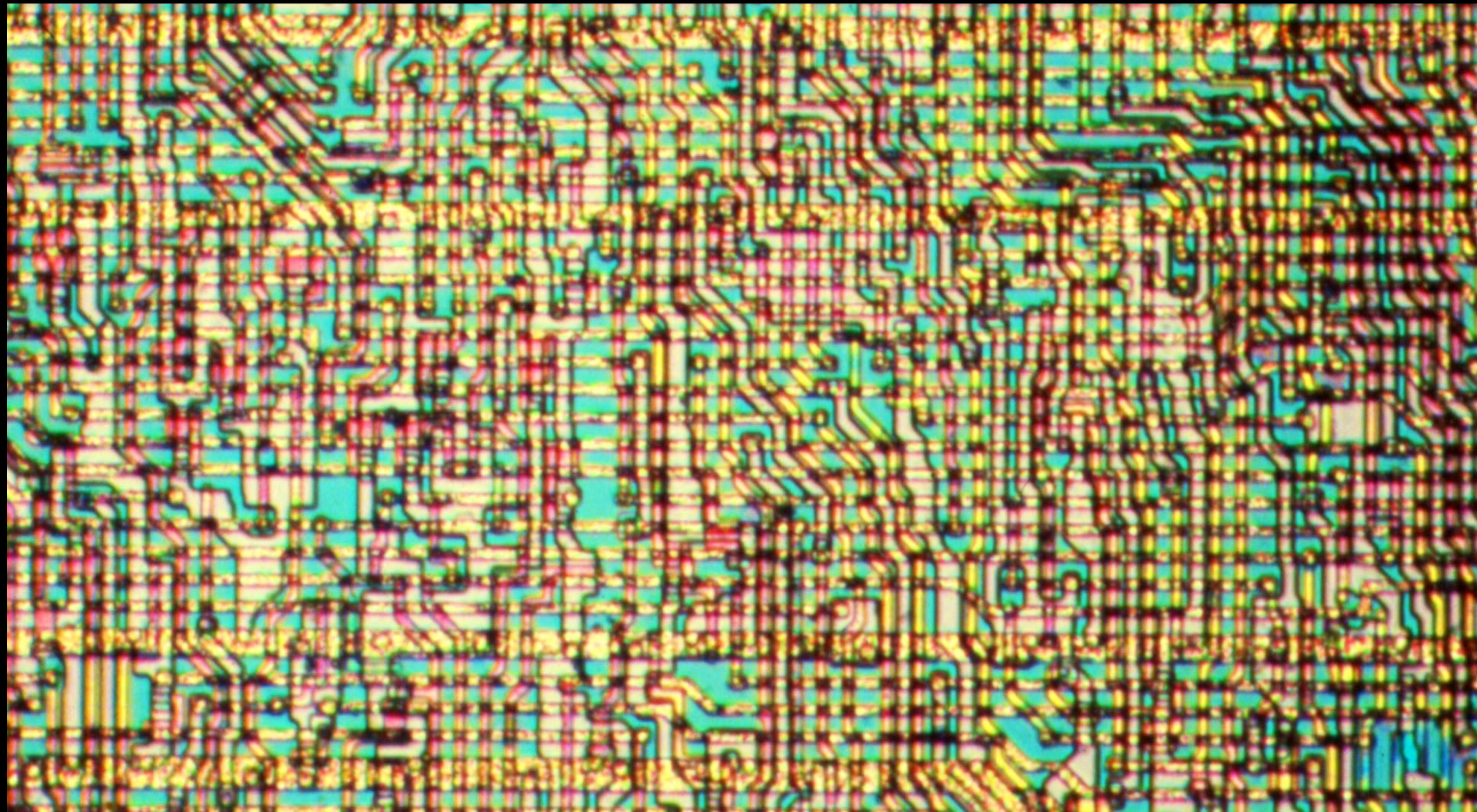
Vertical connections mainly using polysilicon

Rows of cells with more than 20 metal tracks

The rose/green lines (polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor. Substrate is green.

Z8000

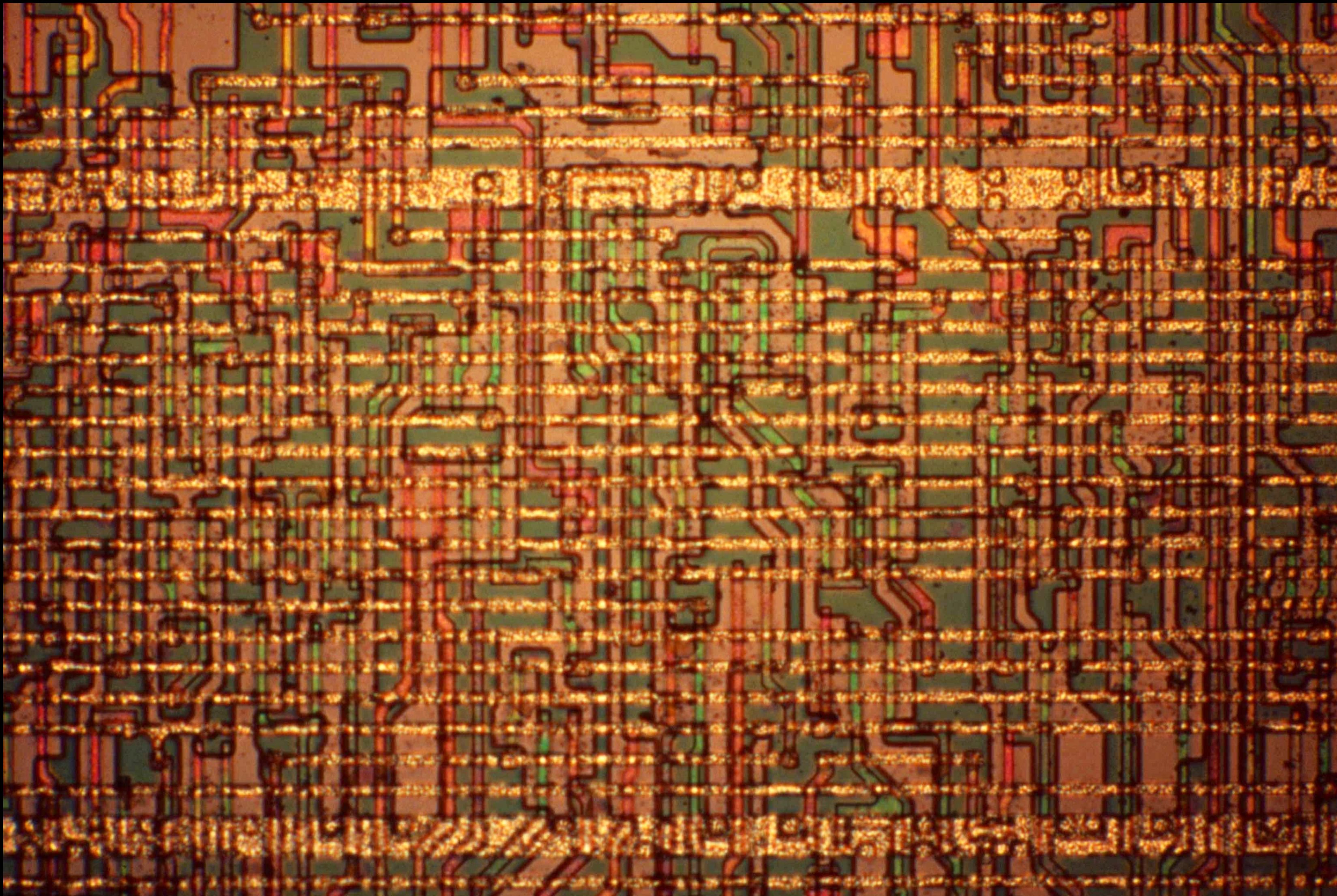
Detail of the Z8000 control part in random logic. The rose/green lines (polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor. Substrate is dark green.



sometimes a supergate was divided, and part of it implemented in one location and part in another location of control block. The two parts were connected by metal I.

Z8000

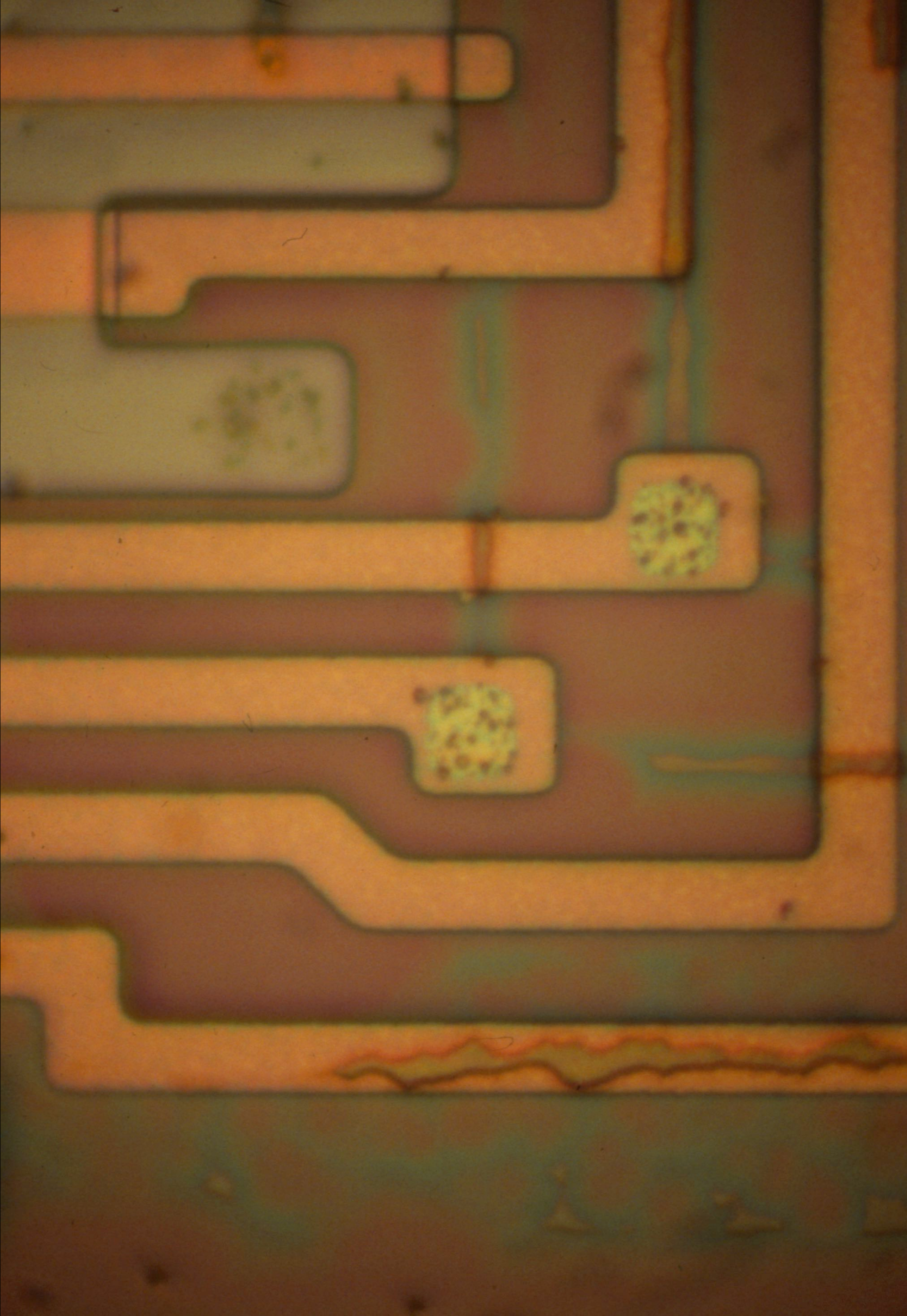
Detail of the Z8000 control part in random logic. The green/rose lines (polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor. Substrate is dark green.



A same logic gate has different layouts and sizing, depending on where it is located

18070

Detail of the 8070 poly lines (in light orange). Metal lines were removed by using an acid. Diffusion is grey and substrate is brown.



The metal layer was taken out before doing the photo. Some brown lines are silicon oxide that were under the metal lines. With this it is possible to know where the metal lines were.

M68000

Detail of the M68000 Data Path. A set of 5 pass transistors can be seen on the left column. Each one of these pass transistor is in a data path bit slice. The orange zones are diffusion ones. Polysilicon is mainly green.

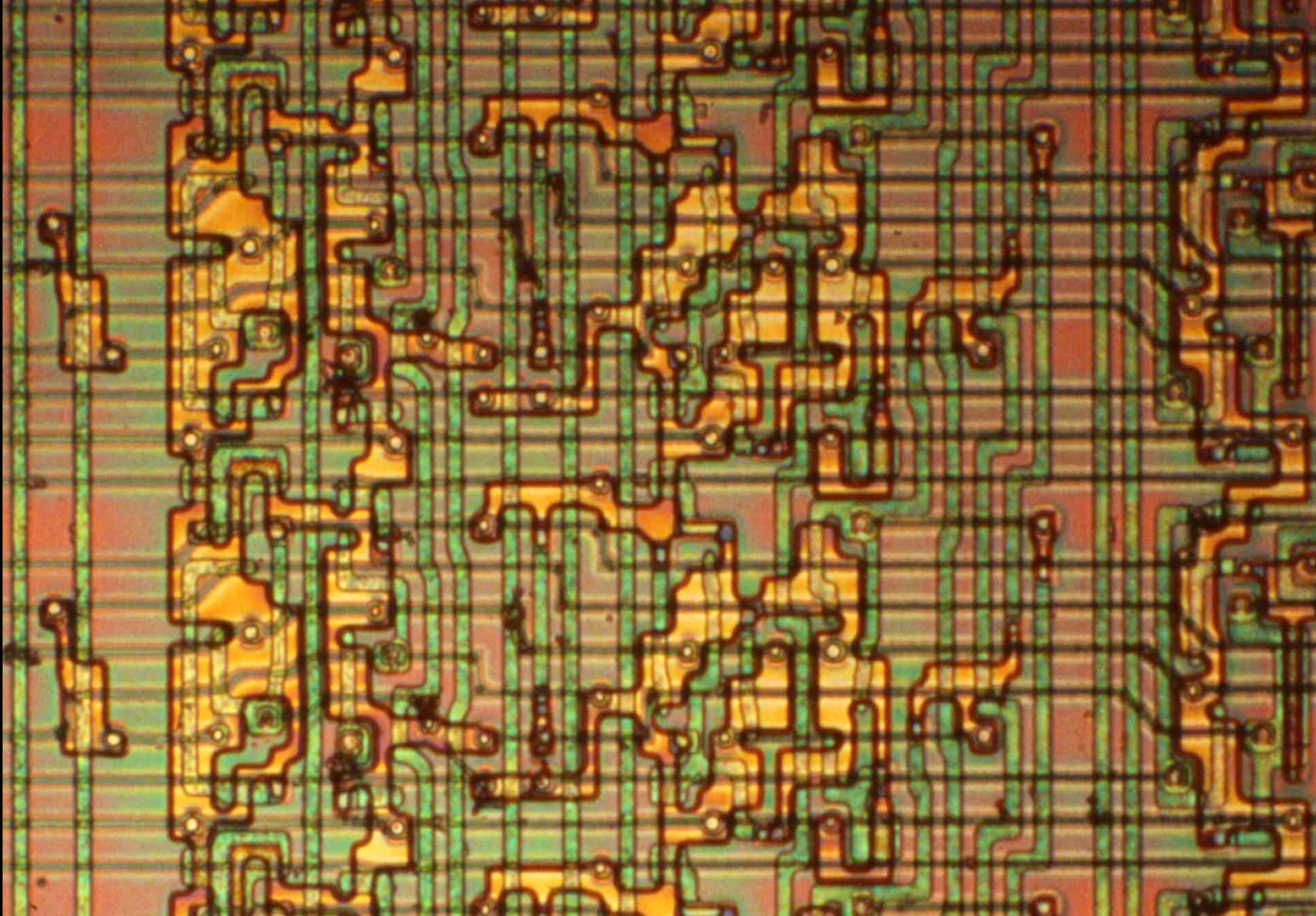
Diffusion regions (in orange) using a large set of formats.

The metal layer was taken out before doing the photo.

by Ricardo Reis

M68000

Diffusion regions
(in orange) using a
large set of
formats.



M68000

Another detail of the M68000. The orange zones are diffusion ones. Polysilicon is mainly green. It is a NMOS one metal technology. Then polysilicon is also used to do some long connections.

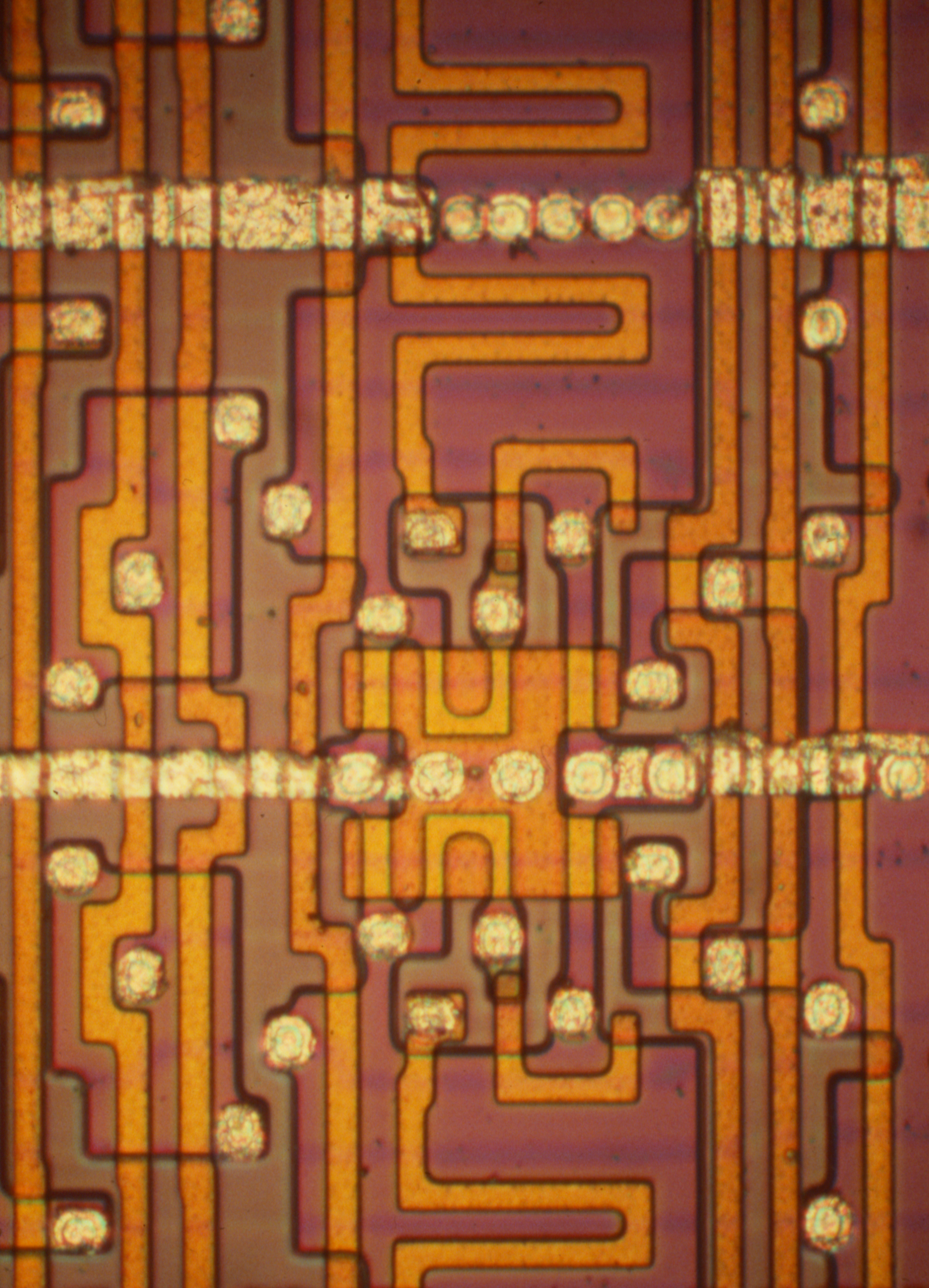
The metal layer was taken out before doing the photo. Some brown lines are silicon oxide that were under the metal lines. With this it is possible to know where the metal lines were.

M68000

A detail of the M68000. The orange zones are diffusion ones. Polysilicon is mainly green. It is a NMOS one metal technology. Than polysilicon is also used to do some long connections.

busses using 45° lines

The metal layer was taken out before doing the photo. Some brown lines are silicon oxide that were under the metal lines. With this it is possible to know where the metal lines were.



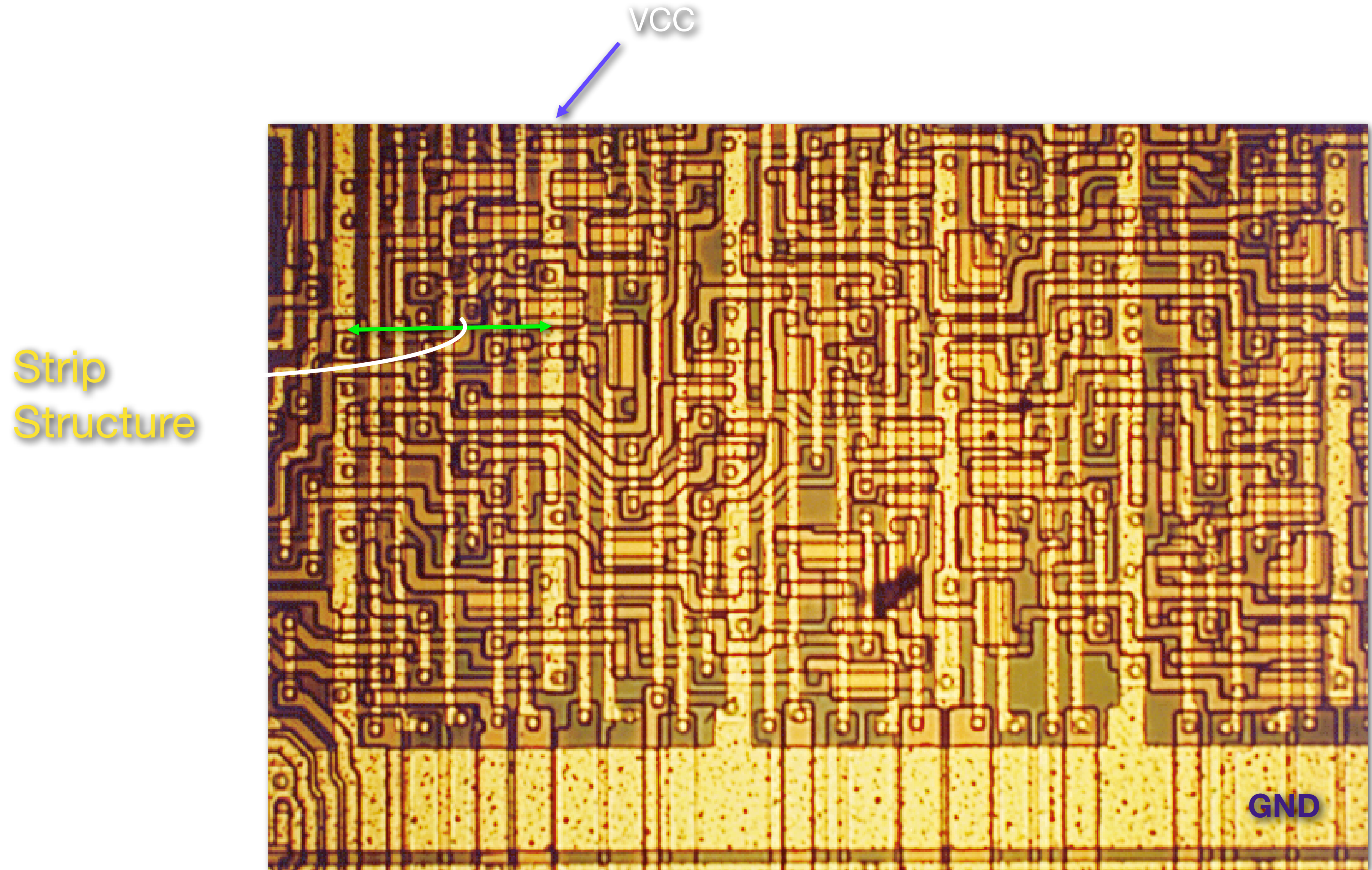
M6809

Detail of the M6809 Register File. Each memory cell has 6 transistors. The orange lines (polysilicon) crossing a wine/purple zone (diffusion) defines the channel of a transistor. The technology used was a NMOS with charge transistors connected to VDD.

The metal layer was taken out before doing the photo, but it still remains metal spots in the contact locations and the metals related to VCC and Ground lines.

Detail of the control part of TMS7000

implemented with random logic



Full Custom

The observation of **circuits designed by hand**, was the **inspiration** to search for tools that could provide a so dense layout as the ones designed by hand

ANCEAU, François e REIS, Ricardo Augusto da Luz
Complex Integrated Circuit Design Strategy,
IEEE Journal of Solid State Circuits,
SC-17(3):459-64, June 1982.
DOI: 10.1109/JSSC.1982.10517601982

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Complex Integrated Circuit Design Strategy

FRANÇOIS ANCEAU AND RICARDO A. REIS, MEMBER, IEEE

Abstract—This paper presents a design strategy for VLSI circuits based on the use of a floor plan as an evaluation and management guide for the design of a future circuit. This approach is widely used in the microelectronic industry and allows global optimizations, which are the key to both high density and design reliability, by improving the assembly and the direct wiring of the blocks. The efficiency of such an approach may be improved by the use of a topological evaluator. This tool will give an evaluation of the shape, size, and connections of the main blocks from their specifications. It is able to take into account the topological constraints given by the designer in order to improve the assembly and connectivity of the floor plan. This tool is composed of a set of evaluation routines for the different kinds of functional blocks constituting a VLSI circuit and a supervisor for dialogue with the user.

I. INTRODUCTION

THE aim of designing a digital integrated circuit is to draw the masks which will be used in its realization. This drawing work is currently the most costly step of the whole design process.

Research into increasing the integration density, synonymous with a good production yield, has to be done with great design reliability to limit errors. Past experience has shown that in order to reach this goal, the search for a global optimization is more important than the search for local optimizations. This principle is expressed here in a few simple rules.

II. GENERAL TOPOLOGY OPTIMIZATION

Unused area between blocks must be reduced as much as possible. This goal is obtained by adjusting the shape of each block to fit its destination place. This flexibility in the shape of the blocks under dimensional constraints differs for each block and corresponds to the scanning of different solutions of implementation.

It is preferable to design a block not for minimal area but in order to fit in well with the general topological structure. Thus, individual optimization of each block's area does not necessarily lead to area optimization of the whole circuit.

A. Interconnection Optimization

The area occupied by the connections in an integrated circuit increases with its complexity. In the case of LSI/VLSI circuits this area is frequently at least equivalent to the area taken up by the logical blocks.

The classical approach, consisting of the placement and routing of functional blocks designed and optimized inde-

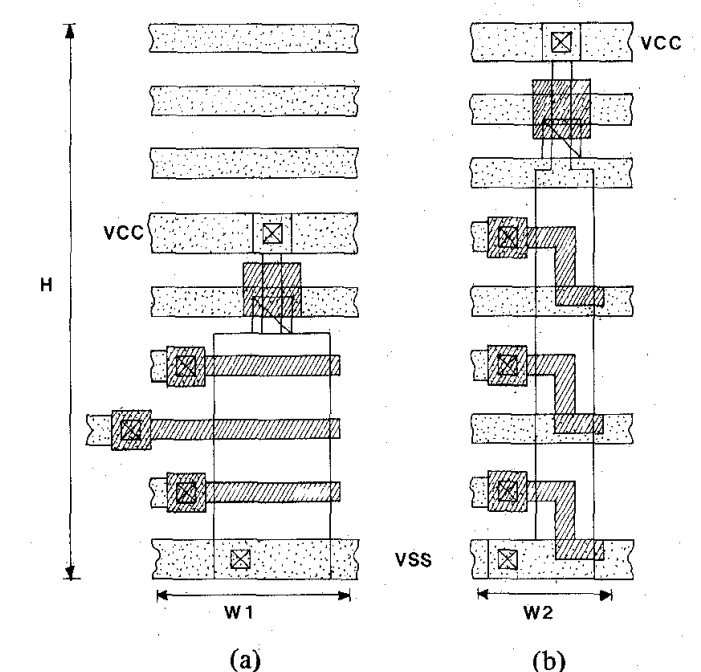


Fig. 1. Example of area optimization by overlaying the cell with interconnections.

pendently, gives a circuit area equal to the sum of the connection area and the gates area.

In order to get a better optimization of the circuit area we suggest the use of the following rules.

Suppression of Pure Interconnection Zones: by the use of direct connections between blocks, which must be designed taking this constraint into account.

Superposition of Connections and Gates: The existence of many conductive layers allows us to draw the gates under the connections, "wires first, gates under."

Use of the "Transparency" of the Block: It is often better that the connections pass through the blocks rather than go around them. In fact, it is often possible to include a connection passing through a block without a large modification of its size. Each block will be characterized by a transparency coefficient in both directions, horizontal and vertical, which indicates how many lines may pass through the block.

The application of these rules suggests that it is possible to characterize the design quality of an integrated circuit by the percentage of its area occupied only by pure interconnection lines without any transistors.

Fig. 1 shows an example of the reduction of the total area (gates + connections) by placing the connections over the gates. This example consists of a cell containing a three input NAND cell and three pass-through interconnection lines. In Fig. 1(a) the NAND cell itself is designed on the basis of a four line strip with the pass-through interconnection lines placed outside the strip. In Fig. 1(b) the pass-through inter-

Manuscript received November 4, 1981; revised February 9, 1982.
The authors are with the Computer Architecture Group, IMAG, Grenoble, France.

Full Over the Cell Routing

By that time, standard cell circuits were using a routing channel between the rows of cells

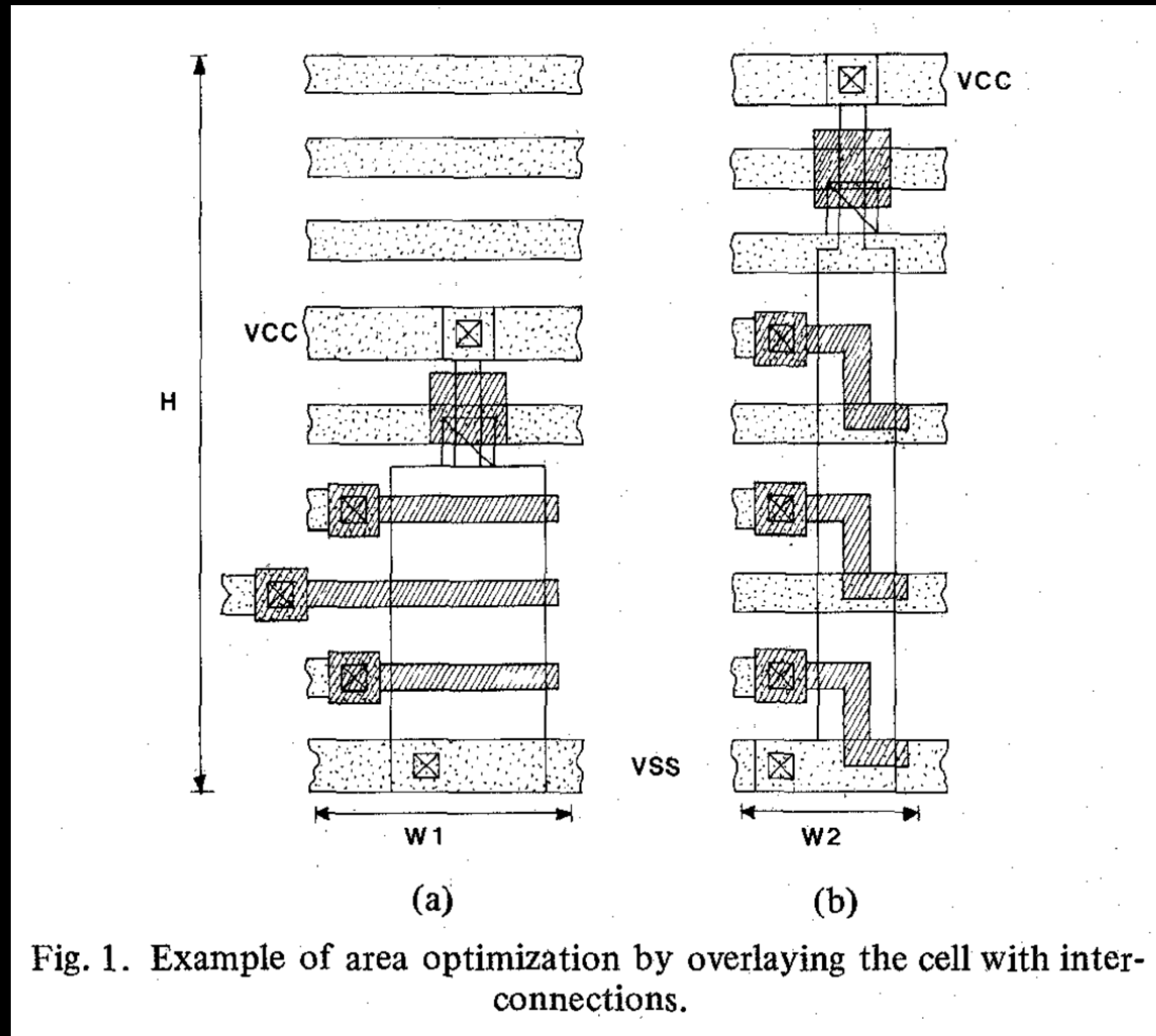


Fig. 1. Example of area optimization by overlaying the cell with interconnections.

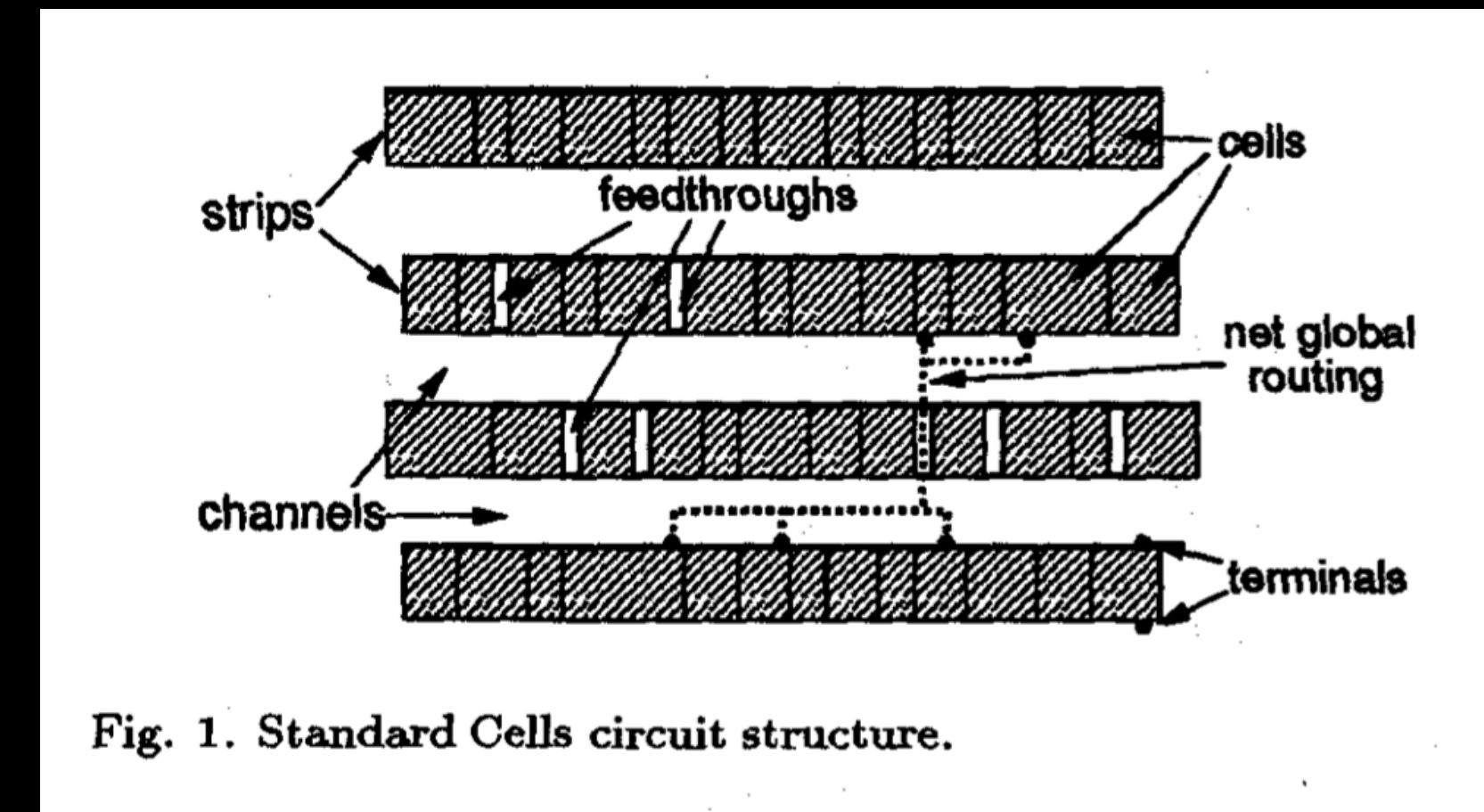


Fig. 1. Standard Cells circuit structure.

JOHANN, Marcelo; REIS, Ricardo.

A Full Over-the-Cell Routing Model.

IFIP VLSI 95, IFIP/IEEE/ACM, Tokyo, Aug. 26 – Sep. 1, 1995,

DOI: 10.1109/ASPDAC.1995.486412



Fig. 3. Transparent Cell circuit structure.

ANCEAU, François e REIS, Ricardo Augusto da Luz

Complex Integrated Circuit Design Strategy,

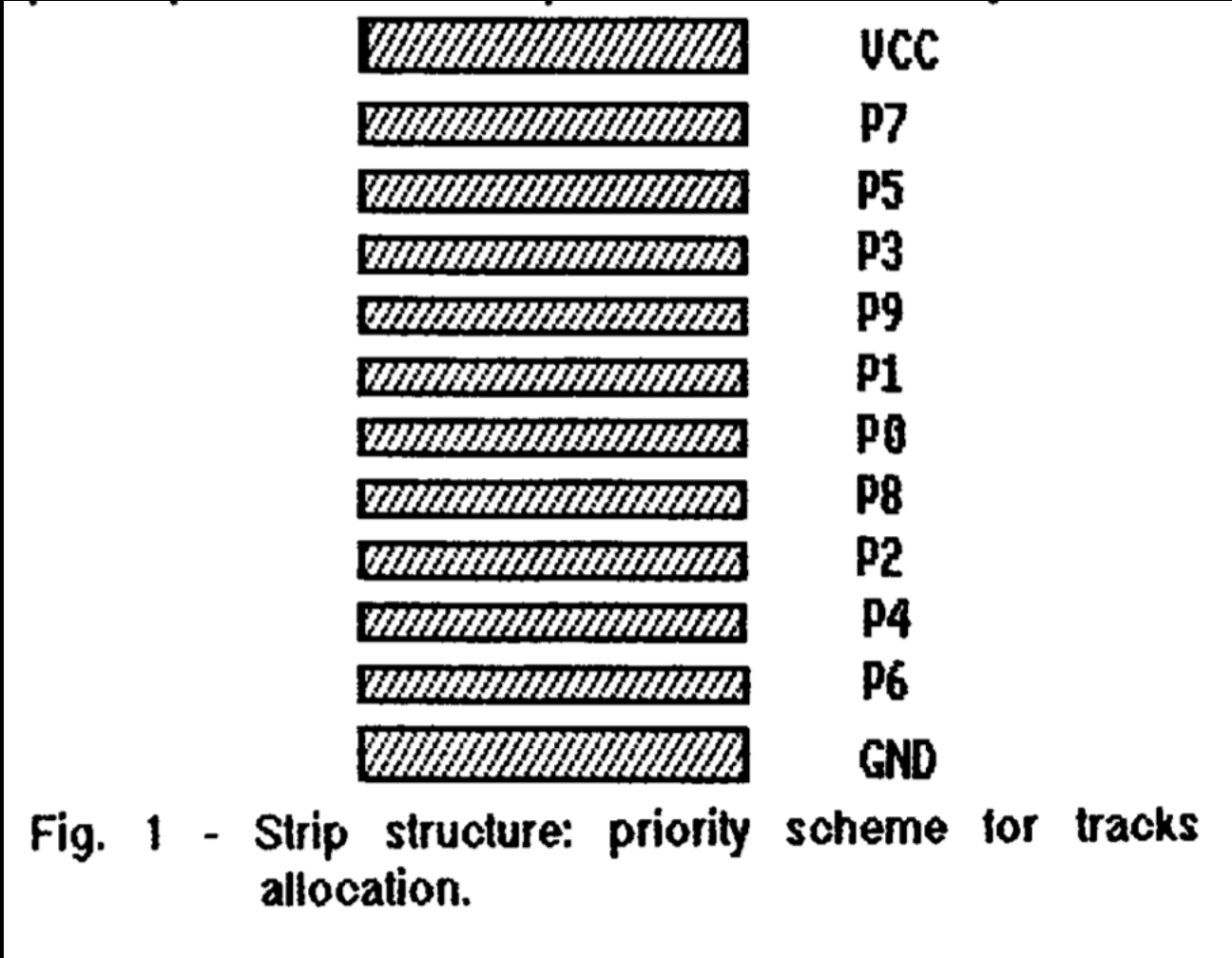
IEEE Journal of Solid State Circuits,

SC-17(3):459-64, June 1982.

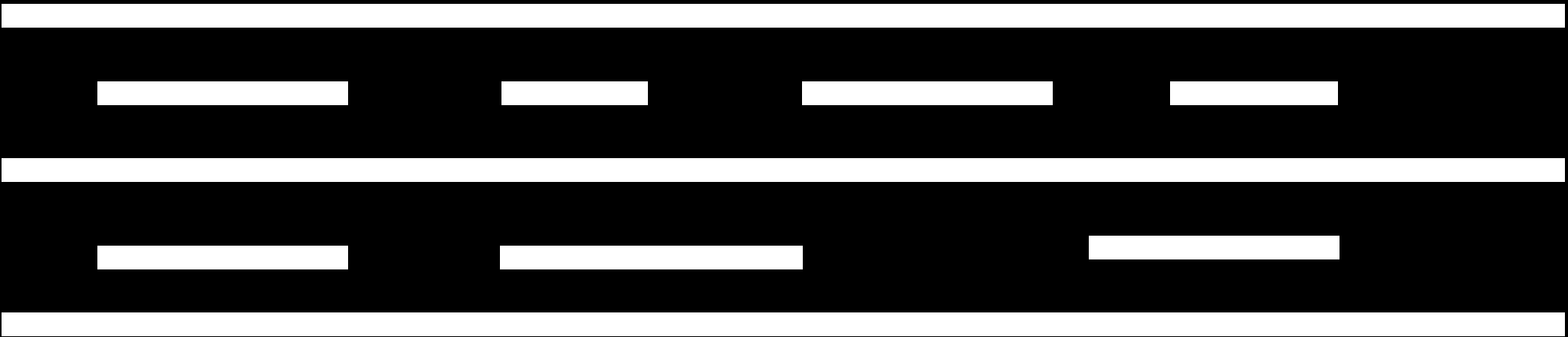
DOI: 10.1109/JSSC.1982.10517601982

Full Over the Cell Routing

REIS, Ricardo
A New Standard Cell CAD Methodology
IEEE Custom Integrated Circuits Conference,
Portland, Oregon, May 4-7, 1987. Proceedings, IEEE, p. 385-388



tracks priority management



No routing channels between rows of cells

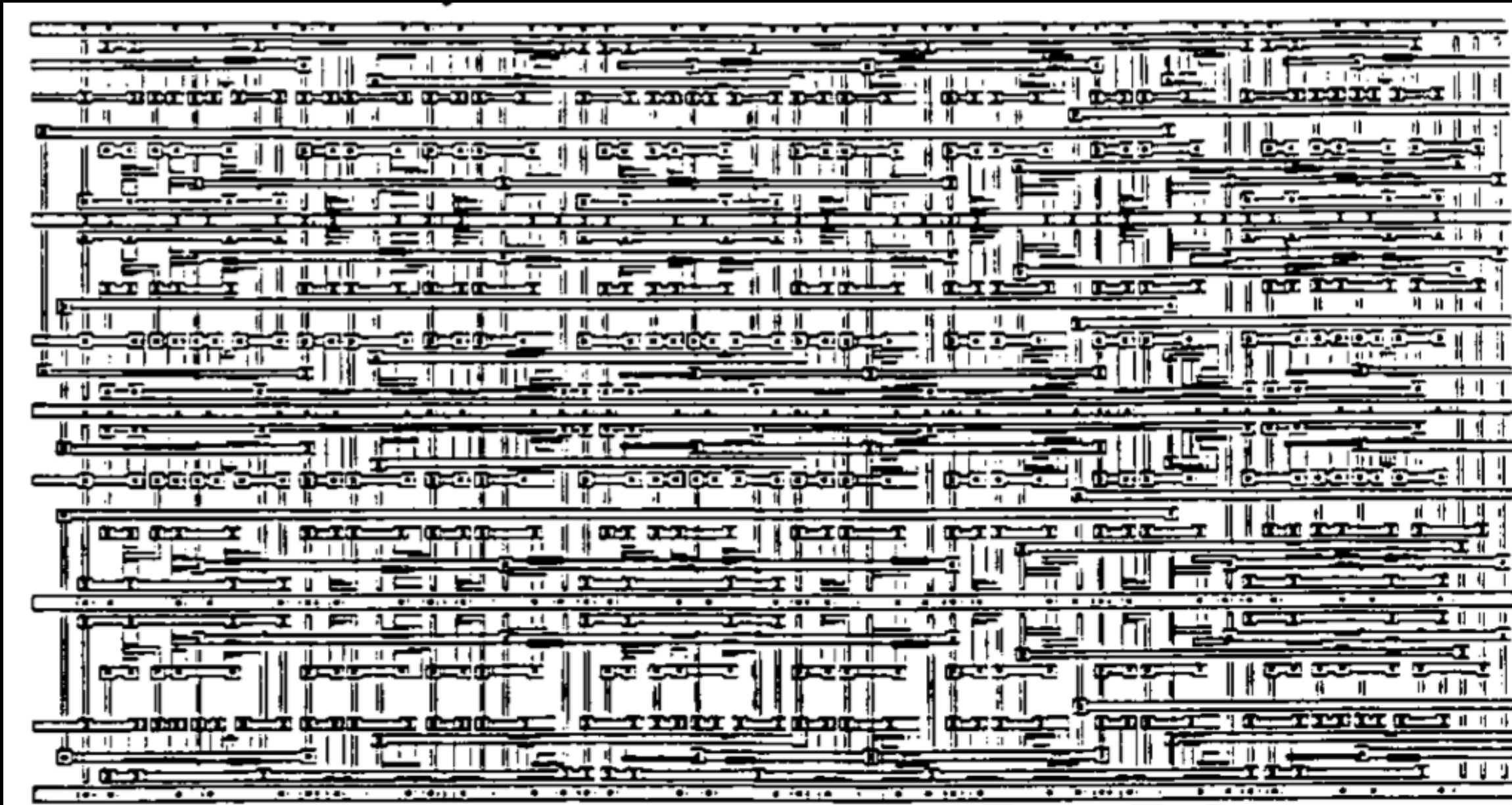


Fig. 5 - A 12-function Arithmetic and Logic Unit.

REIS; Ricardo; GOMES, Rogério Figurelli; LUBASZEWSKI, Marcelo.
An Efficient Design Methodology for Standard Cell Circuits.
IEEE INTERNATIONAL SYMPOSIUM on CIRCUITS and SYSTEMS,
Espoo, Jun. 7-9, 1988. Proceedings. p. 1213-16.
DOI: 10.1109/ISCAS.1988.15145

Full Over the Cell Routing

No routing channels between rows of cells

JOHANN, Marcelo; KINDEL, Marcus; REIS, Ricardo.

Layout Synthesis Using Transparent Cells and FOTC Routing

38th IEEE Midwest Symposium on Circuits and Systems

IEEE Circuits and Systems Society, Rio de Janeiro, August 13-16, 1995

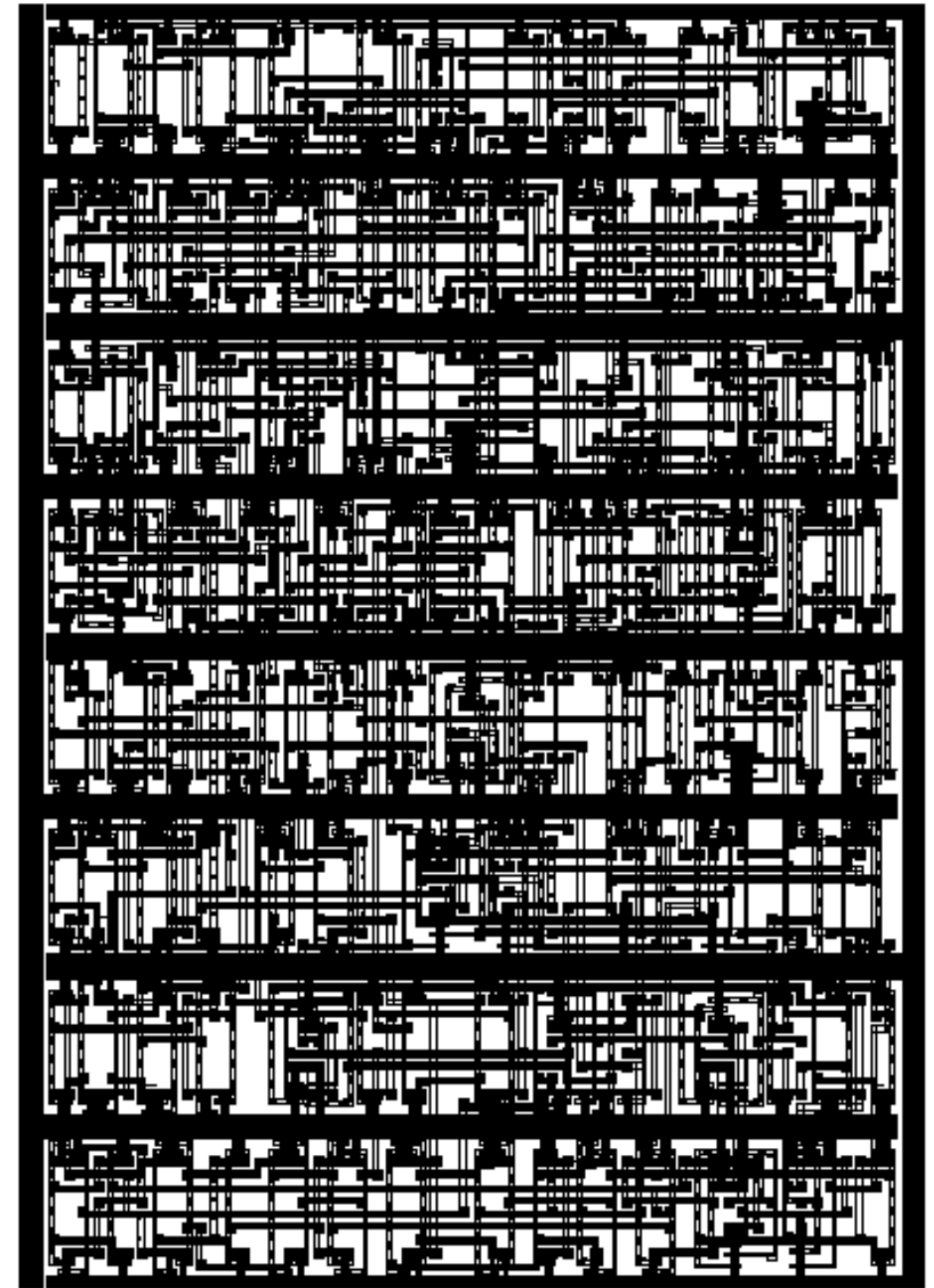
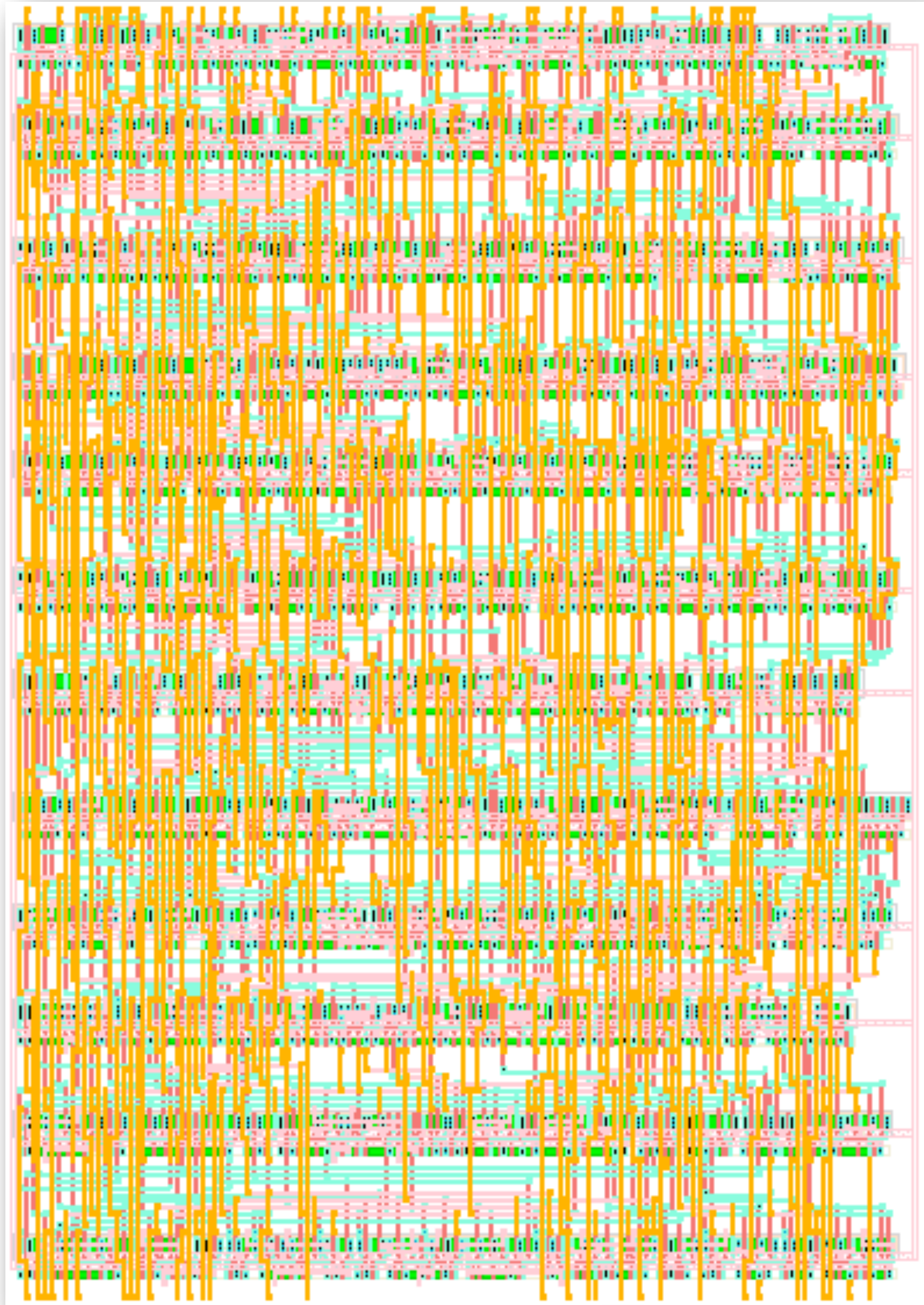


Figure 7: TramoII layout of the Alu181 circuit.

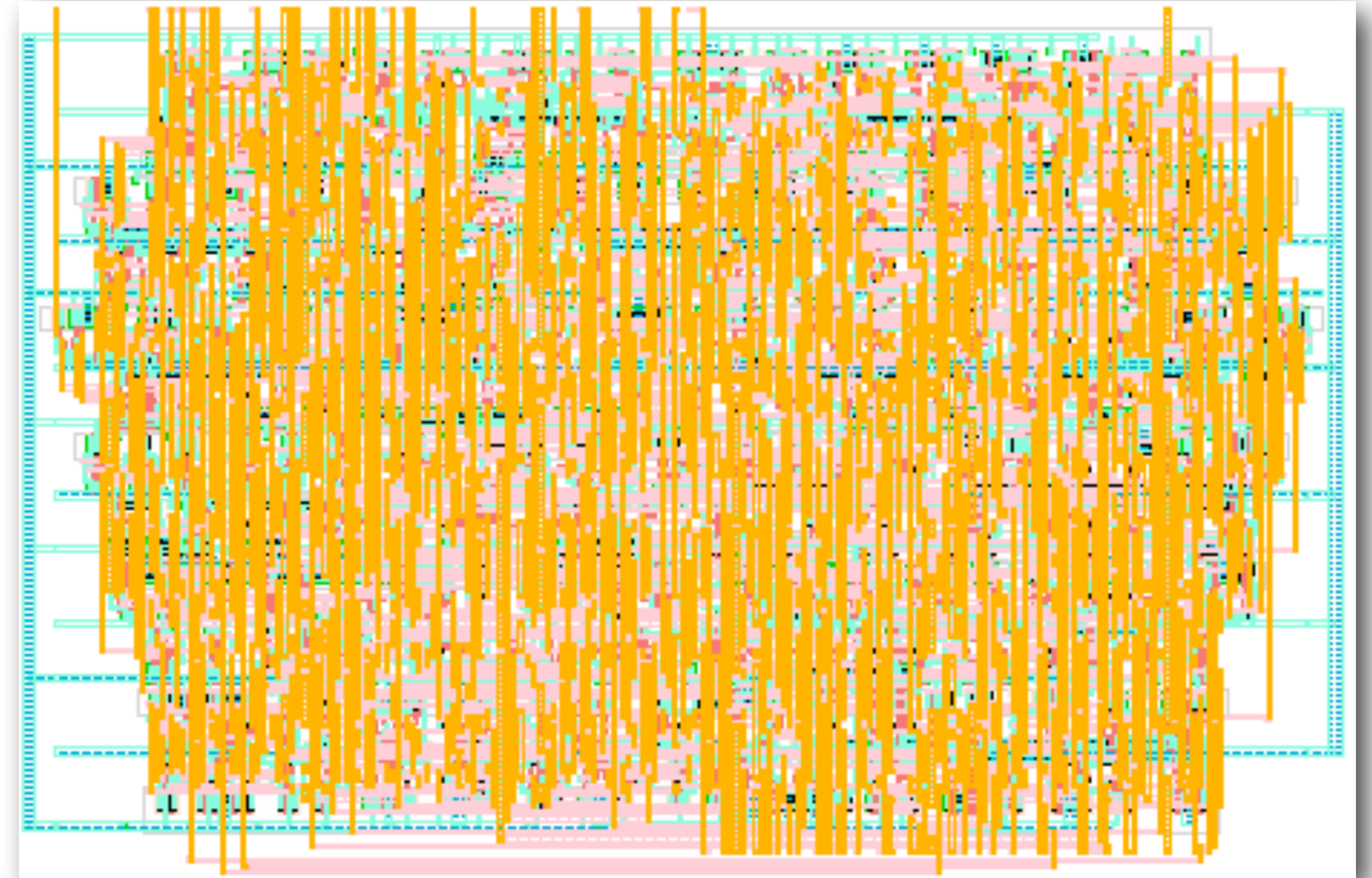
Tools for Automatic Layout Synthesis

TROPIC



Fernando Moraes

PARROT



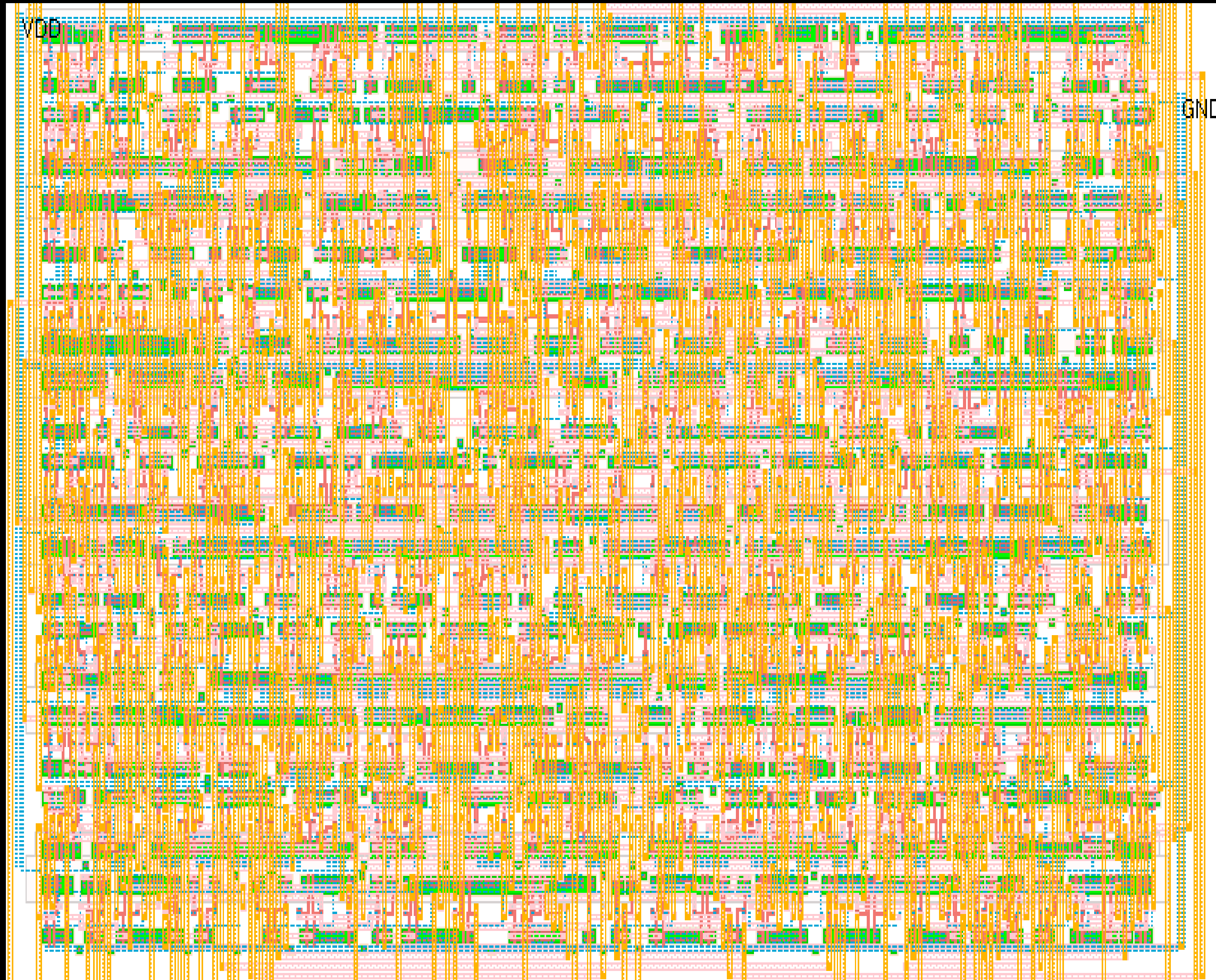
Cristiano Lazzari

1556 transistors

Delay: - 26.0 %

Area: - 37.3 %

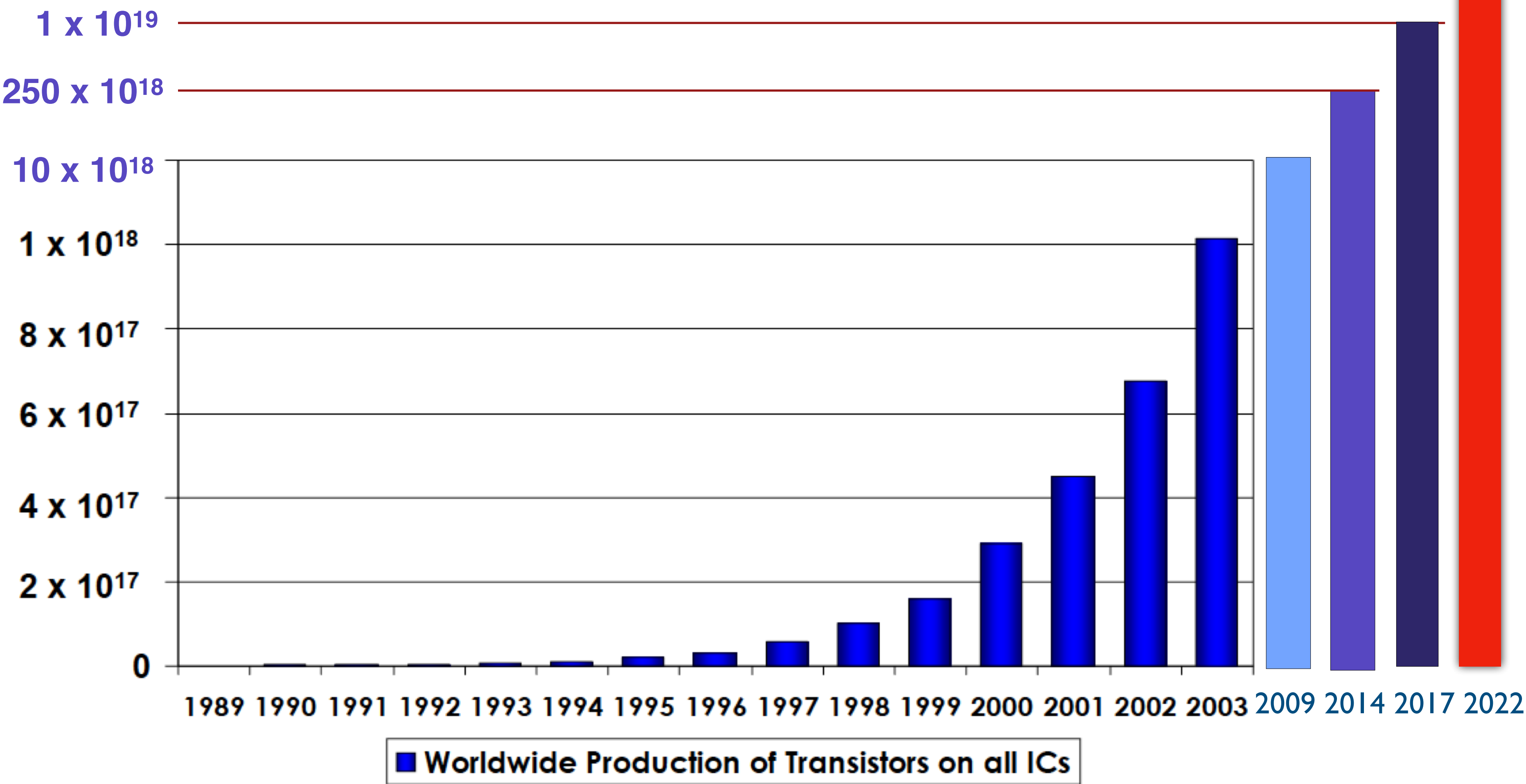
Layout Generated Automatically with Parrot Tool Suite



**From Past to
Present and
Future**

13 Sextillions Transistors Produced from 1947 to 2018

Estimated more than 8 sextillions



Source: SIA

**How much Power
Plants we will need
to cope with the
IoT/IIoE world?**

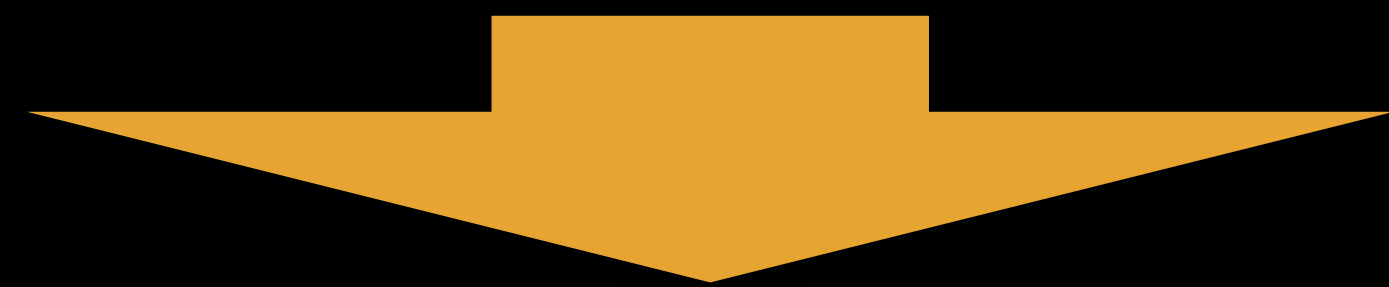
It is Major Issue



Why Optimization is a Keyword in NanoCMOS?

More em More

Embedded Systems that requires Low Power



Dedicated and Optimized ASICs

Most Circuits are using more
transistors than needed

Main goal: to reduce the number
of transistors and connections
in a chip

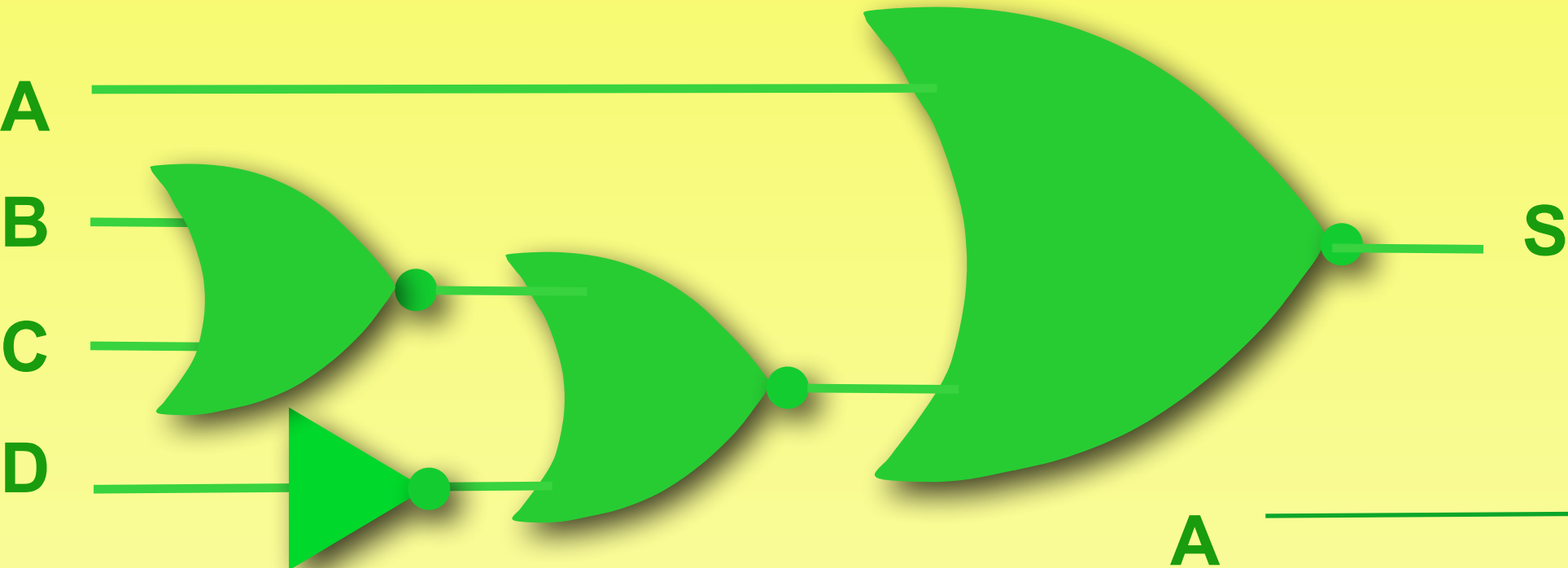
Automatic Layout Synthesis Using Complex Gates (supernates)

NUMBER OF STACKED PMOS TRANSISTORS

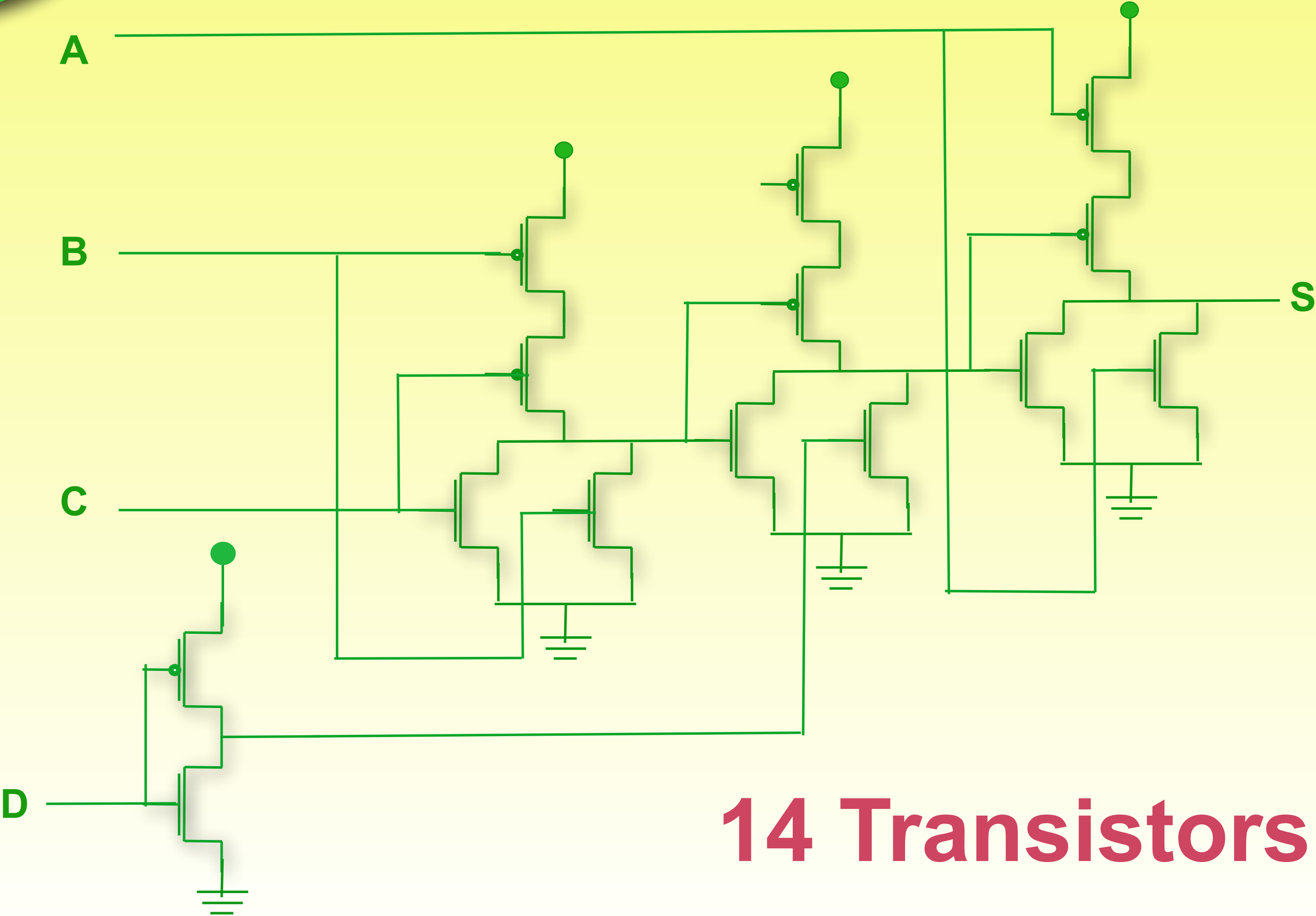
NUMBER OF
STACKED NMOS
TRANSISTORS

	1	2	3	4	5
1	1	2	3	4	5
2	2	7	18	42	90
3	3	18	87	396	1677
4	4	42	396	3503	28435
5	5	90	1677	28435	125803

Example



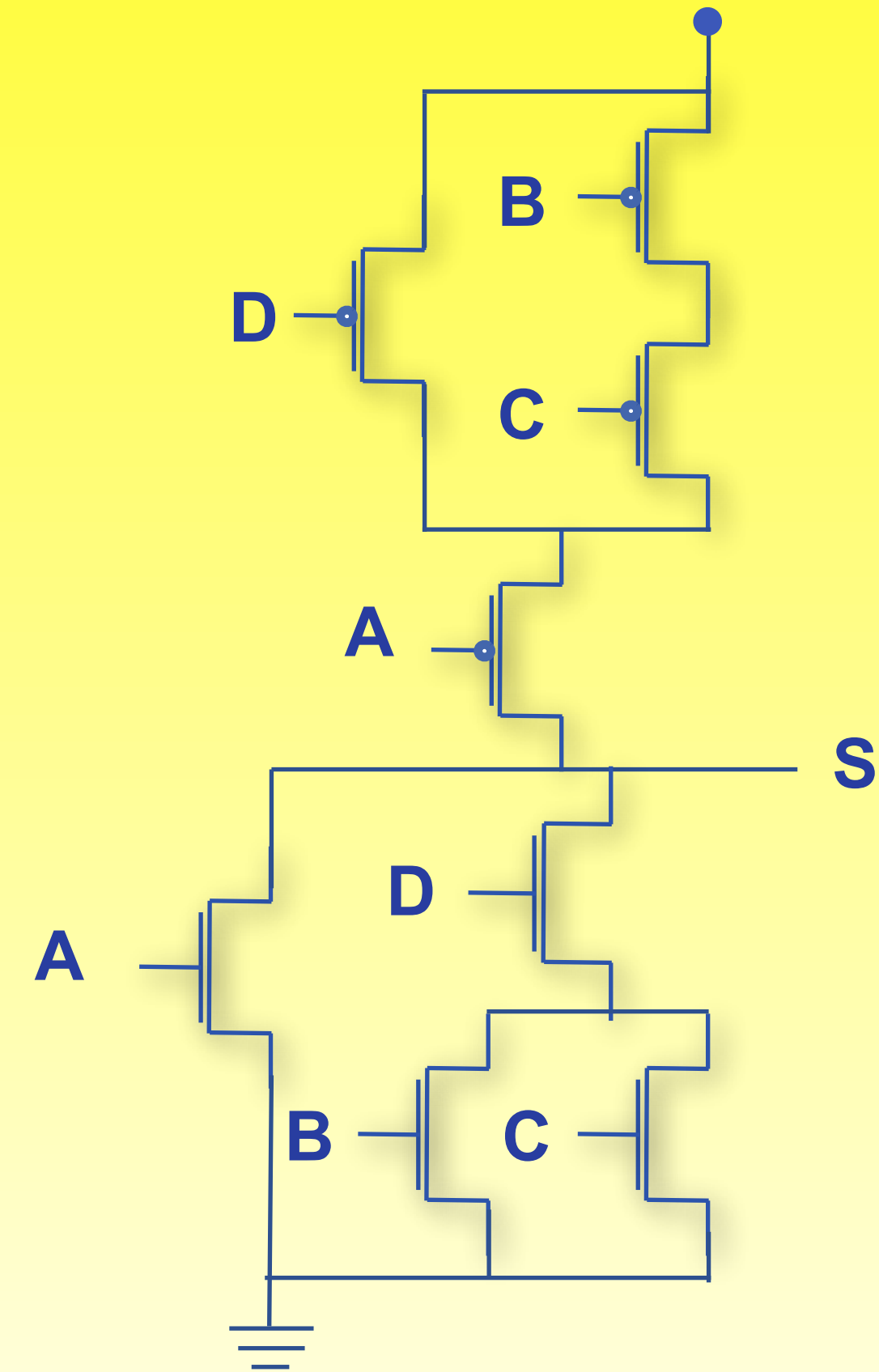
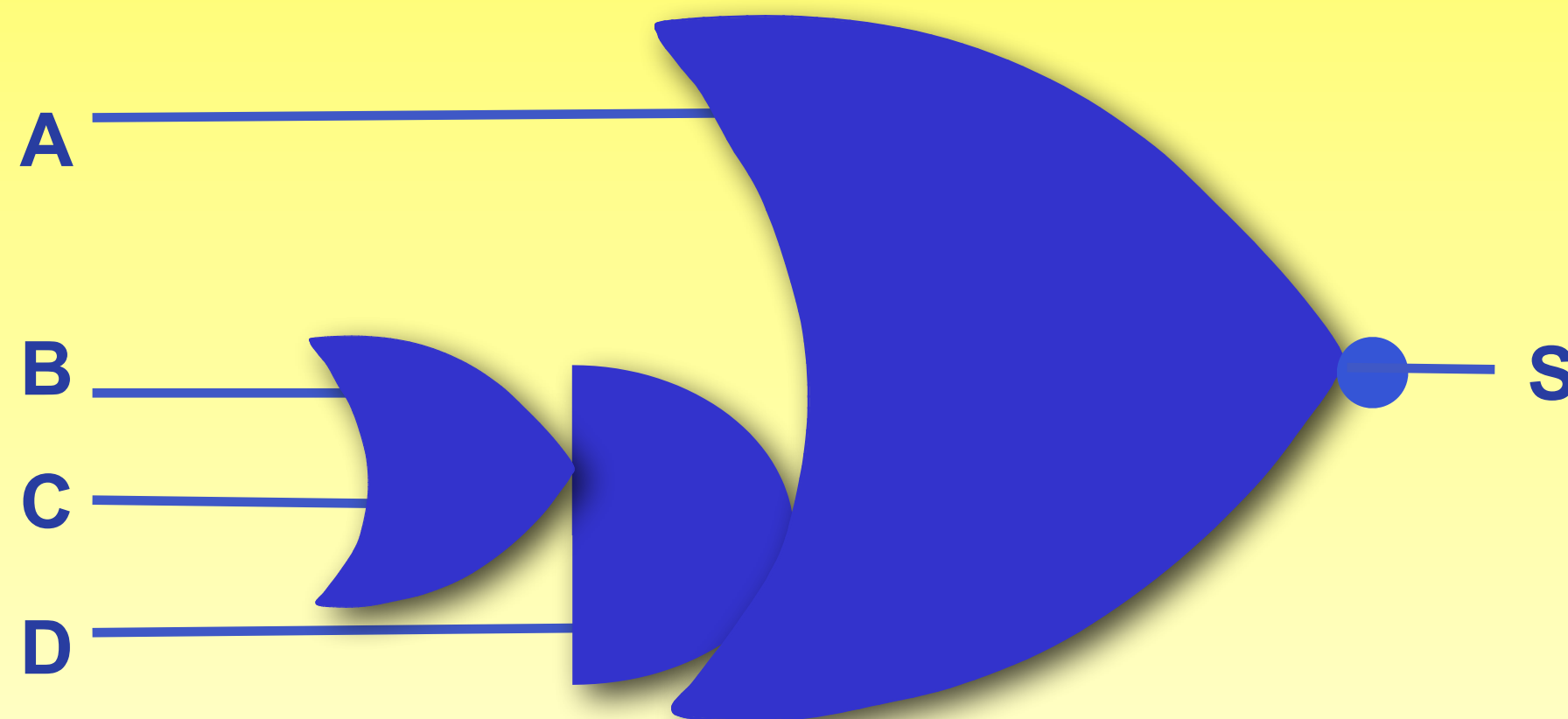
$$S = A + ((\overline{B + C}) + D)$$



14 Transistors

Use of supergates

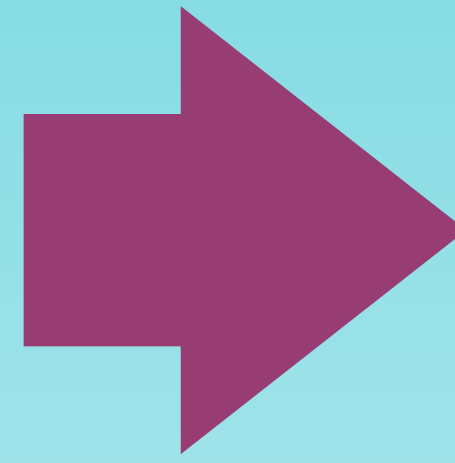
$$\overline{S = A + ((B + C) + D)} \quad \longrightarrow \quad \overline{S = A + ((B + C) \cdot D)}$$



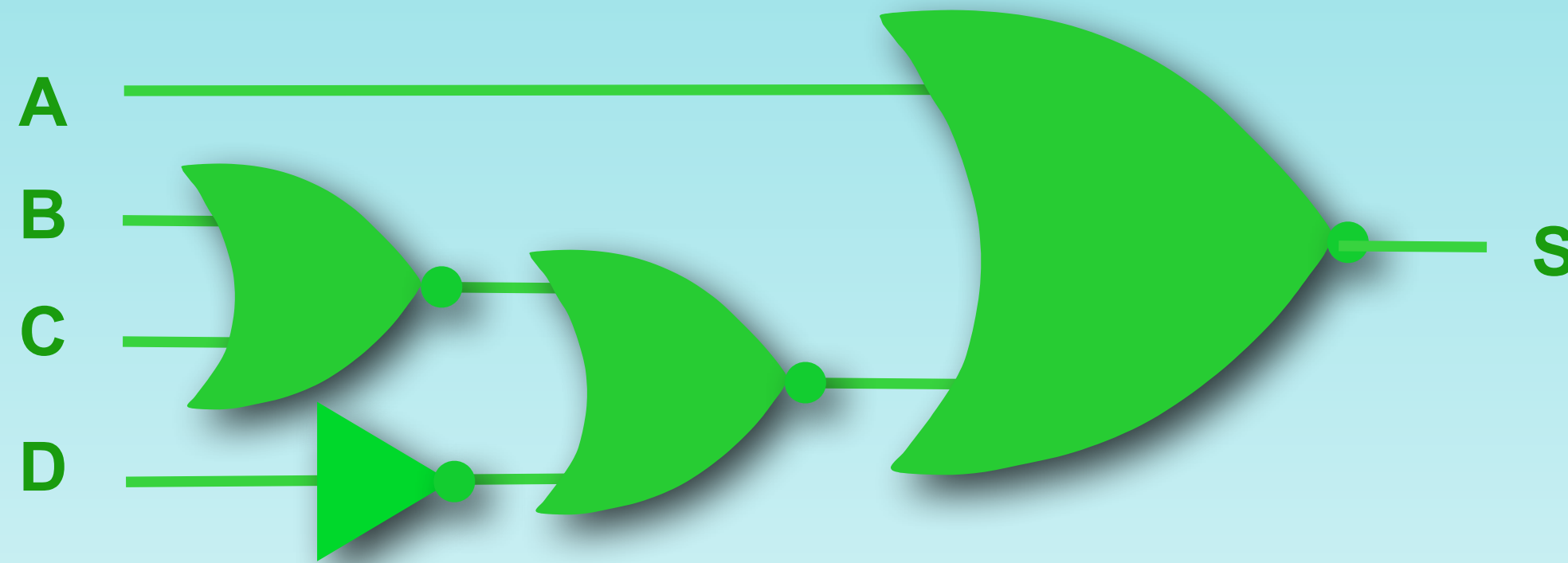
8 Transistors

Use of complex gates

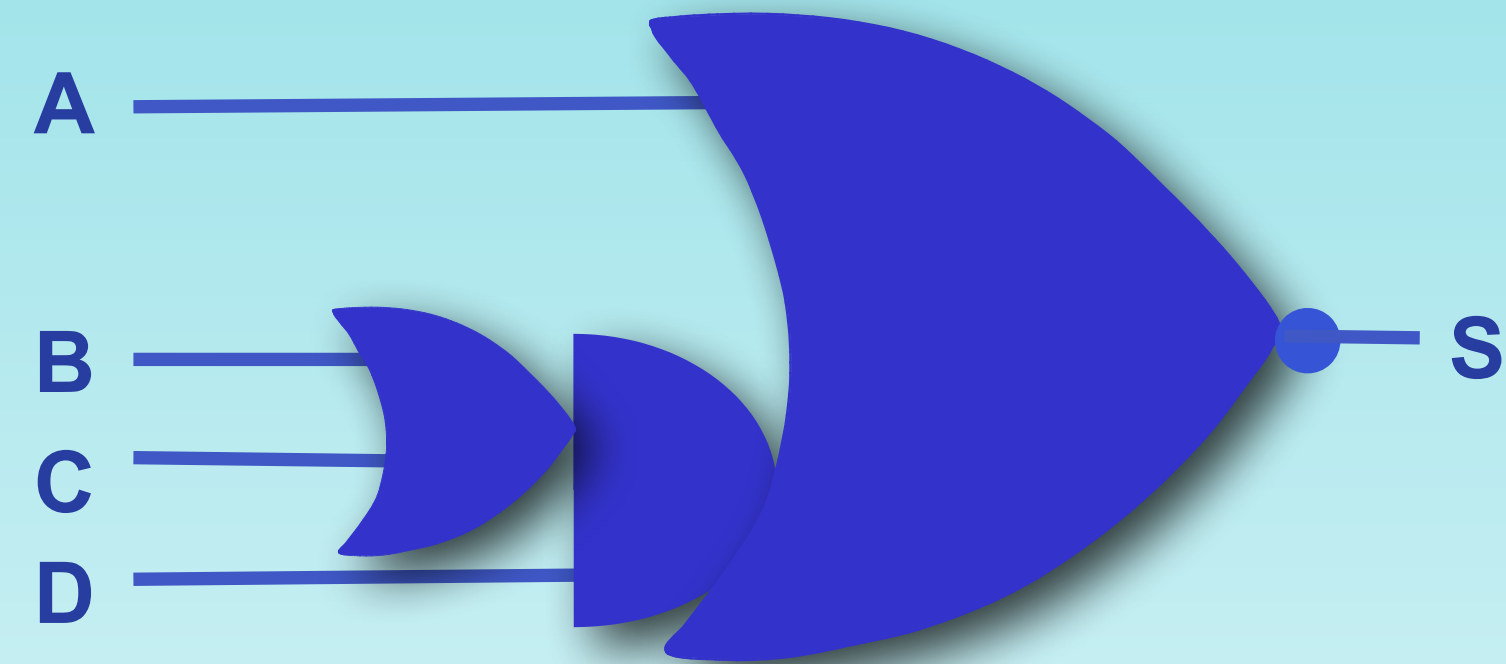
$$S = A + ((B + C) + D)$$



$$S = A + ((B + C) \cdot D)$$



14 Transistors



8 Transistors

3 connections less means also less VIAS and less routing congestion



In Modern Technologies

LESS TRANSISTORS

MEANS

LESS STATIC POWER

Less
Connections and Vias

Helps
Improving
Routing

physical design as the

design of a network
of transistors

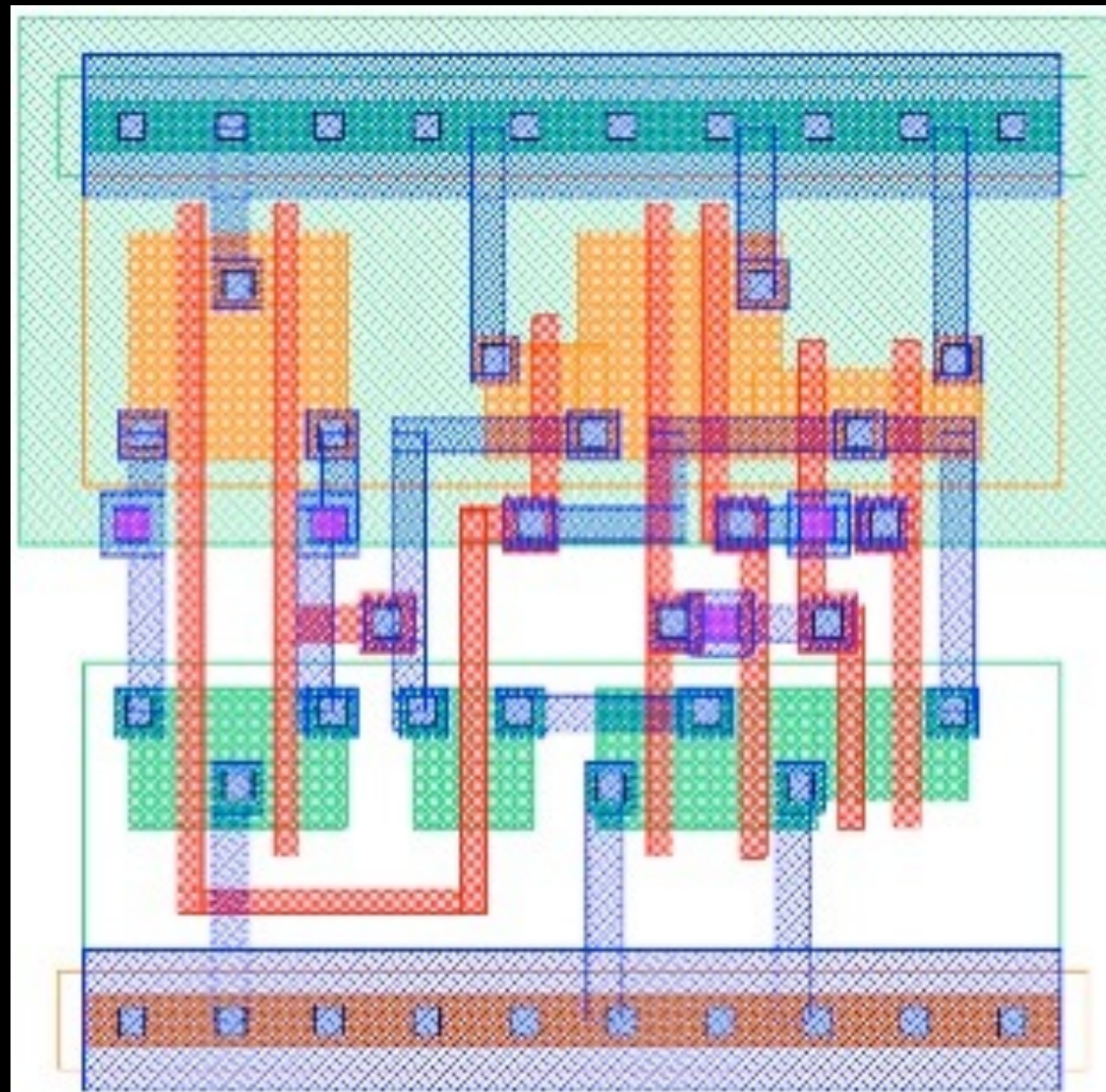
ASTRAN

ASTRAN can generate automatically the layout of
any TRANSISTOR NETWORK

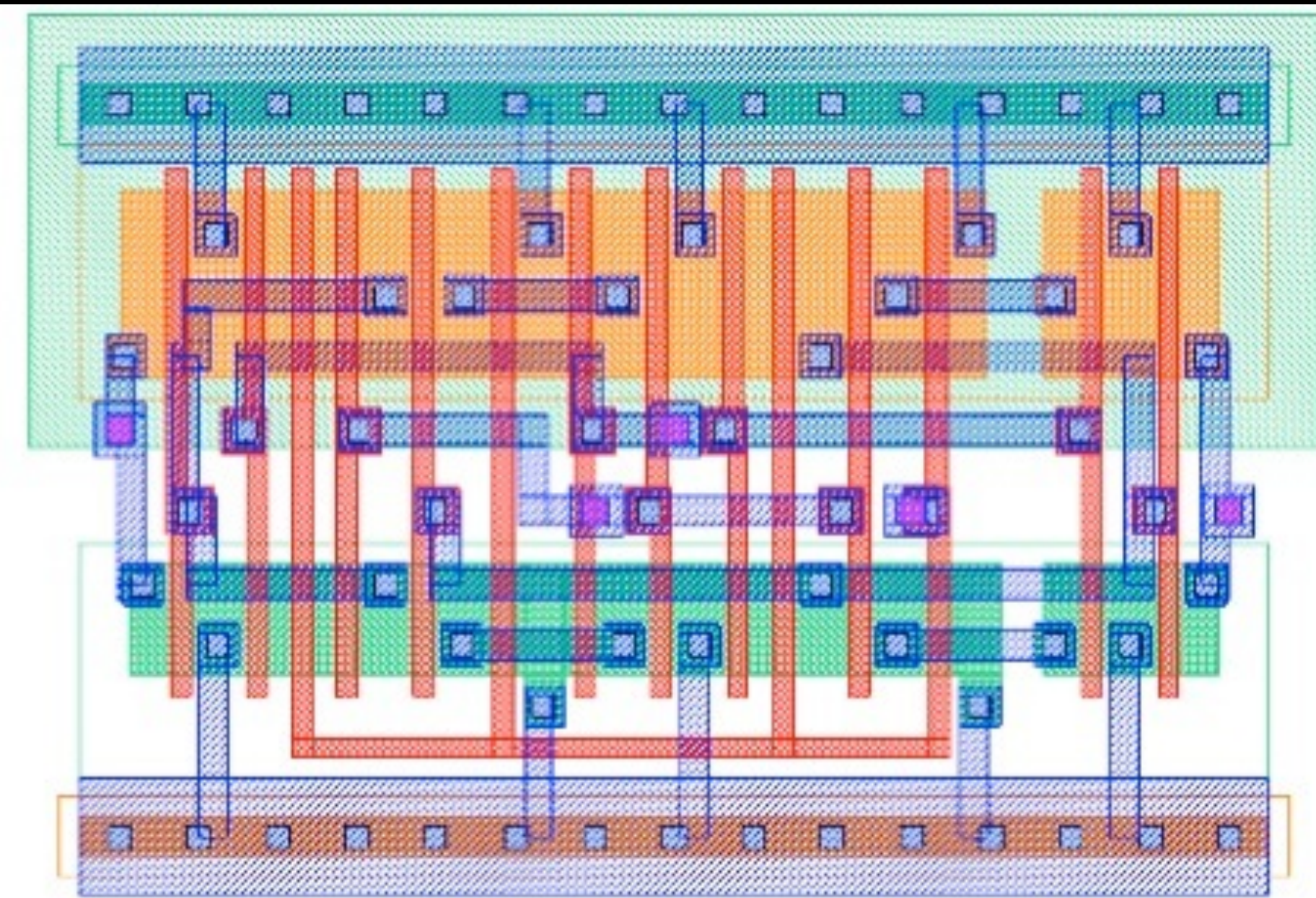
It supports:
transistor folding,
transistor sizing,
and other layout parameters

It can be used to experiment different layout solutions that can cope with many issues, like tolerance to radiation effects and variability

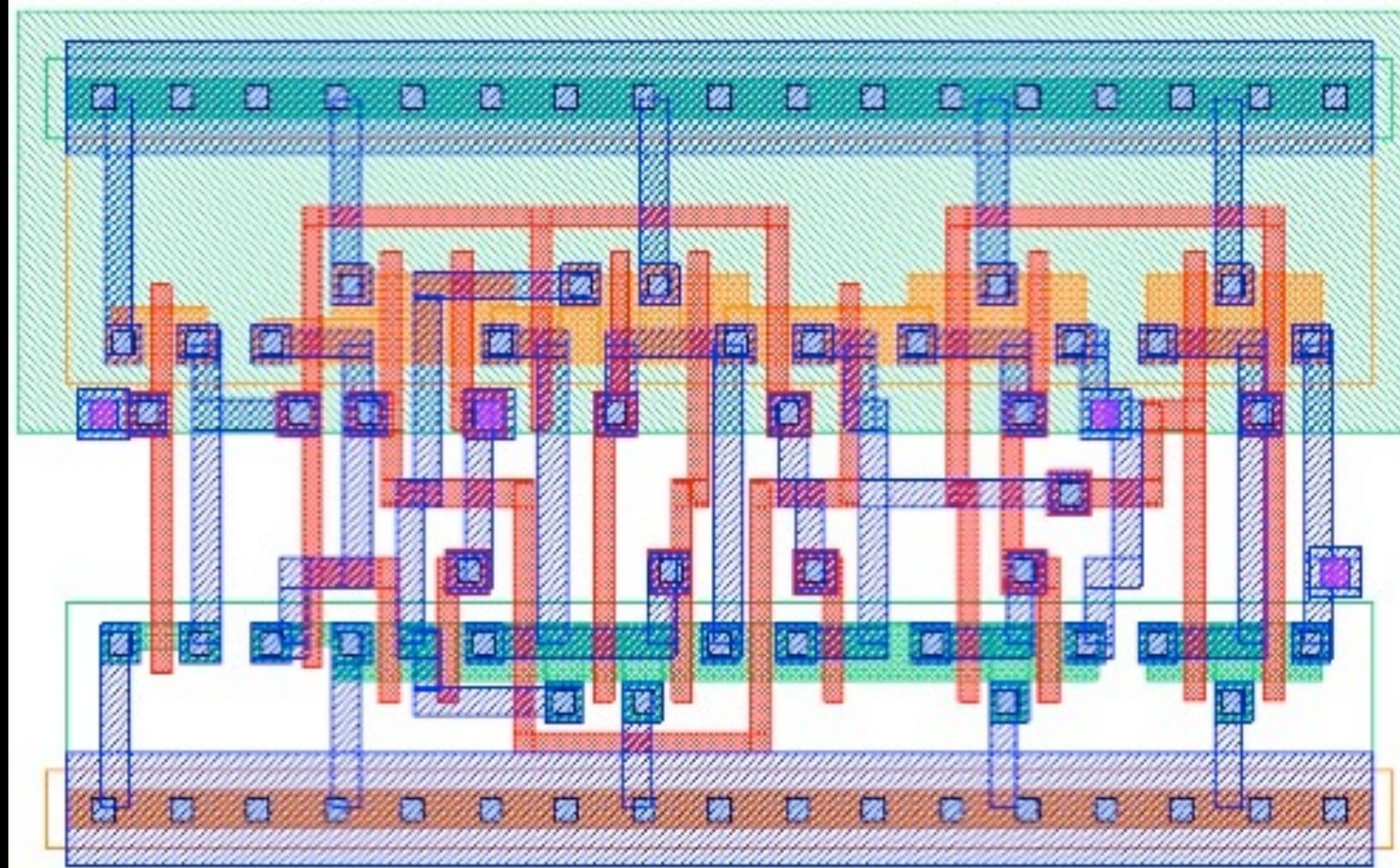
ASTRAN Layouts



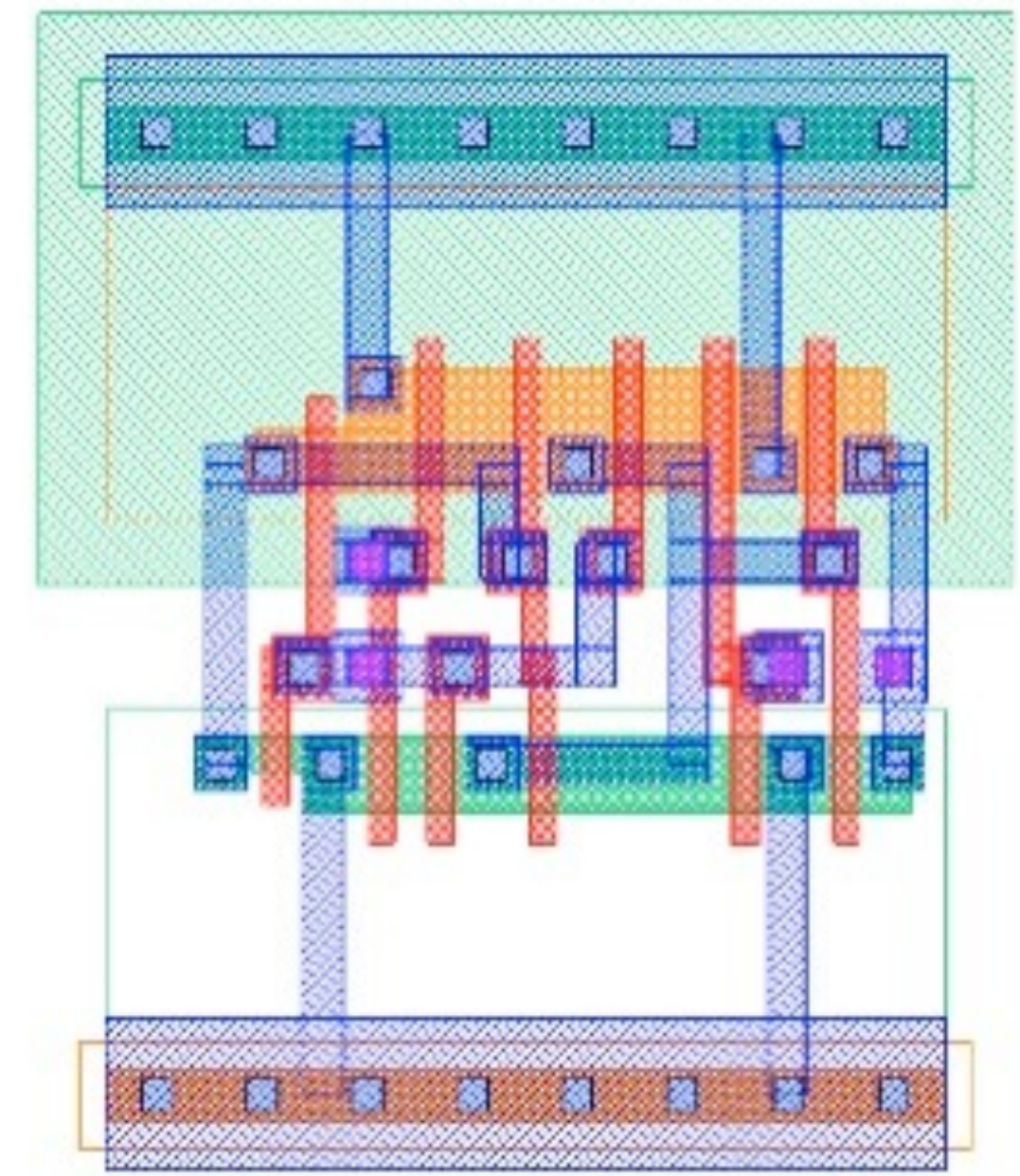
ADD22



ADD32

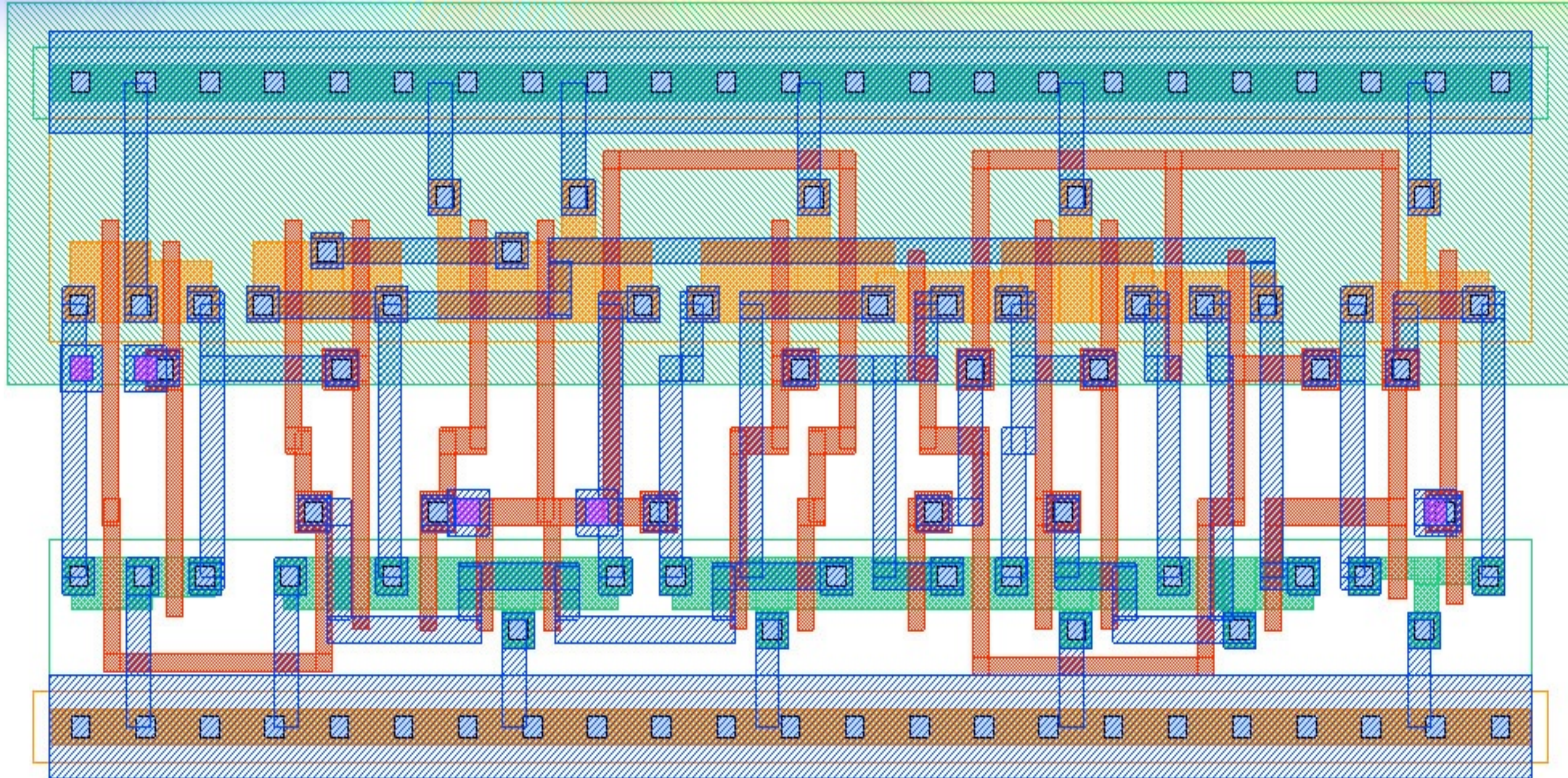


DF1



MUX21

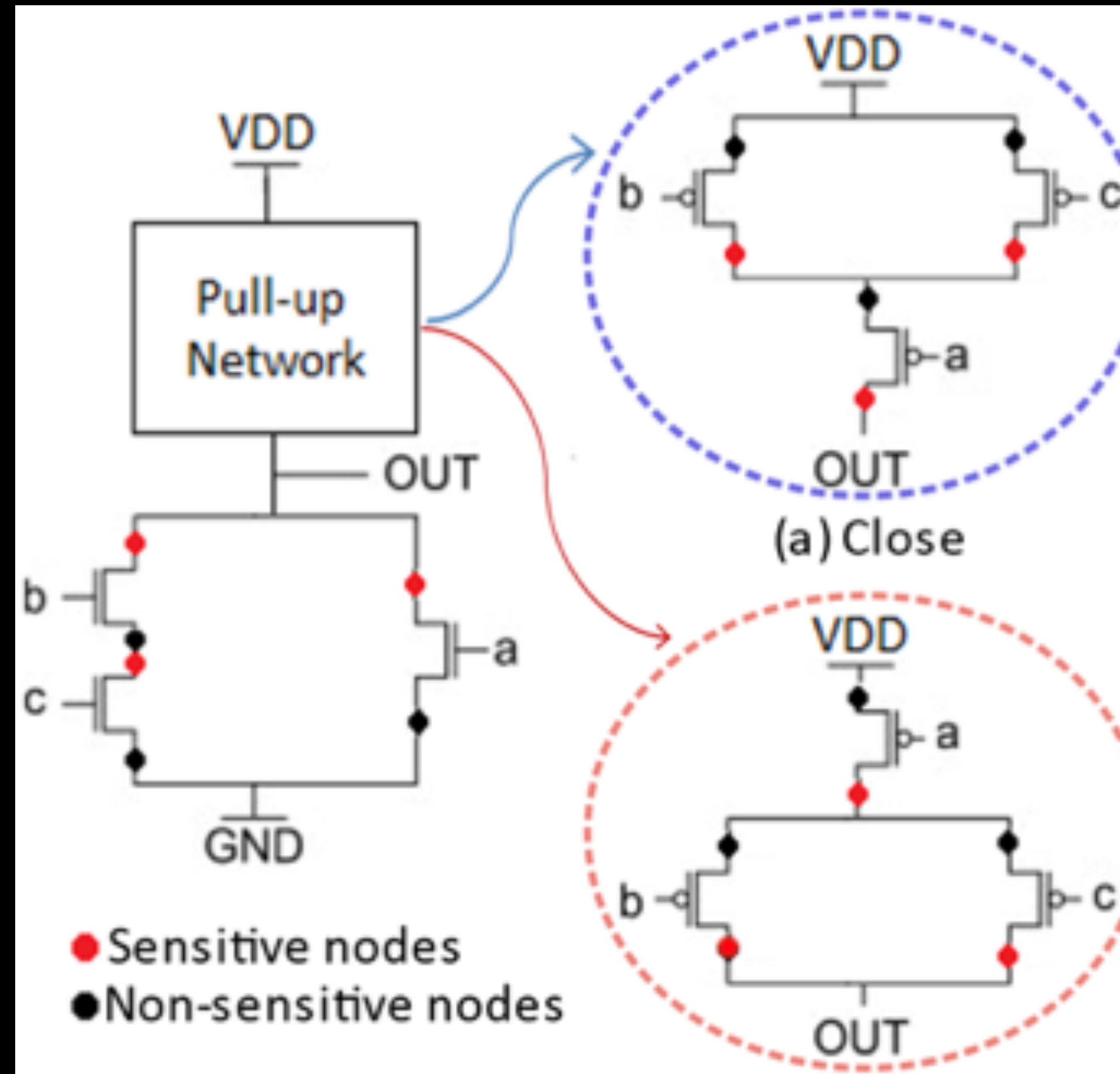
ASTRAN Layouts



Multiplier Carry-Save 4x4

	Standard Cell	Cell Compiler	Gain (%)
Number of Cells	52	28	46
Number of Transistors	634	376	59,3
Area (μm²)	6716	5070	24,5
Delay (ps)	2174	1896	12,8
Power (mW)	6,45	3,97	61,55

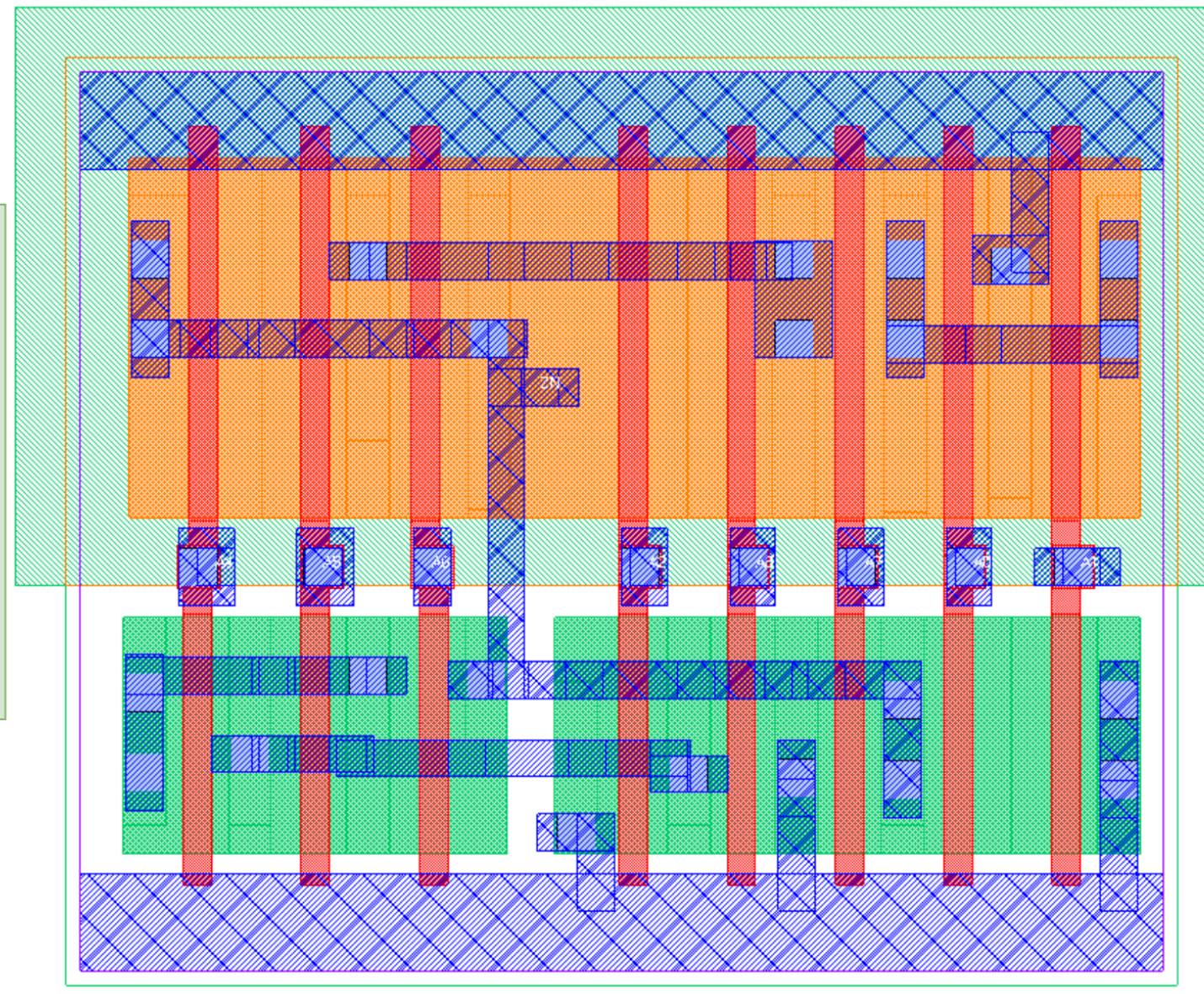
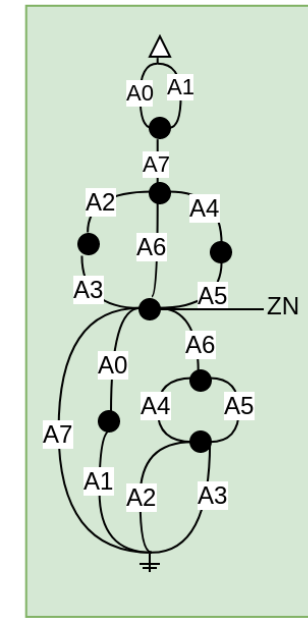
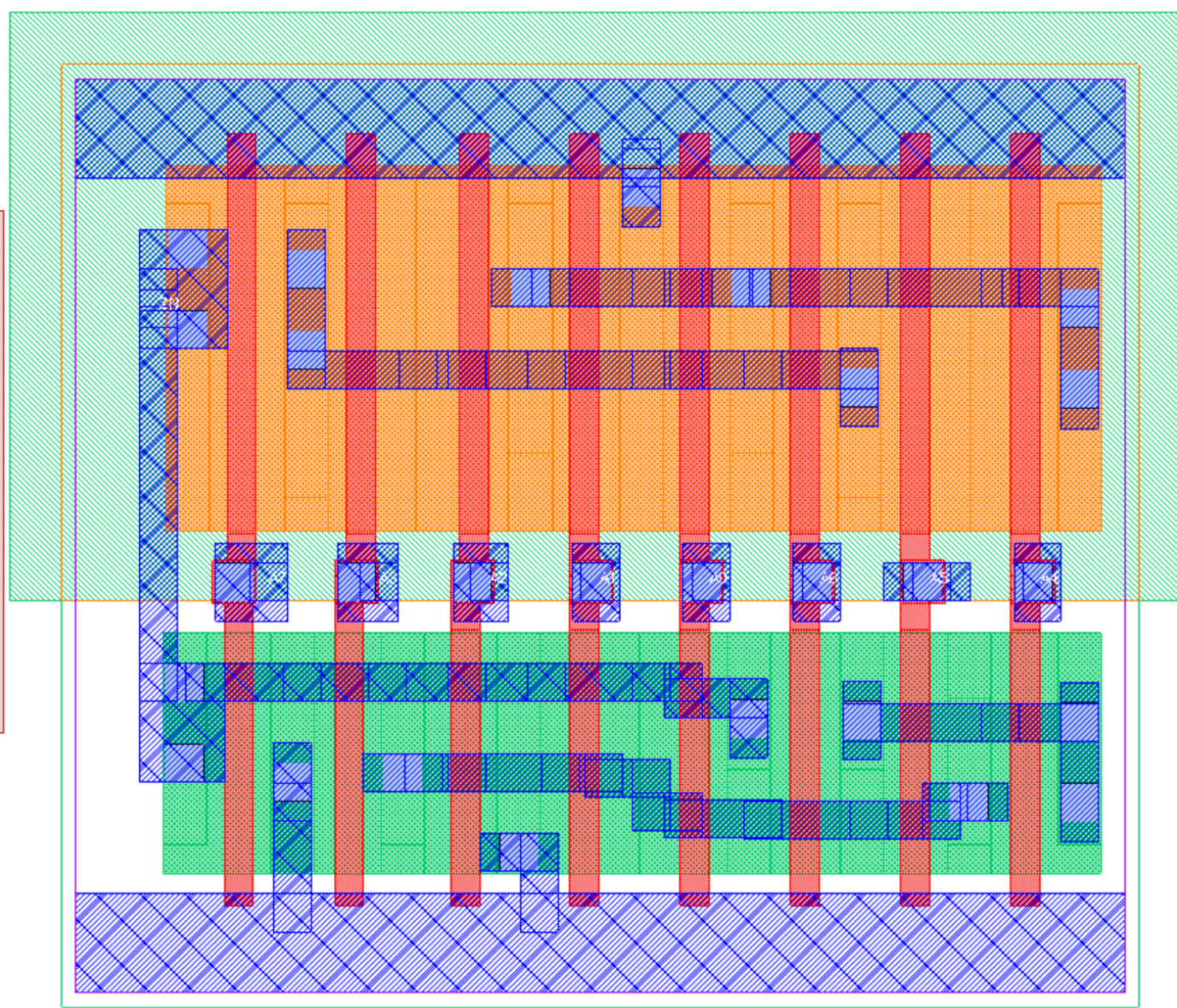
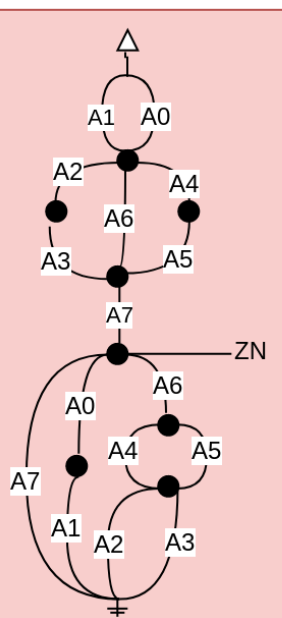
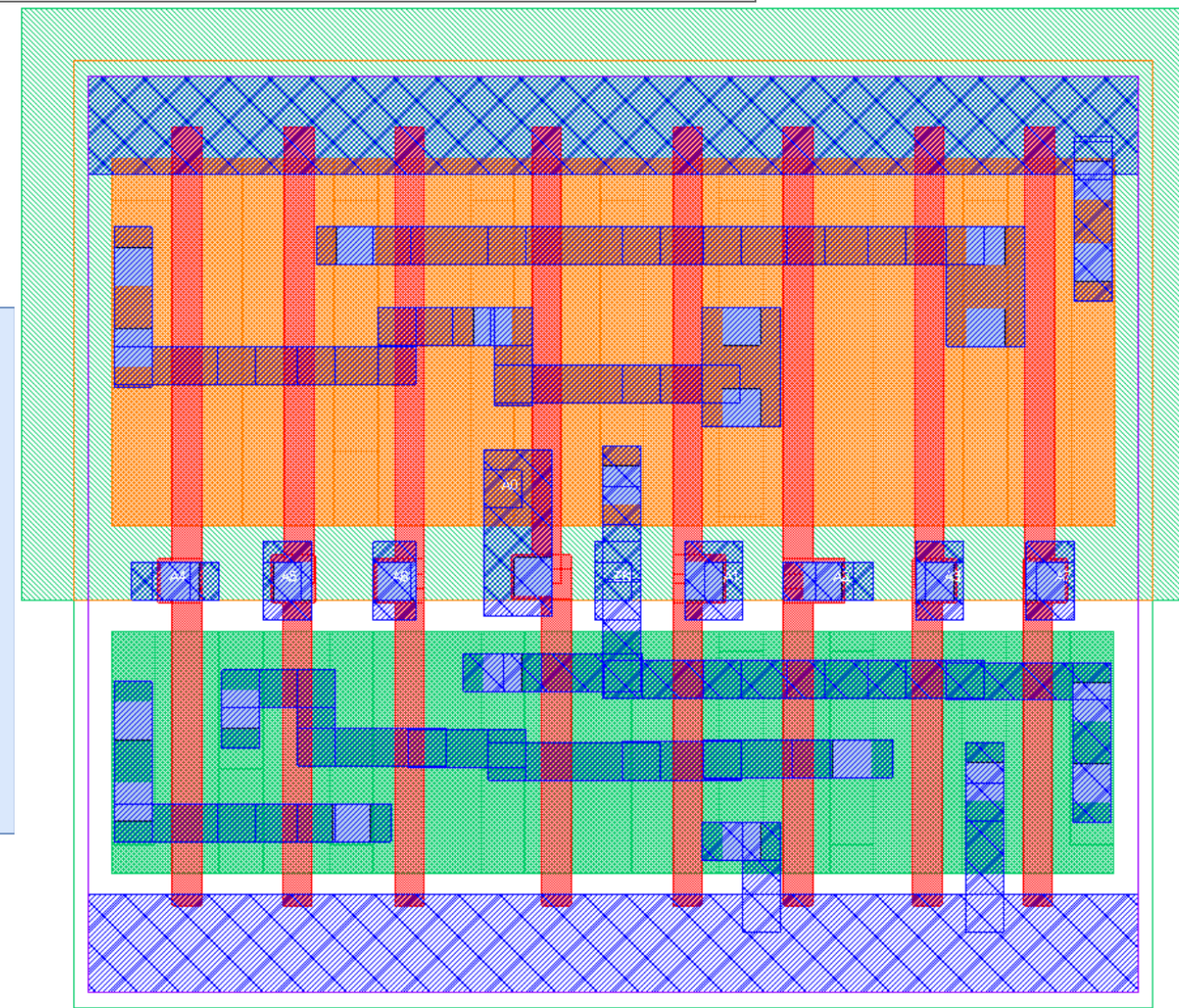
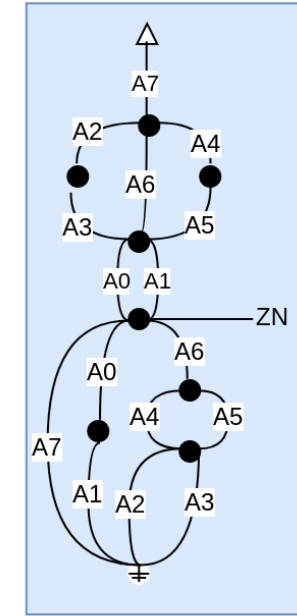
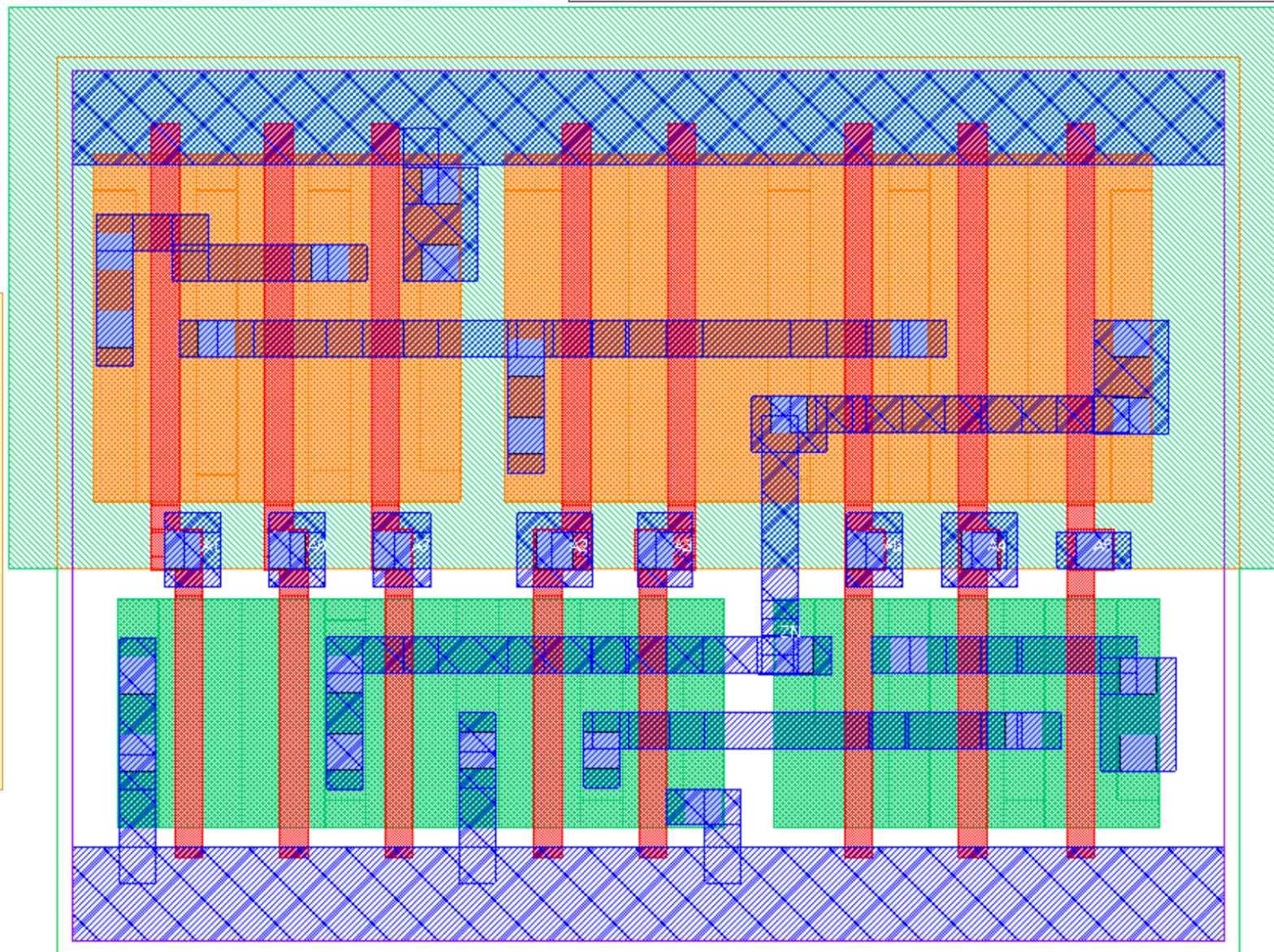
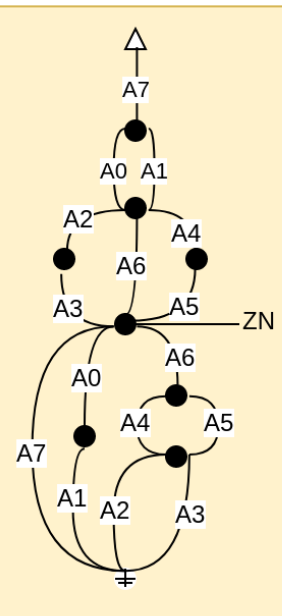
Transistor Arrangements



AOI21 gate designed using (a) close and (b) far topologies

Transistor Reordering

$$ZN = !(((A7+(A0*A1))+((A6*(A4+A5))*(A2+A3))))$$



four different layout options
for a same function

All four options correspond
to circuits with different
transistor orderings

For sure, not all layout optimizations done in past, using nMOS nodes can be done when using nowadays technologies, that are more restrictive

Conclusions

A way to reduce Power Consumption

is to reduce the amount of transistors

Conclusions

**A way to reduce the
amount of transistors is
to use supergates**

Conclusions

keyword in Nanoelectronics

OPTIMIZATION

Conclusions

physical design

as the

design of a network of transistors

place & route of transistors

Something Else

I also would like to thank **all students** that have worked or are working in our research group,
and to my colleague prof. **Marcelo Johann**, a great partner in EDA research and education.

Where are some former graduate students



Renato Hentschke
Henrique Plácido
Guilherme Flach



Gracieli Posser
Gerson Scartezini
Mateus Fogaça
Jerson Paulo Gux
Carolina Metzler



Tiago Reimann



Marcus Kindel
Fábio Klein Ferreira
Cristiano Lopes dos Santos



Lucas Brusamarello



Felipe Rosa da Rocha
José Carlos Sant'Anna Palma
Leandro Nunes



Daniel Lima Ferrão



Fabio Rossato da Silva



Thiago Assis



André Oliveira



Cristiano Lazzari
João Azevedo



Guilherme Medeiros
Marco Terres



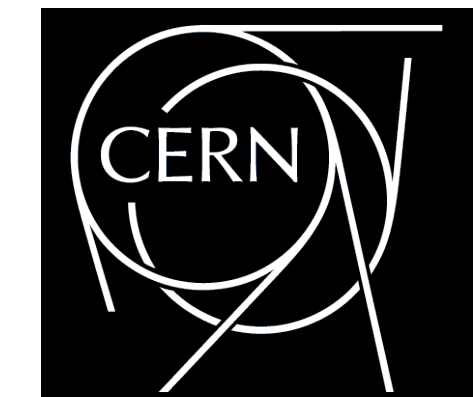
Jorge Tonfat



Chris Dennis Tomás Horna



Paulo Armando Schermer



Ygor Aguiar



Adriel Ziesemer Junior

Where are some former graduate students



Gustavo Wilke



Carlos Hurtado



TRAJECTA

Rogério Figurelli Gomes



Lucas André de Paris



William Guareschi



Marcelo Boeira Barcelos



Luciana Mendes Silva



Felipe Pinto
Daniel Silva Guimarães Jr.



Julia Casarin Puget

Where are some former graduate students



Marcelo Lubaszewski
Marcelo Johann
André Reis
Fernanda Kastensmidt
Marcello Macarthy



Leandro Indrusiak



Fernando Moraes
Marcos Stemmer
Fabian Vargas



João Fragoso



Calebe Conceição
Gustavo Neuberger



Rodrigo Possomai Bastos



Sandro Sawicki



Roger Caputo Llanos



Diego Tumelero



José Guntzel
Cristina Meinhard



João Baptista Martins



Lisane Brisolara



Sidinei Ghissoni



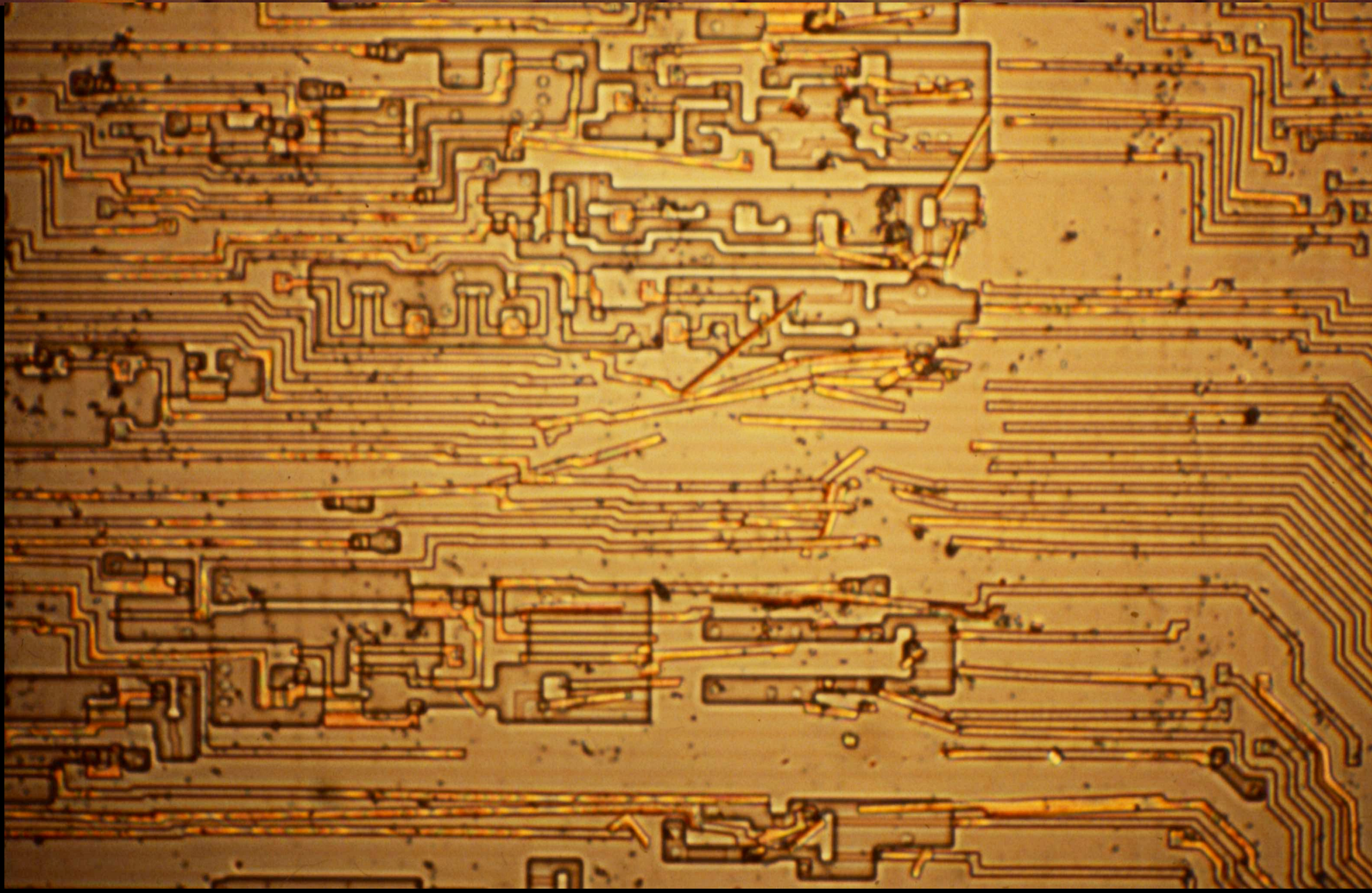
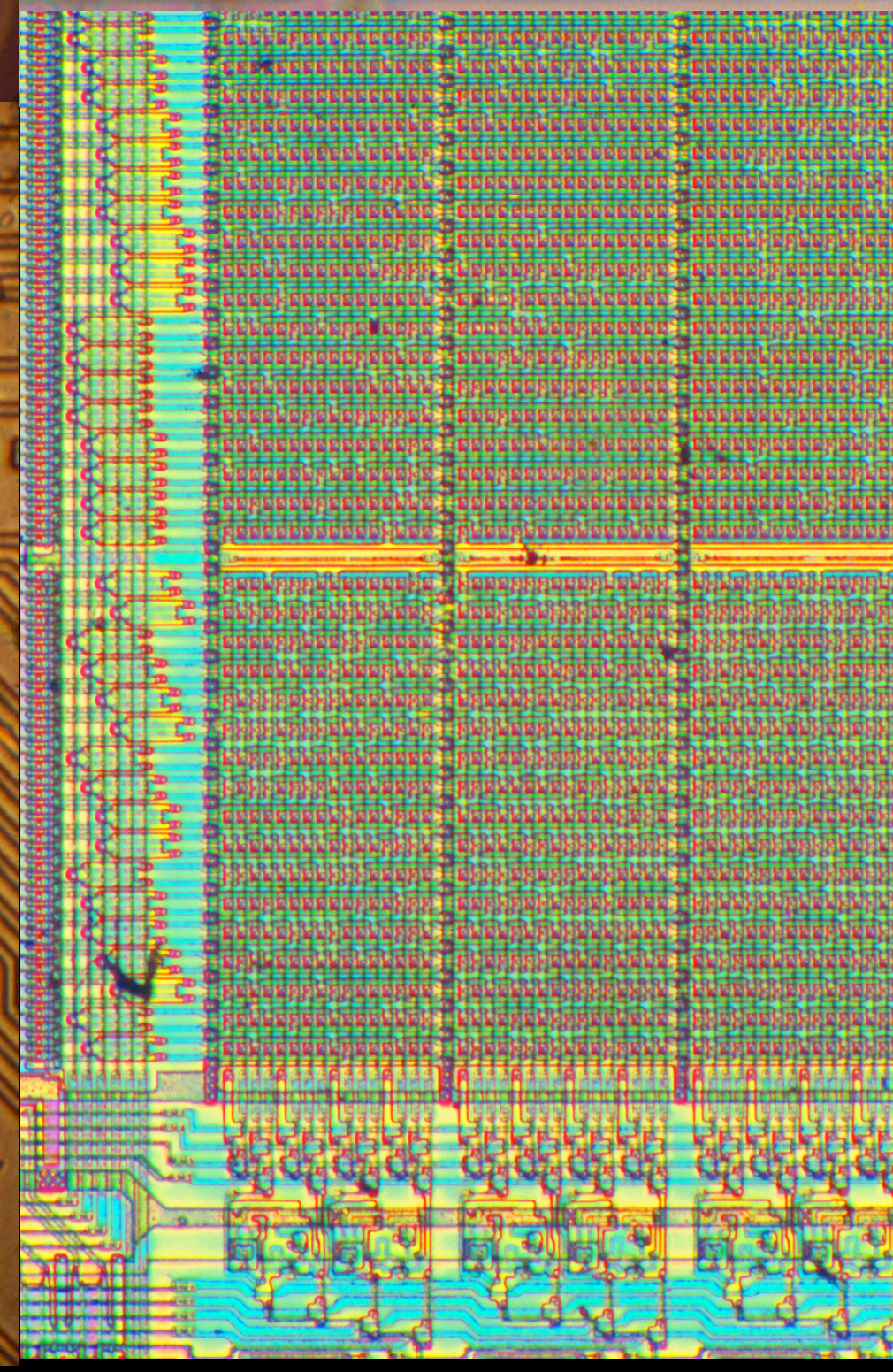
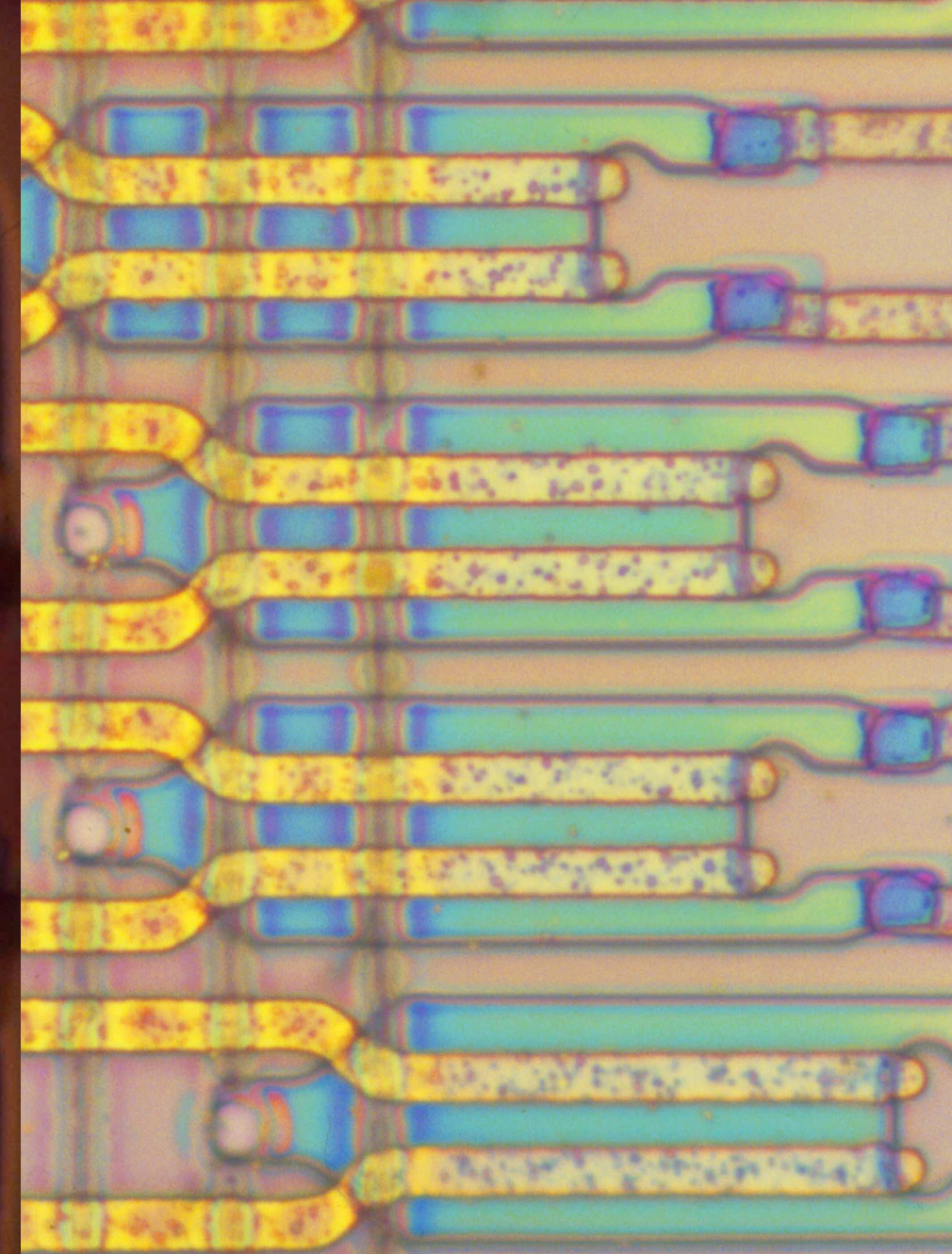
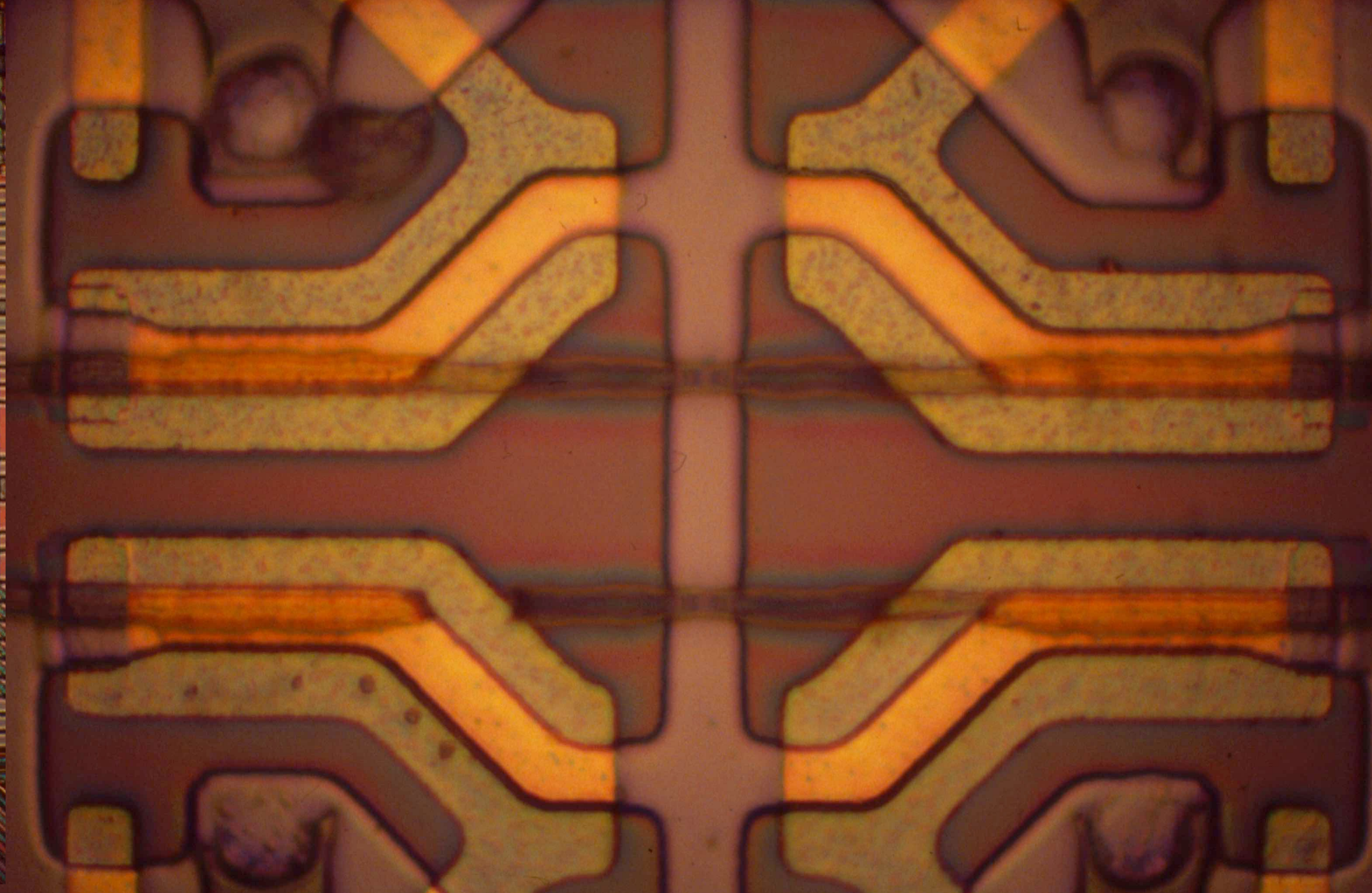
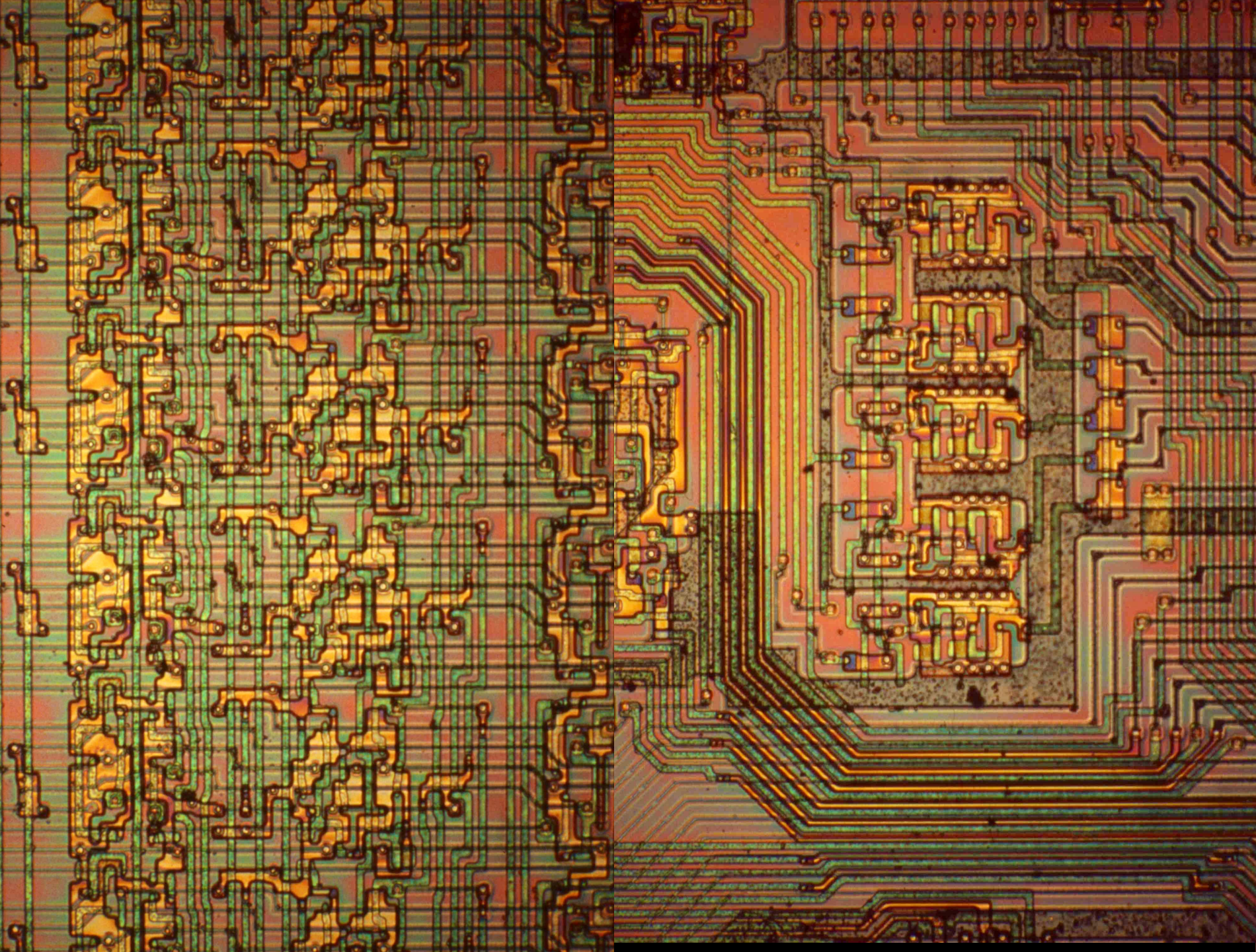
Walter Calienes Bartra



Ricardo Jacobi



Alexandra Zimpeck



more photos at:
facebook.com/artchips1

Ricardo Reis

Physical Design Optimization

From Past to Future

Ricardo Reis

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