Transistor Based Design Beyond Standard Cell Methodology

Renato Hentschke

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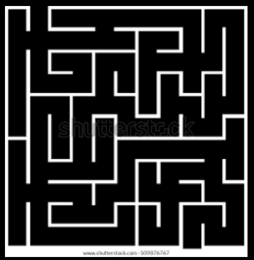
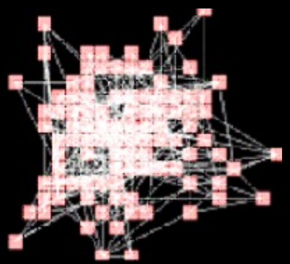
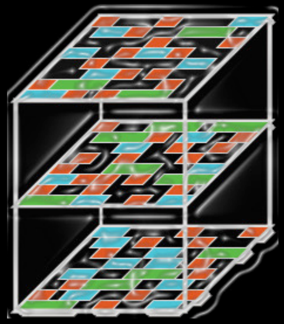
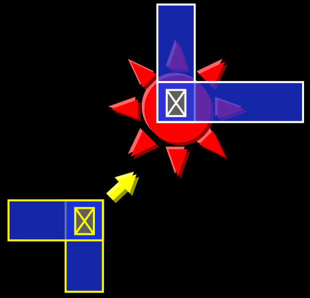
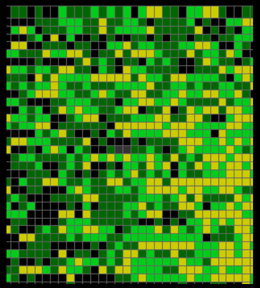
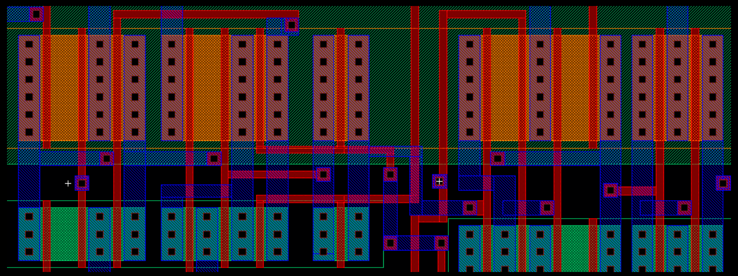
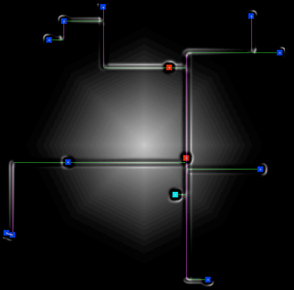
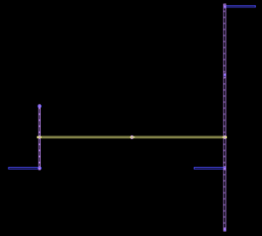
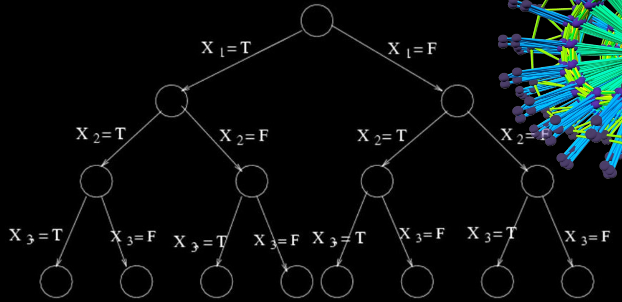
I work on Physical Design since 1998 with professor Reis

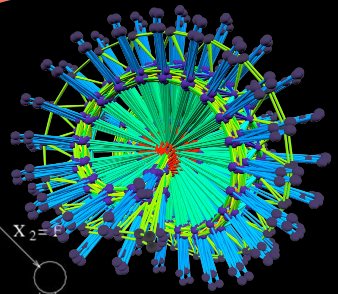
UFRGS IBM intel SYNOPSYS Silicon to Software

1998 2002 2007 2020

MSc PhD Intel Synopsys



For some, Physical Design research was winding down…

But not for professor Reis

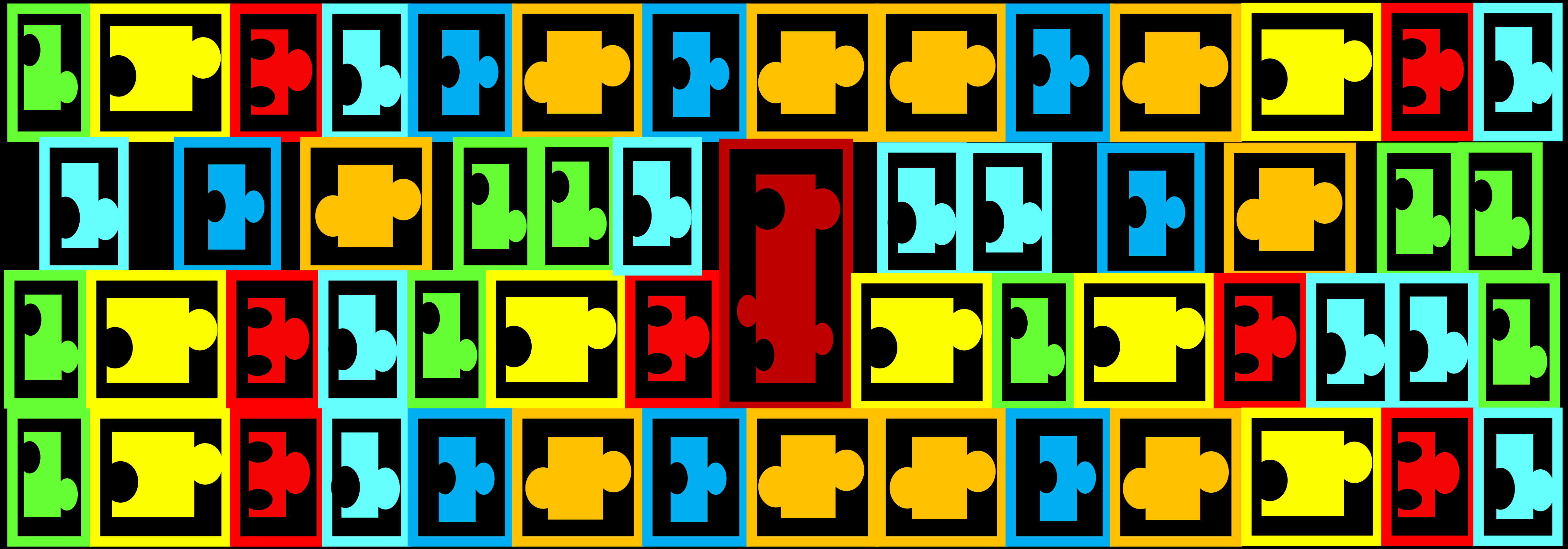
In a direct translation that would be:
there is fabric for the sleeve

Tem pano para manga

Brazilian slang for: "there is a lot to research about, there is a lot of work to be done, etc"

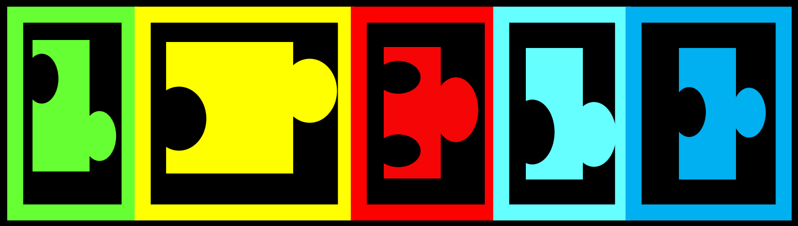
That kept me going…

Standard Cells are crafted to perfection as an individual



But they don't really connect perfectly…

Looking closer, small adjustments can make cells fit better



Unique cells, made for the location

Is it legal???

It goes against the standard cell methodology.

Agenda

1st part: SAT Solvers for Physical Design

- My personal experience, lots of existing publications
- Optimal solutions for known Physical Design Problems

2nd part: Breaking the standard cell paradigm

- Why don’t cells connect very well
- Opportunities for applying optimal physical synthesis techniques for small problems

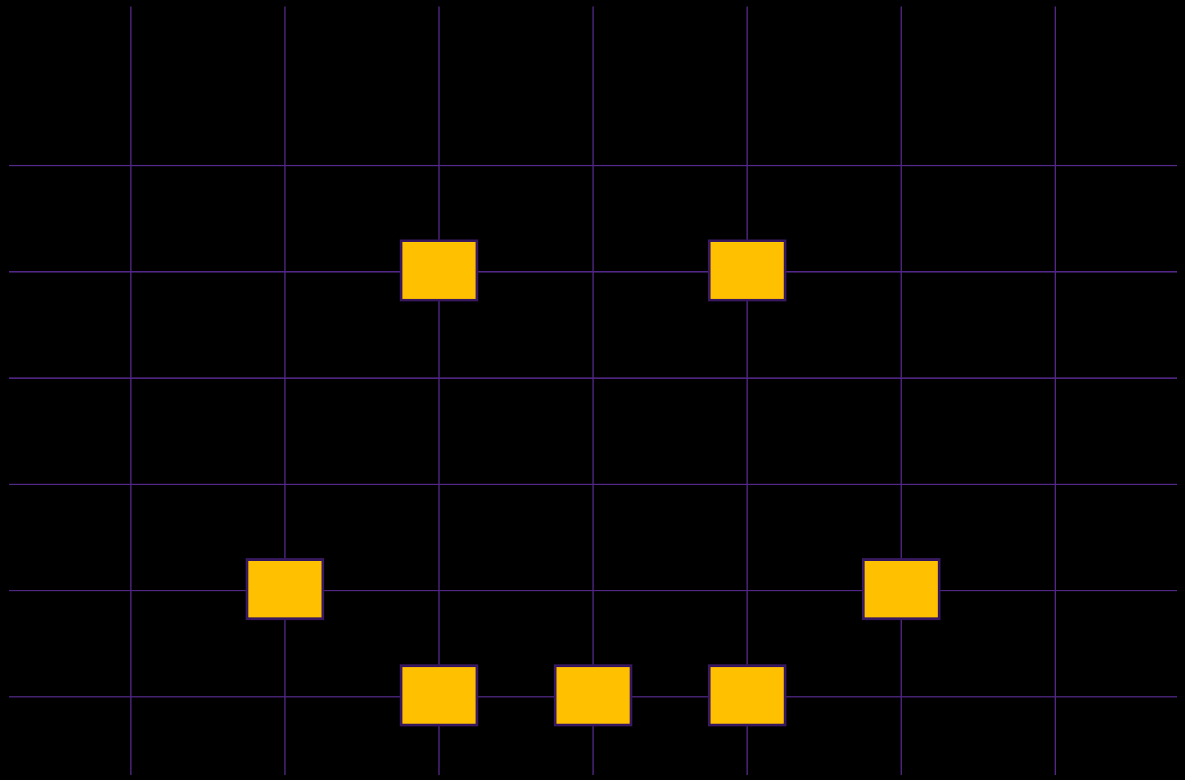
SAT solvers for Physical Design

- Everybody knows that Physical Design Problems are NP-Complete/NP-Hard.
- Optimal solutions can be found for small problems.

- Traditional net-by-net techniques cannot efficiently solve existing design constraints
- Need to deal with present and absent objects

- SAT solvers are way faster than they used to be
- SAT solvers' capacity is huge, can deal with >1B variables
- In my experience, SAT solvers are faster than dedicated code such as exhaustive search

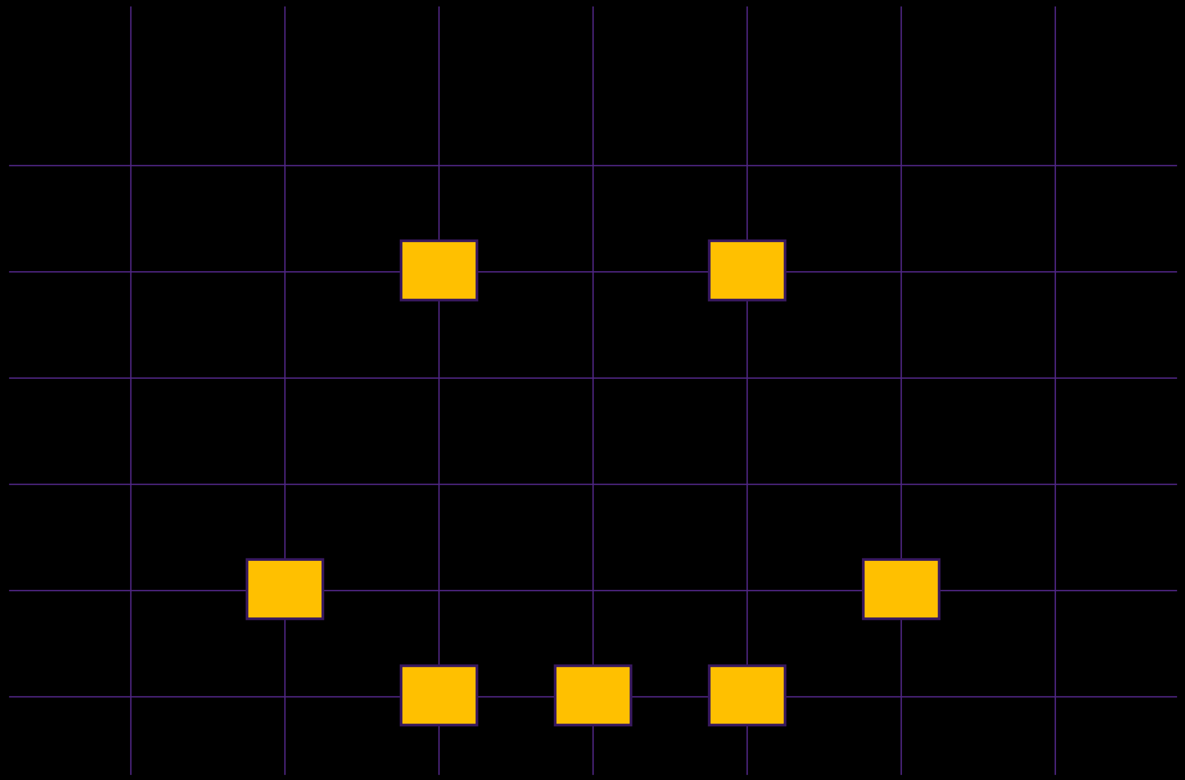
Given a discrete world, SAT Solvers can model any design rule



1 Vias cannot form a smiley face shape

- This can involve up to 8 different nets, net-by-net algorithms will struggle to support such rule without loss of routability.
- SAT solvers can easily model this rule since they consider the all nets at the same time.

Given a discrete world, SAT Solvers can model any design rule



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- This can involve up to 8 different nets, net-by-net algorithms will struggle to support such rule without loss of routability.
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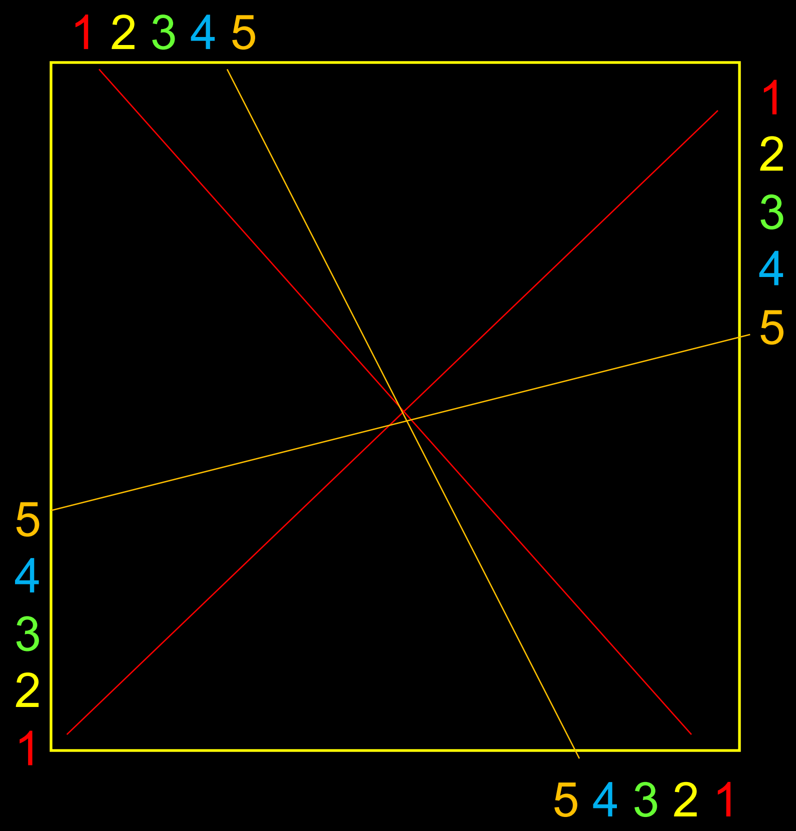
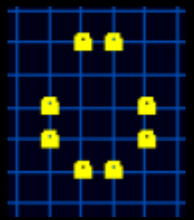
2 Vias can **only** form a smiley face

- Trying to make a stronger point that SAT solvers can model any rule.

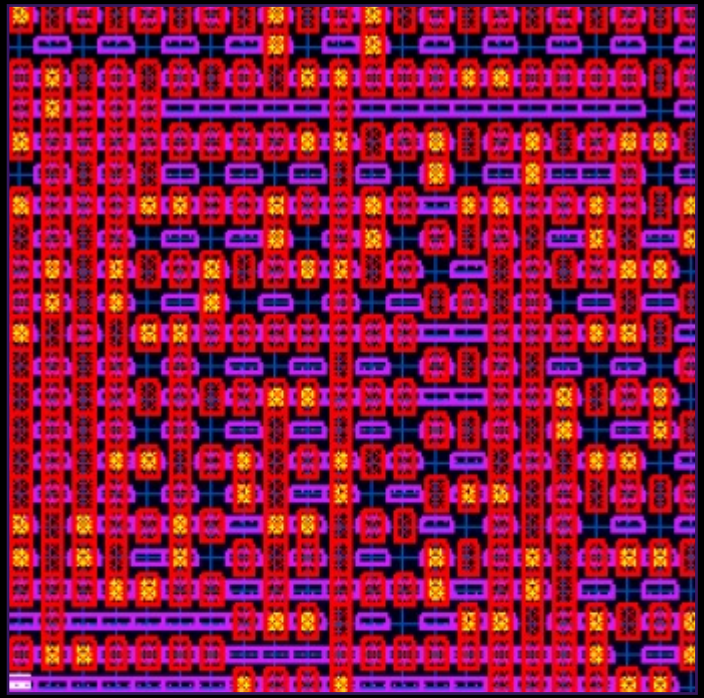
An even more difficult route problem



vias can only appear in a smiley-face configuration



Solution, showing both layers and vias



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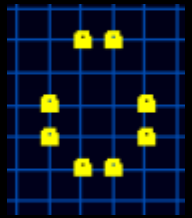
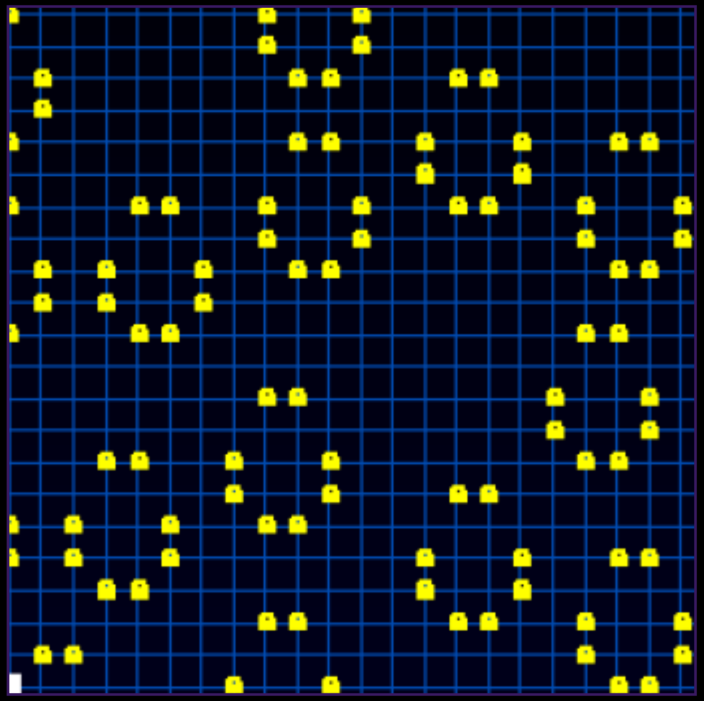


Solution, showing vias only



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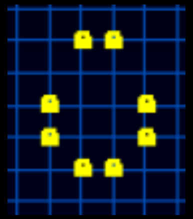


It would be impossible to route and fill this testcase with traditional (net by net) router followed by a filler

Special features with SAT Solvers

Standard-cell Synthesis

Simultaneous Place & Route

Max SAT

Solvers can accept arbitrary constraints

End of First Half

Standard cell methodology induces local inefficiencies

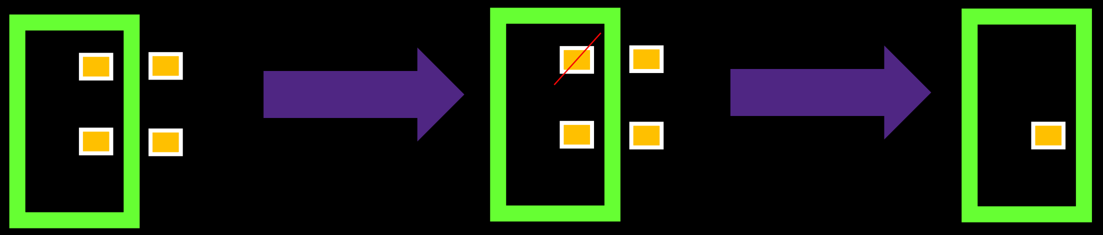
- Design rules beyond cell walls
- Cell I/O pins
- Diffusion breaks and transistor gaps
- In place layout improvement (considering neighborhood)

Cells cannot be touched because of pre-characterization.

Design rules are forced to fit in Standard Cell methodology

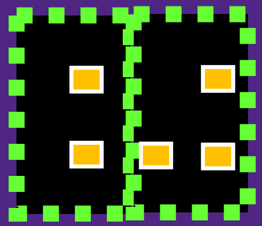
1. In the lithography world, rules can be of a large size

2. In order to fit the standard cell methodology, rules need to be simplified such they fit strictly inside the cell or they can be modelled as a border rule



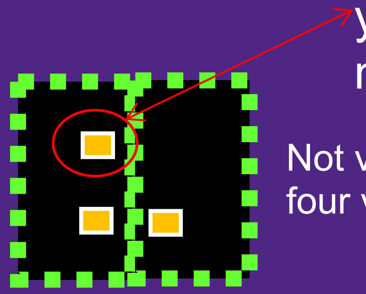
Border rules are always pessimistic because we don’t know the cell’s neighbor.

Disregarding cell borders, these two situations would be fine:



Not violating the original pattern

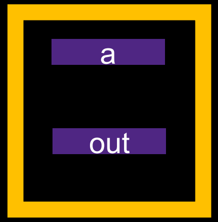
Ok since you know your neighbor

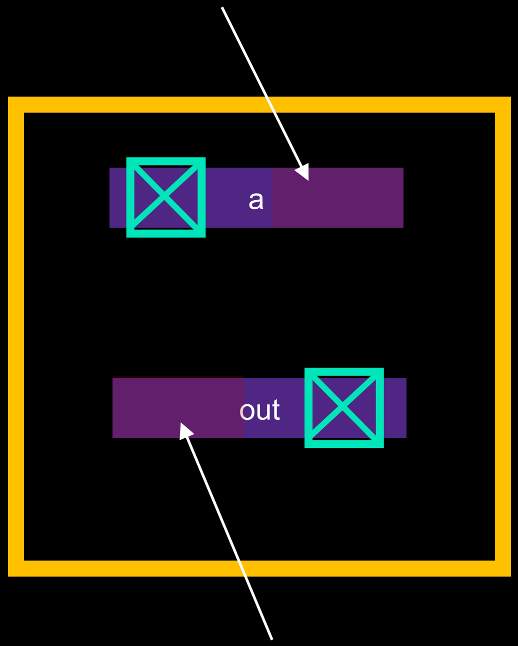


Not violating the four via rule

Cell I/O pins are generally overdesigned to aid block level P&R

1. I/O pins are generally made large in order to ensure enough hit points to the block level

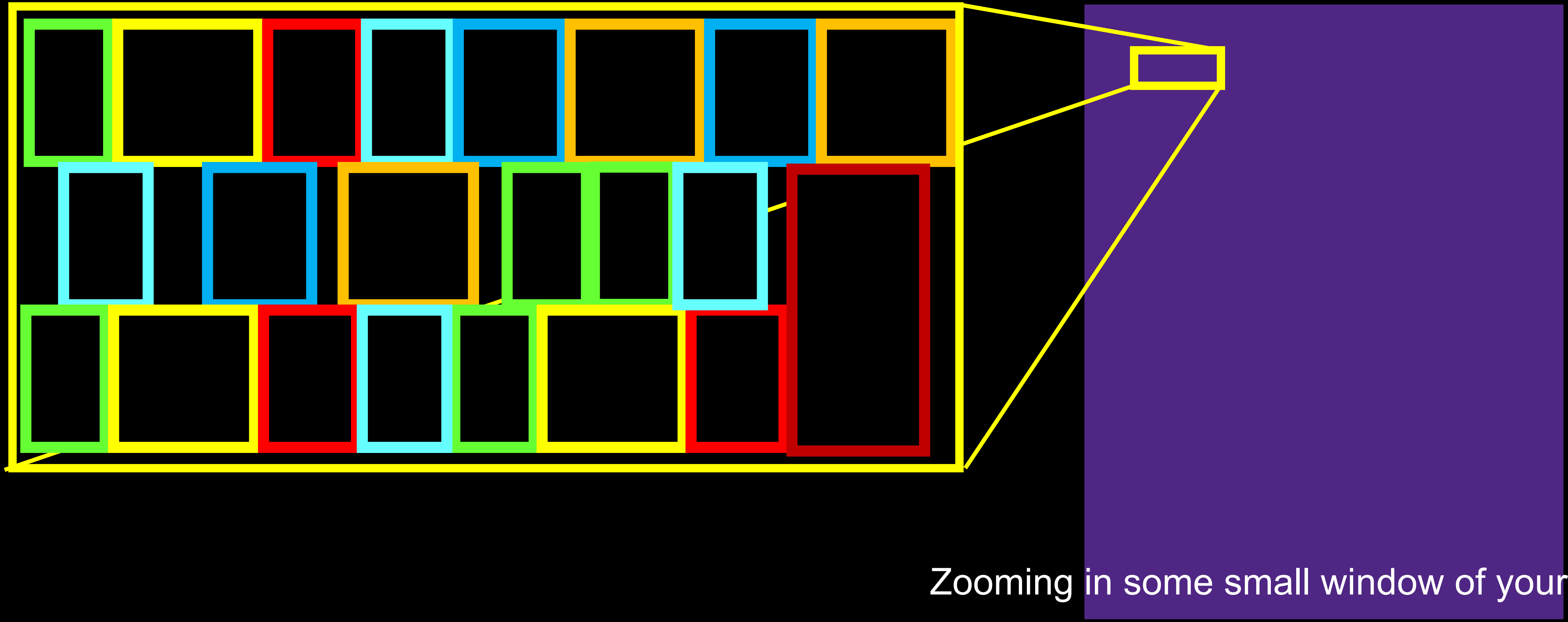




2. After routing, the excessive wiring is left there as an antenna consuming extra capacitance

3. It is well known that excessive input cap is bad for your timing.

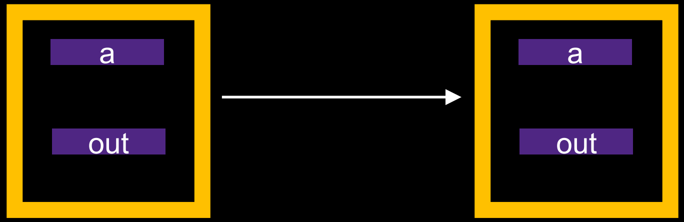
After a block is ready, zooming in to see the problems…



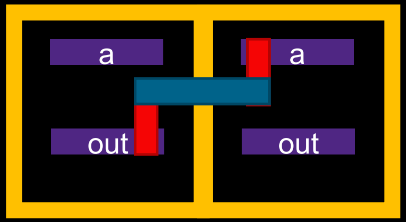
Zooming in some small window of your block…

Scenic routing created due to the fixed pin locations

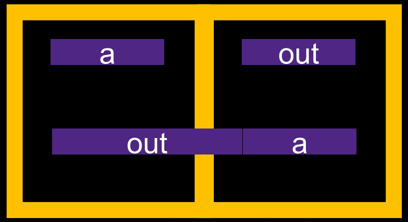
1. For example, consider a situation where two instances of a cell are connected:



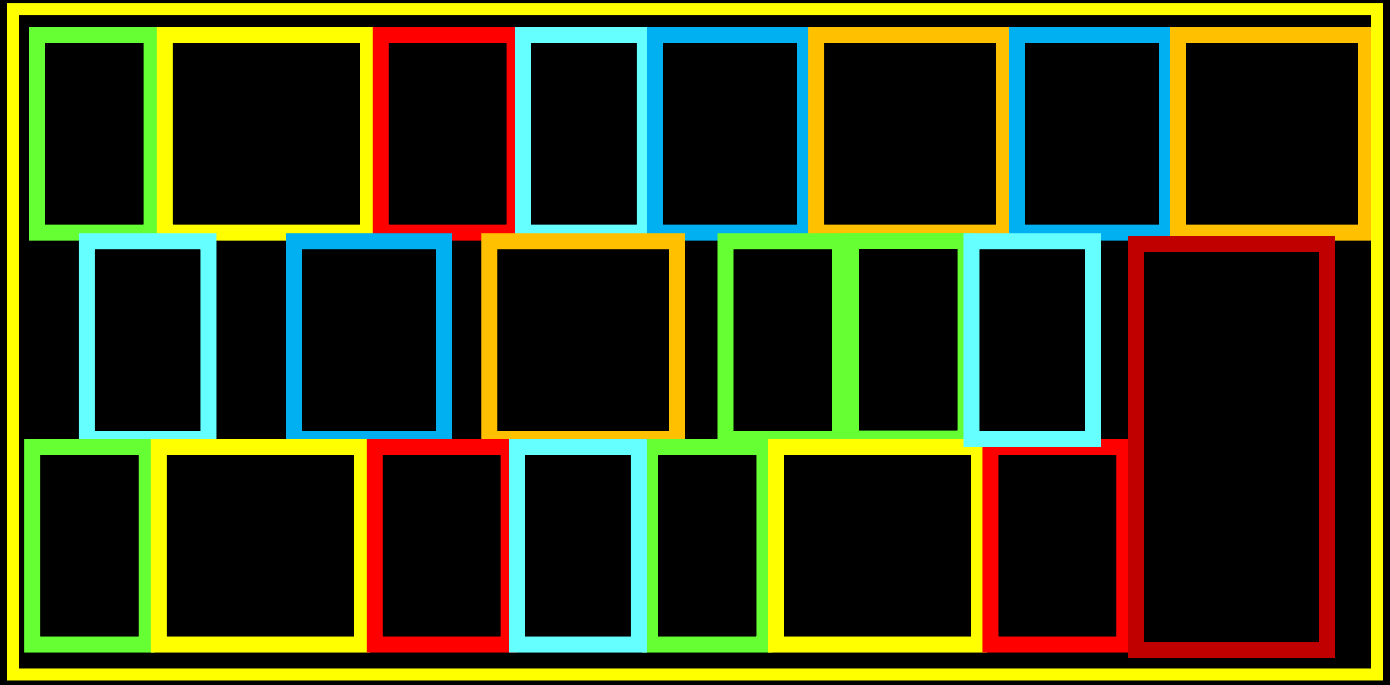
2. If they are placed next to each other, they still need to go up to a higher layer to connect:



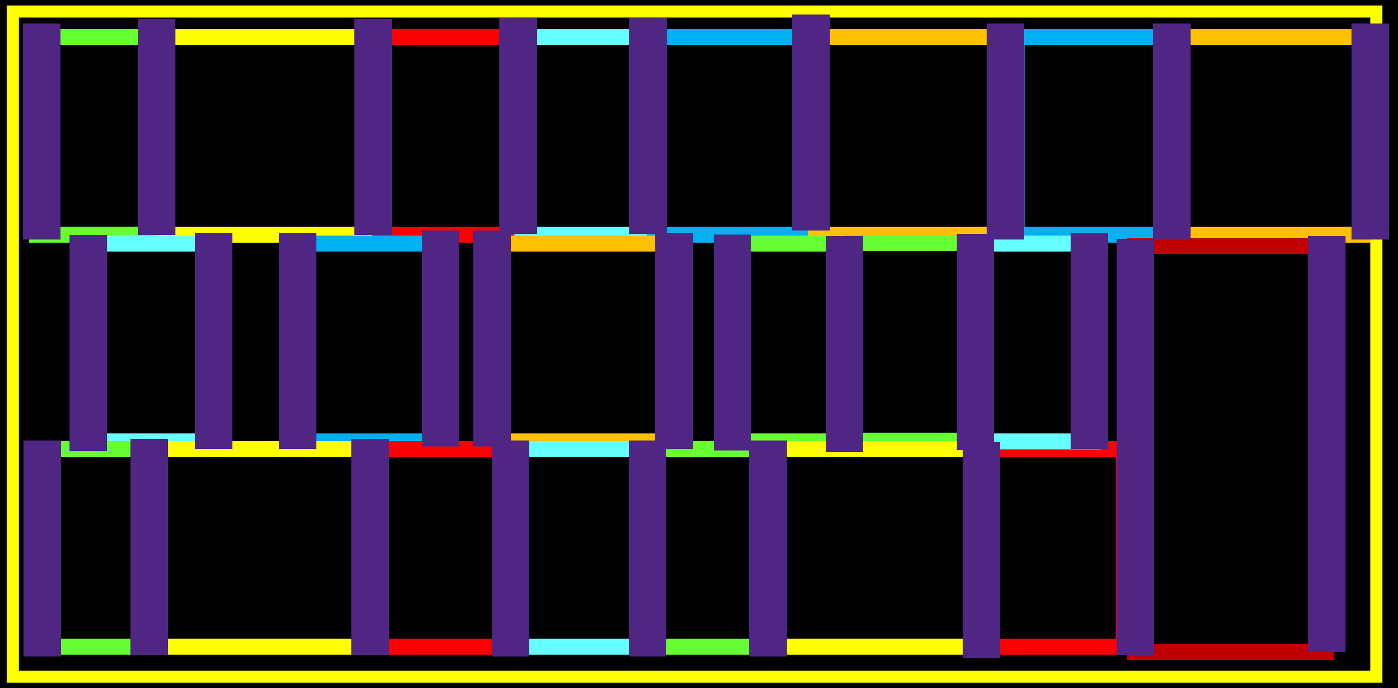
3. However, a simple track swap could enable a much cleaner connection.



Another category of inefficiencies is with transistor gaps.



Standard cells are bordered by transistor gaps



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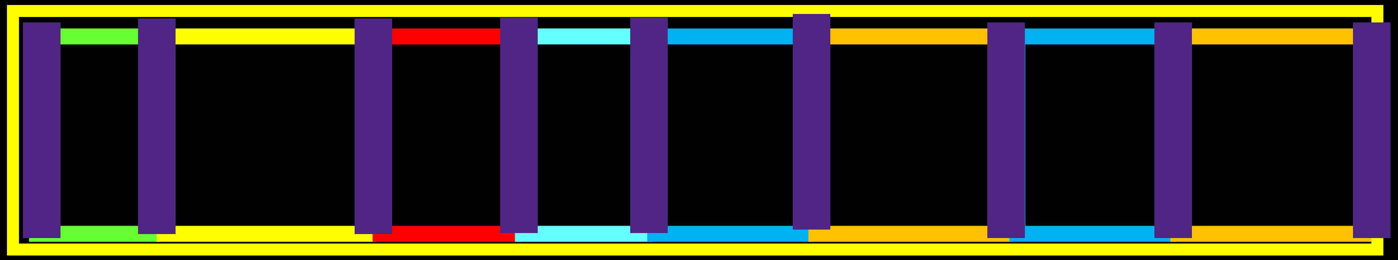
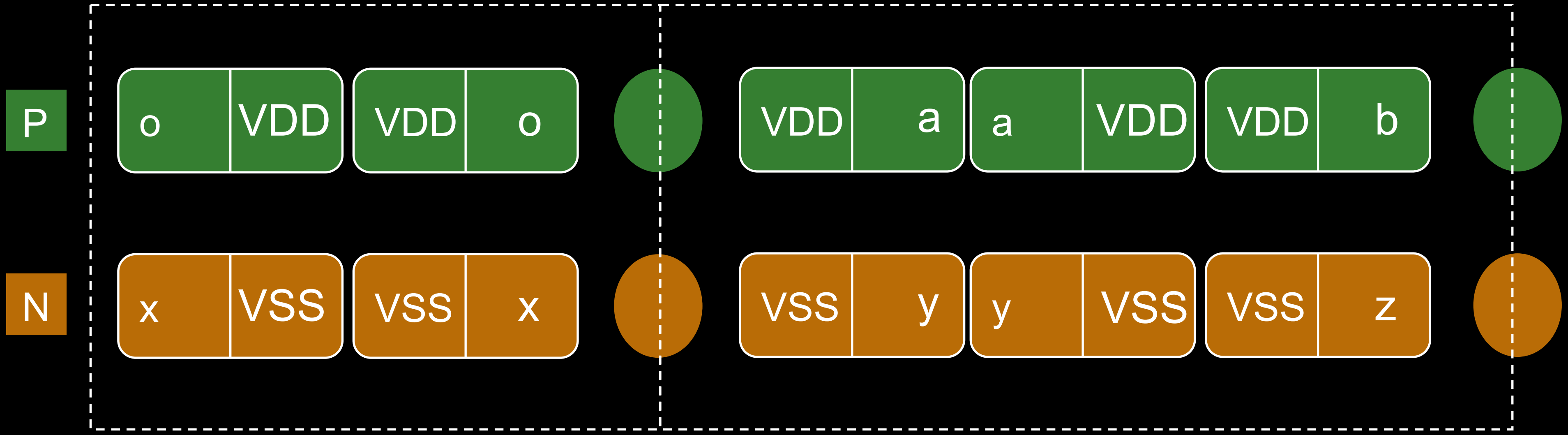
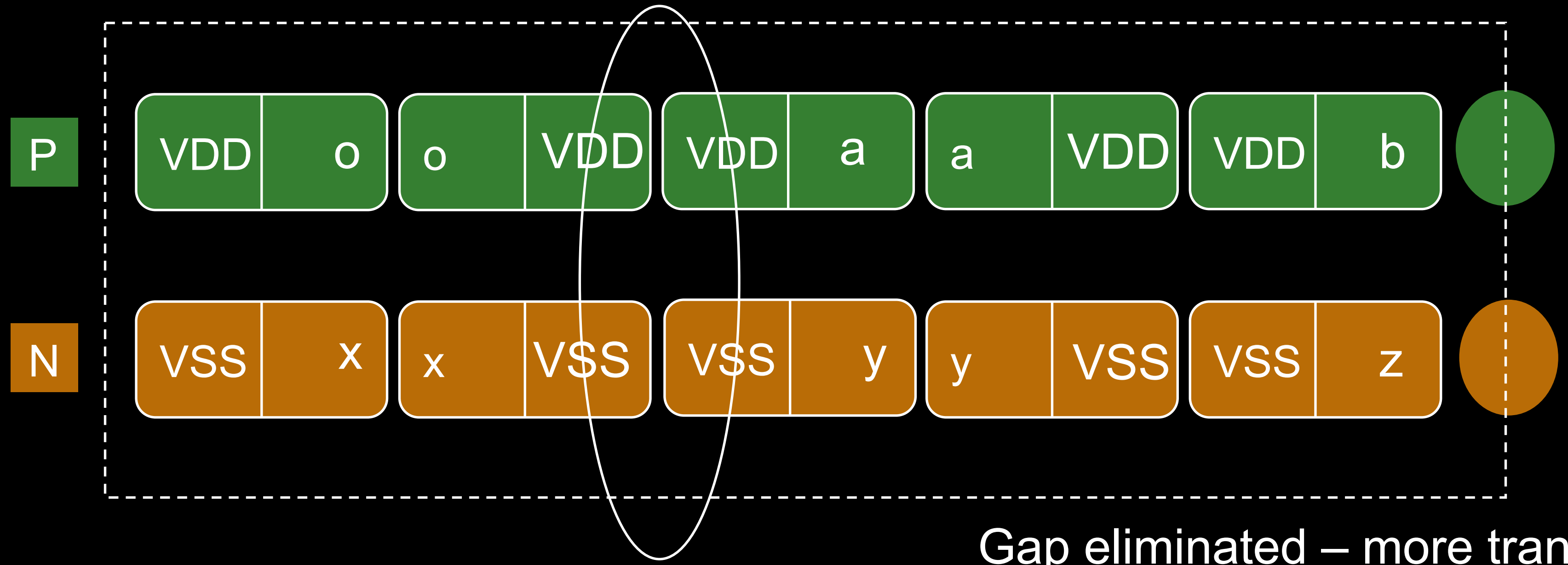


Transistor placement is like dominos…
There are transistor sharing opportunities across cells since they all share power.



Standard cells are bordered by transistor gaps

- Some gaps can be eliminated by shifting and flipping transistors
- Transistors could even benefit from mixing of transistors of other cells



Gap eliminated – more transistor sharing

Cells could have interleaved devices

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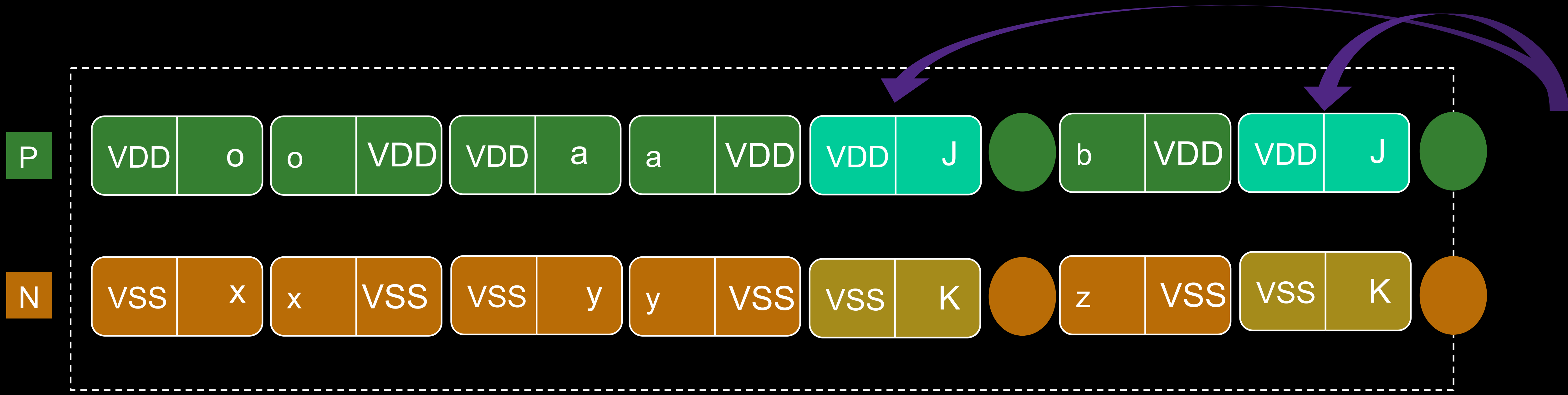

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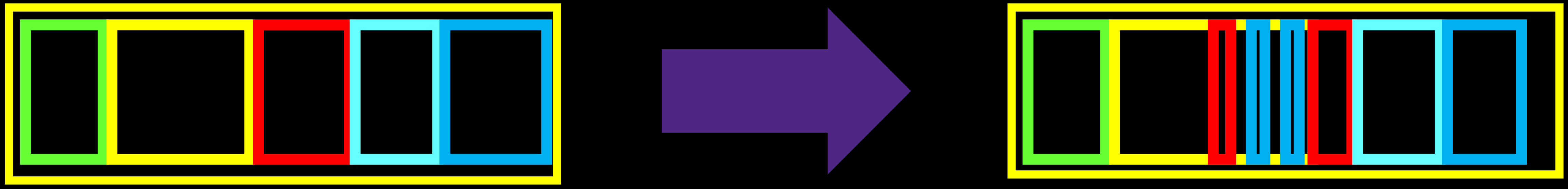
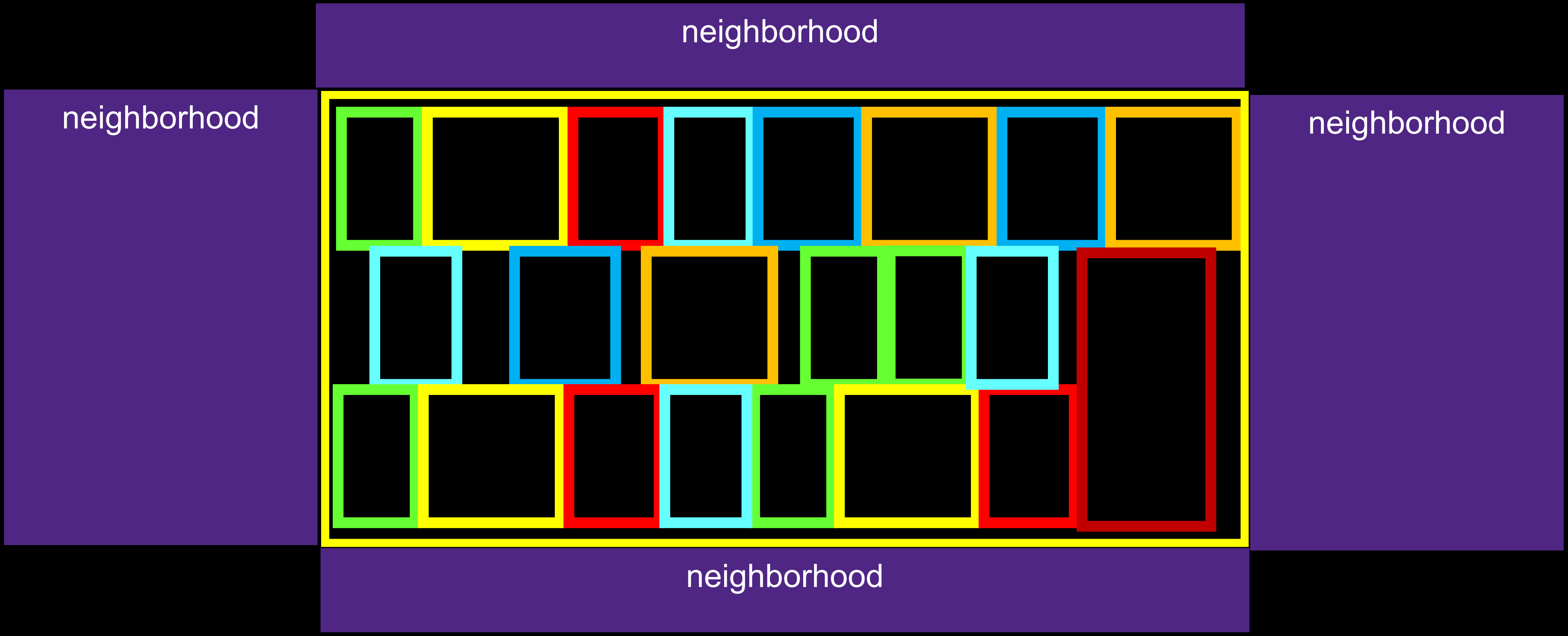


One instance Super cell



One instance Super cell

neighborhood

neighborhood

neighborhood

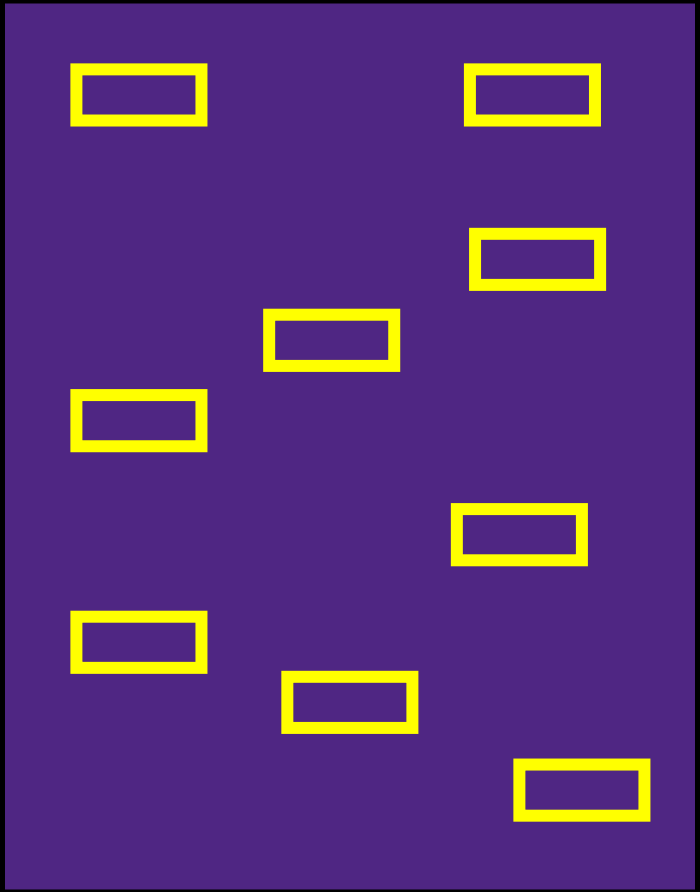
Super cell

- One instance cell
- Optimized for this neighborhood
- Crafted for the cells that are present at this location

- Works under timing constraints (let's talk about this)
- Characterized for one usage only (let's talk again)

neighborhood

After all layout is done, we can run local improvements…



- Sliding window: we can have a very small window that slides over the design and applies “improvements” over that portion of the layout.
- Critical/Relevant regions can be prioritized.

- We have machines, this is absolutely a highly parallel algorithm.

- SAT/SMT Solvers can find optimal solution to local problems and provide place&route improvements subject to constraints from timing analysis.
  - Timing constraints would be in the form of min and max delay; delay can be measured with simulator integrated with the solver.

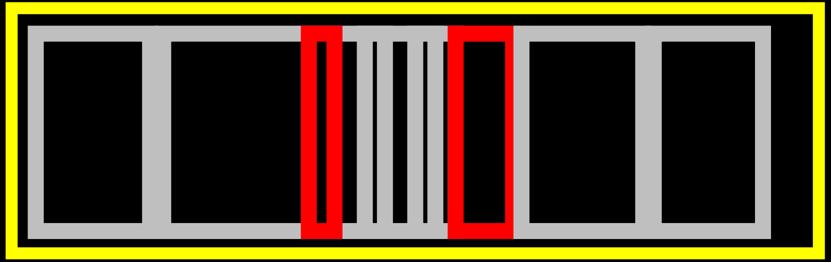
Let’s talk about characterization now…

1) We already live in a world where lots of things are not fully characterized

- Cells are characterized based on some scenarios (for example, typical fanouts) but not all.
- Cell neighborhood is poorly considered.
- Wires are not pre-characterized (and they are responsible for a large chunk of our delay problems)

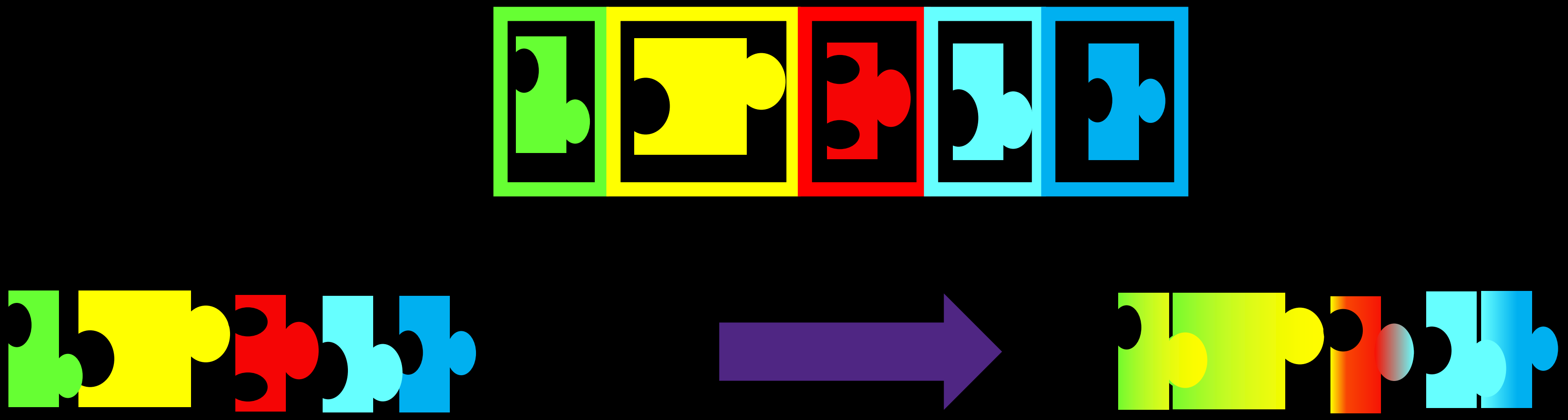
2) Cells can be recharacterized after transformations; if not acceptable, just discard changes.

- Even a cell that is interleaved with other devices (like the one in the picture) can be characterized isolated.
- Re-characterization does not need to be like traditional std. cell, can be specific to this instance.
- The neighborhood is completely known and can be considered
- The output load is known and exact



3) Timing of a super cell can be measured in context using transistor level analysis.

Conclusions – degree of freedom not explored today



Less vias
Less wires
Less resistance
Less capacitance
Less antennas
Less area
Less masks
Less border rules
…

Unique cells, made for the location

Is it legal??? Yes, it is legal, and we don't have tools that explore that!

Is it doable??? Yes it is doable and it requires research

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Thank you!

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