International Symposium on Physical Design

sigda

Design and Optimization of Quantum Electronic Circuits

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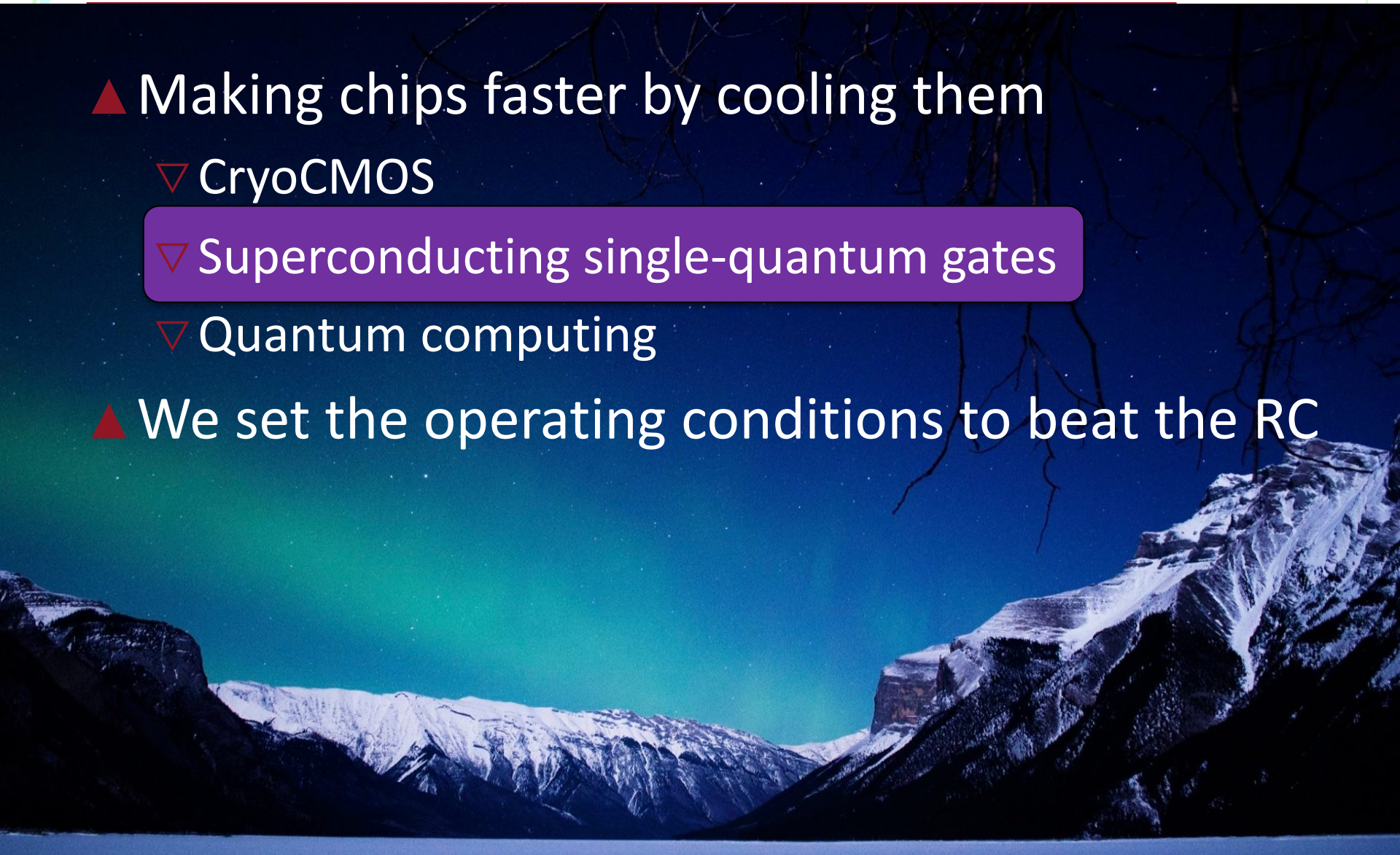
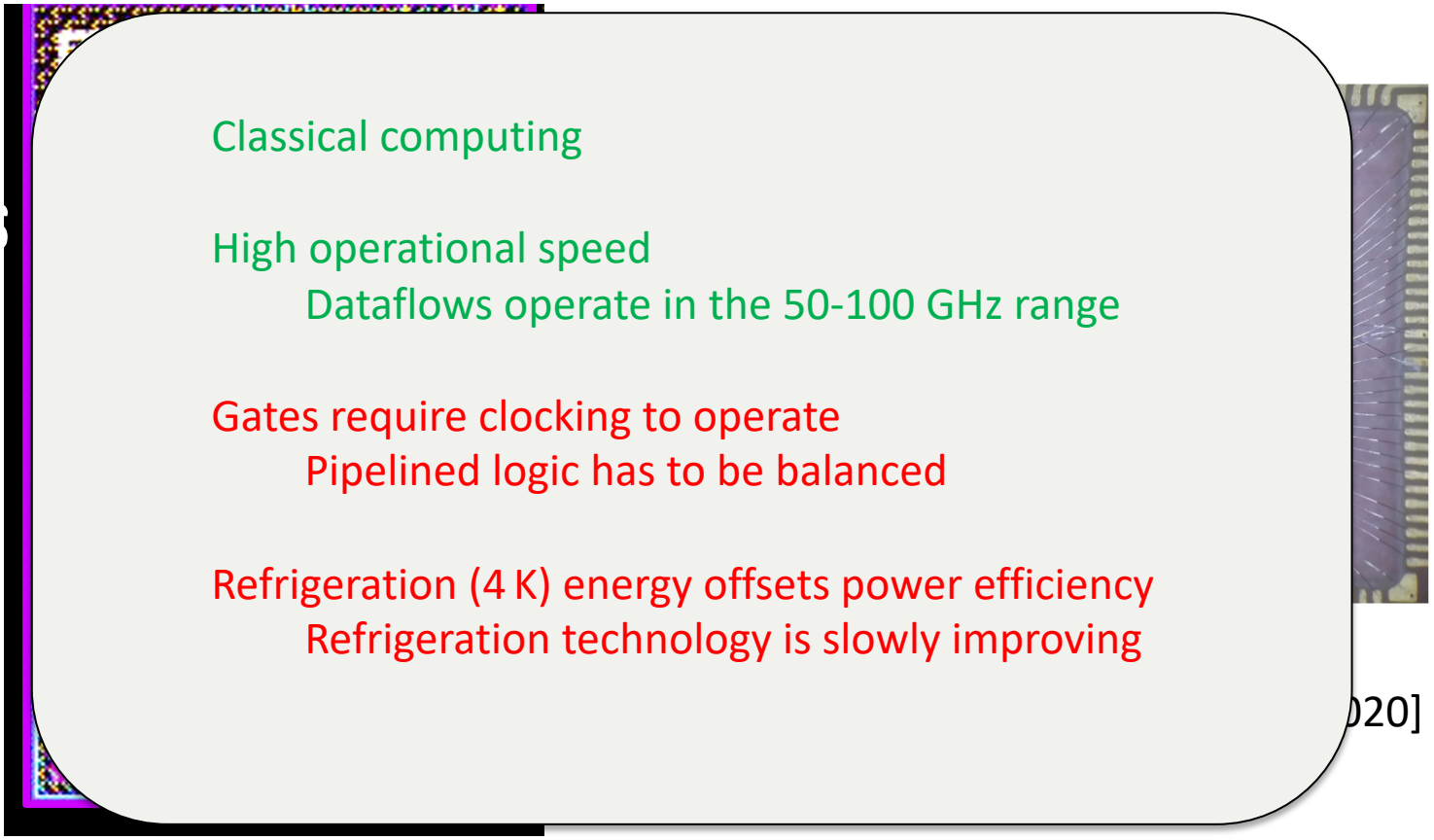
What is cool out there?



- Making chips faster by cooling them
  - CryoCMOS
  - Superconducting single-quantum gates
  - Quantum computing
- We set the operating conditions to beat the RC

Superconducting electronics



Classical computing

High operational speed
- Dataflows operate in the 50-100 GHz range

Gates require clocking to operate
- Pipelined logic has to be balanced

Refrigeration (4 K) energy offsets power efficiency
- Refrigeration technology is slowly improving

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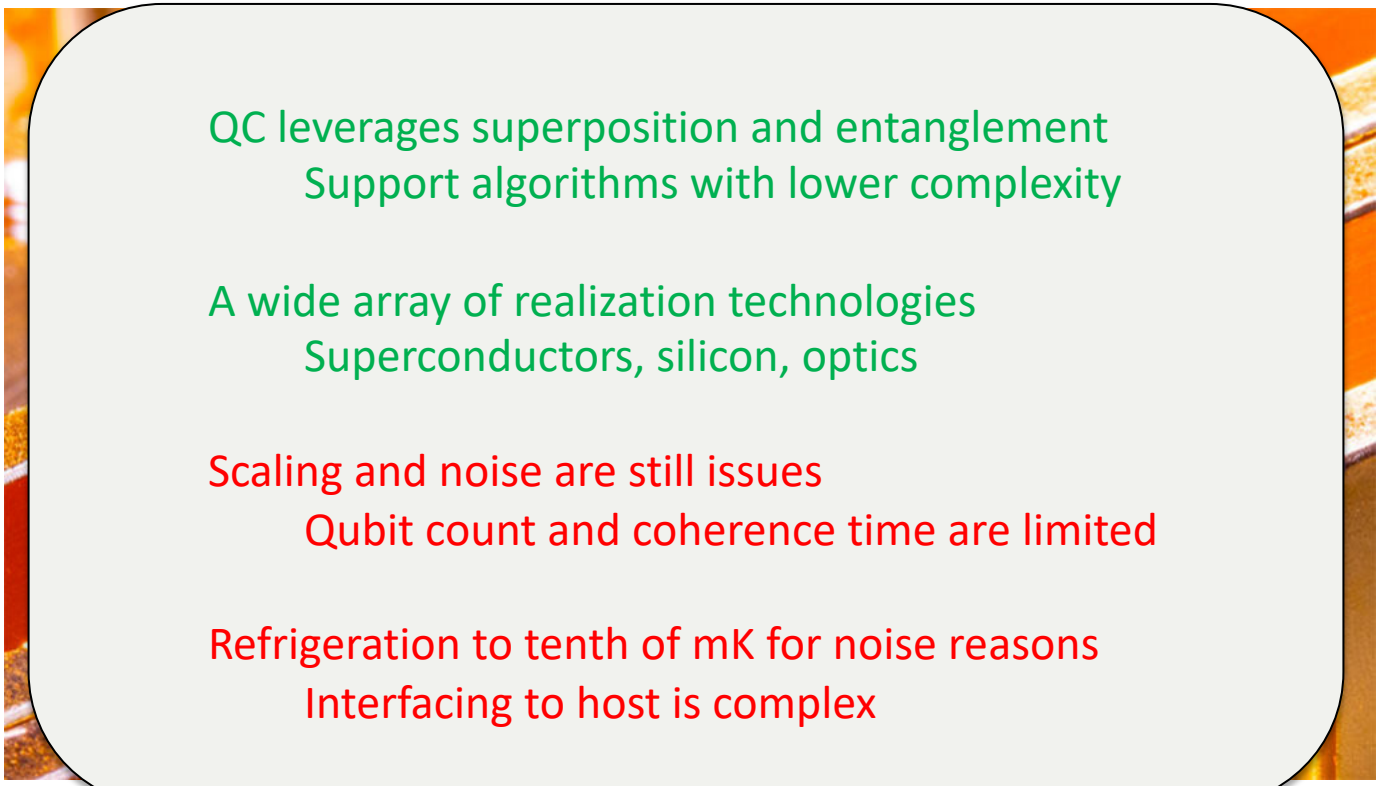
Quantum computing technologies



QC leverages superposition and entanglement
- Support algorithms with lower complexity

A wide array of realization technologies
- Superconductors, silicon, optics

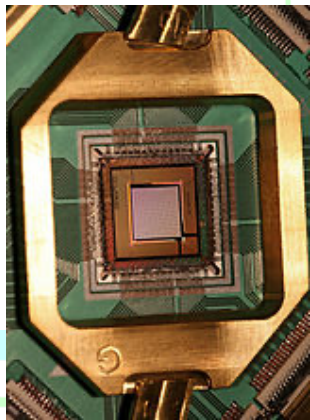
Scaling and noise are still issues
- Qubit count and coherence time are limited

Refrigeration to tenth of mK for noise reasons
- Interfacing to host is complex

Superconductors and JJs

- A superconductor is a material where
  - *Resistivity* vanishes and *magnetic flux* field is expelled
  - When below a *critical temperature* T_c
- *Josephson junction* - JJ
  - Superconducting wire interrupted by thin insulator
  - $Nb/AlO_x/Nb$ or $Al/AlO_x/Al$

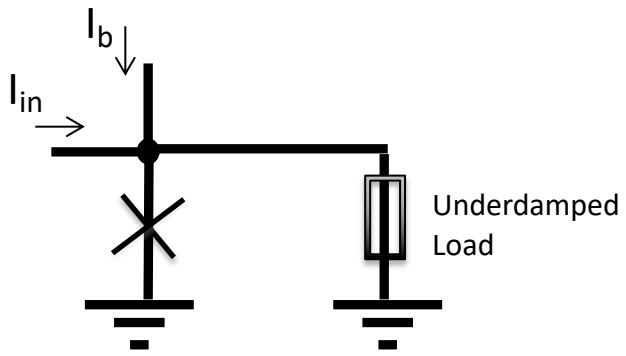
- *Supercurrent* $I_s = I_c \sin(\phi)$, where ϕ is the phase difference of electrodes wave functions
- *Critical current:* I_c – max current in SC state



[Source: Dwave]

Some history

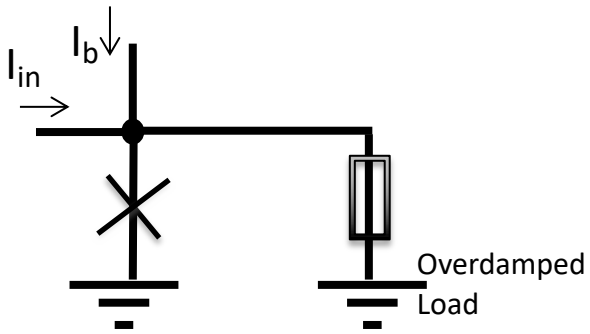
- IBM ran a large SCE program until 1983
  - The project failed because of the *latching* issue
- Several Japanese companies followed IBM's path
  - They improved the *materials* but still had latching issues



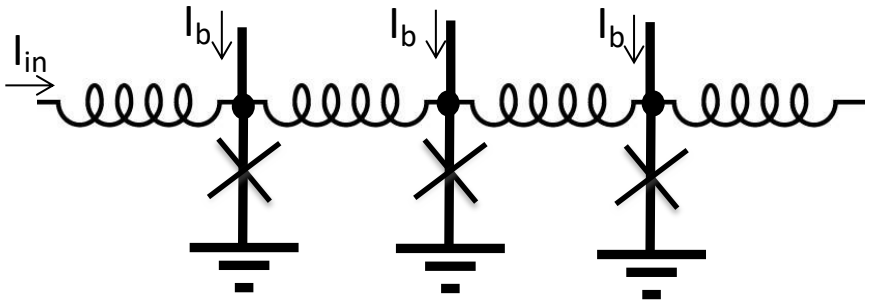
- I_b is slighly below I_c
- I_{in} makes the JJ be resistive
- A fast voltage transition 0 -> 1
- More difficult to reset JJ -- latching
- Slower transition 1 -> 0

Some history - *Single-flux quantum* SFQ

- Likharev radically changed to *pulse-based* signalling
  - *Single-flux quantum* logic SFQ
  - Input is short pulse $\int V(t)dt = \phi_0 = h/2e = 2.07$ mv ps
  - Load is *overdamped*
  - An output pulse is generated



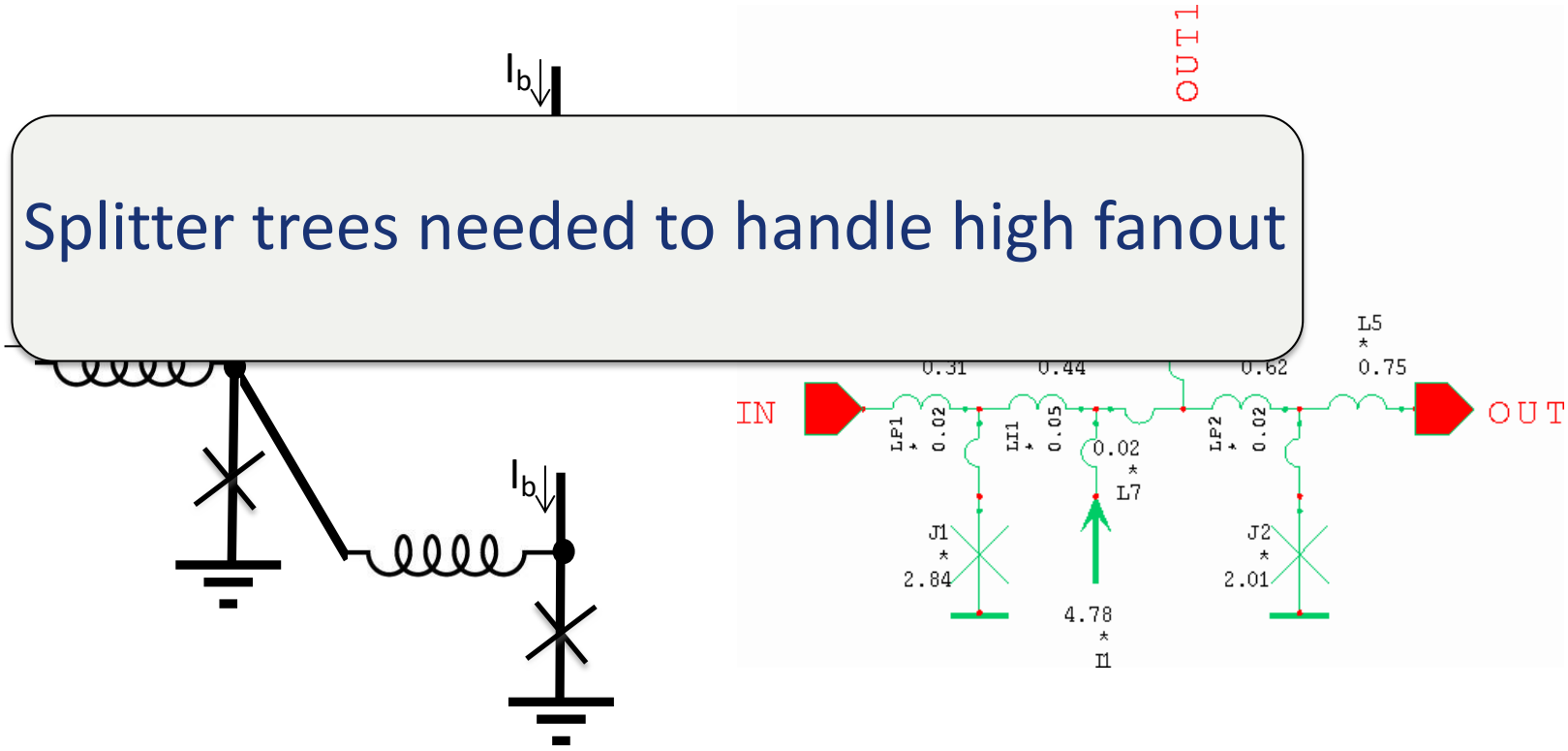
Josephson transmission line



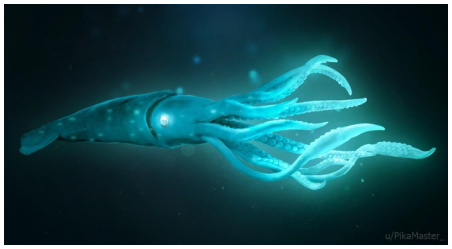
[Likharev et al., TAS, 91]

Fanout and Splitters

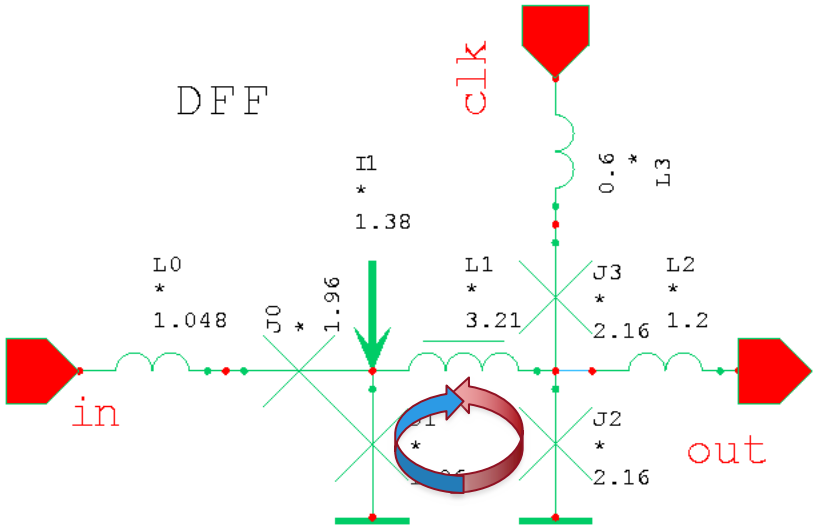
- Output pulse has fanout equal to 1
  - Splitter circuit – splitter trees

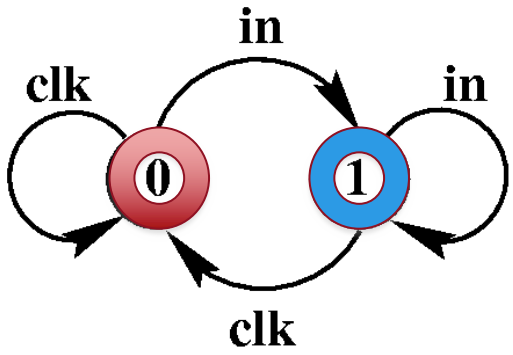


The S/R latch or SQUID



- Two persistent states
  - Corresponding to direction of current in loop J1 – L1 - J2
  - Flux quantum
- Input sets to 1 – Clock resets to 0

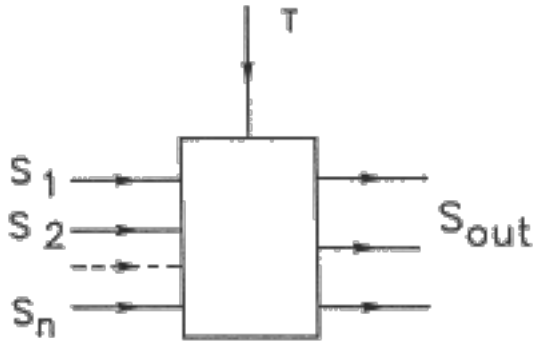


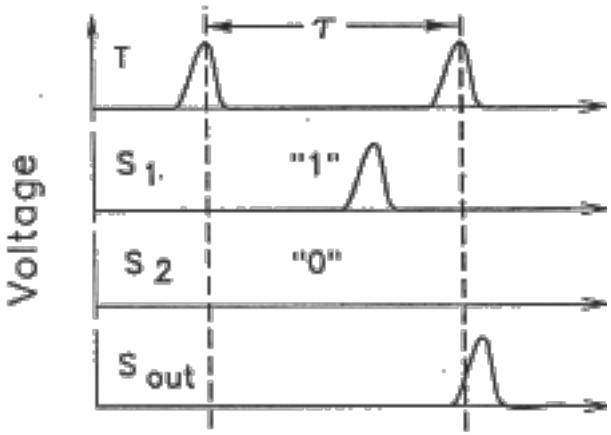


Principles of combinational cells

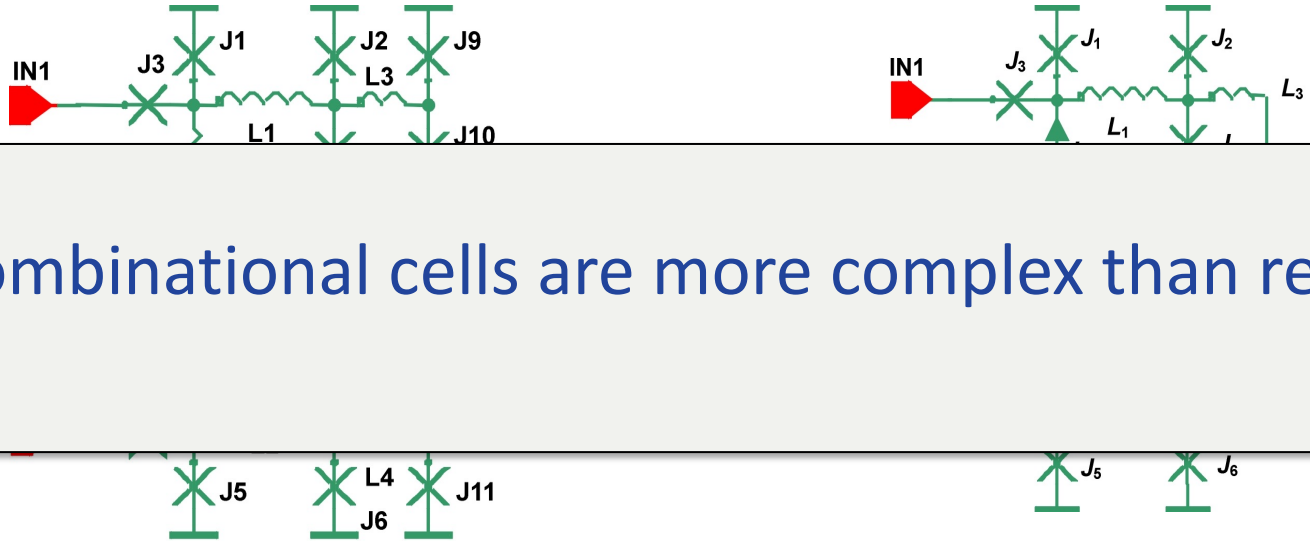
- Signal encoding: 1 = pulse -- 0 = no pulse
- Cell has two stable states:
  - Direction of current flow in a loop
- Op
  -
  -
  - Output is issued at end of clock
  - Clock resets the state

Inputs are evaluated when clock is present





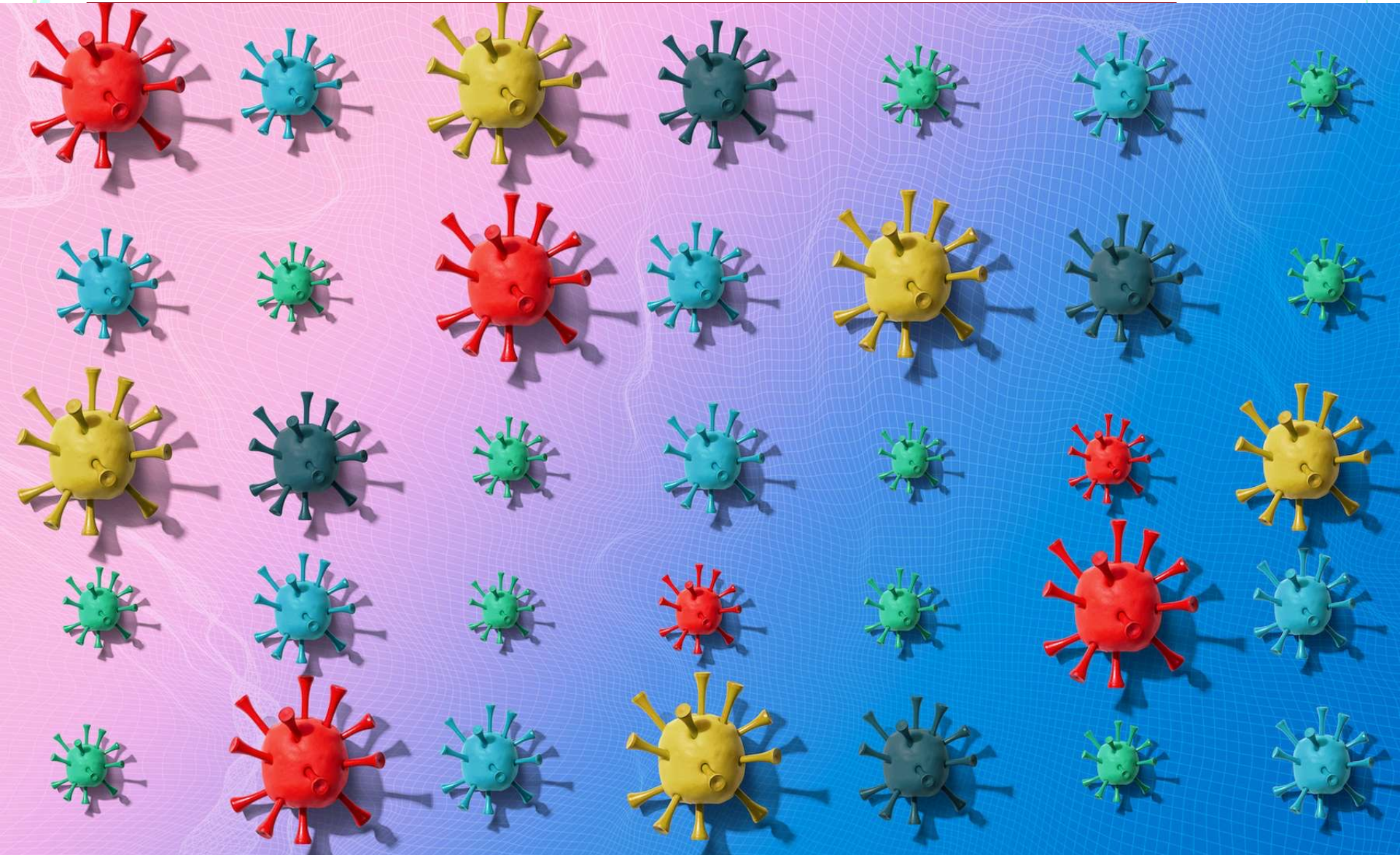
Example of OR and AND



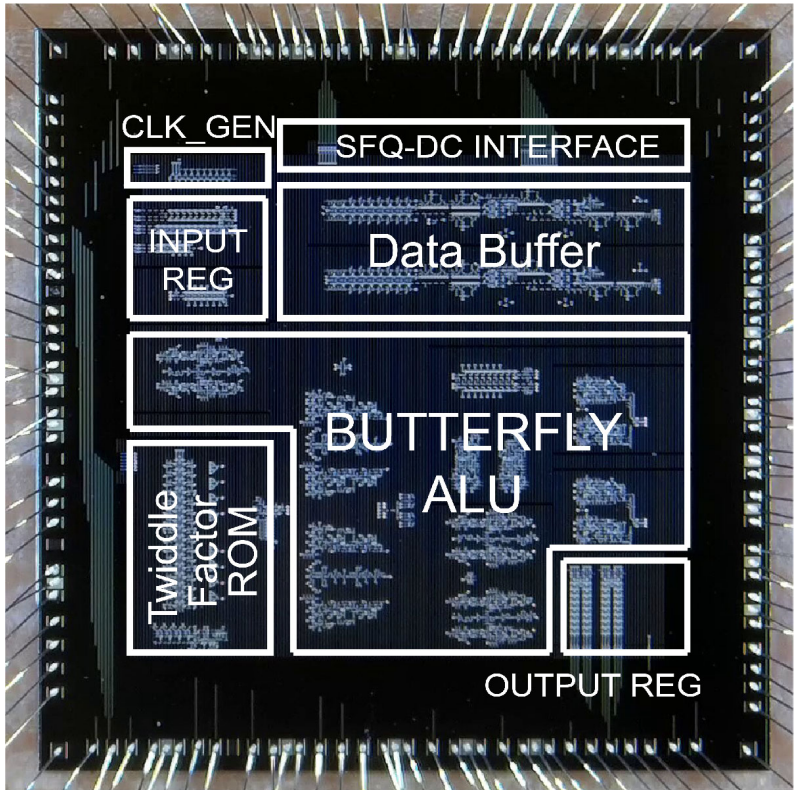
Combinational cells are more complex than registers

[Likharev – Stony Brook]

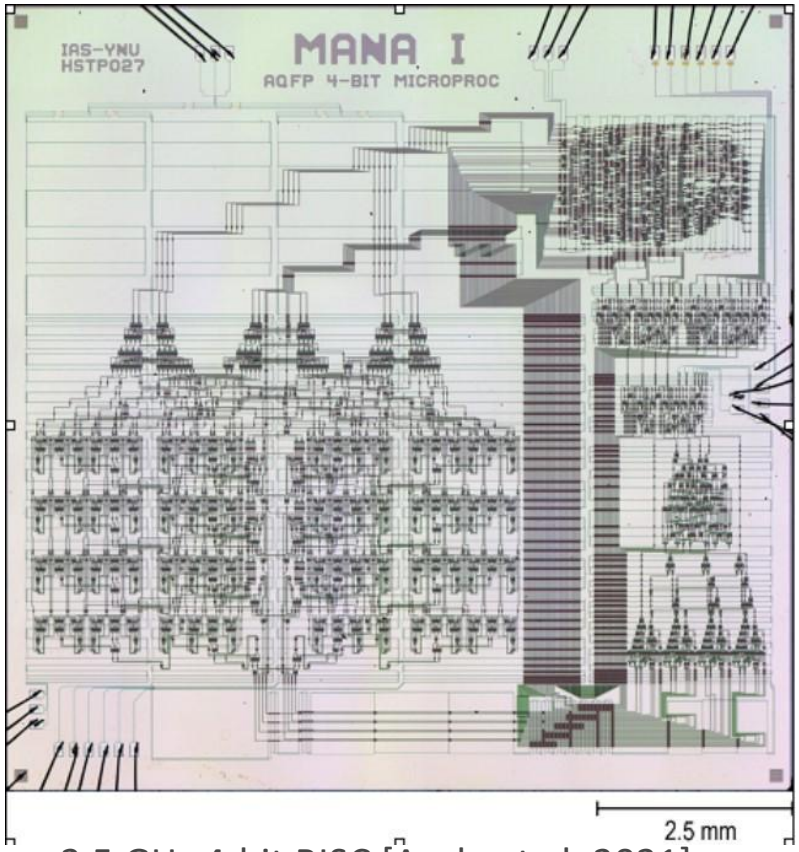
The SFQ variants



Achievements



47 GHz SFQ FFT Processor [Ke et al.,2021]



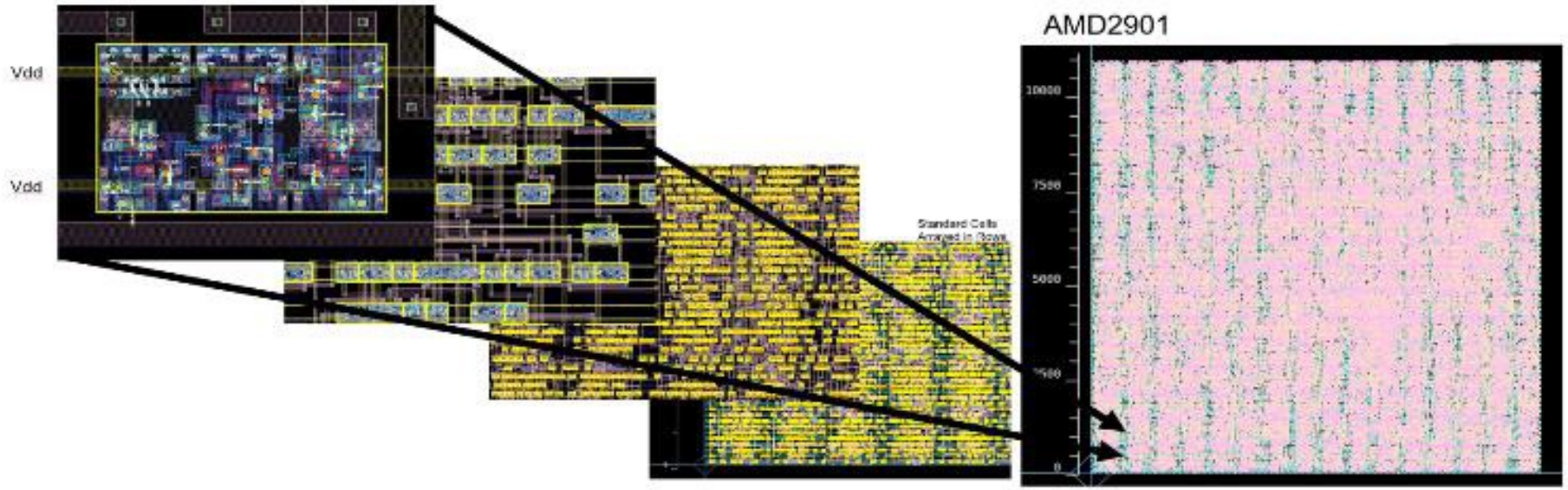
2.5 GHz 4-bit RISC [Ayala et al.,2021]

Achievements

Synopsys SuperTools Superconducting Electronics Phase 2A Program

First Fully Automated Superconducting Microcontroller Design Demonstration with Fusion Compiler

The First Fully-Automated ERSFQ Microcontroller Circuit including CTS, Splitter Insertion, Power Delivery and PTL Routing – all desired features for SCE Technology automation



Fully synthesisized AMD 2901 [Amaru et al., 2021]

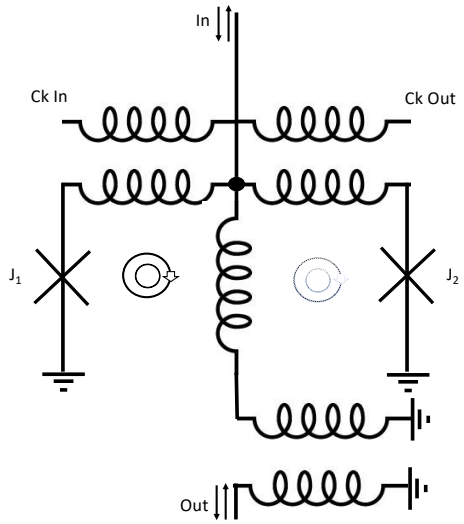
Some ballpark numbers

Logic	Clock Freq. [GHz]	$E_{bit} / I_c\Phi_0$	Typical I_c [mA]	EDP [aJ·ps]
CMOS	4	-	-	~10^5
RSFQ [1]	50	19	150	120
eSFQ [2]	20	0.8	150	12
RQL [3]	10	0.33	150	10
LV-RSFQ [4]	20	3.5	150	54
AQFP [5]	5	0.0083	50	0.086
Quantum limit	-	-	-	5.3×10^{-5}

[1] X. Peng et al., IEICE Trans. Electron. **E97.C**, 188 (2014).
[2] M. H. Volkmann et al., Supercond. Sci. Technol. **26**, 015002 (2013).
[3] Q. P. Herr et al., J. Appl. Phys. **109**, 103903 (2011).
[4] M. Tanaka et al., IEEE Trans. Appl. Supercond. **23**, 1701104 (2013).
[5] N. Takeuchi et al., Supercond. Sci. Technol. 28, 015003 (2015).

AQFP -- Adiabatic quantum flux parametron

- Input is a current
- Direction of current encodes 1/0
- Circuit has two loops
  - Either one is conducting – state 1/0
- Input evaluated when clock is present
  - May force a gradual transition of conducting loop
  - Creates a corresponding output signal

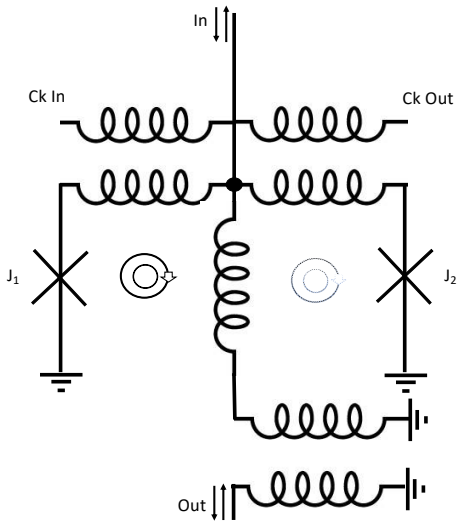


[Goto 56]

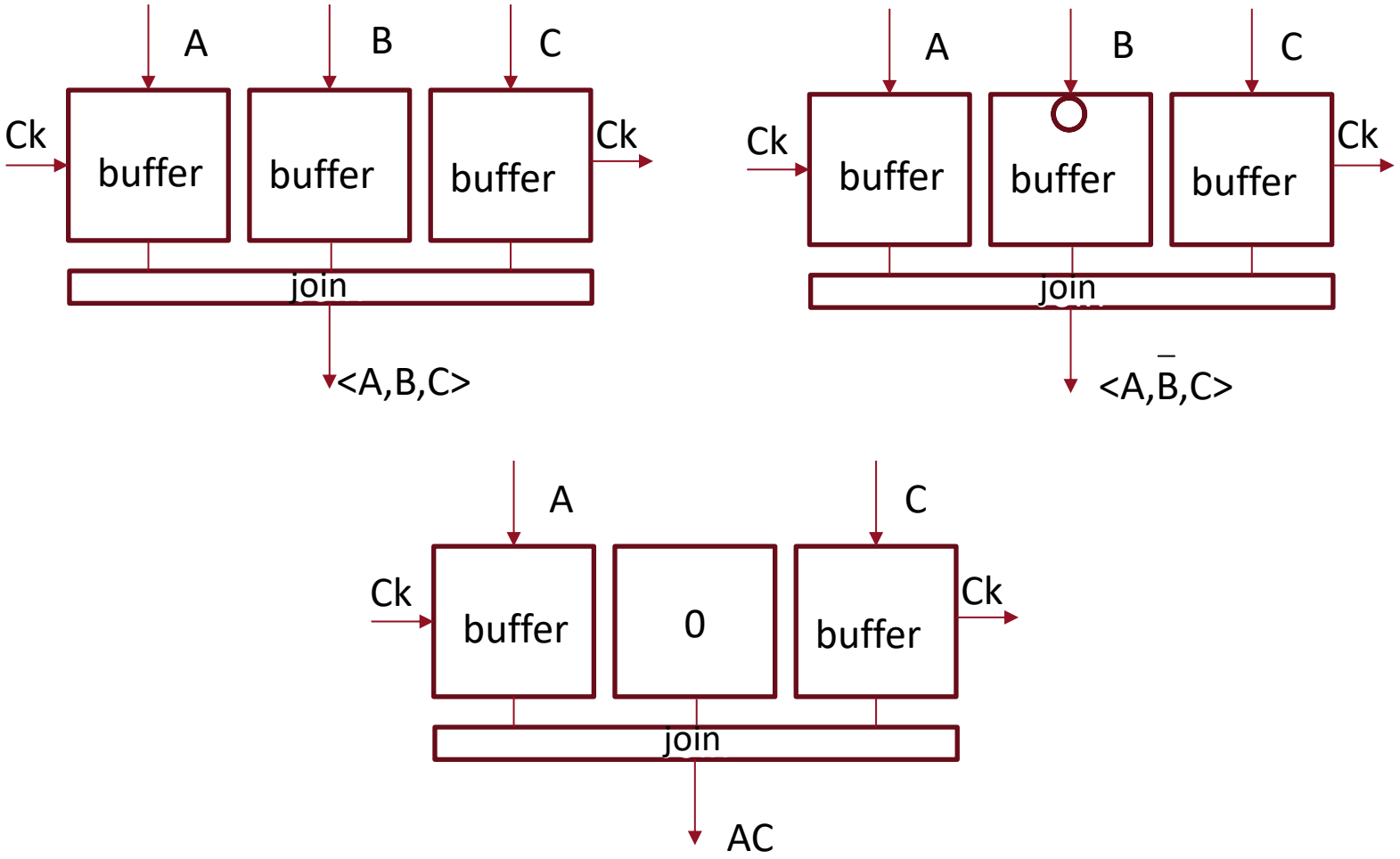
[Yoshikawa, Ayala et al. Yokohama National University]

AQFP buffer and derivatives

- Buffer
  - Output follows input
- Inverter
  - Buffer where output coil is reversed
- Majority gate
  - Three buffers in parallel with an inductive coupler
- Extensions:
  - Logic gates NPN-equivalent to majority
  - AND-2 and OR-2 by creating “constant buffers”



Adiabatic Quantum Flux Parametron (AQFP)

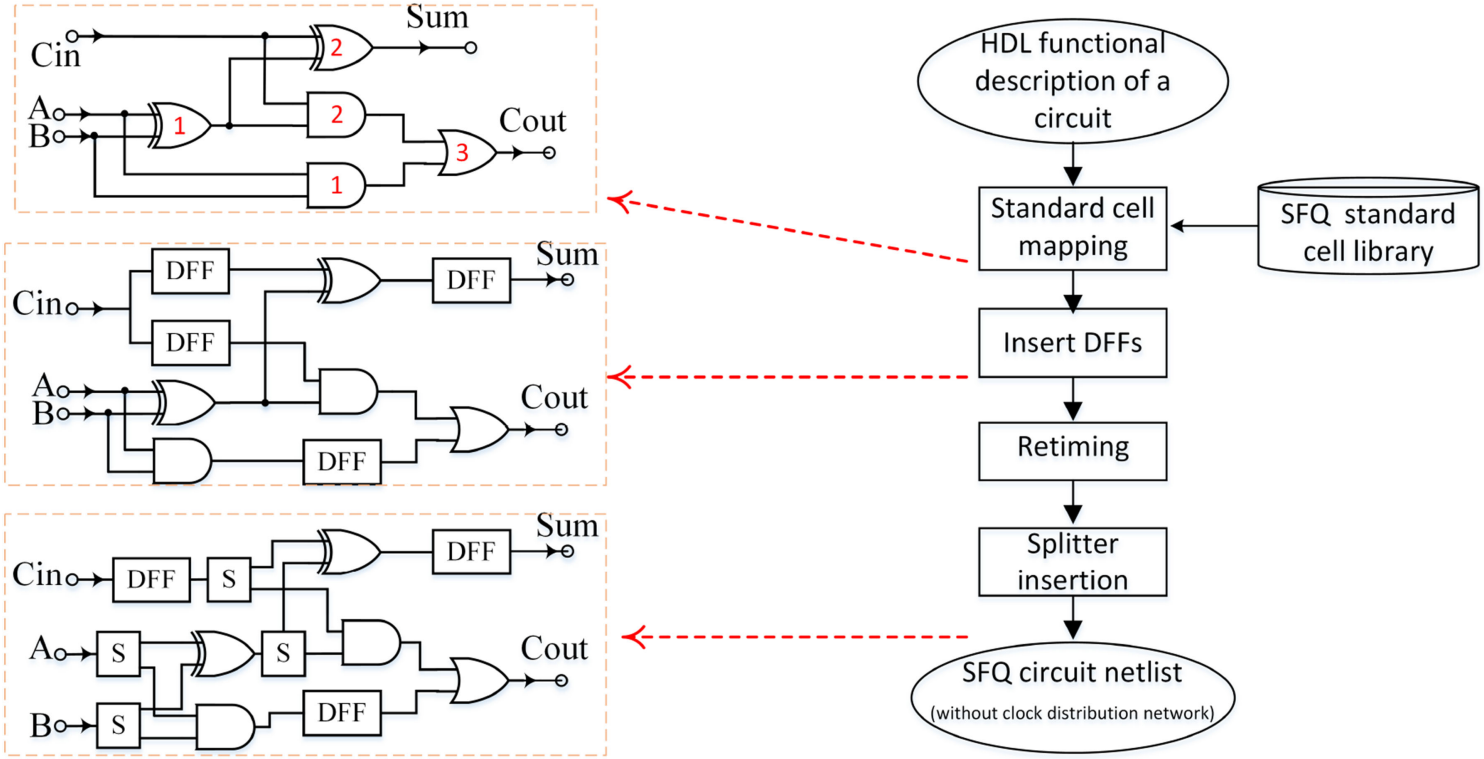


Logic design principles

- Balancing:
  - When considering a logic network graph, all paths from inputs to any node have same *length*
- Fanout:
  - All multiple fanout points need signal *splitting*
- Logic optimization:
  - Logic should be optimized by *majority logic,* especially when majority is native abstraction

Path balancing for SFQ

- Assumption: splitters are not clocked in SFQ



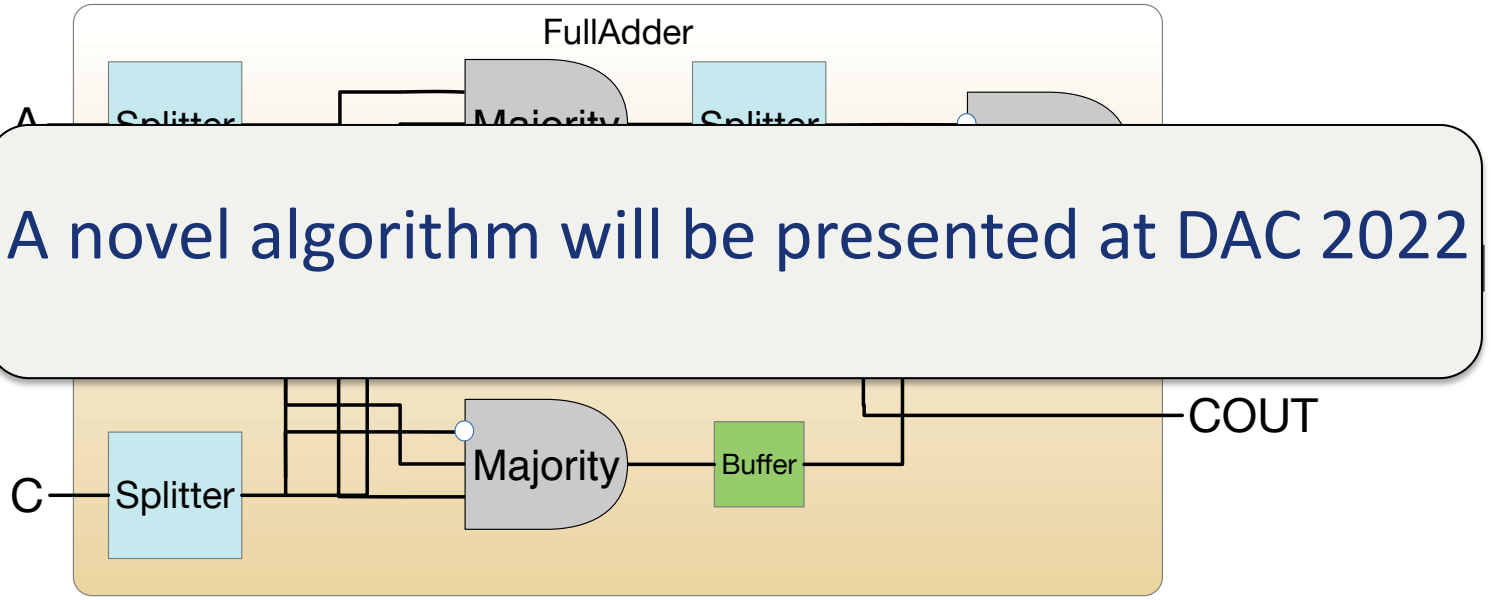
[Katam, Pedram, TAS18]

Dynamic programming for SFQ

- Assumption: splitters are not clocked in SFQ
- PBMap (based on AIG representation in ABC)
  - Given a node and its cuts
  - Best local solution minimizes the sum of cost of the *children nodes* plus cost of the *inserted buffers*
  - Proceed bottom up
- For tree topologies gives optimum solution
- For DAGs, it is a heuristic
  - Area-retiming can refine solution

[Pasandi, Pedram, ICCAD 19]

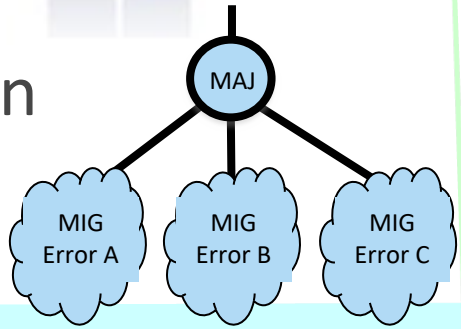
Splitter insertion for AQFP

- A splitter is a clocked buffer with a passive fork
  - Inserting splitters imbalances a circuit
  - Require additional buffers
- 

[Cai et al., ICCD 19]

Majority logic synthesis

- Exploit redundancy of majority function
- Boolean substitution



What is in for physical design ?

- A new set of interesting problems
  - Inductors are the limit in placement
- Wiring can be done by *passive or Josephson* transmission lines
  - Relatively less critical for speed (compared to CMOS)
- Clock routing is complicated
  - Because of reaching out to all gates
- Adiabatic realizations are even more complex
  - Power and clock routing

Conclusions

- There is strong evidence that SCE circuits can provide us with:
  - Faster computing
  - Higher energy-efficient computation
- Current limitations are:
  - Scalability to larger realizations
  - Lack of EDA design tools and open libraries
  - Cooling systems
- The technical difficulties are surmountable and new opportunities are in reach

Thank you

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Warm congratulations to Ricardo Reis

- Recipient of the Lifetime Achievement Award