A Lifetime of Physical Design Automation and EDA Education

ISPD 2022 Lifetime Achievement Award Bio

Ricardo Augusto da Luz Reis
Universidade Federal do Rio Grande do Sul
Porto Alegre, Rio Grande do Sul, Brazil
reis@inf.ufrgs.br

ABSTRACT

The 2022 International Symposium on Physical Design lifetime achievement award goes to Prof. Ricardo Reis for his instrumental impact on EDA research in South America and contributions to the physical design community.

CCS Concepts/ACM Classifiers

• Hardware → Electronic design automation
• Hardware → Very Large Scale Integration Design

Author Keywords

CAD, EDA, Radiation Effects, Low Power

BIOGRAPHY

Prof. Ricardo Reis had a short introduction to Microelectronics in his EE at UFRGS (Universidade Federal do Rio Grande do Sul), in Brazil. Then, he went to INPG, France, to pursue his Ph.D. degree, but before starting the Ph.D. study, he did the reverse engineering of the Z8000 microprocessor, that was a great experience to learn many issues that were not in books or papers. The PhD was related to Floorplanning. After finishing his Ph.D. study, he returned to UFRGS, where he was a founder of the UFRGS Microelectronics Group. He is a full professor at the Informatics Institute of Federal University of Rio Grande do Sul. He received the title of Doctor Honoris Causa by the University of Montpellier, France, in 2016. The experience with reverse engineering of the Z8000 inspired the beginning of research in layout design automation. One of the first research works was related to the development of a cell-based layout design automation tool with connections over the cells, avoiding the standard cell approach used that time that included routing channels between cell rows. Since then, he has advised more than 100 graduate students, those are working in Brazil and in several countries around the world, in companies and institutions like Cadence, Synopsys, Siemens EDA, Apple, Silvaco, Impinj, EnSilica, Qualcomm, ARM, Roku, NXT, Thales, HP, Chipus, IWF, Université Grenoble-Alpes, University of York, UFSC, UFRGS. Several teams with UFRGS students won some

EDA Contests like ISPD and ICCAD ones. One of his main research projects is still related to layout design automation of any transistor network. His main research includes physical design automation, design methodologies, fault tolerant systems and microelectronics education. He has more than 700 publications including books, journals and conference proceedings [1-9]. He was Vice President of IFIP (International Federation for Information Processing) and he was also President of the Brazilian Computer Society (two terms) and Vice President of the Brazilian Microelectronics Society. He is an active member of IEEE CASS, and he received the 2015 IEEE CASS Meritorious Service Award. He was Vice President of CASS for two terms (2008/2011). He is the founder of the Rio Grande do Sul CASS Chapter, which received the World CASS Chapter of The Year Award in 2011, 2012, and 2018, and R9 Chapter of The Year 2013, 2014, 2016, 2017 and 2020. He was also the founder of the IEEE CEDA Chapter. He is a founder of several conferences and events like SBCCI, LASCAS, SERESSA, EMicro. Those conferences brought knowledge and research opportunities to Brazil and Latin America. He was the General and Program Chair of several conferences such as IEEE ISVLSI, SBCCI, IFIP VLSI-SoC, ICECS, PATMOS. Ricardo was the Chair of the IFIP/IEEE VLSI-SoC Steering Committee, vice-chair of the IFIP WG10.5 and he is Chair of IFIP TC10. In 2002 he received the Researcher of the Year Award in the state of Rio Grande do Sul. He is a founding member of the SBC (Brazilian Computer Society) and also founding member of

ISPD '22, March 27–30, 2022, Virtual Event, Canada.

ACM ISBN 978-1-4503-9210-5/22/03.
https://doi.org/10.1145/3505170.3511039

SBMicro (Brazilian Microelectronics Society). He was a speaker of CASS DLP Program (2014/2015), and he has conducted more than 70 invited talks in conferences. Member of IEEE CASS BoG and IEEE CEDA BoG. In 2021, Ricardo received the IFIP Fellow Award.

PERSONAL COMMENTS

I would like to share this award will my students and colleagues. I have advised more than a 100 hundred graduate students that have done excellent work. This can be endorsed by the awards the teams composed by our students have received at ISPD and ICCAD contests and by the papers published in international journals and conferences, as well some books. It is not easy to do research in Latin America, as there is a lack of grants provided by local governments and industry. But there is a large set of qualified students, as the quality of undergraduate and graduate programs have as reference the international state-of-art in the field. I can say that, considering the quality of professionals in the field, the region has a great potential to attract companies that are looking for students and professionals with good skills on EDA and IC Design. South of Brazil is a region that already attracted companies like Silvaco, Saggi/Real Intent, EnSilica, Impinj, HT Micron, CEITEC and Chipus.

REFERENCES

[1] ANCEAU, François e REIS, Ricardo Augusto da Luz, **Complex Integrated Circuit Design Strategy**, IEEE Journal of Solid State Circuits, New York, SC-17(3):459-64, June 1982. DOI: 10.1109/JSSC.1982.1051760

[2] HENTSCHKE, R., NARASIMHAM, J., JOHANN, M., REIS, R., **Maze Routing Steiner Trees with Delay vs. Wire Length Trade-off**, IEEE Transactions on Very Large Scale Integration, Volume 17, Issue 8, ISSN 1063-8210, August 2009, p. 1073-1086. DOI: 10.1109/TVLSI.2009.2019798

[3] GUTHAUS, M., WILKE, G., REIS, R., **Revisiting Automated Physical Synthesis of High-Performance Clock Networks**, ACM TODAES - ACM Transactions on Design Automation of Electronic Systems, Vol. 18, Issue 2, DOI: 10.1145/2442087.2442102, ISSN: 1084-4309, EISSN:1557-7309, March 2013.

[4] FLACH, G., REIMANN, T., POSSER, G., JOHANN, G., REIS, R.**, An Effective Method for Simultaneous Gate Sizing and V^{th} Assignment using Lagrangian Relaxation**, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 33, Issue 4, April 2014, p. 546-557, DOI: 10.1109/TCAD.2014.2305847, ISSN 0278-0070

[5] ZIESEMER, A., REIS, R., **Physical Design Automation of Transistors Network**, Microelectronics Engineering, V. 148, p. 122-128, December 2015, Elsevier B.V., ISSN: 0167-9317, doi:10.1016/j.mee.2015.10.018

[6] POSSER, G., MISHRA, V., JAIN, P., REIS, R., SAPATNEKAR, S., **Cell-Internal Electromigration: Analysis and Pin Placement Based Optimization**, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 35, N.2, February 2016, p. 220-231, ISSN 0278-0070, DOI: 10.1109/TCAD.2015.2456427.

[7] CONCEIÇÃO, C., REIS, R., **Transistor Count Reduction by Gate Merging**, IEEE Transactions on Circuits and Systems I, Vol. 66, Issue 6, June 2019, ISSN: 1558-0806, DOI: 10.1109/TCSI.2019.2907722.

[8] REIS, R., **Design Automation of Transistor Networks, a New Challenge**. IEEE International Symposium on Circuits and Systems, ISCAS2011, Rio de Janeiro, Brasil, May 15-19, 2011. IEEE Press. p. 2485-2488, ISBN: 978-1-4244-9472-9. DOI 10.1109/ISCAS.2011.5938108

[9] FOGAÇA, M., KAHNG, A., REIS, R., WANG, L., **Finding Placement-Relevant Clusters with Fast Modularity-Based Clustering**, 24th Asia and South Pacific Design Automation Conference (ASP-DAC) 2019, Tokyo, Japan, January 21-24, 2019. P. 569-576, DOI: 10.1145/3287624.3287676