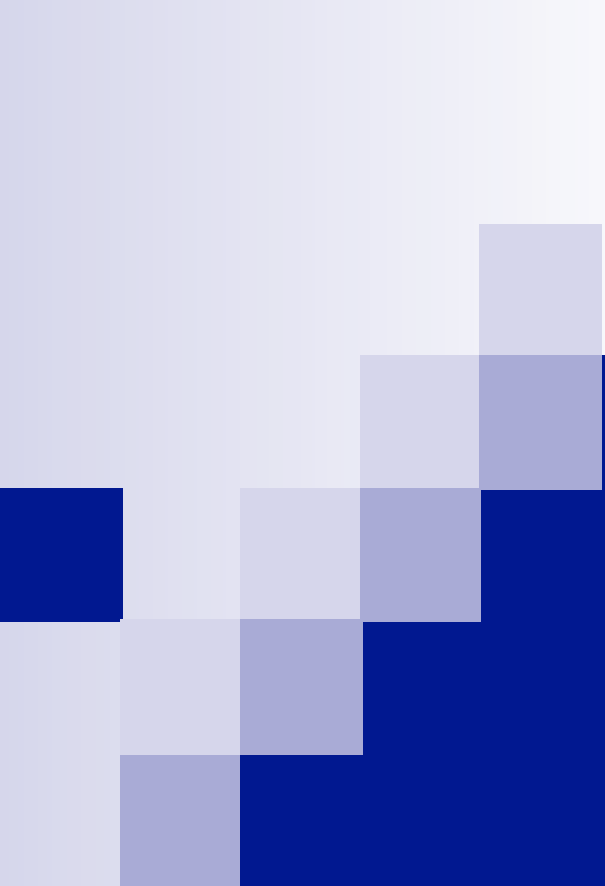




TAU 2014

Contest and more ...

Igor Keller

TAU 2014: Timing Workshop

- STA and related areas
 - Analog circuits ... also related
- Right forum for top STA experts
- Covers both mainstream and controversial topics
- Goals:
 - Re-discover STA
 - Bring STA science to design houses
 - Bring design experience to academics and EDA
 - Exchange ideas and build networking
 - Entice students to stay in EDA
 - Have fun ...

Technical Program

- 48 registered attendees
- EDA, design houses, foundries, academia
 - Altera, IBM, Intel, Cisco, Qualcomm, Broadcom, ADI, TI, Oracle, ARM, Swatch group, Samsung, TSMC, NVIDIA, Cadence, Synopsys
 - 8 universities
 - Countries: Switzerland, Greece, Ireland, Netherlands, Taiwan, Japan, Korea, USA
- 6 technical sessions squeezed into 2 days
- 17 papers (2 invited)
- 2 emotional panel discussions
- Timing Contest: 8 teams



The TAU 2014 Contest

Removing Pessimism during Timing Analysis



Jin Hu

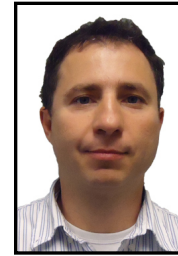
IBM Corp.

[Speaker]



Debjit Sinha

IBM Corp.



Igor Keller

Cadence

Sponsors:



cā dence



SYNOPSYS®

Past and Present Timing Contests

Goal of Coordinated Academic-Industry Contests

- ↳ Guided awareness of challenging projects at earlier academic stages
- ↳ Encourage novel parallelization techniques (including multi-threading)
- ↳ Facilitate infrastructure/benchmarks for future research

Develop Clever Methods for Solving Difficult Problems

- ↳ Gain insight from other perspectives and approaches
- ↳ Allow algorithm development through focused problem statement

Previous Contests



PATMOS'2011

Timing Analysis Contest



TAU 2013 contest: Variation aware timing analysis



Focused Problem Statement

Develop an algorithm to perform

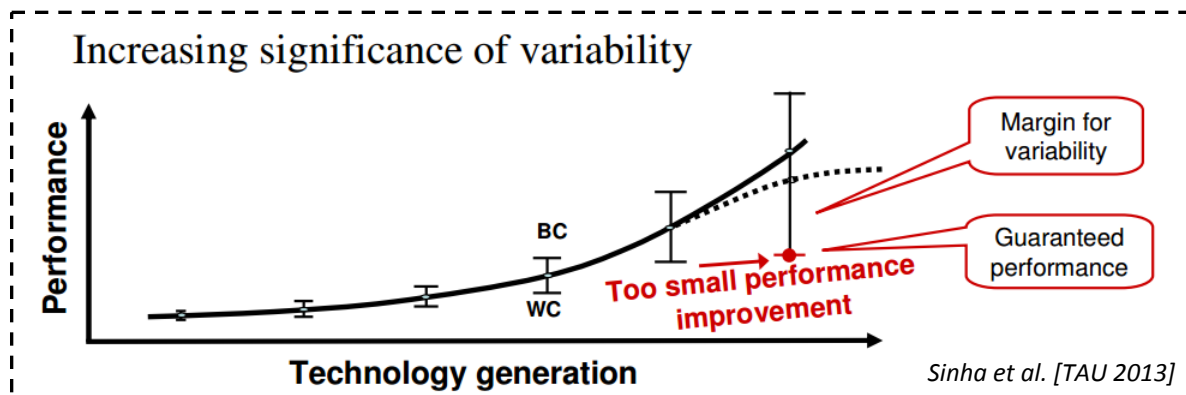
Common Path Pessimism Removal CPPR

during timing analysis

CPPR: the process of removing inherent but artificial pessimism from timing tests and paths

CPPR Relevance

Variability causes many sources of timing uncertainty



Manufacturing Variations

- ↳ Metal thickness (CMP)
- ↳ Random dopant effects (V_t)
- ↳ Line-edge roughness

Voltage & Temperature Variations

- ↳ Across surface of chip
- ↳ From cycle to cycle

Electrical Effects

- ↳ Potential coupling noise
- ↳ Simultaneous signal switching

**Global chip-to-chip variations*

Difficult to accurately and quickly model for all variation sources

Create **lower** (early) and **upper** (late) delay bounds [*lb*, *ub*]

- ↳ Commonly found by **derating** original delay, e.g., $\pm 5\%$
- ↳ Any unknown, difficult-to-model effect can be accounted for

✚ **Good news**: additional pessimism introduced (desirable for safe chip operation)

✗ **Bad news**: additional pessimism introduced (unnecessary)

CPPR prevents over-optimization of design due to **false timing fails**

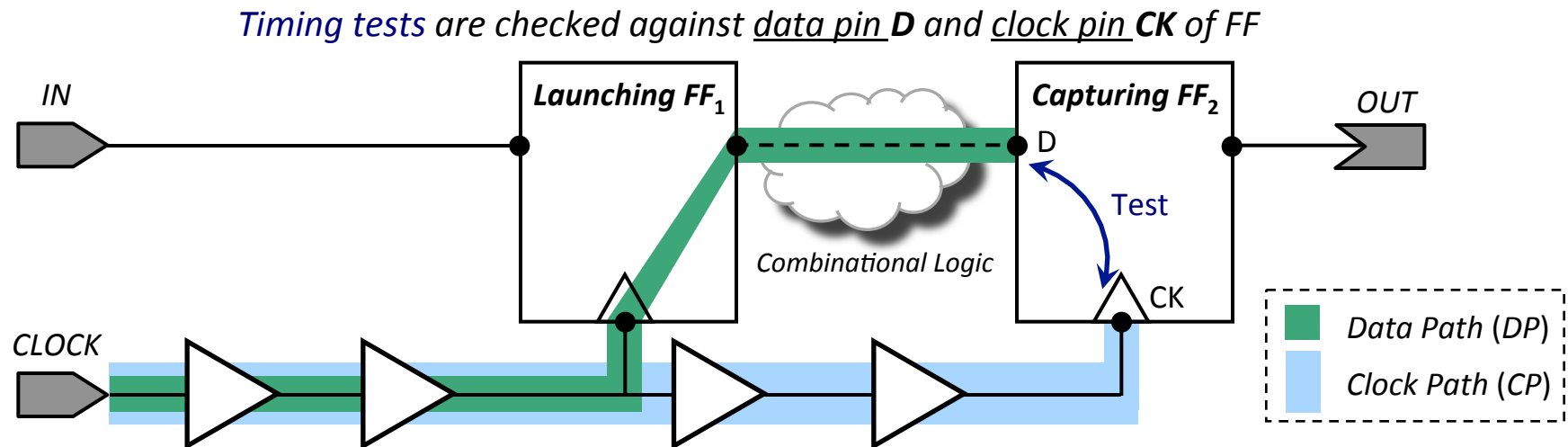
Sequential Timing Analysis

Details provided in
contest_education.pdf

Hold Tests (Same Cycle)

[data must be stable t_{HOLD} time after clock arrives]

$$\underbrace{slack_{HOLD}}_{\text{pre-CPPR slack}} = \underbrace{at(D)}_{\text{arrival time at D}} - \underbrace{at(CK)}_{\text{arrival time at CK}} - \underbrace{t_{HOLD}}_{\text{hold time}}$$



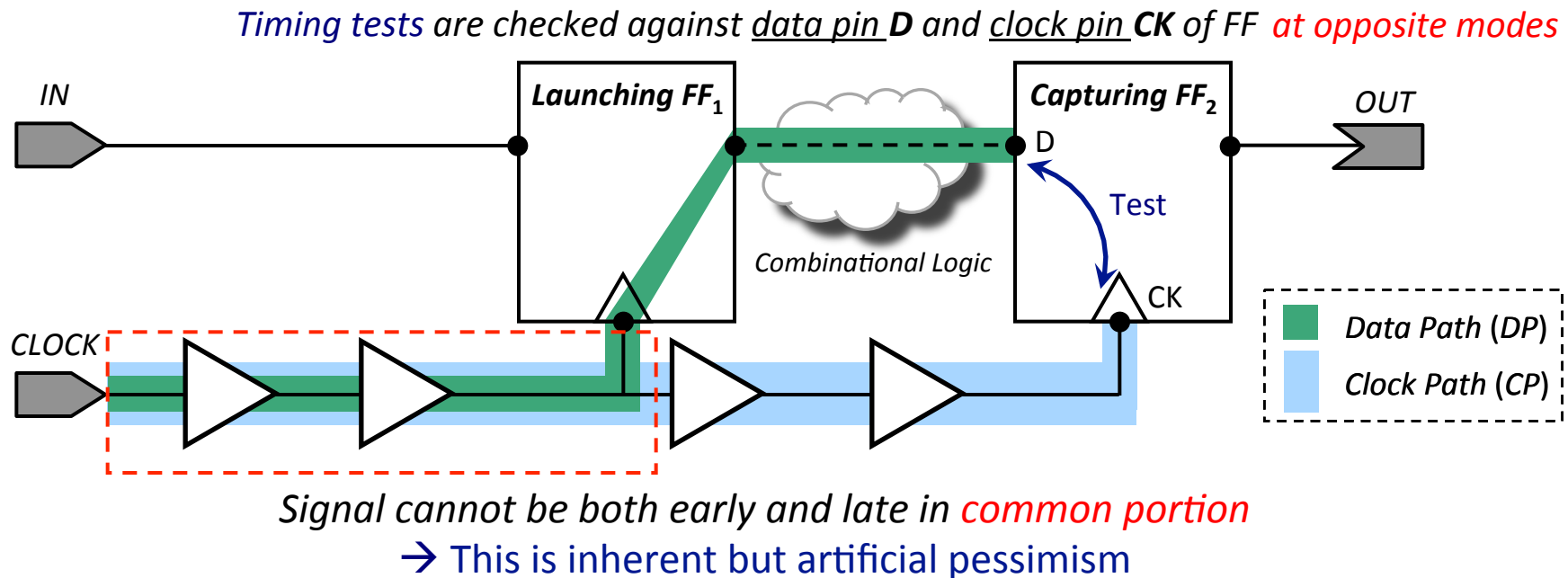
Sequential Timing Analysis

Details provided in
contest_education.pdf

Hold Tests (Same Cycle)

[data must be stable t_{HOLD} time after clock arrives]

$$\underbrace{slack_{HOLD}}_{\text{pre-CPPR slack}} = \underbrace{at^E(D)}_{\text{early arrival time at D}} - \underbrace{at^L(CK)}_{\text{late arrival time at CK}} - \underbrace{t_{HOLD}}_{\text{hold time}}$$



Common Path Pessimism Removal

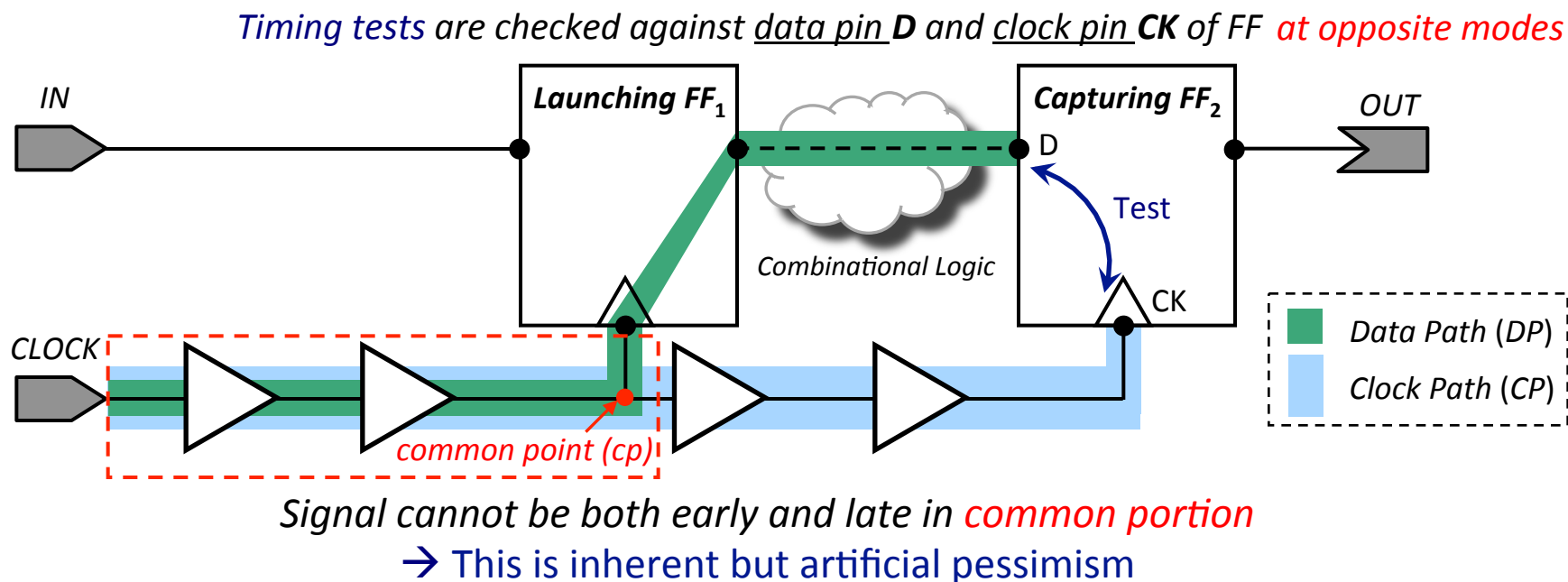
Details provided in
contest_education.pdf

Hold Tests (Same Cycle)

$$\underbrace{\text{slack}_{HOLD}}_{\text{post-CPPR slack}} = \underbrace{\text{at}^E(D)}_{\text{early arrival time at D}} - \underbrace{\text{at}^L(CK)}_{\text{late arrival time at CK}} - \underbrace{t_{HOLD}}_{\text{hold time}}$$

$$+ [\underbrace{\text{at}^L(cp)}_{\text{late arrival time at cp}} - \underbrace{\text{at}^E(cp)}_{\text{early arrival time at cp}}] \leftarrow \text{Apply [Hold CPPR credit]}$$

[data must be stable t_{HOLD} time after clock arrives]

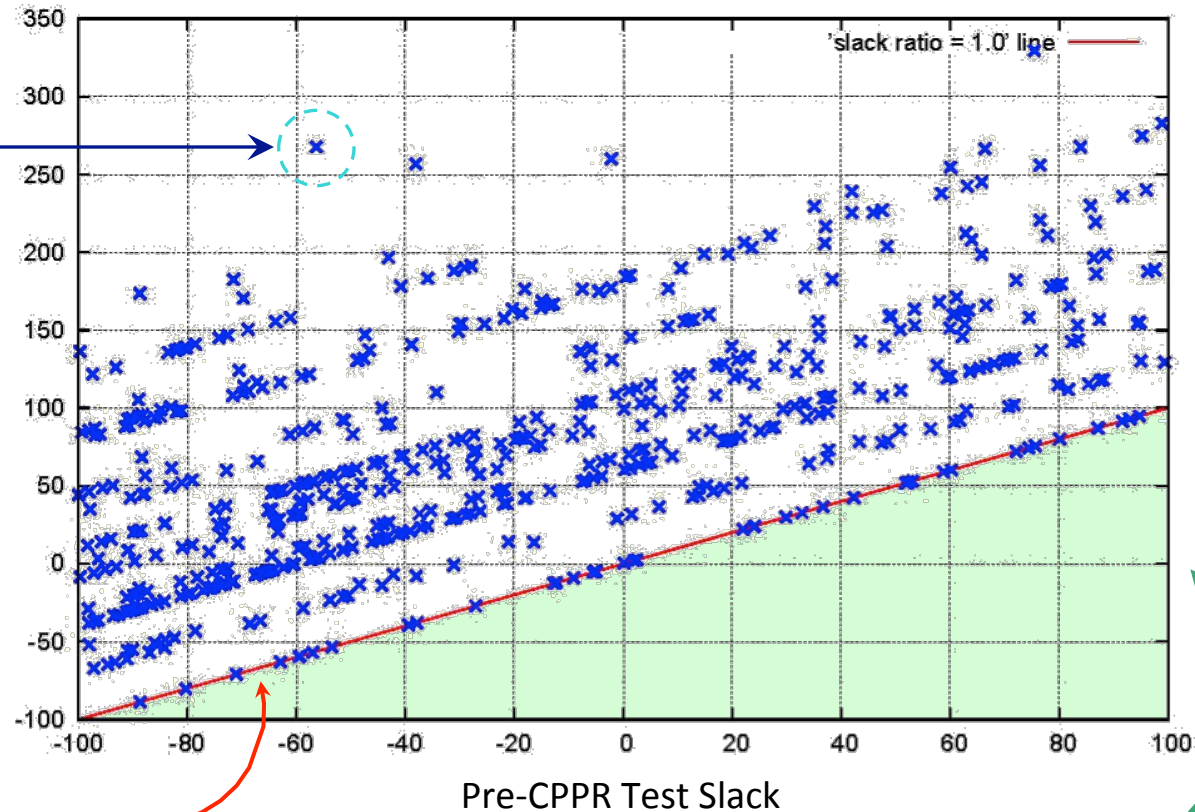


Potential Impact of CPPR

**if done correctly*

CPPR can only improve test slacks (never overly optimistic)

Scatter plot showing pessimism reduction with CPPR for Hold tests for des_perf



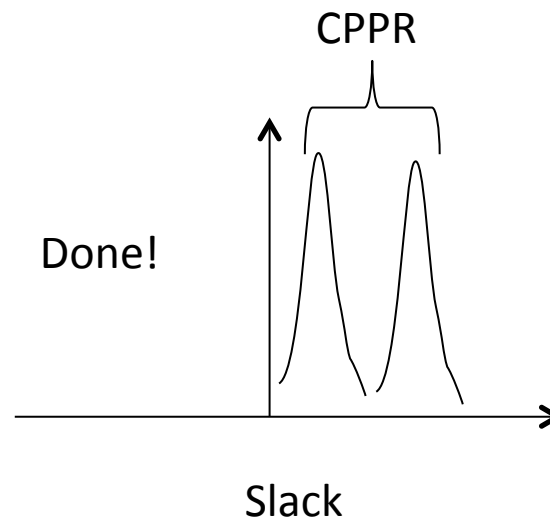
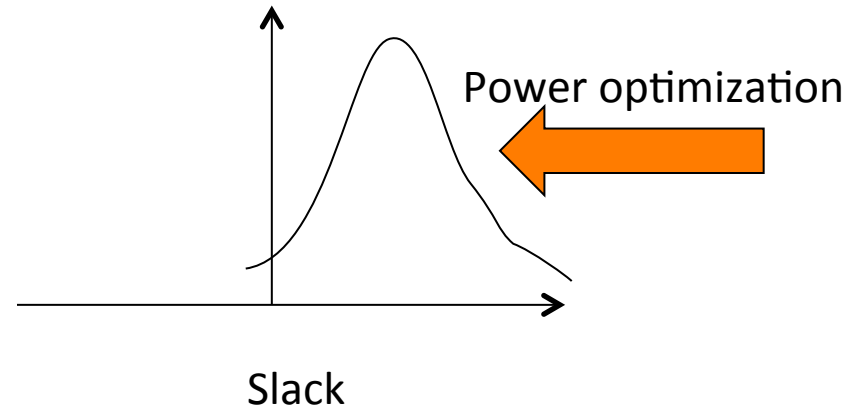
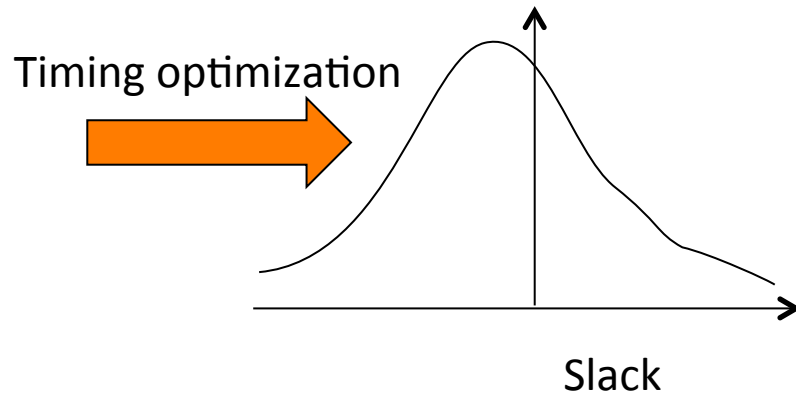
Pre-CPPR slack ≈ -55
Post-CPPR slack $\approx +275$

Post-CPPR Test Slack

pre-CPPR slack = post-CPPR slack

no post-CPPR slack worse
than its pre-CPPR slack

Why is CPPR Important?





Why is CPPR Difficult?

- Exponential complexity
- Analysis of graph for re-converging paths
- High runtime and memory
- Grows fast with number of clock nets in the design
- Possible but not easy to parallelize
- Devil is in the details ...

TAU 2014 Contest Motivation

CPPR Challenges

- ↳ Analysis is path-based: can have **exponential runtime**
 - CPPR can be **overly optimistic** if not enough paths are considered
- ↳ Existing literature and research is **limited**

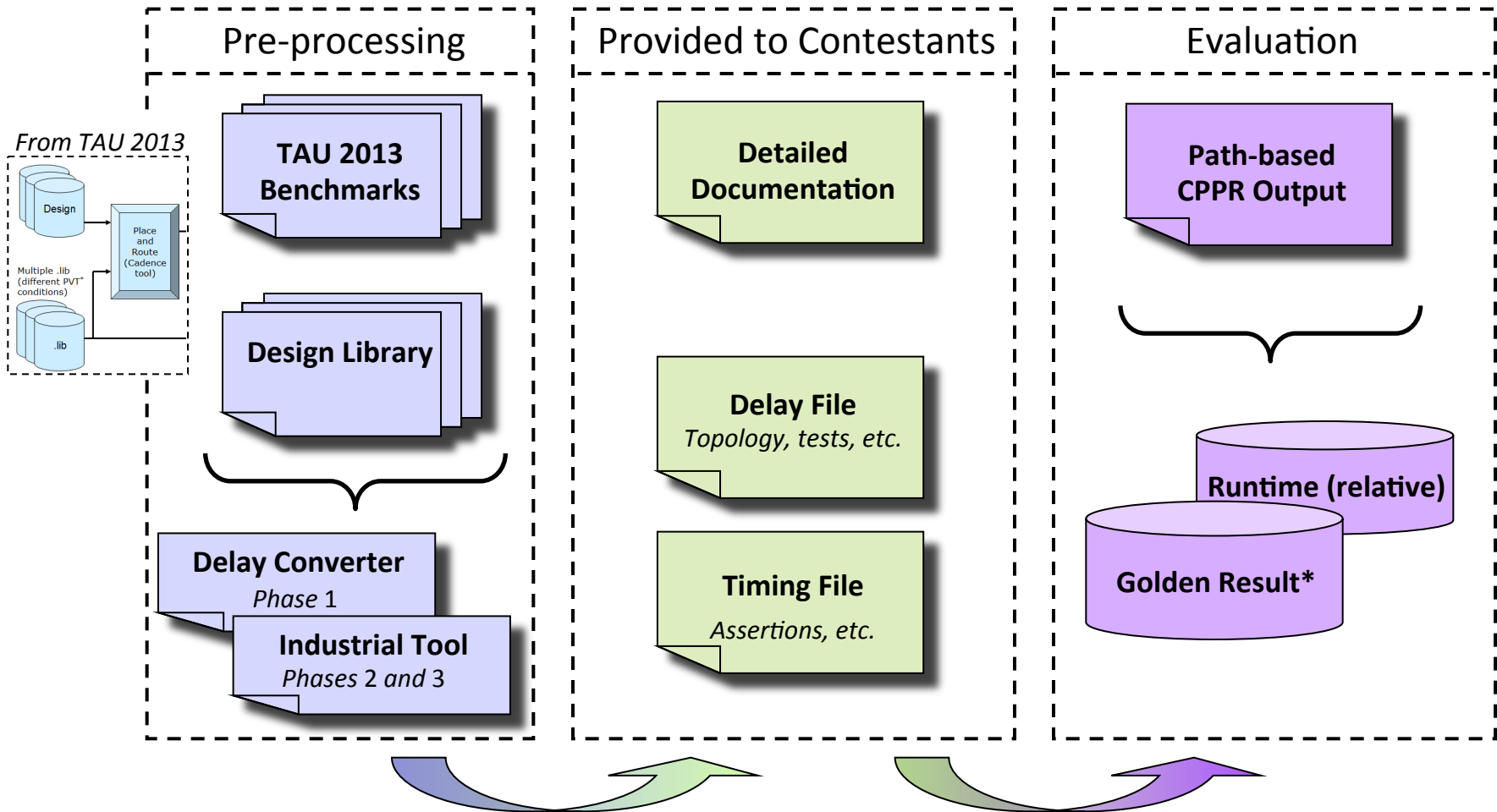
Contest / Topic Scope

- ↳ Timeline spans roughly 2.5 months **not accounting for holidays*
- ↳ Only **Hold** + **Setup** tests considered
- ↳ *No latches (flush segments) considered*
- ↳ *Limited design topologies, e.g., clock tree reconvergence*
- ↳ *Limited to deterministic timing (no statistical)*

Lessons Learned from Previous Contests

- ↳ Simplify **input / output** processing
 - focus on **algorithm development** and **performance optimizations**
- ↳ Provide adequate **documentation**
 - assumes **no** prior knowledge of timing analysis or CPPR

TAU 2014 Contest Guidelines

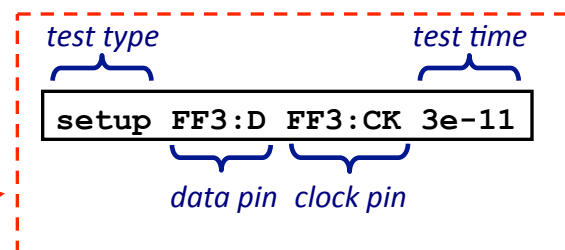
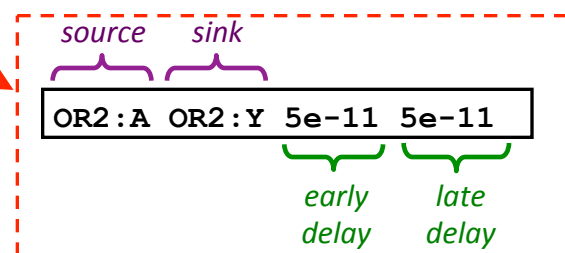
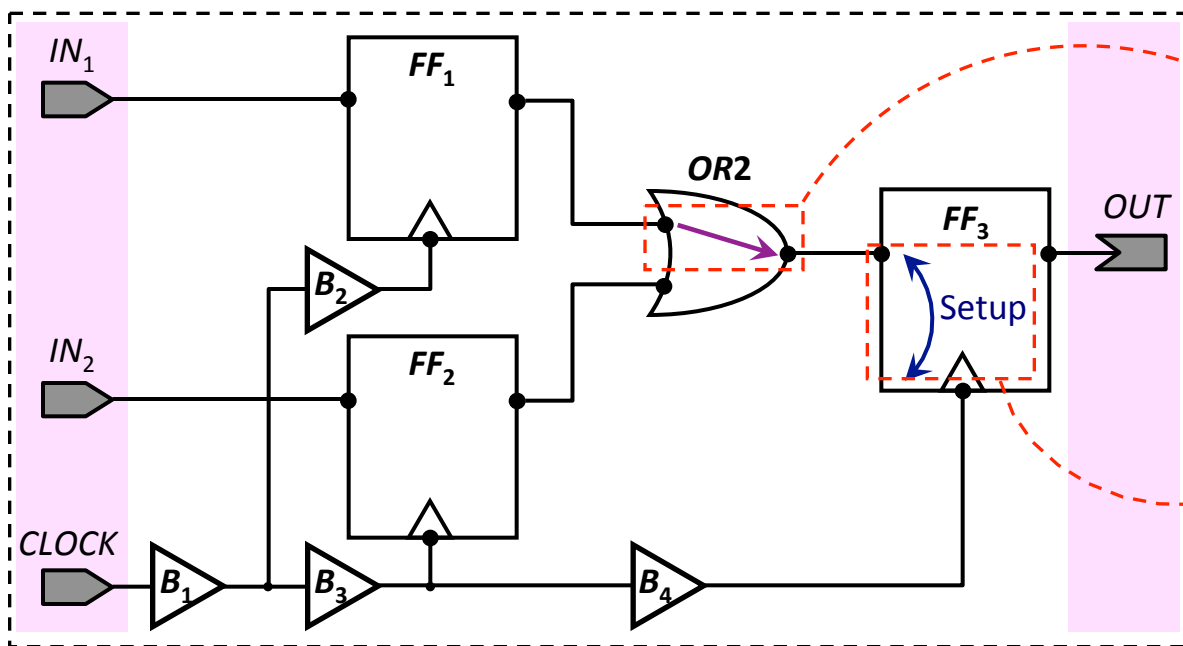
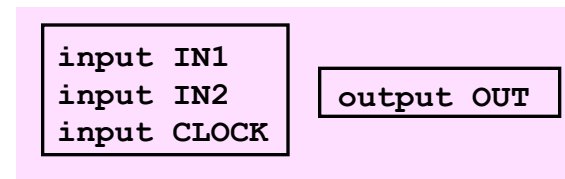
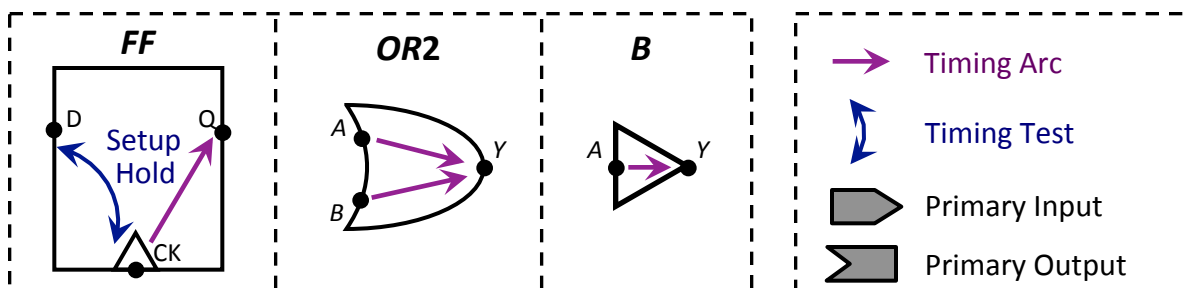


*Industrial tool

Inputs: Delay File

Details provided in
contest_file_formats.pdf

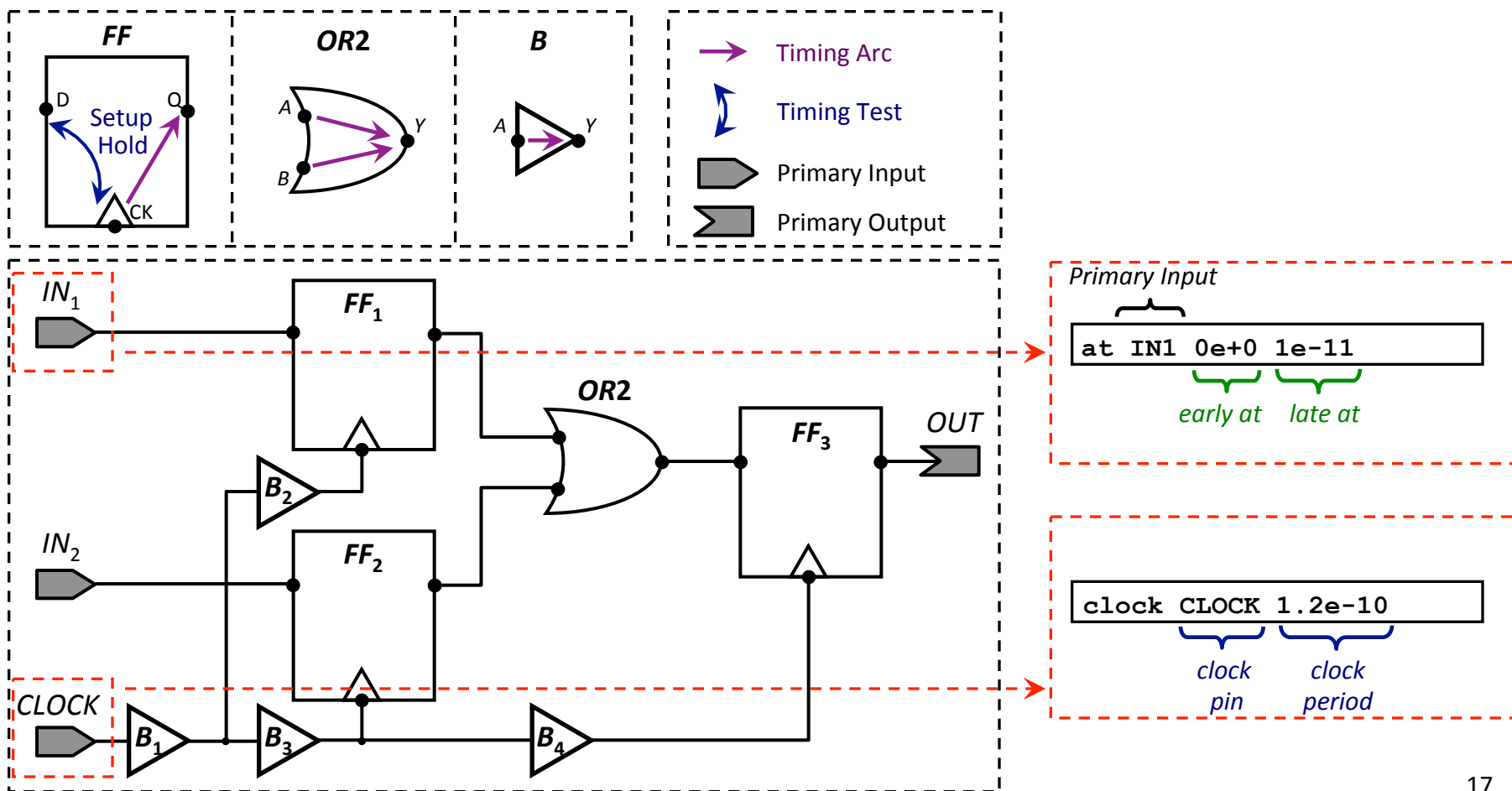
- ↳ Specifies **primary inputs** and **outputs**
- ↳ Provides **early** and **late propagation delay** for every **source-to-sink timing arc**
- ↳ Provides **setup** and **hold times** for every **data-to-clock timing test**



Inputs: Timing File

Details provided in
contest_file_formats.pdf

- ↳ Provides **early** and **late arrival times** for each **primary input**
- ↳ Provides **clock period** for the **clock source**



Benchmarks

Phase 1

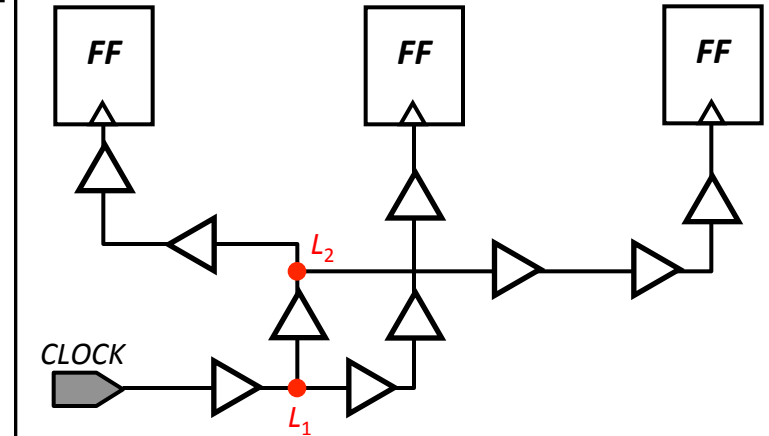
[6-42 Tests]

Based on TAU 2013 v1.0
benchmarks (sequential circuits)

Design	Number of:			
	PIs	POs	Segments	Tests
s27	6	1	112	6
s344	11	11	658	30
s349	11	11	682	30
s386	9	7	701	12
s400	5	6	813	42
s510	21	7	1091	12
s526	5	6	1097	42
s1196	16	14	2.4K	36
s1494	10	19	2.9K	12

Added more complex (randomized) clock tree

- ↳ **BRANCH**(CLOCK, initial FF)
- ↳ For each remaining FF
 - ↳ Select random location L in current tree
 - ↳ **BRANCH**(L , FF)
- **BRANCH**(src, sink): create buffer chain from src to sink



Phase 2

[380-50.1K Tests]

Based on TAU 2013 v2.0
benchmarks (openCore)

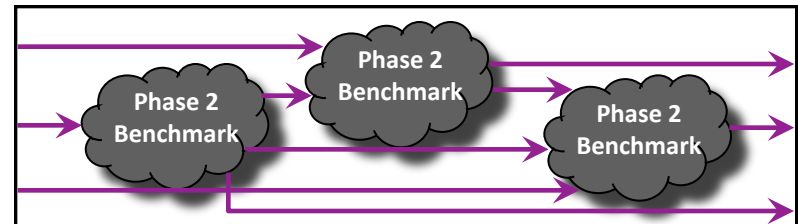
Design	Number of:			
	PIs	POs	Segments	Tests
systemcdes	132	65	13.3K	380
wb_dma	217	215	17.4K	1374
tv80	14	32	23.7K	838
systemcaes	260	129	29.6K	2.5K
mem_ctrl	115	152	45.0K	3.7K
ac97_ctrl	84	48	55.7K	9.3K
usb_funct	128	121	66.1K	4.3K
pci_bridge32	162	207	78.2K	16.4K
aes_core	260	129	86.7K	2.5K
des_perf	235	64	404.2K	19.7K
vga_lcd	89	109	525.6K	50.1K

Phase 3

(Evaluation)

[8.2K to 109.6K Tests]

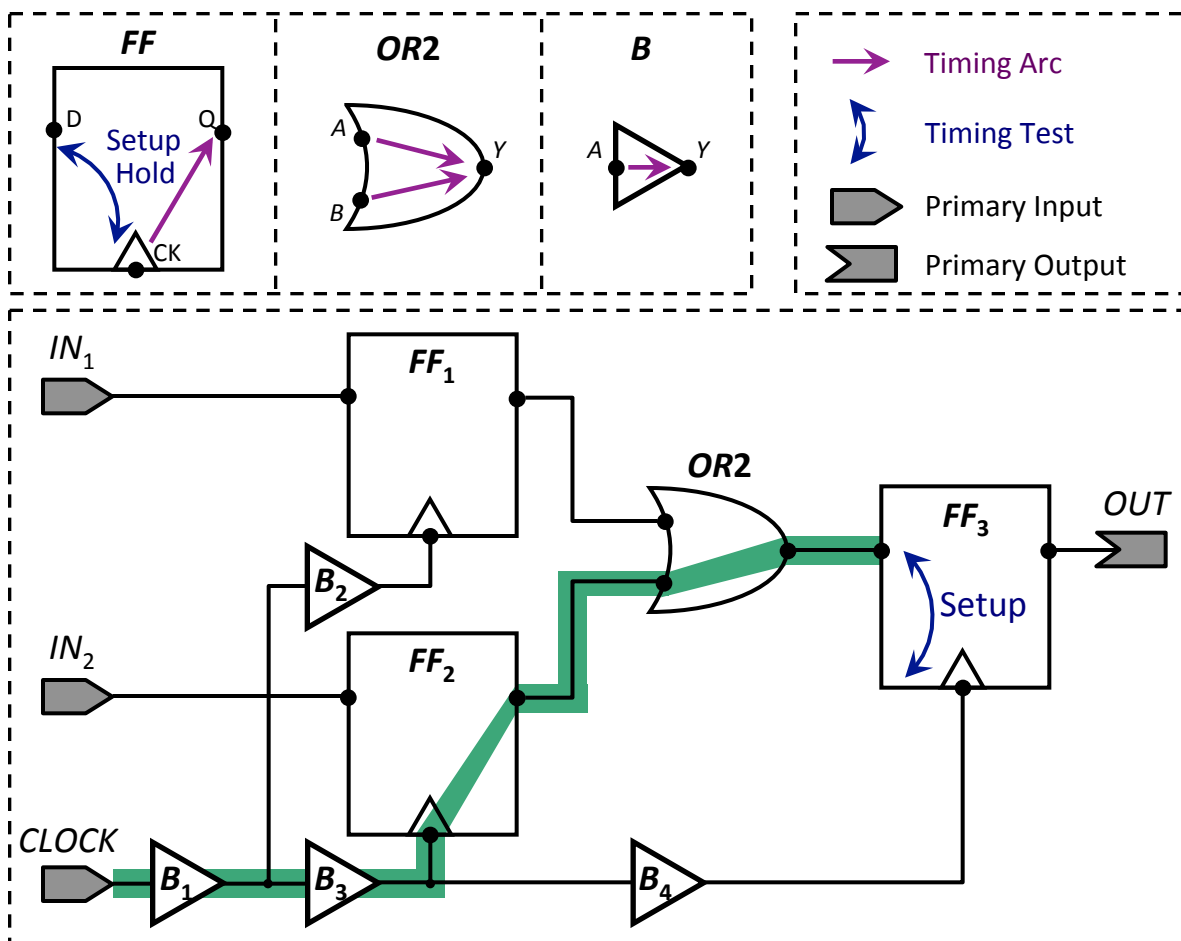
Design	Number of:			
	PIs	POs	Segments	Tests
Combo2	170	218	284.4K	29.5K
Combo3	353	215	216.2K	8.2K
Combo4	260	169	866.3K	53.5K
Combo5	432	164	2229.6K	79.0K
Combo6	486	174	3843.9K	128.2K
Combo7	459	148	3012.3K	109.6K



Output File

Details provided in
contest_file_formats.pdf
contest_rules.pdf

- [timing analysis] [after CPPR]
- Requires pre-CPPR and post-CPPR slacks for each **test** and **path**
 - Controllable options: **<testType>** **-numTests <int>** **-numPaths <int>**
 - [setup/hold/both] [number of tests] [number of paths per test]



test type -numPaths

setup	-3e-11	-1e-11	1
-------	--------	--------	---

pre-CPPR test slack post-CPPR test slack

path length

-1.5e-11	-1e-11	10
----------	--------	----

pre-CPPR path slack post-CPPR path slack

FF3:D
OR2:Y
OR2:A
FF2:Q
FF2:CK
B3:Y
B3:A
B1:Y
B1:A
CLOCK

pin-to-pin data path
from: data pin of test
to: primary input

Evaluation Metrics

Accuracy (Compared to “Golden” Results)

T : set of all tests in D
 P : set of all paths in D

Slack Accuracy (Difference)

[0, 1]	ps	100
(1, 3]	ps	80
(3, 5]	ps	50
(5, ∞)	ps	0

Test t Slack Accuracy $A(t)$

- ↳ Pre-CPPR test slack
- ↳ Post-CPPR test slack

Path p Slack Accuracy $A(p)$

- ↳ Pre-CPPR path slack
- ↳ Post-CPPR path slack
- ↳ Correctness of path

(Raw) Testcase D Accuracy $A(D)$

- ↳ Average of $A(t)$ for all tests t in T
- ↳ Average of $A(p)$ for all paths p in P
- ↳ Average of $A(dp(t))$ for all tests t in T , where $dp(t)$ is the critical path of t
- ↳ Minimum of $\{A(t)\}$ for all tests t in T
- ↳ $A(critT)$, where $critT$ is the most critical test

*First three considers overall tool quality;
 Last two considers worst tool quality*

Runtime Factor (Relative)

$$RF(D) = \frac{\text{runtime}(D)}{\text{Average of all contestants}}$$

Composite Testcase Score

$$\text{score}(D) = A(D) \times (0.5 + 0.5 \times RF(D))$$

Overall Contestant Score

Average of $\text{score}(D)$ for all designs

TAU 2014 Contestants

	University	Country	Team Name
	National Chiao Tung University	Taiwan	iTimerC
	University of Thessaly	Greece	The TimeKeepers
	National Tsing Hua University	Taiwan	TTT
	India Institute of Technology, Madras	India	ElecEnthus
	University of Illinois at Urbana-Champaign	USA	UI-Timer
	India Institute of Technology, Madras	India	LightSpeed
	Missouri University of Science and Technology	USA	MST_CAD
	Peking University	China	PKU-HappyTimer

Contestant Performance

Overall quality of submitted binaries was superb

One testcase comprised of $\langle \text{benchmark}, \text{testType}, -\text{numTests}, -\text{numPaths} \rangle \rightarrow 24 \text{ total}$

↳ For each **Combo** benchmark, used 4 settings: $\begin{bmatrix} -\text{setup} \\ -\text{hold} \end{bmatrix} \times \begin{bmatrix} -\text{numTests } N & -\text{numPaths } 1 \\ -\text{numTests } n & -\text{numPaths } m \end{bmatrix}$
 $n < N < 50K, m < 20$

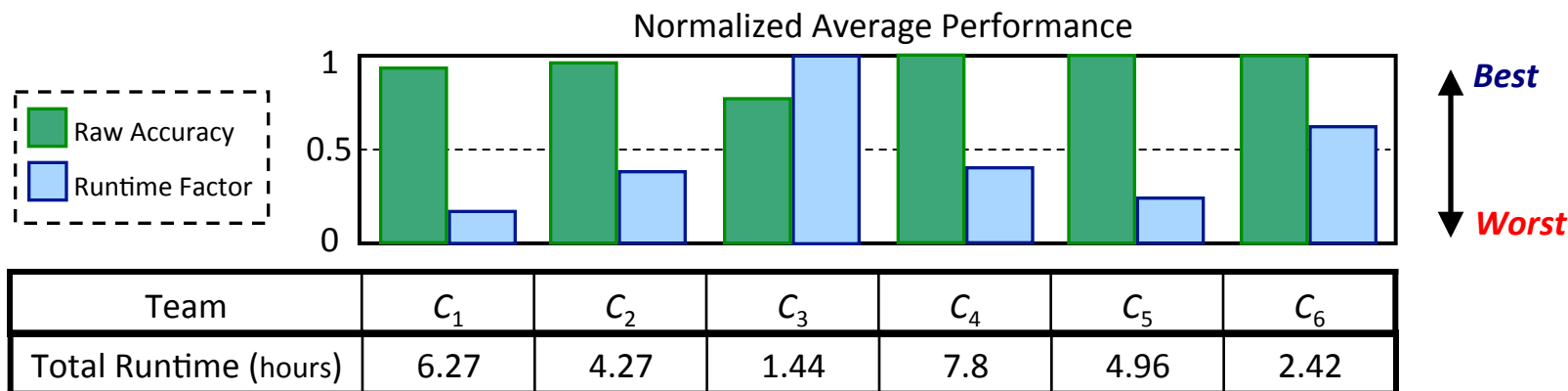
Ex: Combo7 -setup -numTests 35000 -numPaths 1

↳ **5 of 7** final submissions had **no crashes**; 1 of 7 crashed on only 5 testcases

↳ 6 of 7 final submissions had full accuracy on 12 designs

Evaluation Machine: 8X Intel(R) Xeon CPU E7-8837 @2.67GHz

↳ **6 of 7** final submissions used **8 threads** [maximum allowed];
 1 of 7 final submissions used 2 threads



*Final evaluation is design-specific, not based on total runtime or overall averages

Acknowledgments

↳ Jobin Kavalam, Nitin Chandrachoodan [IITimer from TAU 2013]
Provided timer source code, helped with initial input file conversions

↳ Jin Hu (IBM), Debjit Sinha (IBM) , Chirayu Amin (Intel)

Special Thanks to
the TAU 2014 Contestants

*This contest would not have been successful
without your hard work and dedication*



Winners



TAU 2014 Timing Contest

Removing Common Path Pessimism

Third Place Award

Presented to

Yu-Ming Yang, Yu-Wei Chang and Iris Hui-Ru Jiang

National Chiao Tung University, Taiwan

For
iTimerC

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair



TAU 2014 Timing Contest

Removing Common Path Pessimism

Honorable Mention

Presented to

Christos Kalonakis, Charalampos Antoniadis, Panagiotis Giannakou,
Dimos Dioudis, George Pinitas and George Stamoulis

University of Thessaly, Greece

For
The TimeKeepers

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair



TAU 2014 Timing Contest

Removing Common Path Pessimism

Second Place Award

Presented to

M S Santosh Kumar and Sireesh N

IIT Madras, India

For
LightSpeed

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair



TAU 2014 Timing Contest

Removing Common Path Pessimism

First Place Award

Presented to

Tsung-Wei Huang, Pei-Ci Wu and Martin D. F. Wong

University of Illinois at Urbana-Champaign, USA

For
UI-Timer

Chirayu Amin
General Chair

Igor Keller
Technical Chair

Jin Hu
Contest Chair



Thank you!



Backup

Contest Timeline

Date	Activity
10/13/2013	Contest release date https://sites.google.com/site/taucontest2014 • Timing analysis and CPPR tutorial [contest_education.pdf] • Contest overview and guidelines [contest_rules.pdf] • Contest input and output specifications [contest_file_formats.pdf] • Source code from the winners of TAU 2013 Contest (IITimer)
11/22/2013 – 12/02/2013 – 01/06/2014	End of contest registration • Phase 1 Benchmark Set [9 testcases] • Phase 2 Benchmark Set [6 testcases]
01/15/2014	Alpha binary submission
02/01/2014 [~2.5 months]	Final binary + short report submission
03/07/2014	Winners announced (today!)

Common Path Pessimism Removal

Details provided in
contest_education.pdf

Hold Tests (Same Cycle)

$$\underbrace{\text{slack}_{\text{HOLD}}}_{\text{post-CPPR slack}} = \underbrace{\text{at}^E(D)}_{\text{early arrival time at D}} - \underbrace{\text{at}^L(\text{CK})}_{\text{late arrival time at CK}} - \underbrace{t_{\text{HOLD}}}_{\text{hold time}}$$

$$+ [\underbrace{\text{at}^L(\text{cp})}_{\text{late arrival time at cp}} - \underbrace{\text{at}^E(\text{cp})}_{\text{early arrival time at cp}}] \leftarrow \text{Apply [Hold CPPR credit]}$$

[data must be stable t_{HOLD} time after clock arrives]

Setup Tests (Next Cycle with clock period P)

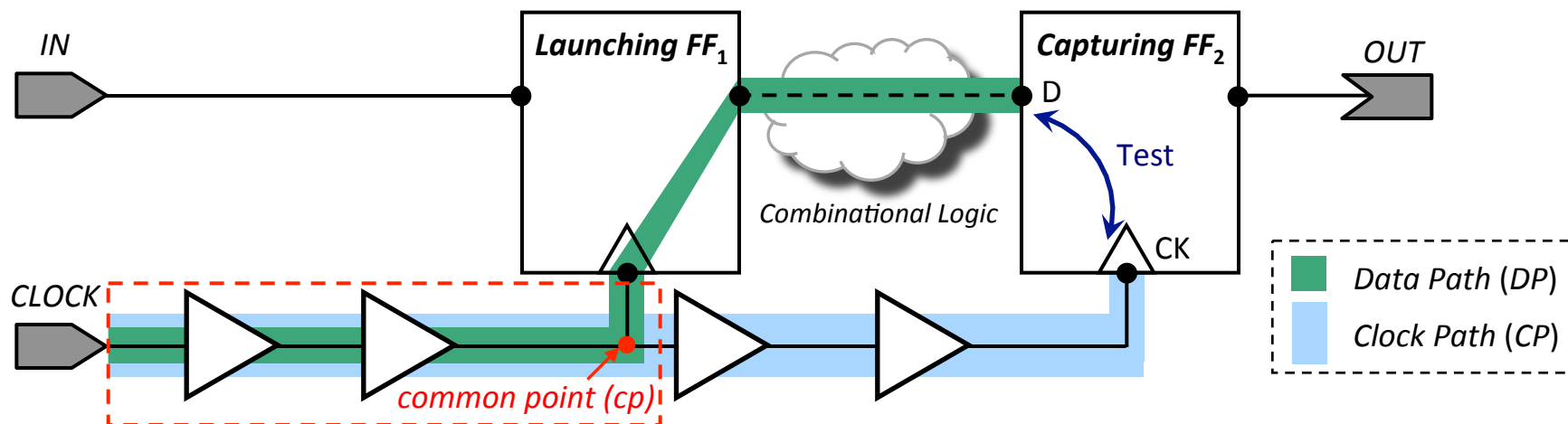
$$\underbrace{\text{slack}_{\text{SETUP}}}_{\text{post-CPPR slack}} = \underbrace{\text{at}^E(\text{CK})}_{\text{early arrival time at CK}} + \underbrace{P}_{\text{clock period}} - \underbrace{\text{at}^L(D)}_{\text{late arrival time at D}} - \underbrace{t_{\text{SETUP}}}_{\text{setup time}}$$

$$+ [\underbrace{\text{delay}^L(\text{OL})}_{\text{late delays of CP and DP overlap}} - \underbrace{\text{delay}^E(\text{OL})}_{\text{early delays of CP and DP overlap}}] \leftarrow \text{Apply [Setup CPPR credit]}$$

[data must be stable t_{SETUP} time before clock arrives]

$\text{OL} = \text{CP} \cap \text{DP}$

Timing tests are checked against data pin D and clock pin CK of FF **at opposite modes**



Signal cannot be both early and late in **common portion**
→ This is inherent but artificial pessimism