

Carbon Nanotube Computer

Transforming Scientific Discoveries into Working Systems

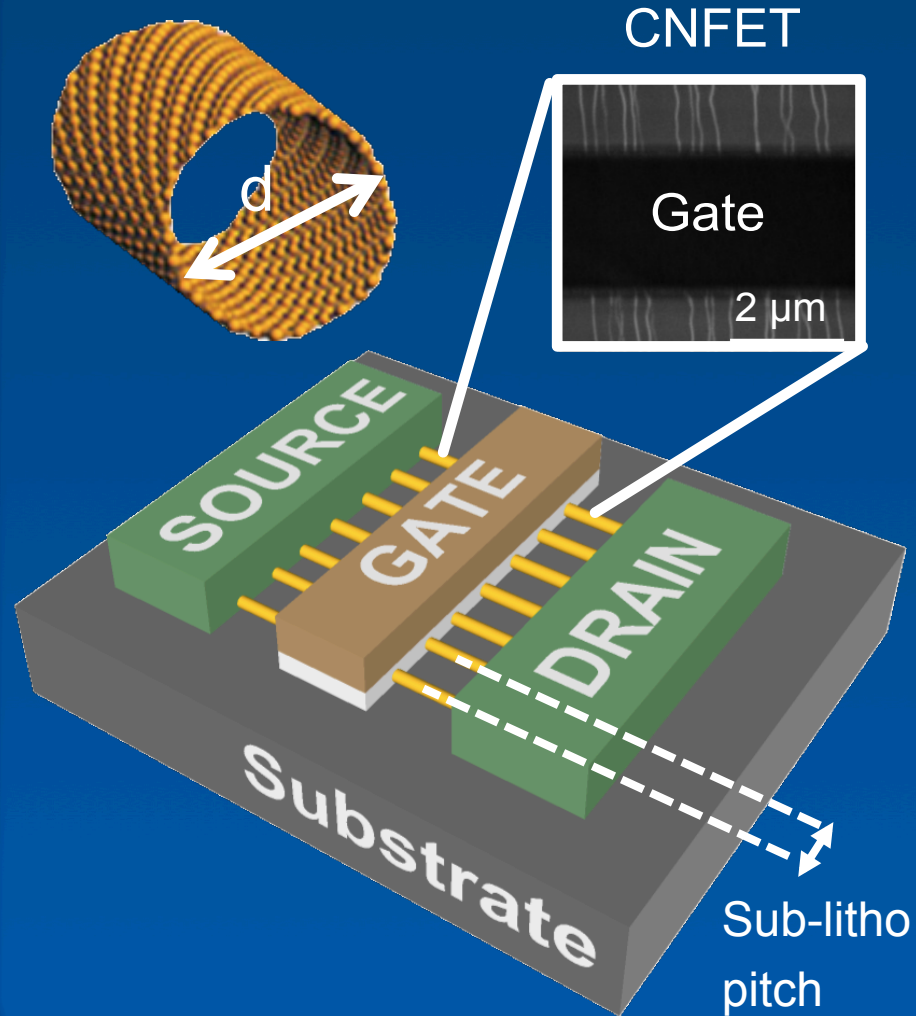
Subhasish Mitra



Department of EE & Department of CS
Stanford University

Carbon Nanotube FET (CNFET)

CNT: $d = 1.2\text{nm}$



Scalability (9nm)

- IBM

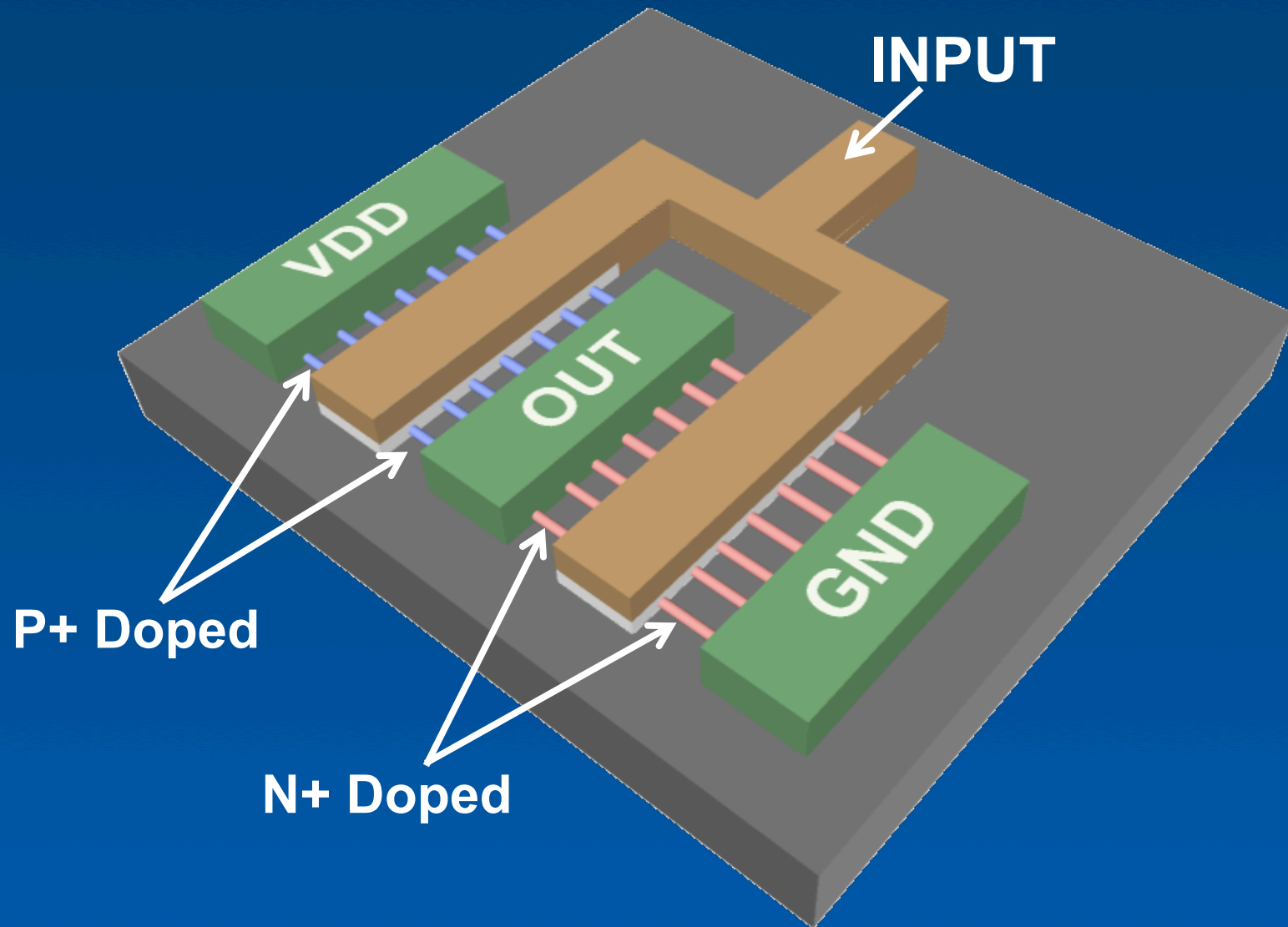
Supply: $\leq 0.4\text{V}$

- PKU, Stanford

Energy efficiency: 10X

- IBM Power 7 model

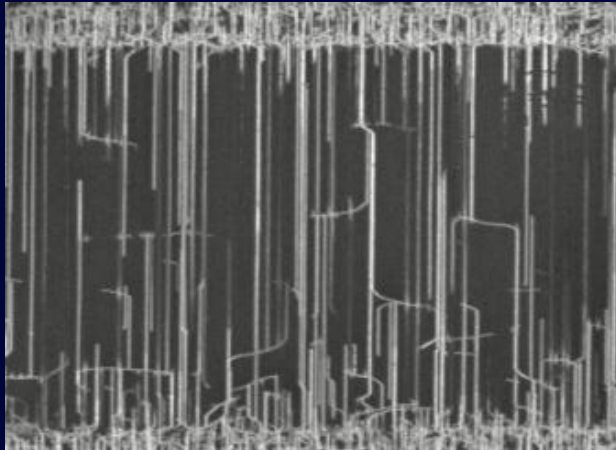
CNFET Inverter



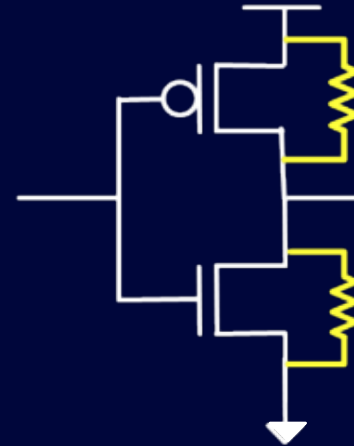
Big Promise, Major Obstacles

- Process advances alone inadequate

Mis-positioned CNTs

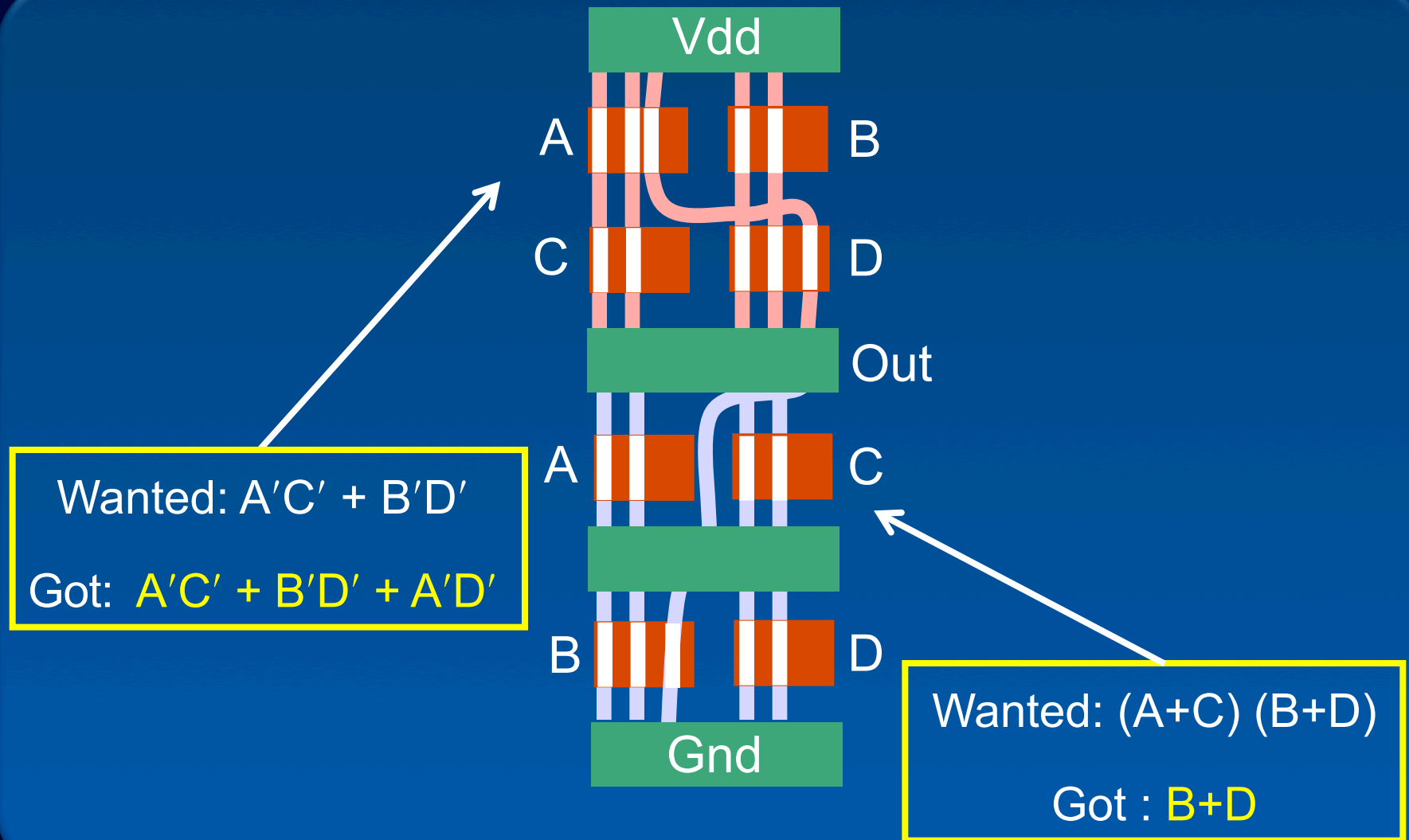


Metallic CNTs



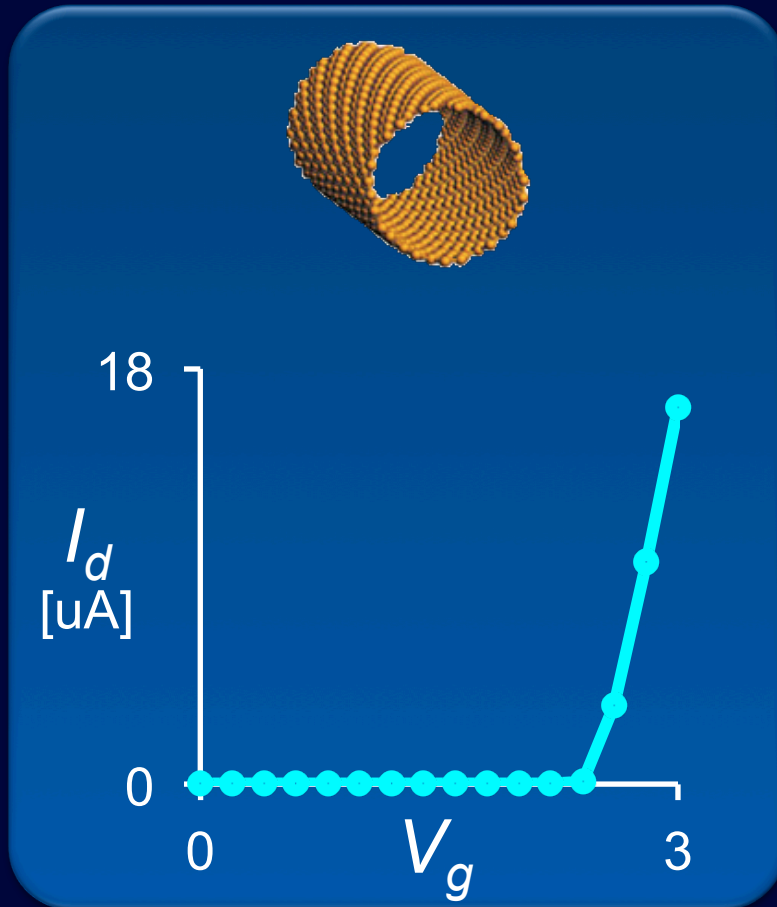
Solution: Imperfection-immune design

Mis-positioned CNTs

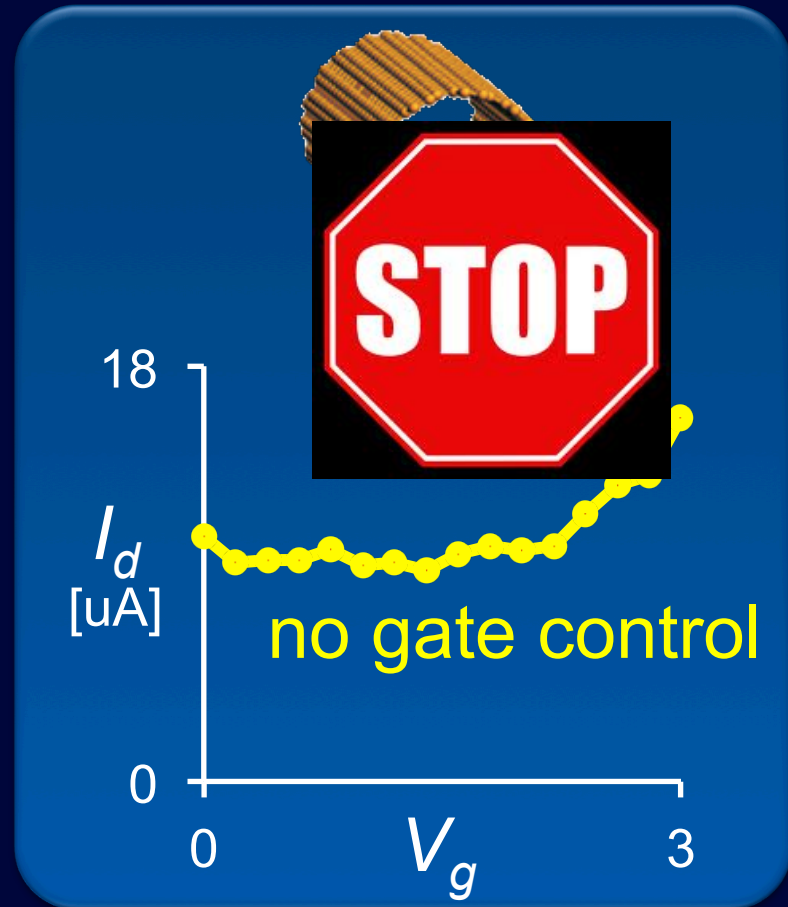


Metallic CNTs

Semiconducting CNT (s-CNT)



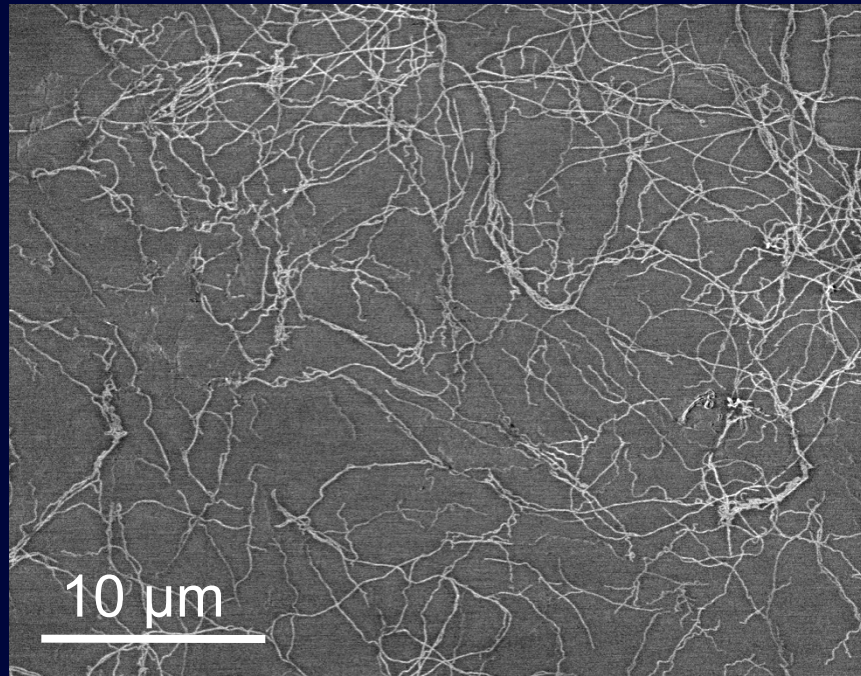
Metallic CNT (m-CNT)



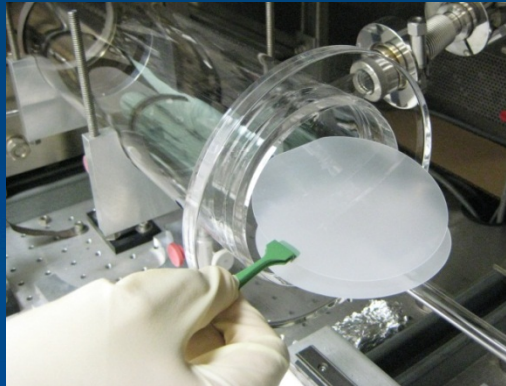
1 – 50% grown CNTs metallic

CNT Growth on Silicon

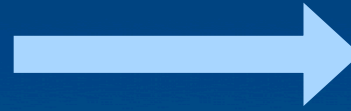
- Highly mis-positioned



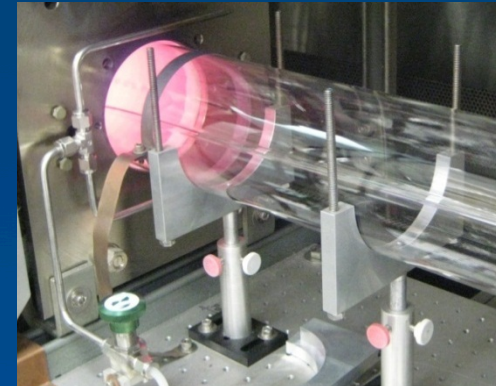
First Wafer-Scale Aligned CNT Growth



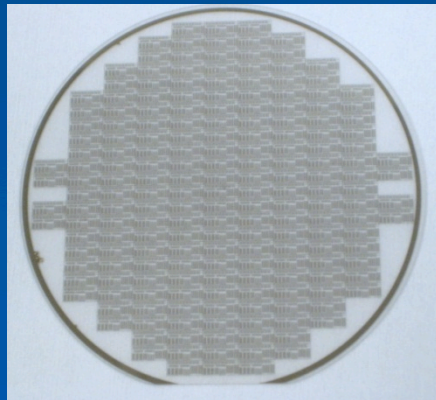
Quartz wafer
with catalyst



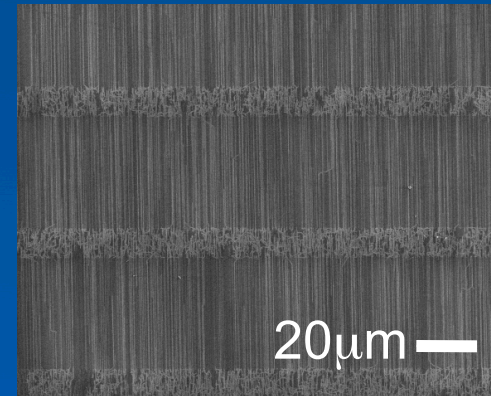
Aligned
CNT growth



Quartz wafer with CNTs



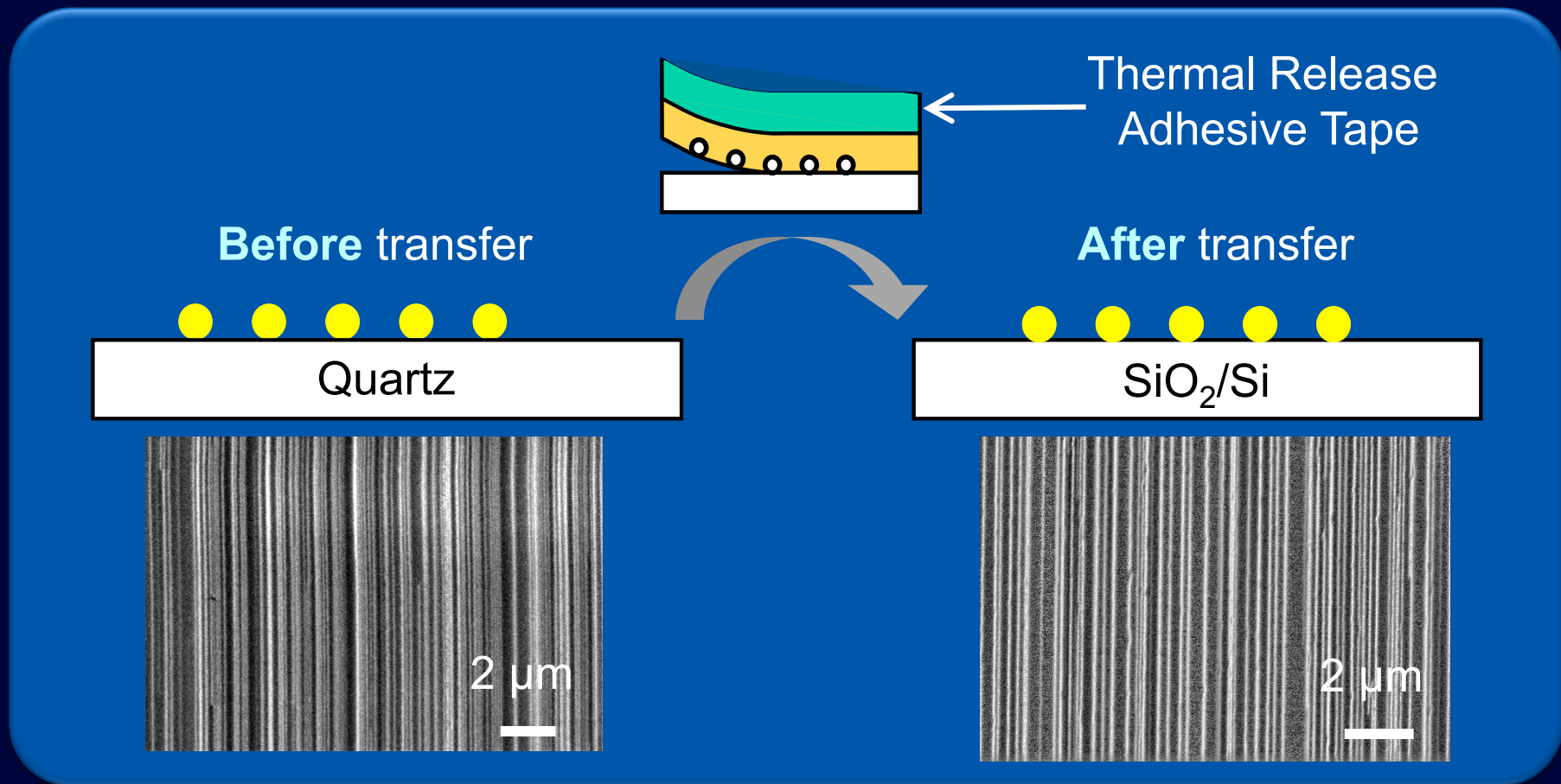
99.5% aligned CNTs



Stanford Nanofabrication Facility

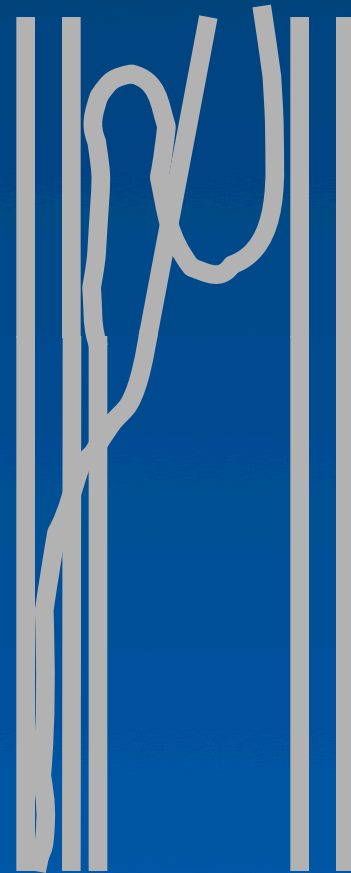
Wafer-Scale CNT Transfer

- Low temperature (90°C – 120°C)



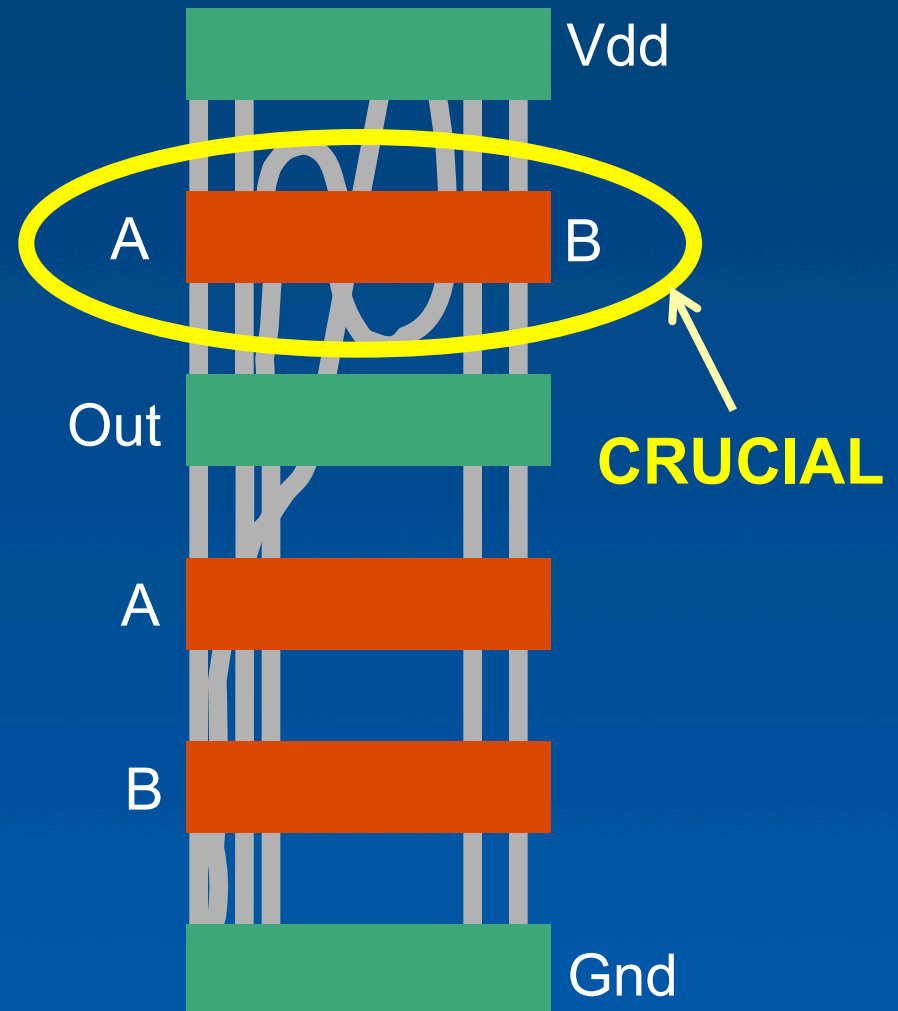
Mis-Positioned CNT-Immune NAND

1. Grow CNTs



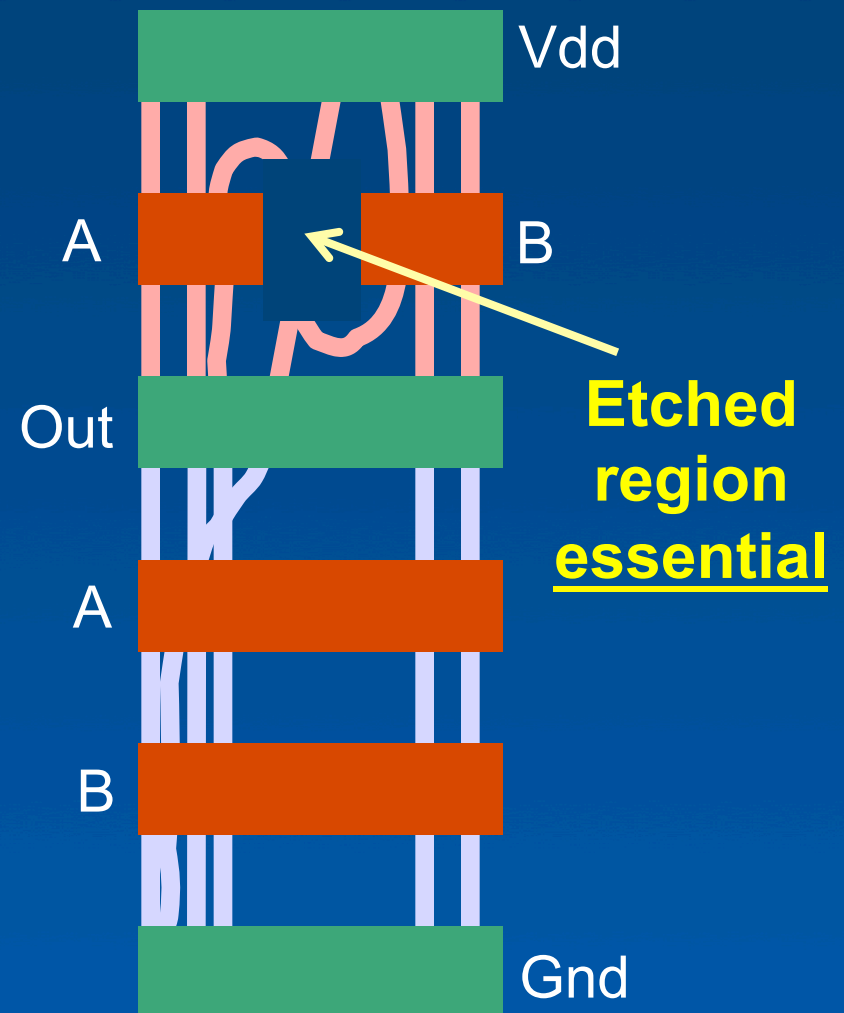
Mis-Positioned CNT-Immune NAND

1. Grow CNTs
2. Extended gate, contacts



Mis-Positioned CNT-Immune NAND

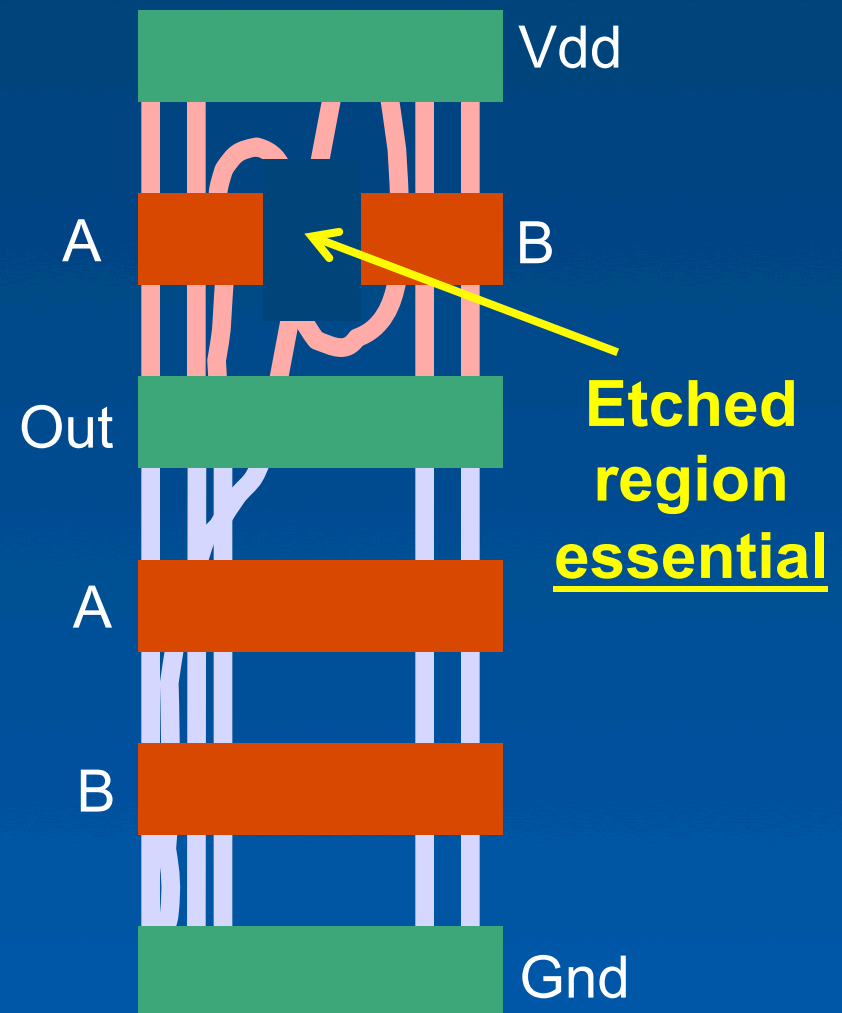
1. Grow CNTs
2. Extended gate, contacts
3. Etch gate & CNTs
4. Dope P & N regions



Mis-Positioned CNT-Immune NAND

1. Grow CNTs
2. Extended gate, contacts
3. Etch gate & CNTs
4. Dope P & N regions

- Arbitrary logic functions
 - Graph algorithms



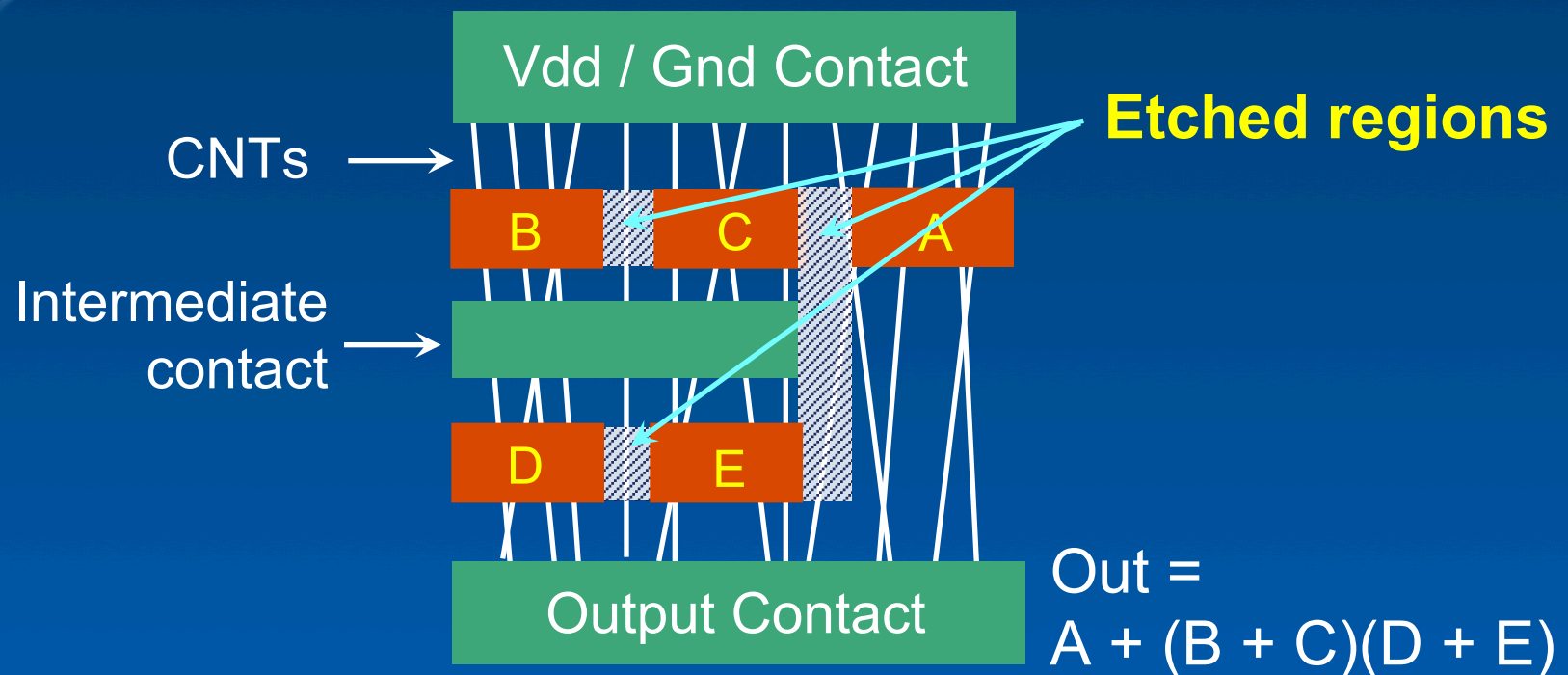
Most Importantly

- VLSI processing
 - No per-unit customization
- VLSI design
 - Immune CNT library

Algorithms

- Given: Layout
 - Determine
 - Mis-positioned CNT-immune ?
- Given: Logic function
 - Produce
 - Mis-positioned CNT-immune layout

Mis-Positioned CNT-Immune Layout



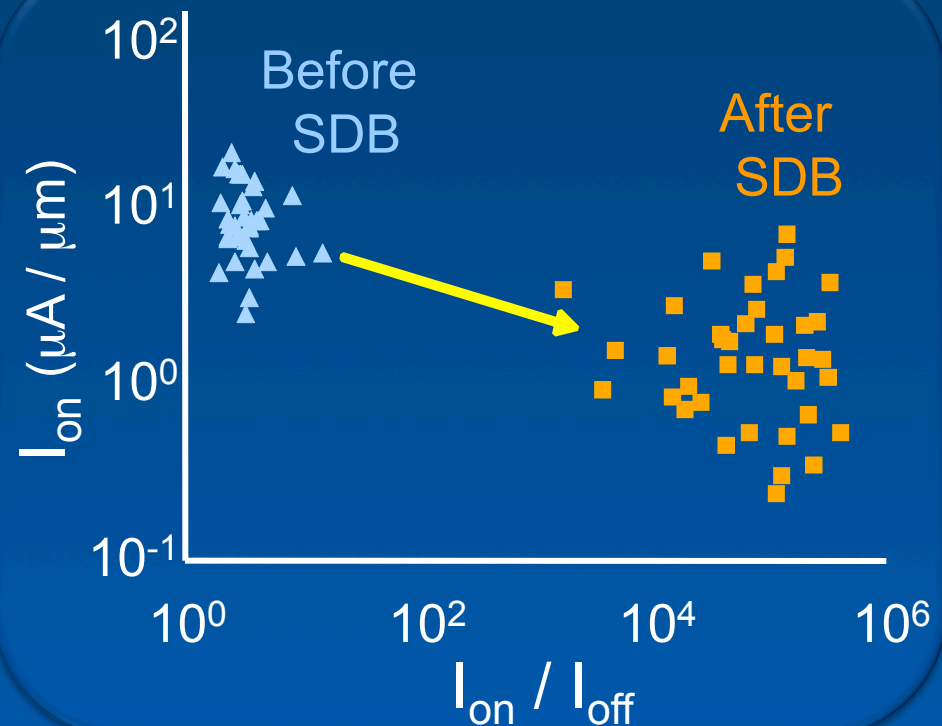
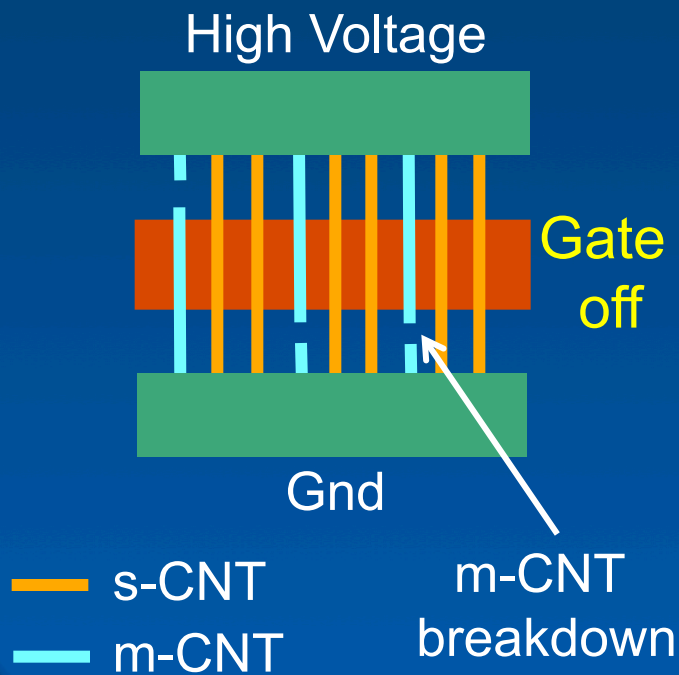
- **Many** mis-positioned CNTs
- Inexpensive

m-CNT Processing Options

- Grow 0% m-CNTs
 - Open challenge
- Remove m-CNTs after growth
 - 99.99%
- Early attempts inadequate
 - **S**ingle **D**evice electrical **B**reakdown

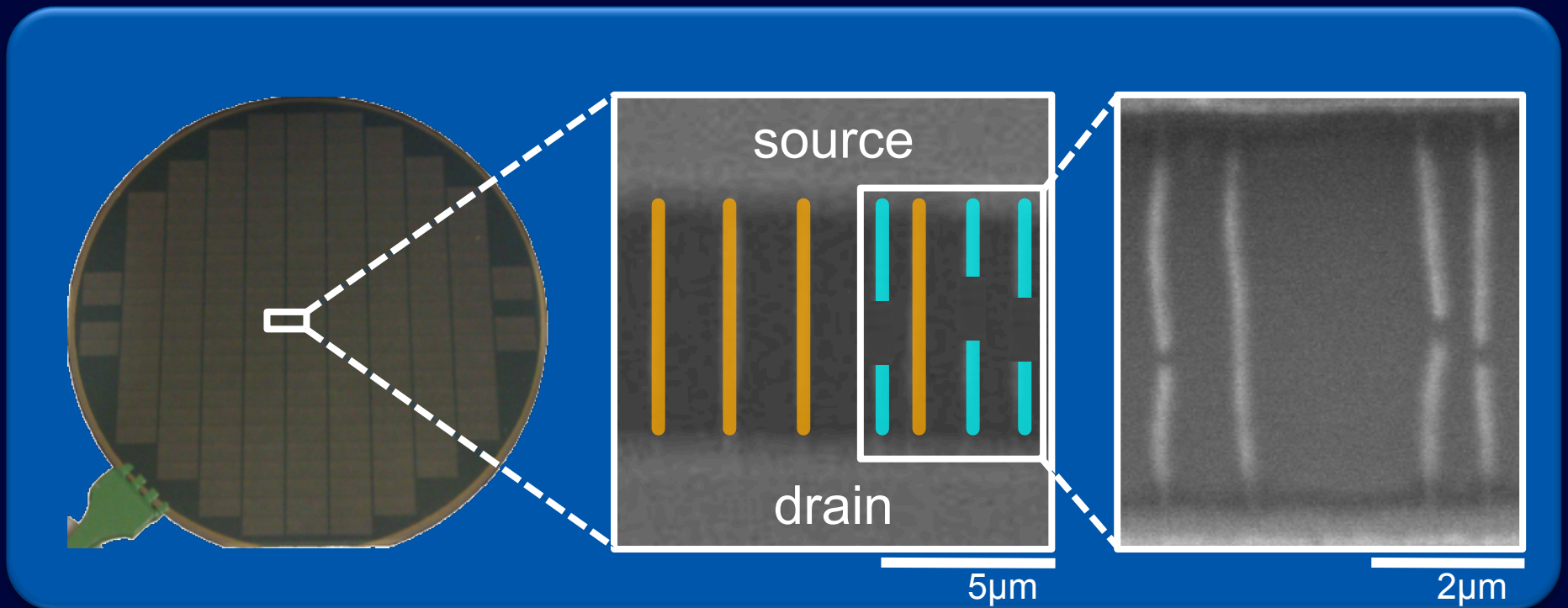
SDB: Useful Tool, BUT...

- Incorrect logic, VLSI scalability



VLSI Metallic CNT Removal

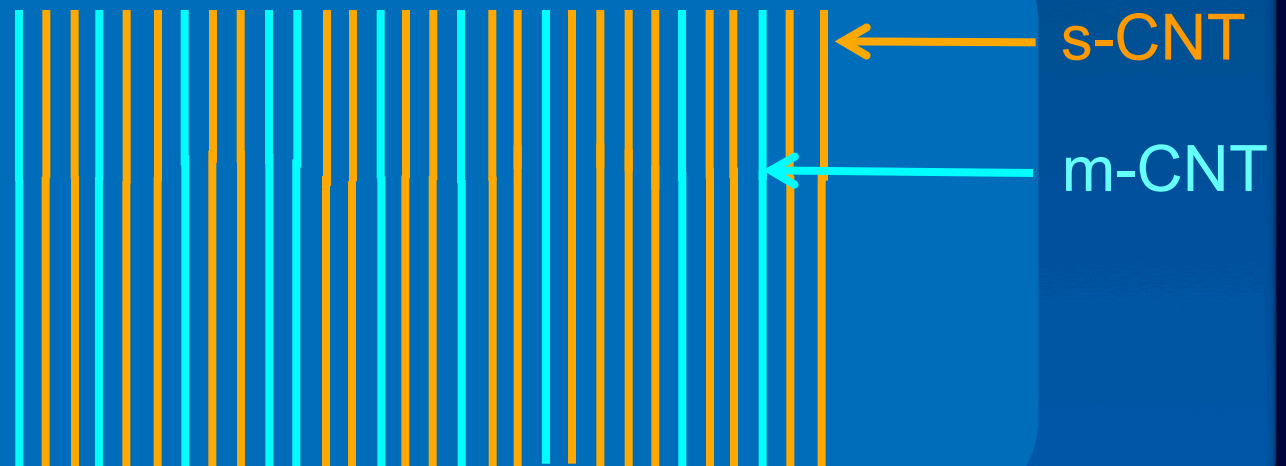
- Universally effective
- VLSI processing & design
- Sub-20nm scalable



VMR Example

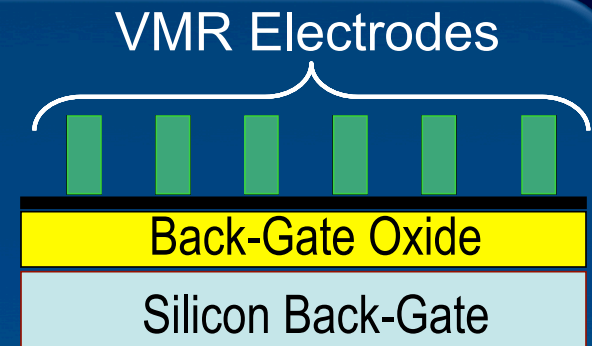
1. Grow and transfer CNTs

Back-Gate Oxide
Silicon Back-Gate

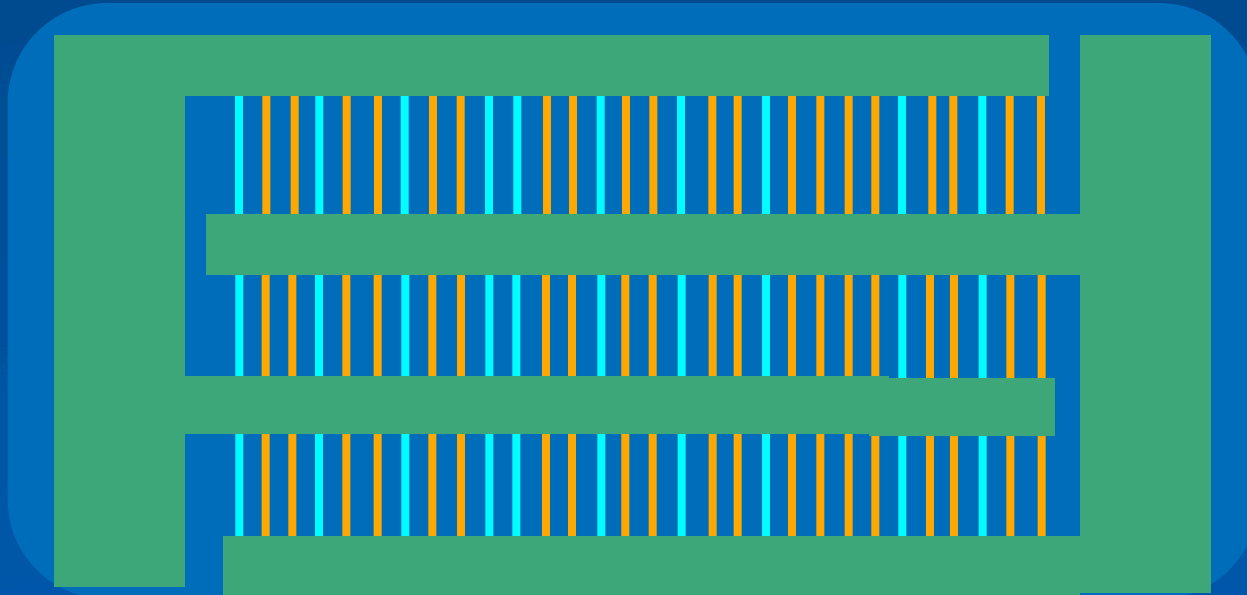


VMR Example

1. Grow and transfer CNTs
2. Fabricate VMR electrodes

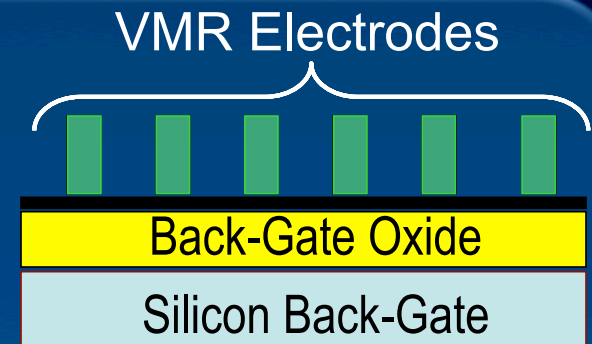


VMR electrodes

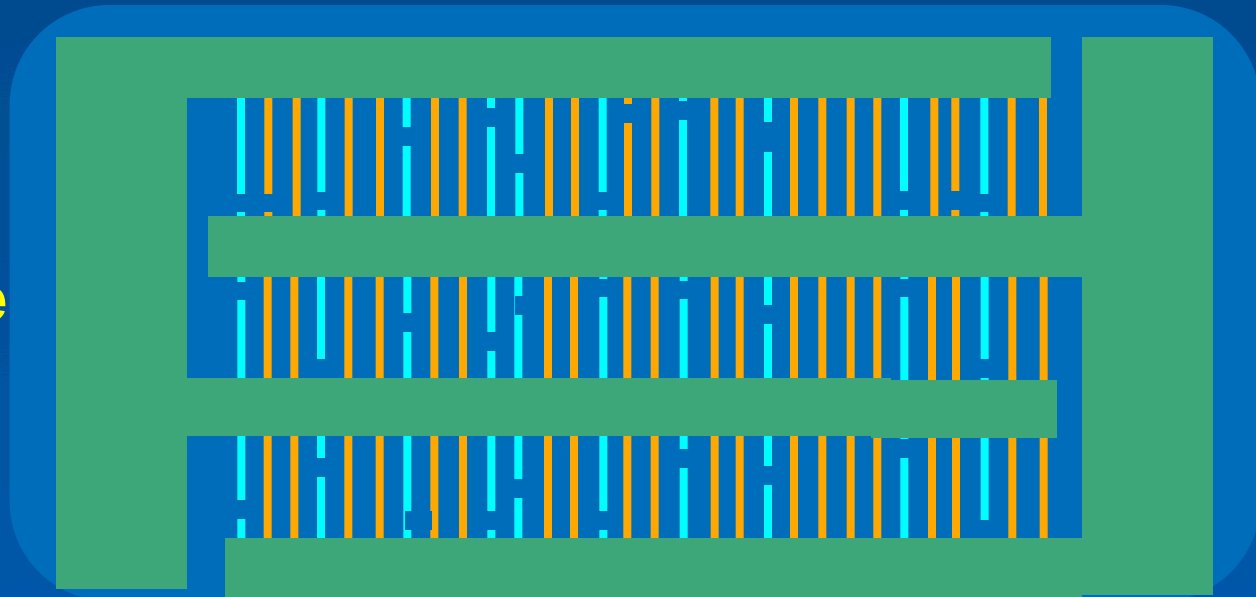


VMR Example

1. Grow and transfer CNTs
2. Fabricate VMR electrodes
3. Electrical breakdown (back-gate)



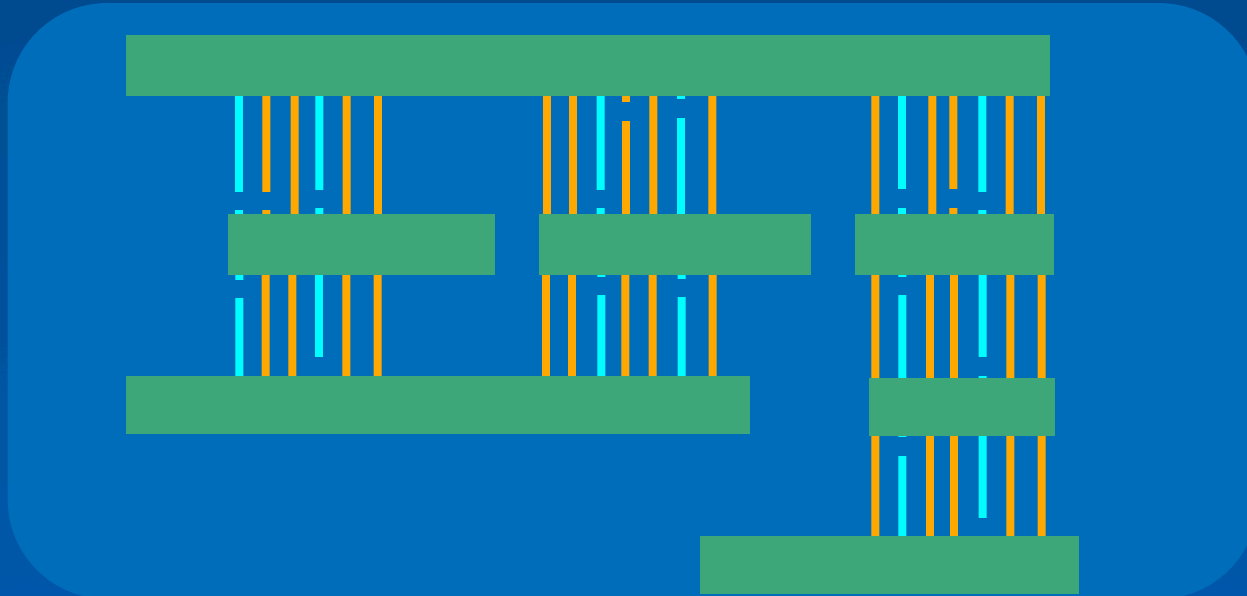
**High
voltage**



VMR Example

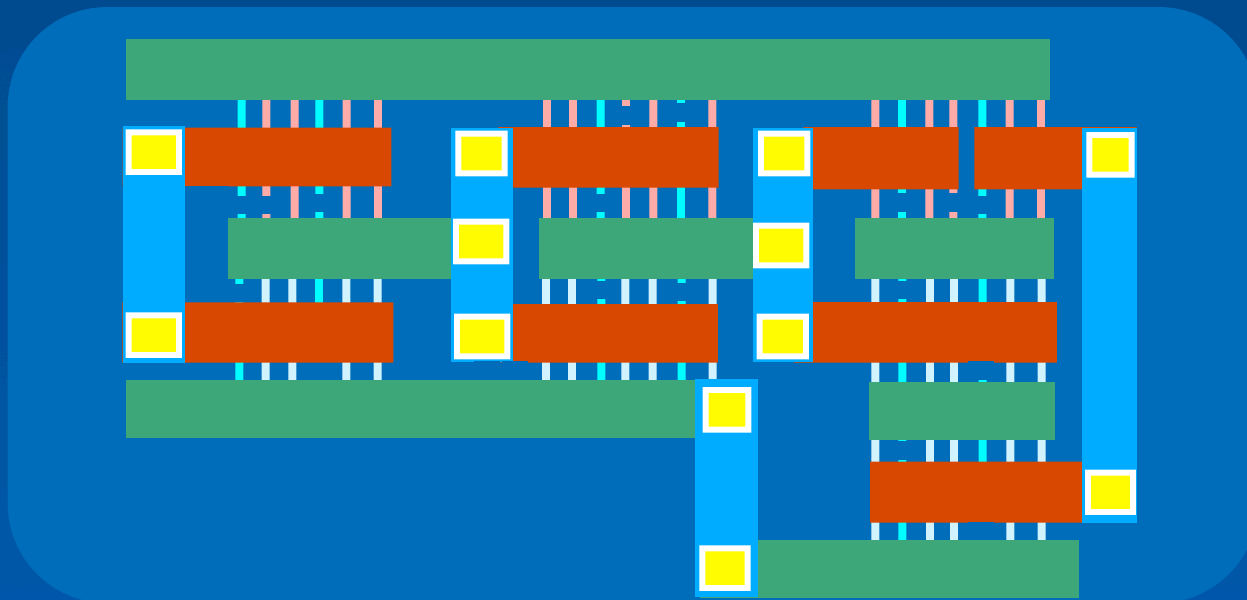
1. Grow and transfer CNTs
2. Fabricate VMR electrodes
3. Electrical breakdown (back-gate)
4. Etch CNTs & unneeded VMR electrodes: predefined

CNFET contacts intact

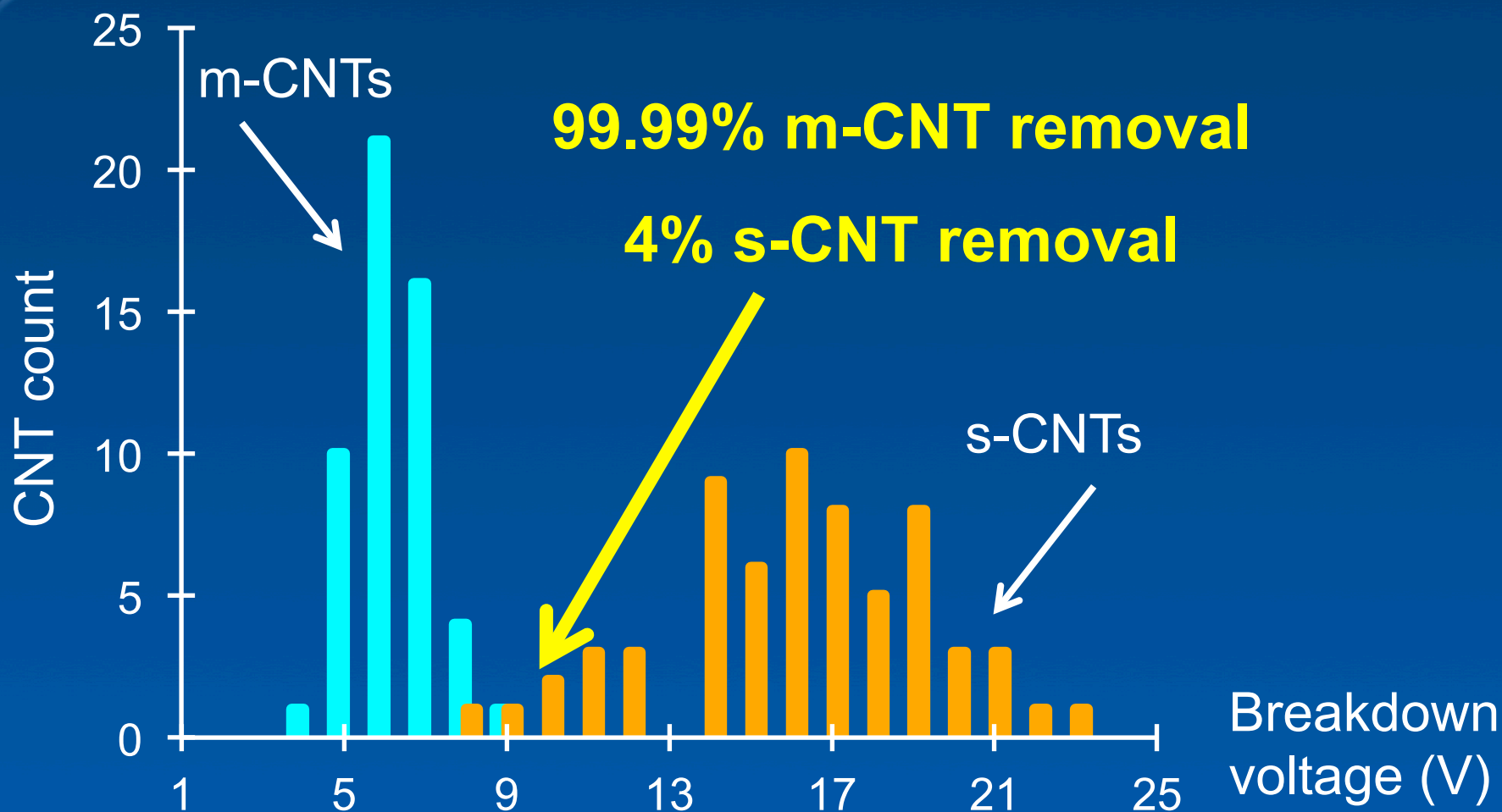


VMR Example

1. Grow and transfer CNTs
2. Fabricate VMR electrodes
3. Electrical breakdown (back-gate)
4. Etch CNTs & unneeded VMR electrodes: predefined
5. Top-gates (**mis-positioned CNT-immune layout**), doping, wires



VMR Selectivity



First Sub-system: ISSCC Demo

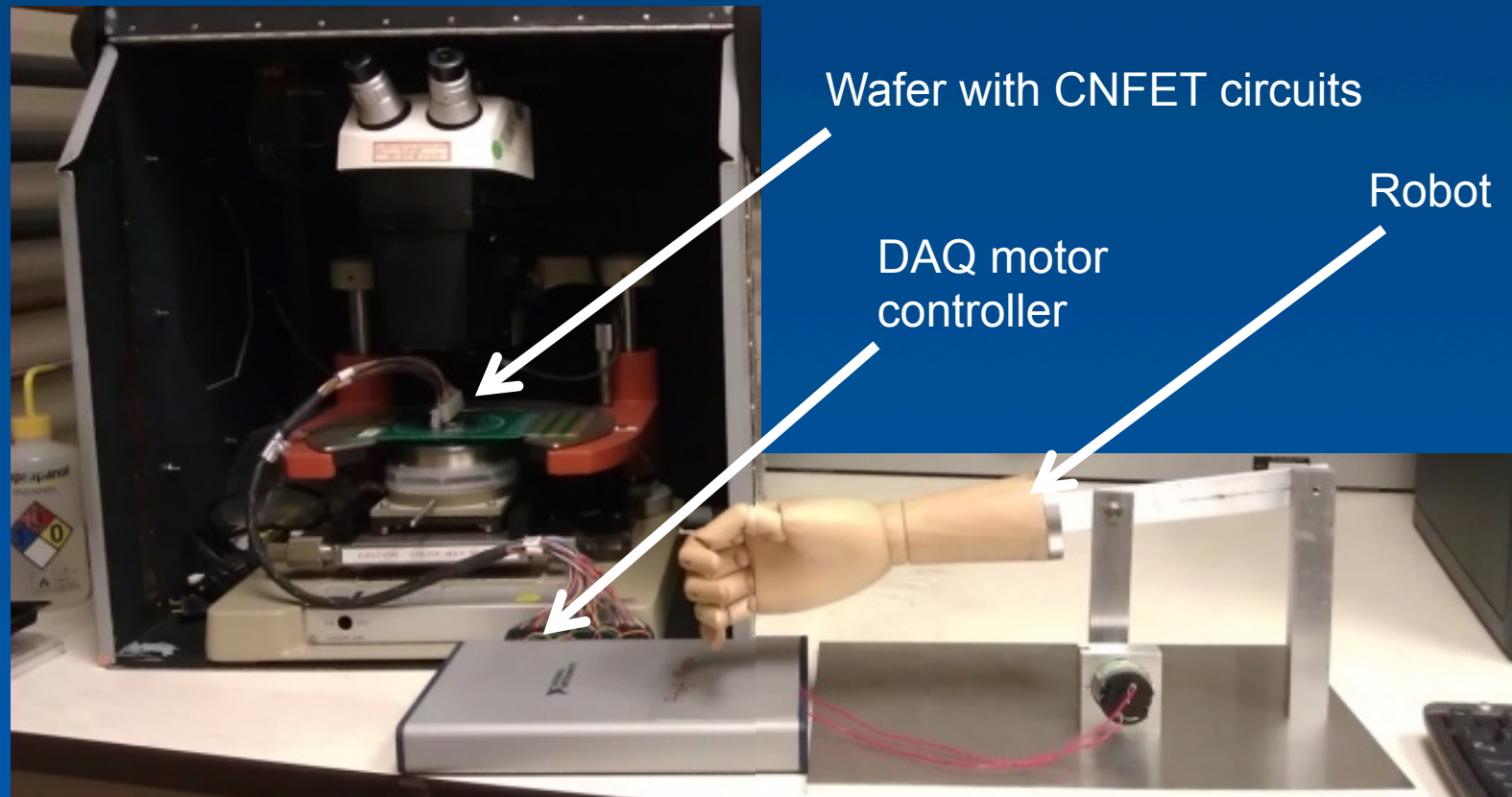
ISSCC Jack Raper Outstanding Technology Directions Paper



First Sub-system: ISSCC Demo

ISSCC Jack Raper Outstanding Technology Directions Paper

Sacha: CNT Controlled Hand-shaking Robot

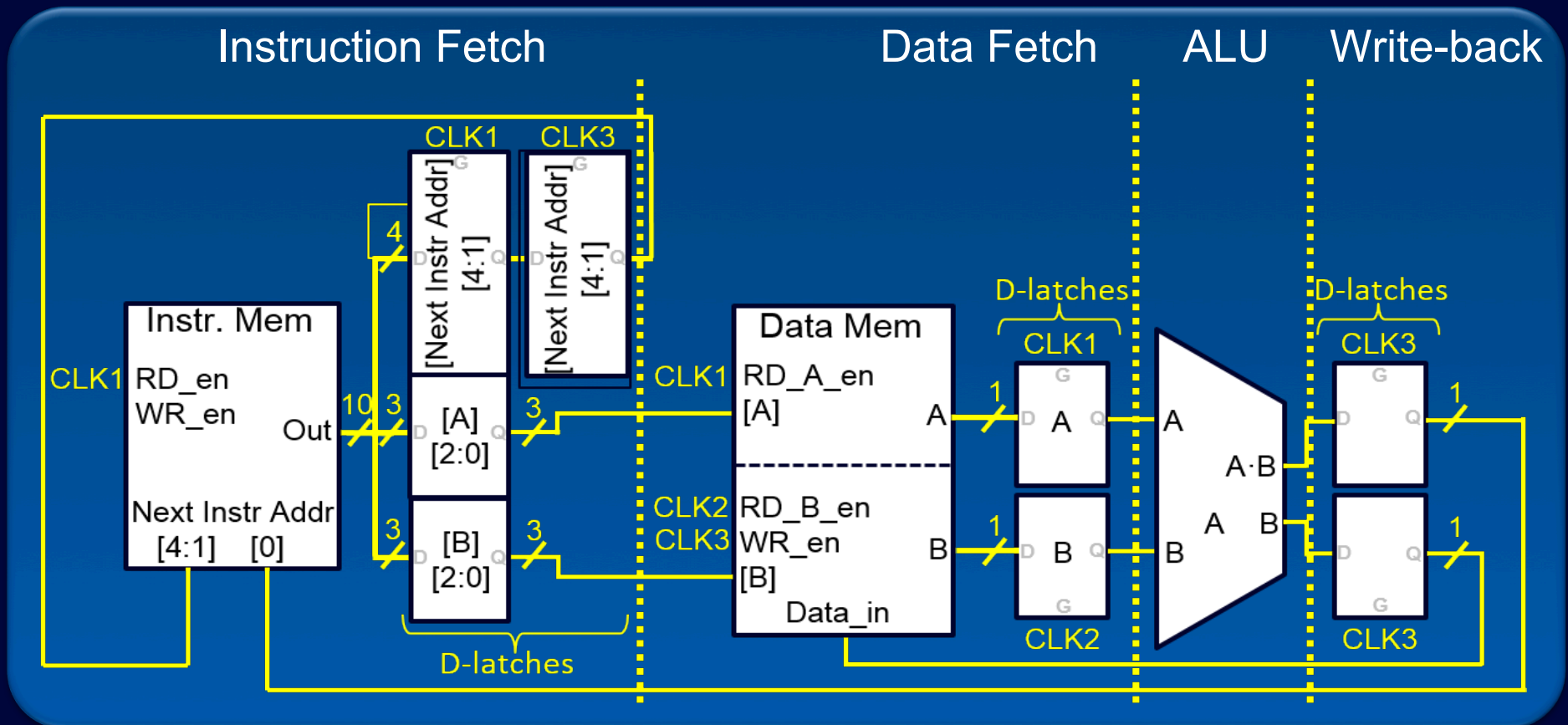


CNT Computer



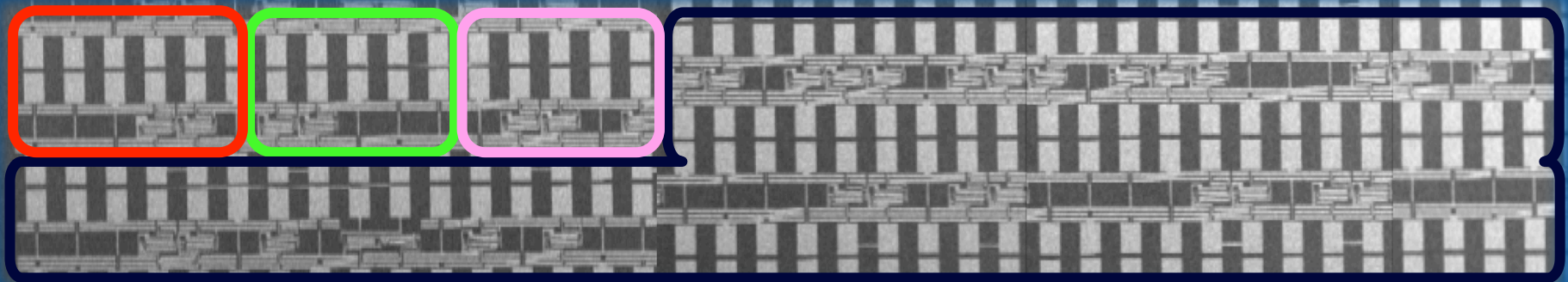
CNT Computer

- Turing-complete processor: entirely CNFETs



CNT Computer

■ Instruction Fetch ■ Data Fetch ■ Arithmetic block ■ Write-back

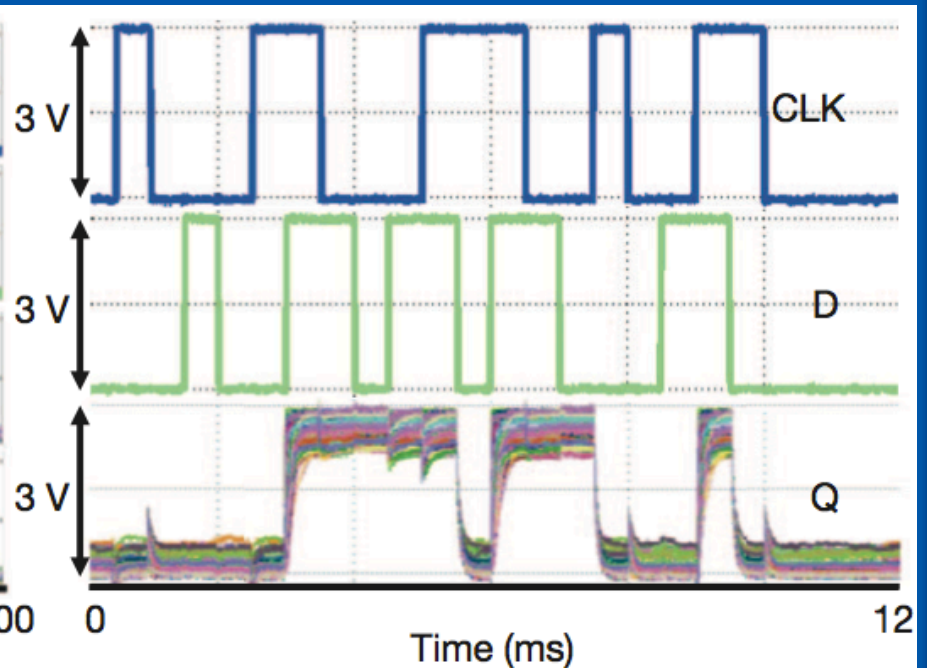
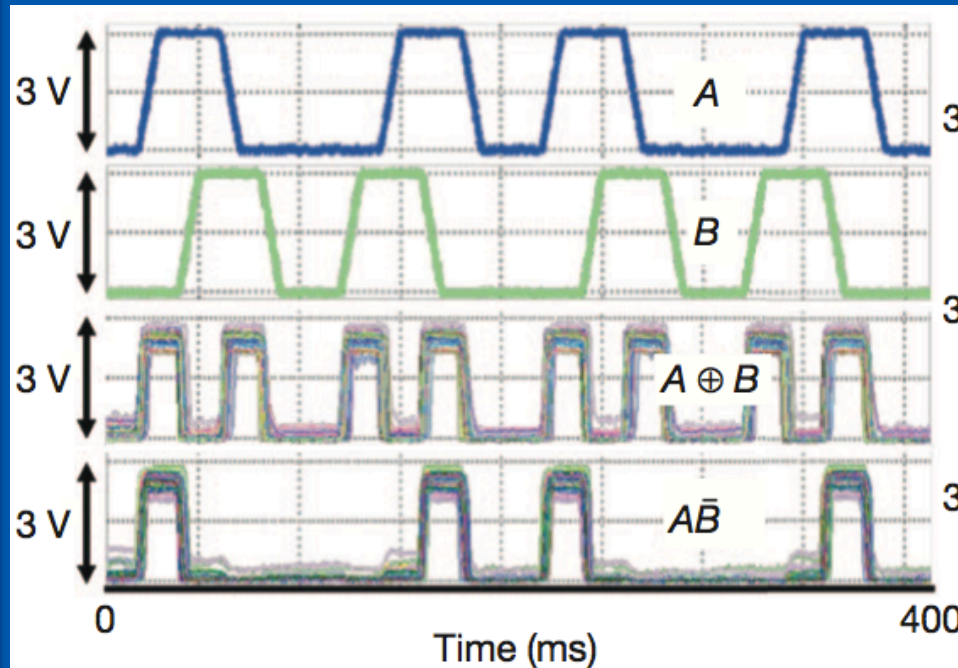


- 178 CNFETs
 - ~ 30K CNTs
- 7-15 cascaded logic stages

Reproducible Results

80 ALUs

200 D-Latches



~ 1,600 CNFETs

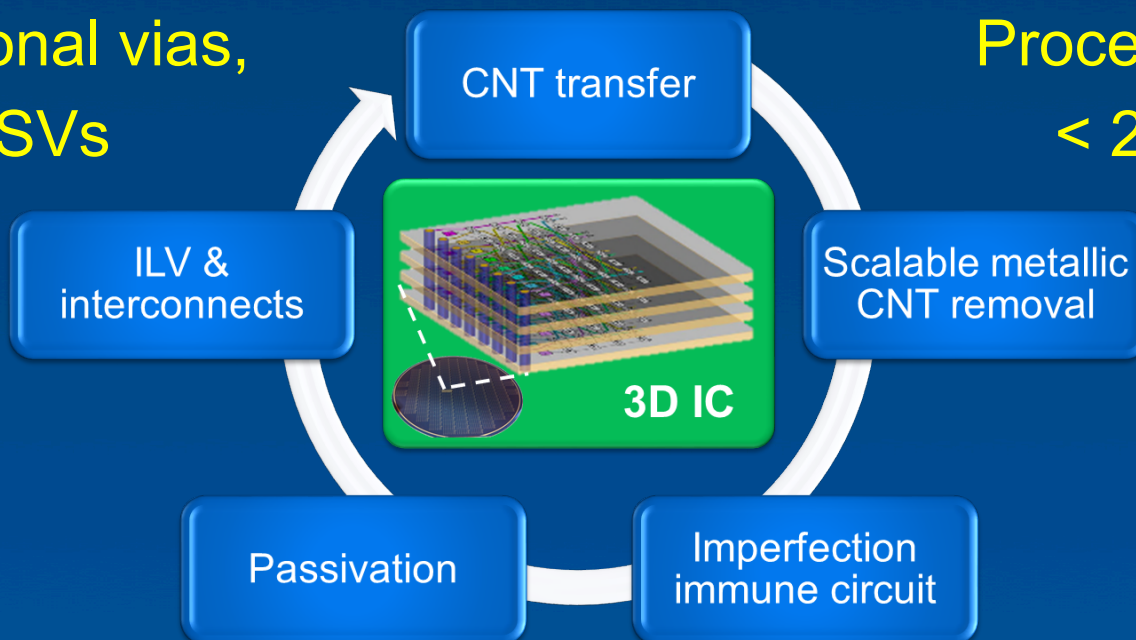
~ 1,800 CNFETs

Waveforms overlaid

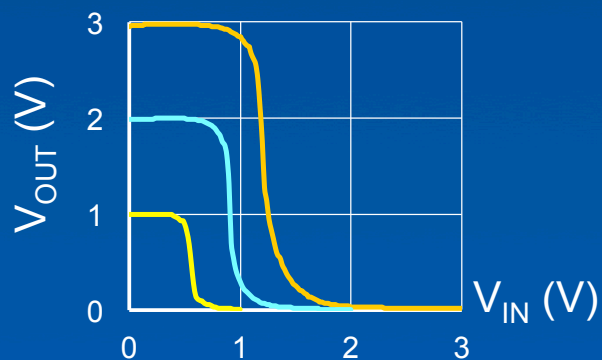
First CNT Monolithic 3D IC

Conventional vias,
no TSVs

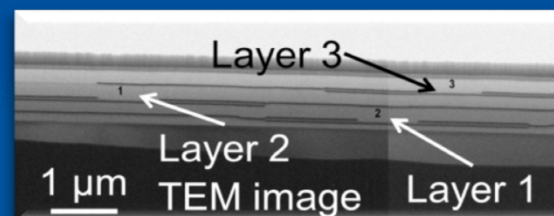
Process temp.
< 250 °C



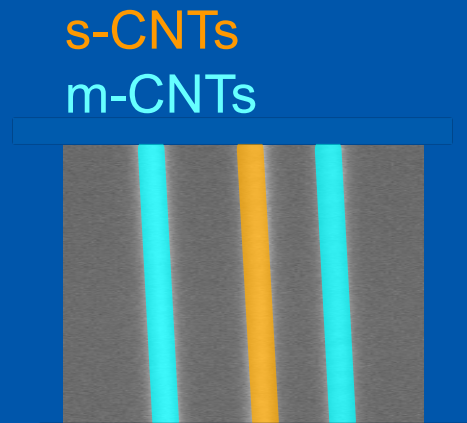
Inter-layer digital circuits



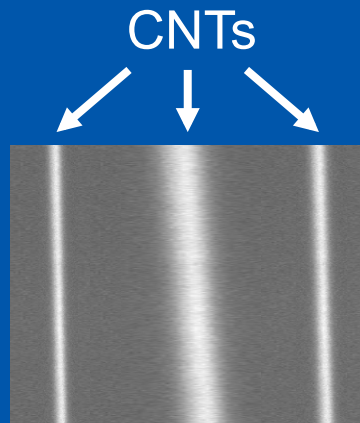
3-Layer integration



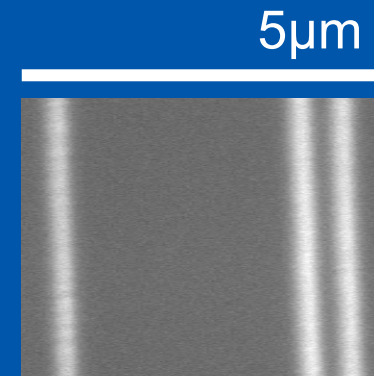
CNT Variations



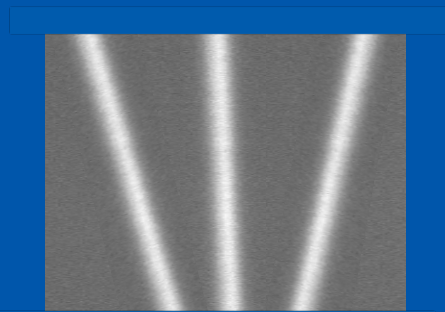
CNT type



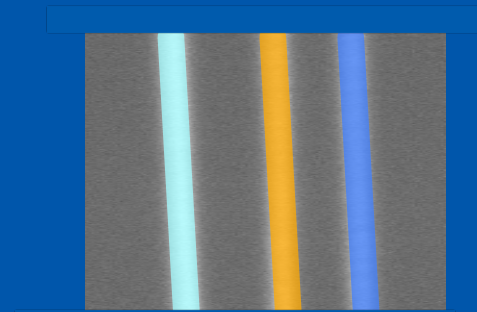
CNT diameter



CNT density



CNT alignment



CNT doping

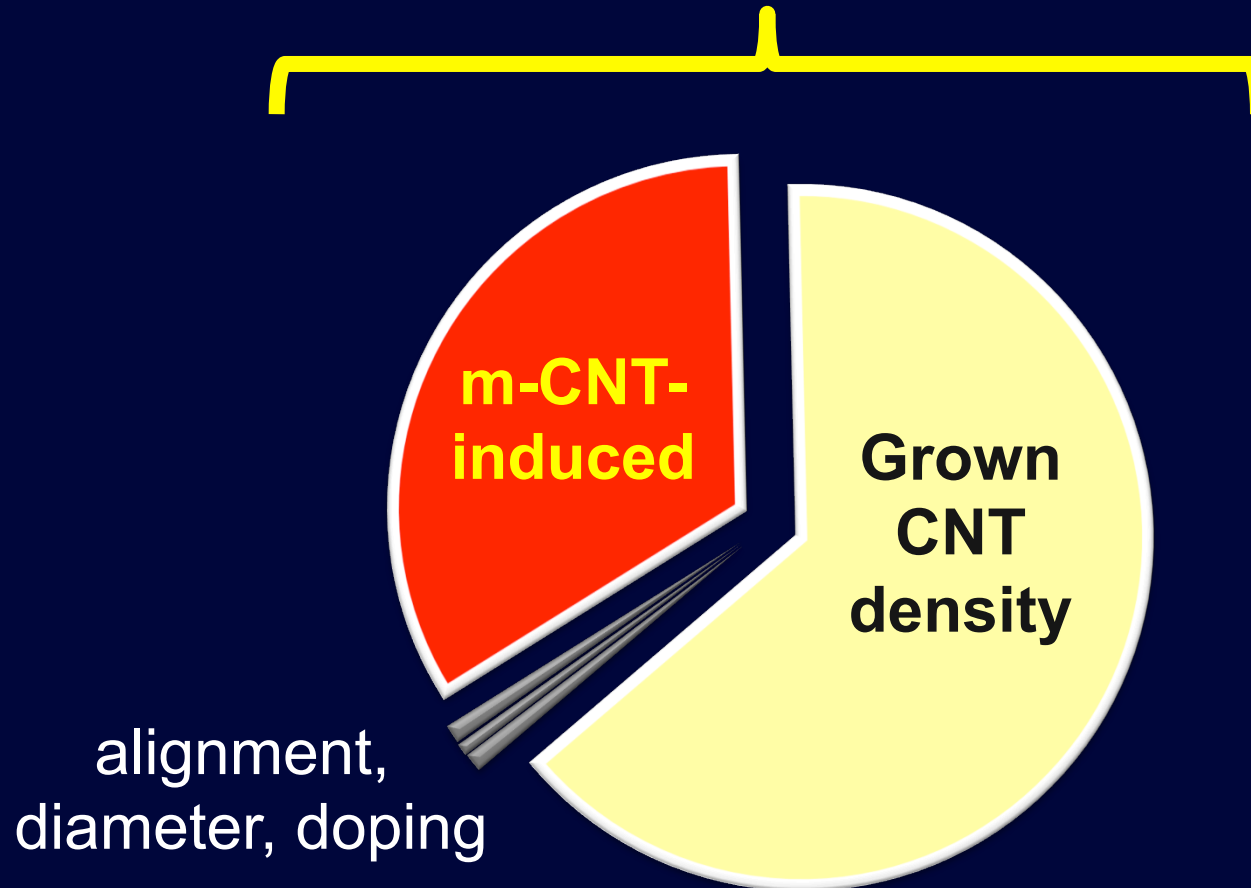
+ t_{ox}

+ V_t

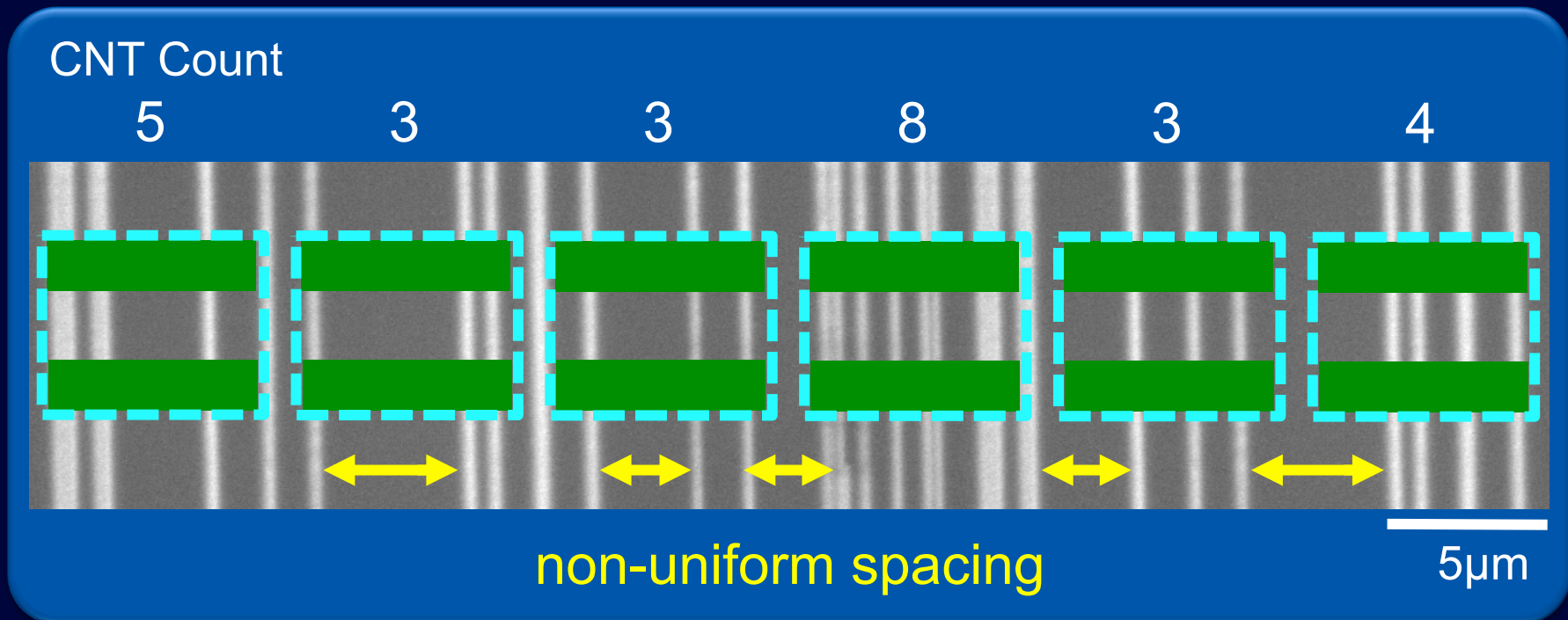
+ $L_{channel}$

CNFET I_{ON} Variations: System-Level

CNT count variations



Grown CNT Density Variations



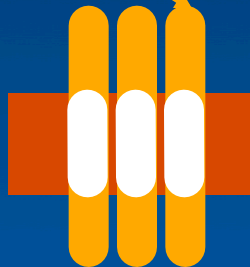
- Index of Dispersion for Count

$$IDC = \frac{\sigma_{spacing}^2}{\mu_{spacing}^2}$$

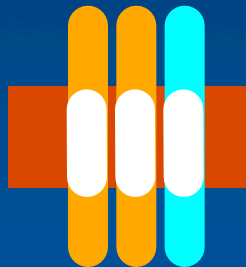
Probabilistic CNT Growth

- $\Pr(\text{m-CNT}) = p_m$
- $\Pr(\text{s-CNT}) = 1 - p_m$
- i.i.d. (experimentally verified)

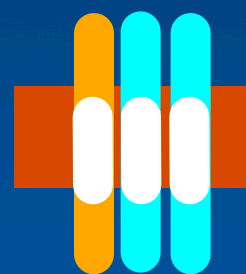
s-CNT



97.03%

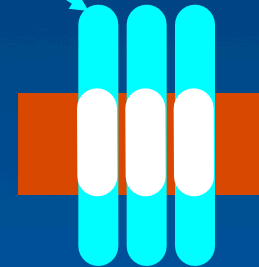


2.94%



0.029%

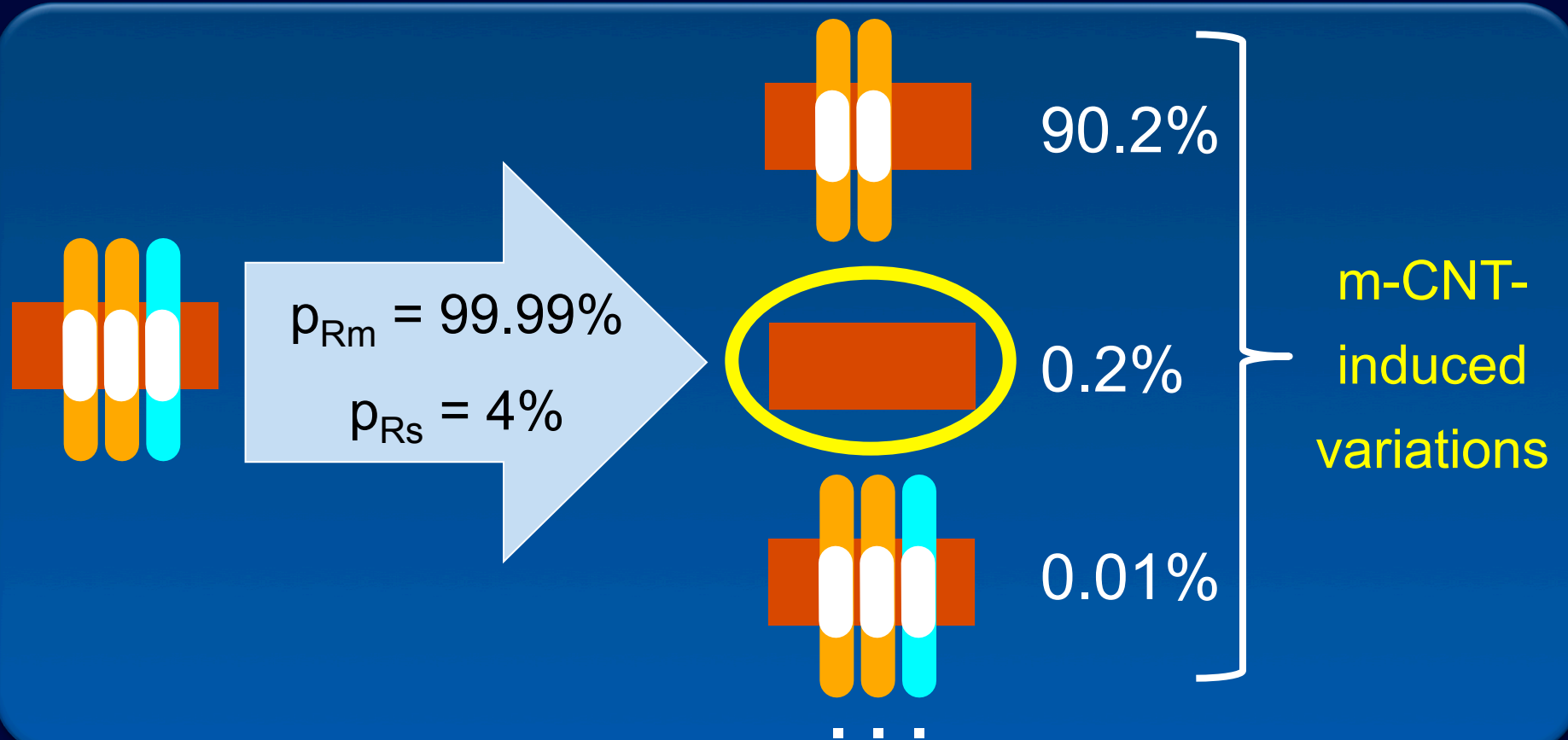
m-CNT



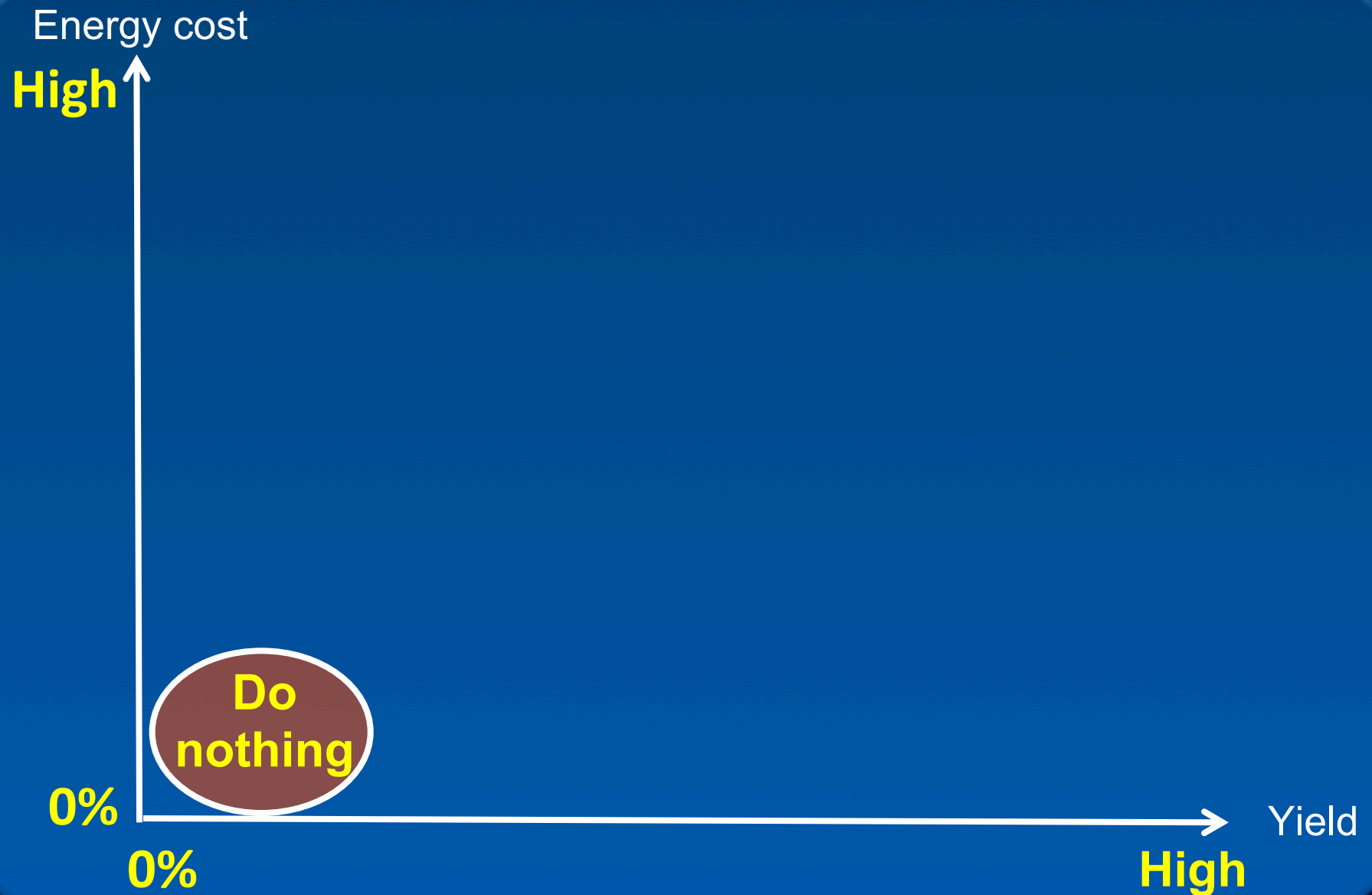
0.001%

Probabilistic CNT Removal

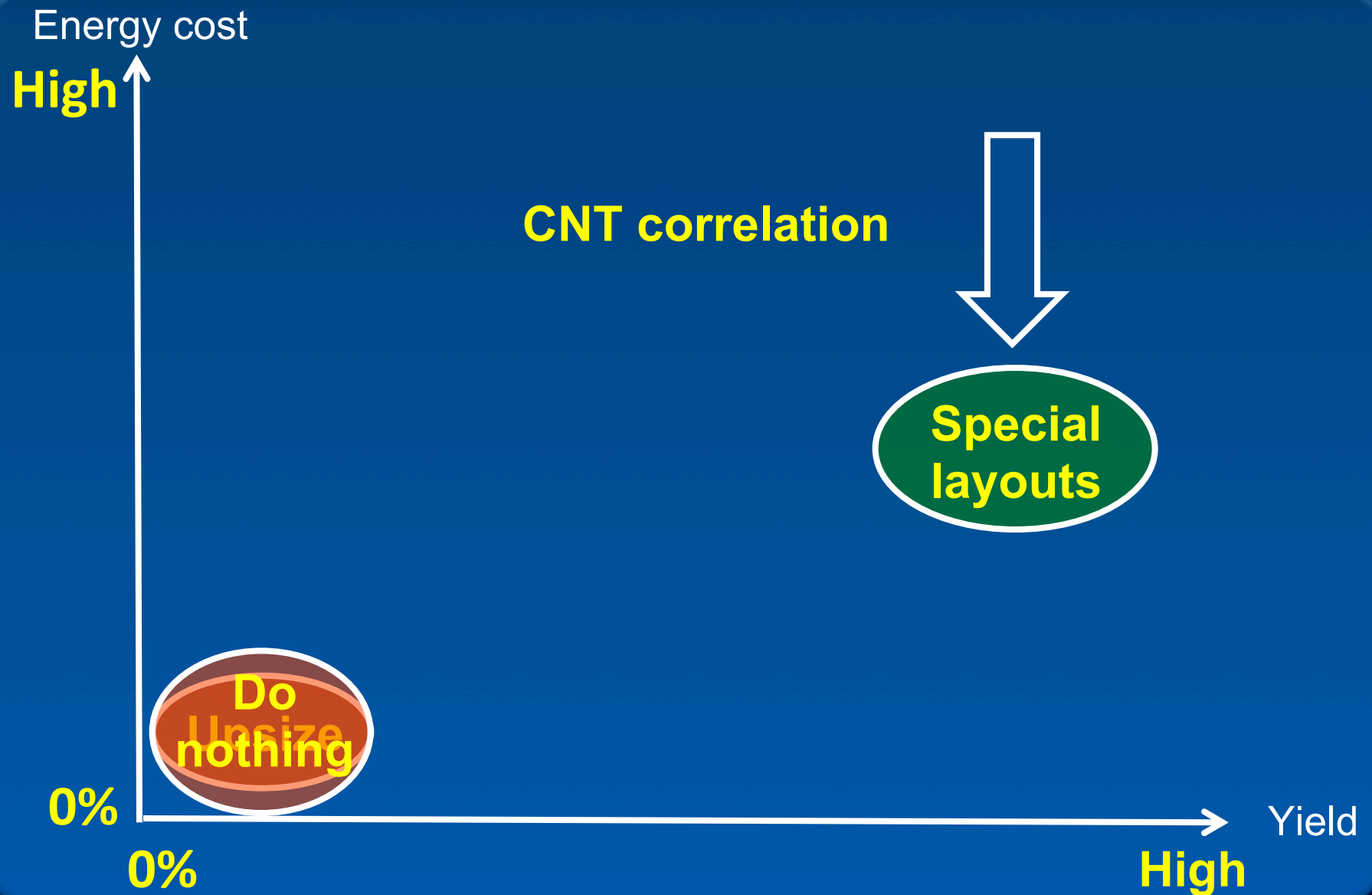
- $\Pr(\text{Removed} \mid \text{m-CNT}) = \rho_{Rm}$
- $\Pr(\text{Removed} \mid \text{s-CNT}) = \rho_{Rs}$



Overcoming CNT Variations



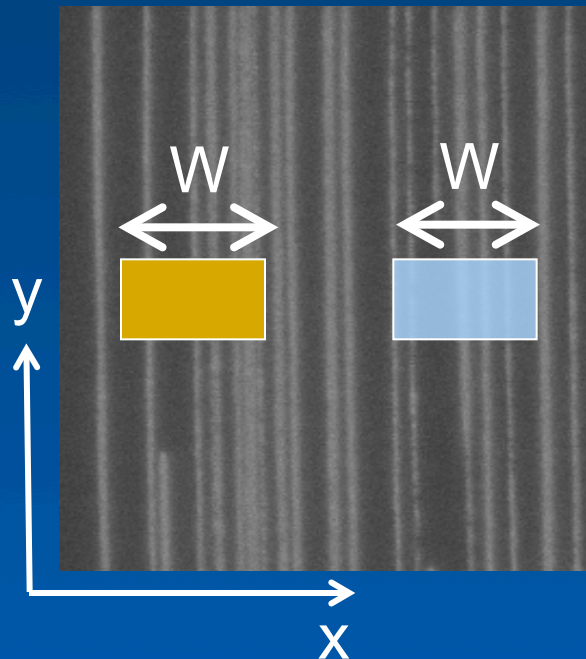
Overcoming CNT Variations



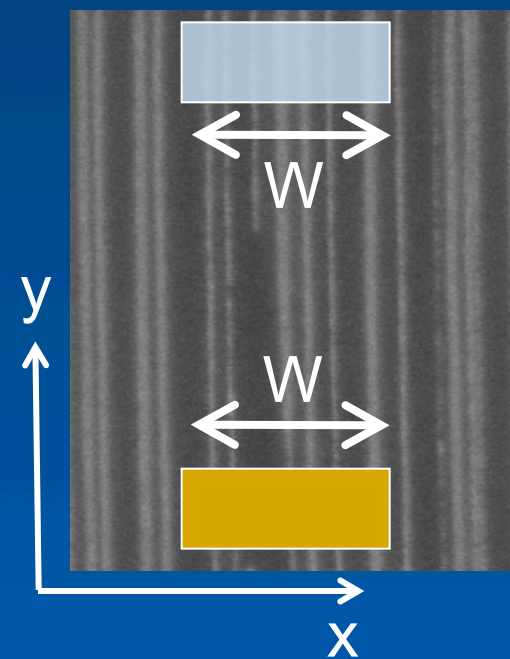
CNFET Correlation

- Unique CNT feature

Uncorrelated



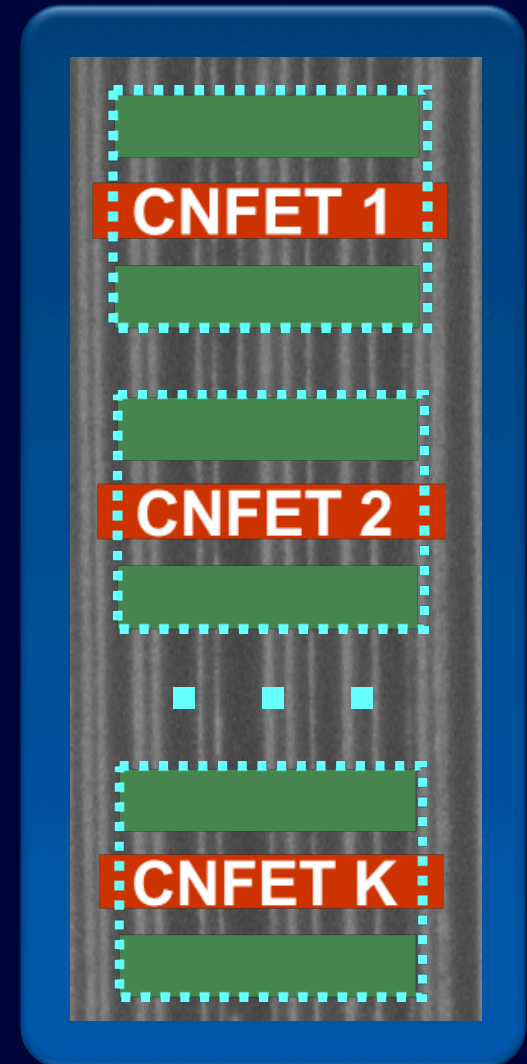
Correlated



“Engineer” CNFET Correlation

- **Aligned-active layout**

$$\begin{aligned} \text{Pr (No failure)} = & \\ & \text{Pr (No CNFET 1 failure} \\ & \quad \text{AND} \\ & \quad \text{No CNFET 2 failure} \\ & \quad \text{AND ... AND} \\ & \quad \text{No CNFET K failure)} \end{aligned}$$



“Engineer” CNFET Correlation

- Aligned-active layout

BIG BENEFIT

$\Pr(\text{No failure}) =$

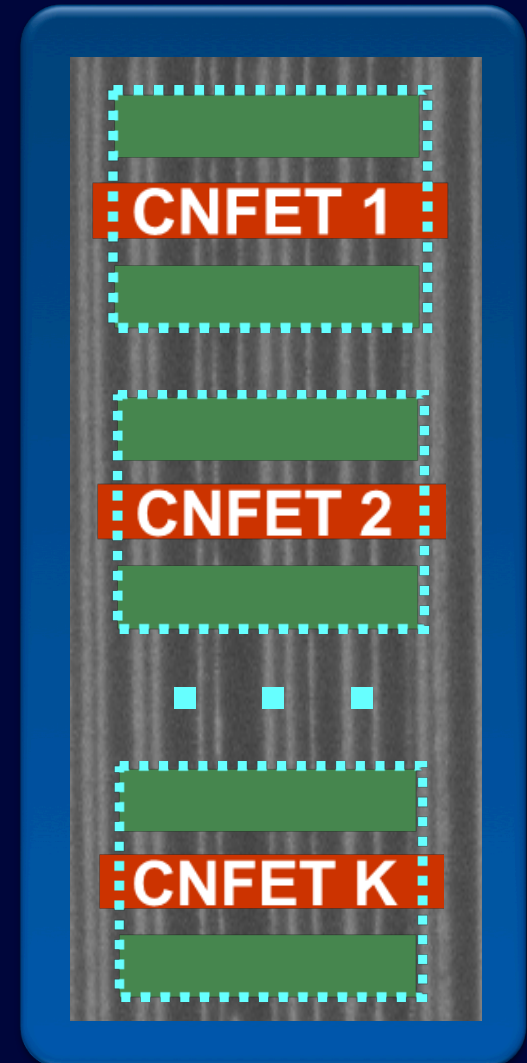
$\Pr(\text{No CNFET 1 failure})$

$\approx$

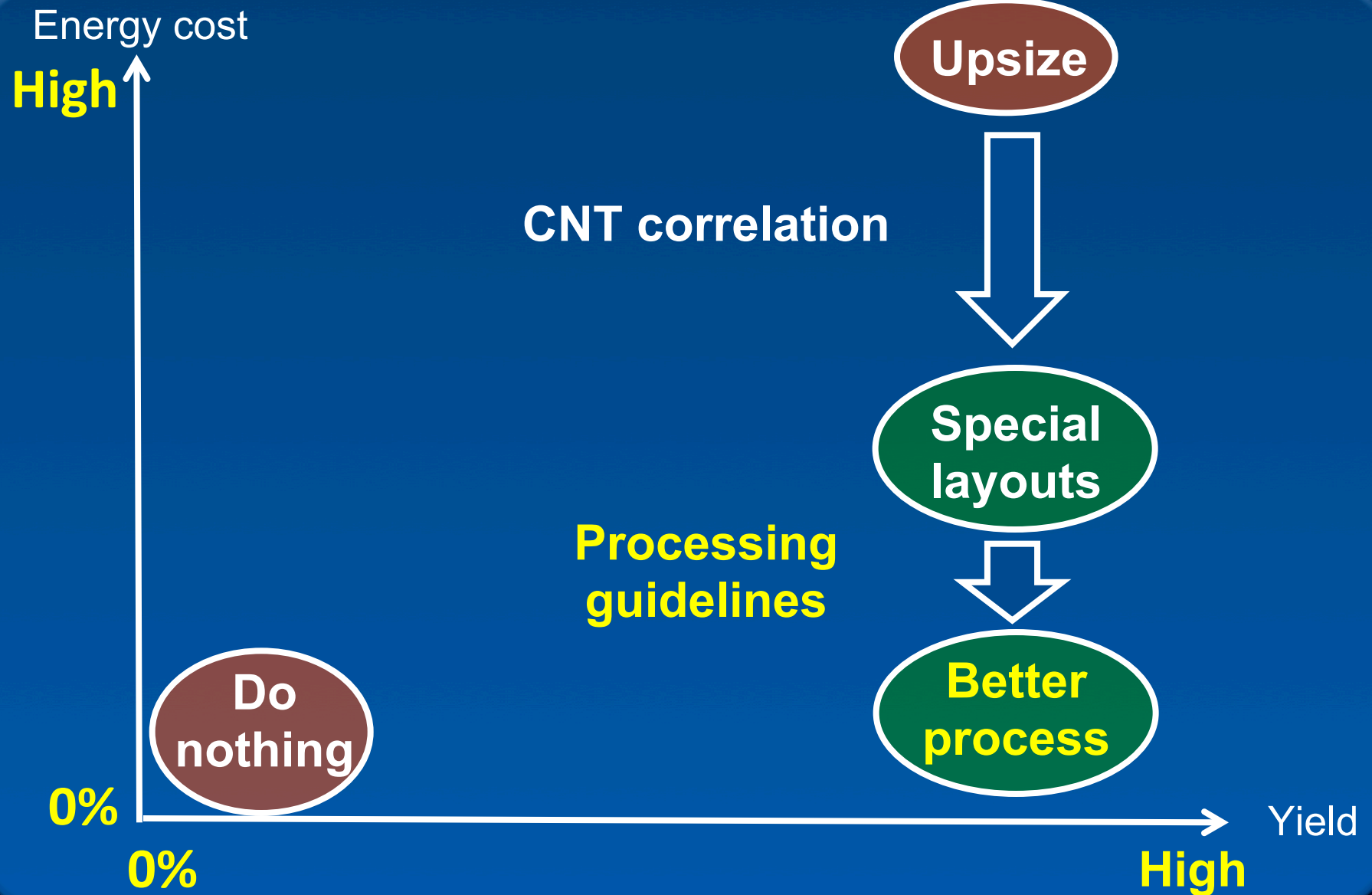
$\Pr(\text{No CNFET 2 failure})$

$\approx \dots \approx$

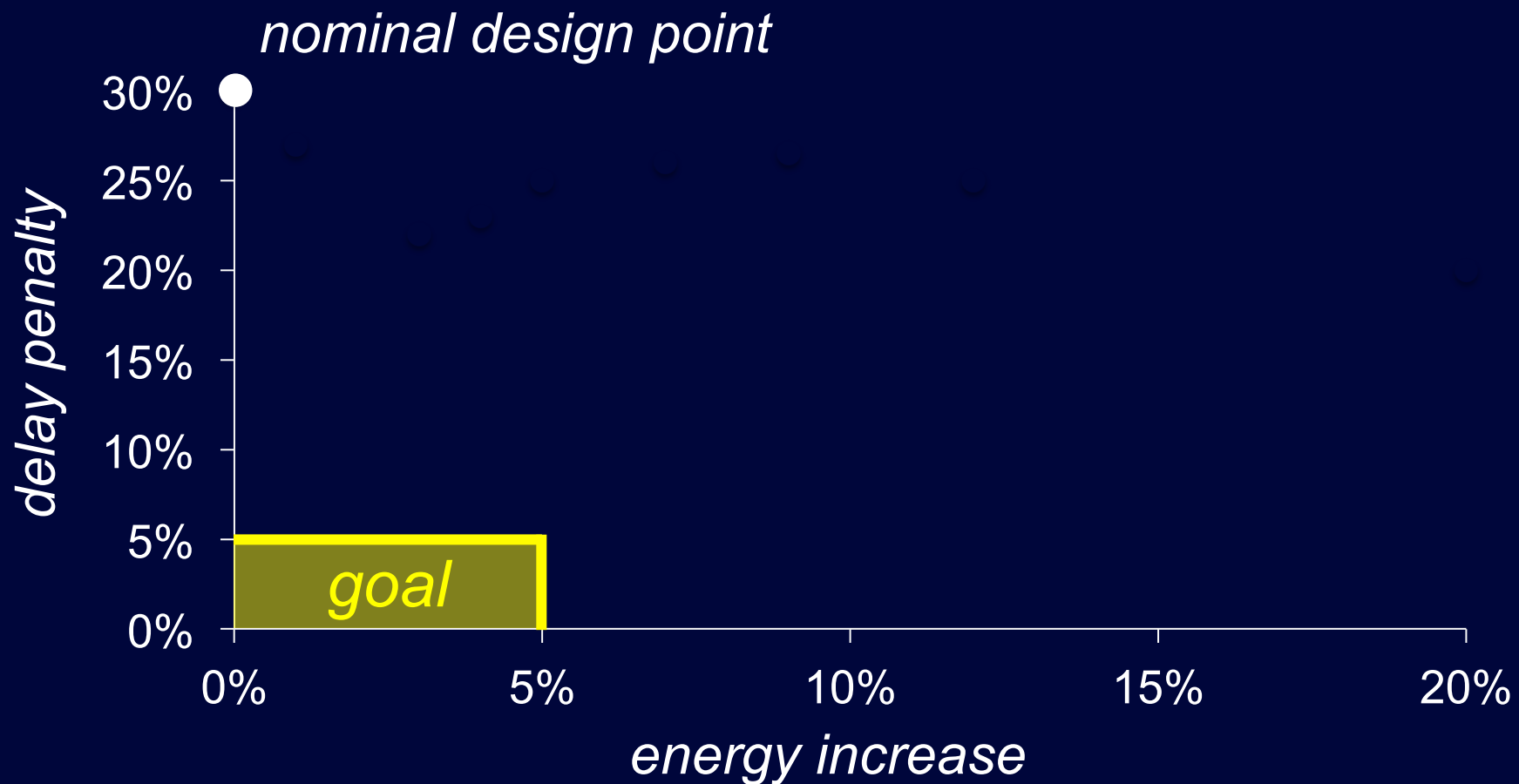
$\Pr(\text{No CNFET K failure})$



Overcoming CNT Variations

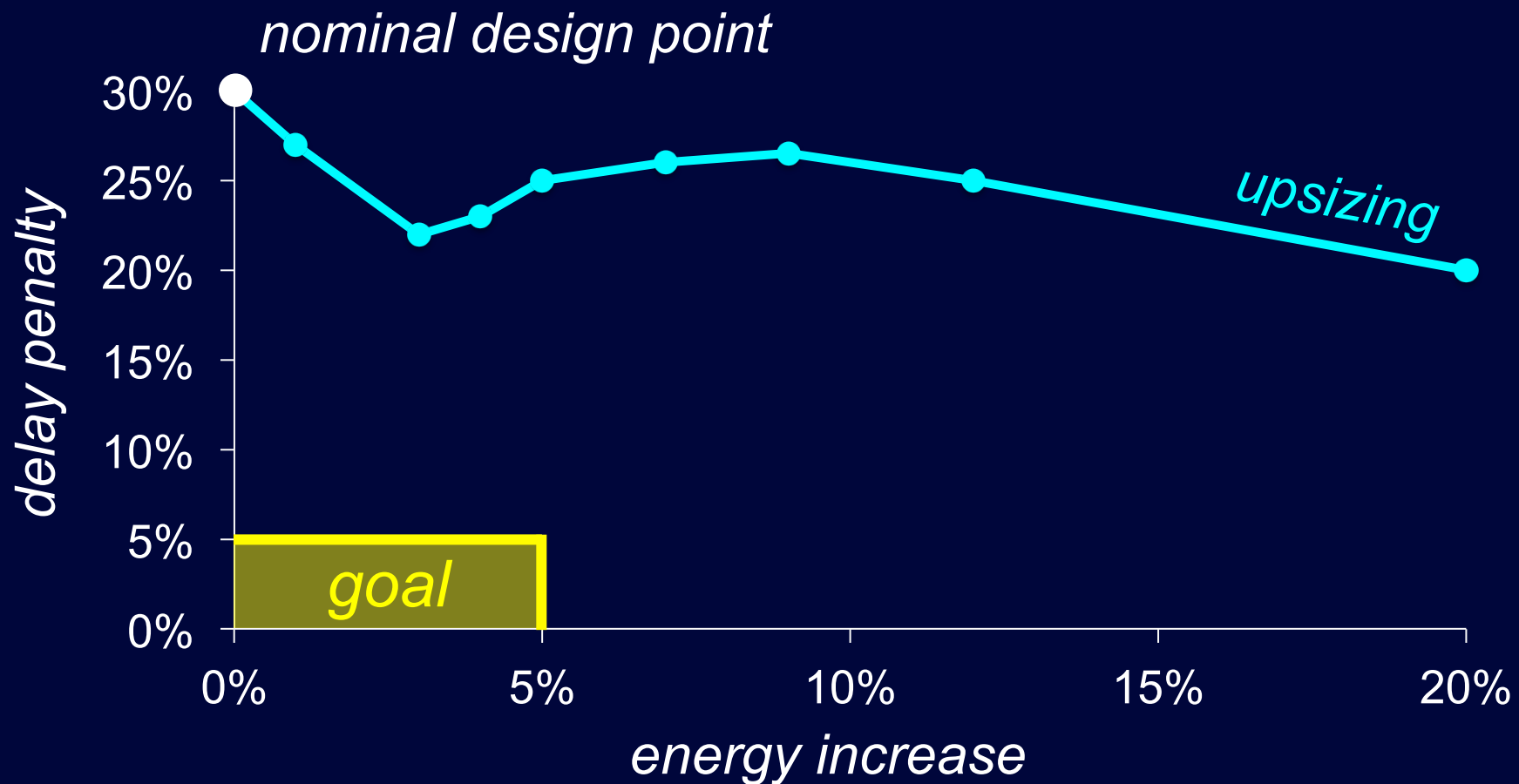


Delay vs. Energy



example: 16nm "Isu", $IDC = 0.5$, $p_m = 10\%$, $p_{Rs} = 5\%$, $p_{Rm} = 99.99\%$

Upsize: High Energy Cost



Improve p_m : Diminishing Returns

Krupke, R., *et al.*, *Science*, 2003.

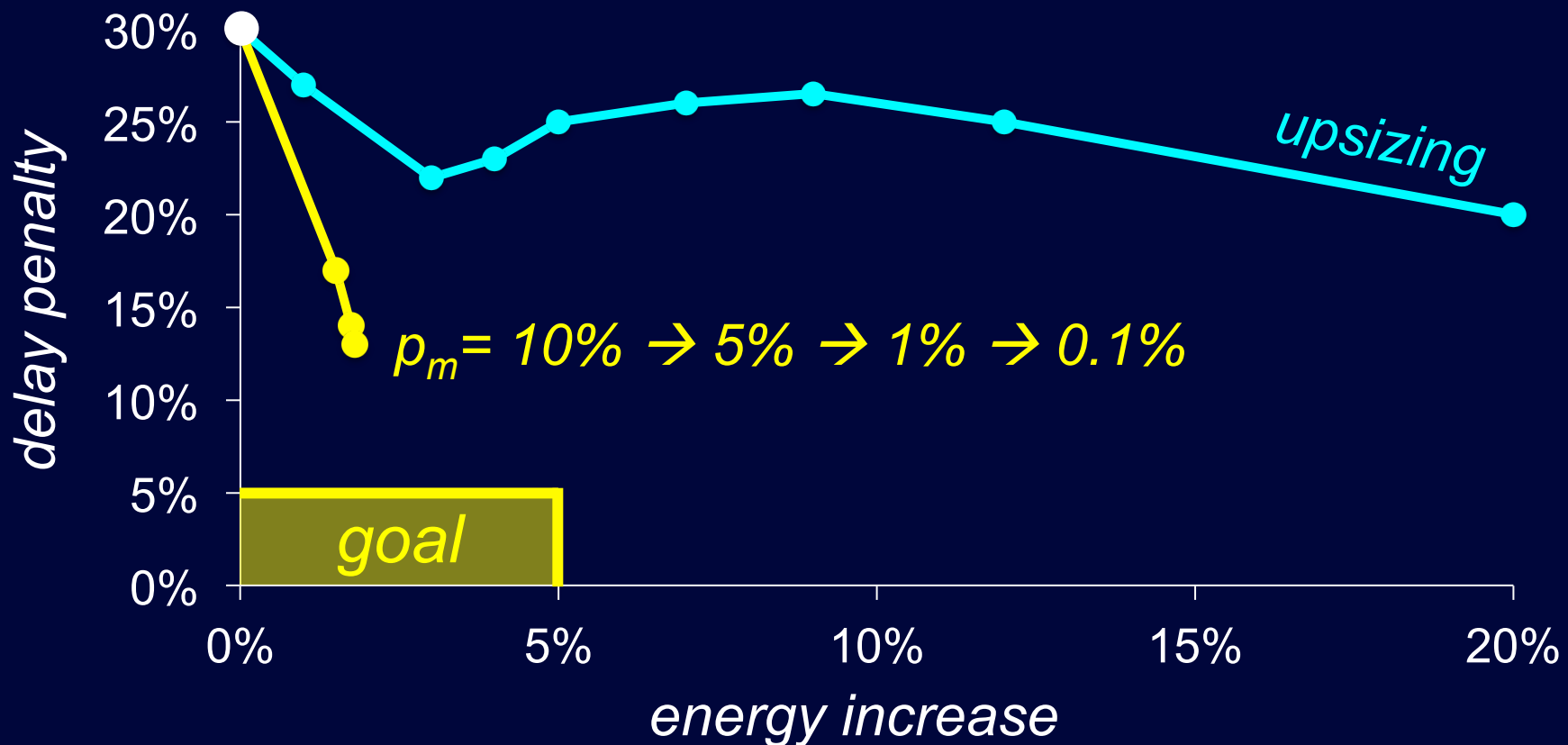
Arnold, M. S., *et al.*, *Nature Nanotech.*, 2006.

Hersam, M. C., *Nature Nanotech.*, 2008.

Tanaka, T., *et al.*, *Nano Letters*, 2009.

Ghosh, S., *et al.*, *Nature Nanotech.*, 2010.

Li, S., *et al.*, *ACS Nano*, 2012.



Processing & Design Co-Optimization



Parameters

$\rho_m, \rho_{Rm}, \rho_{Rs}$

IDC

Sizing

CNT correlation



Search

Optimized Guidelines



Energy



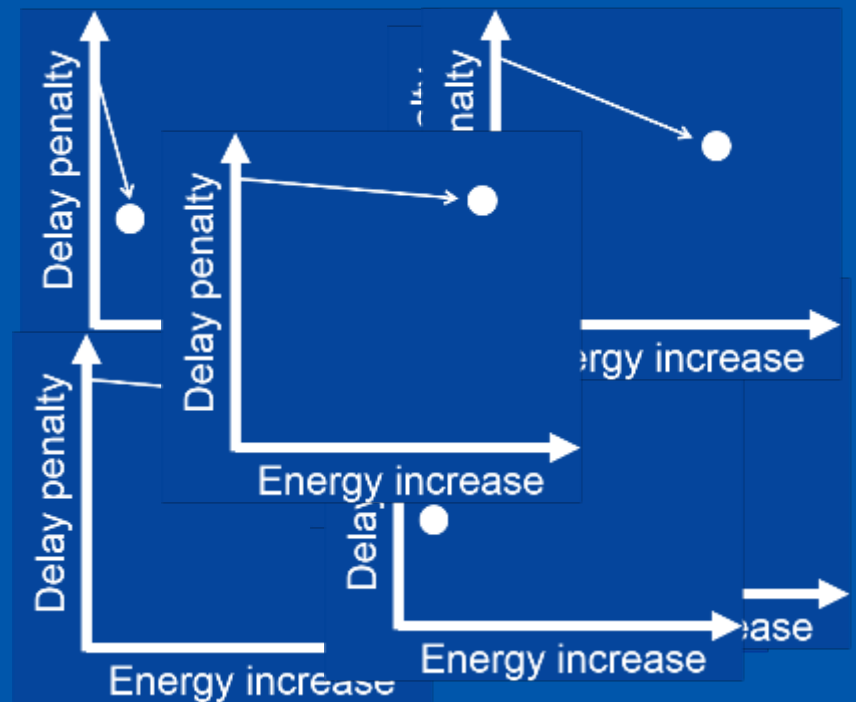
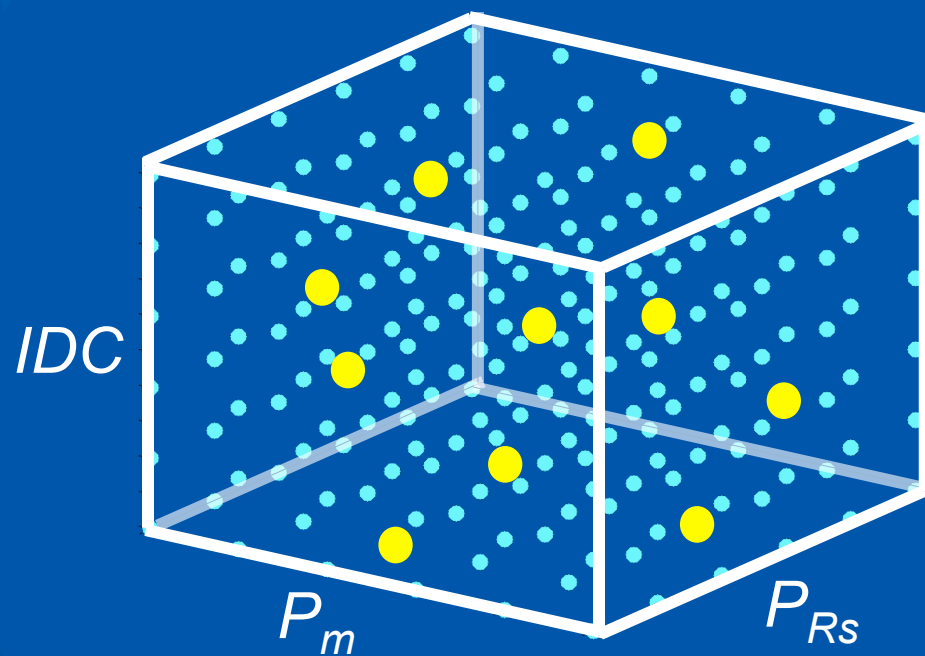
Noise margin

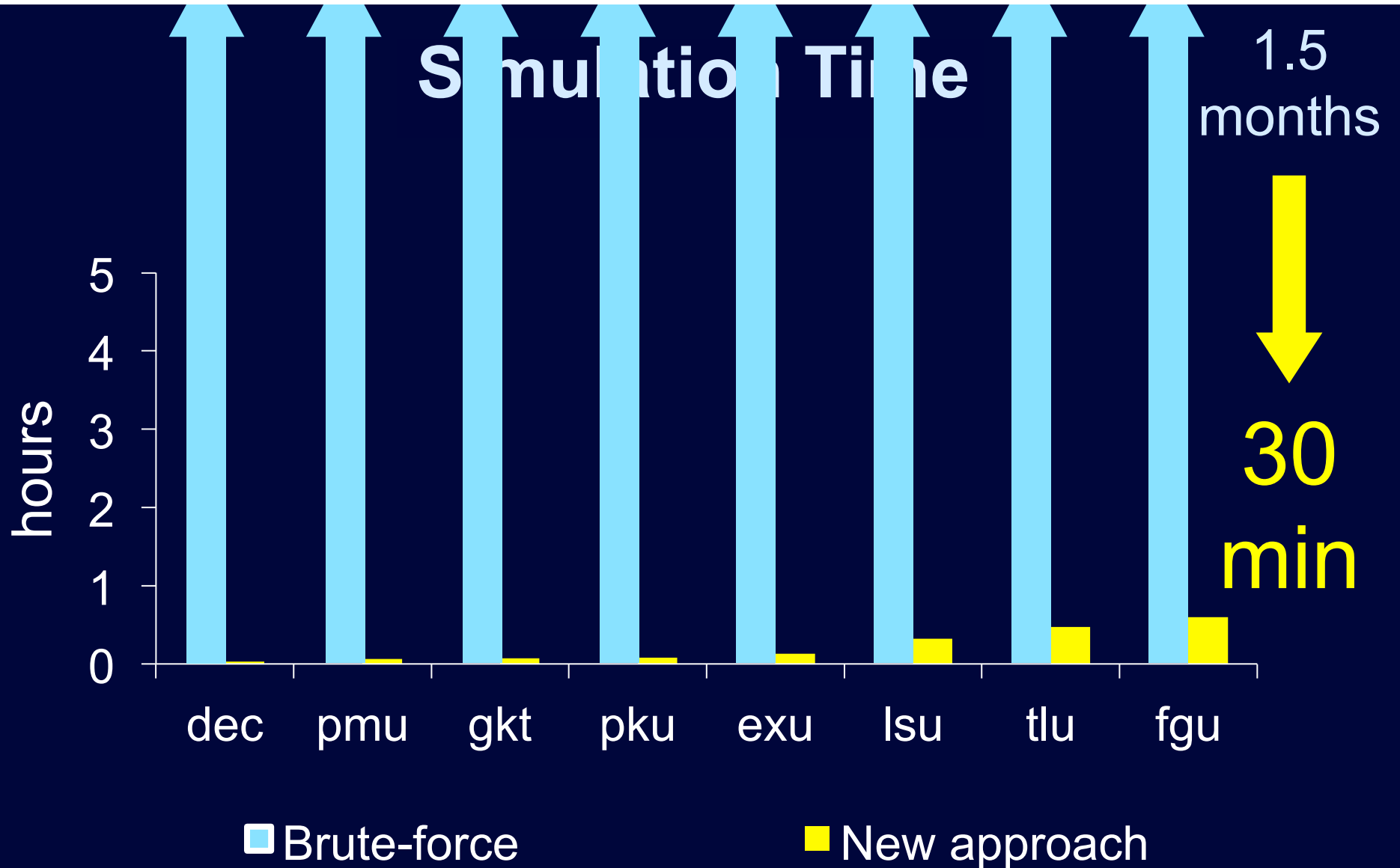


Delay

What Parameter Values ?

- Exhaustive search infeasible



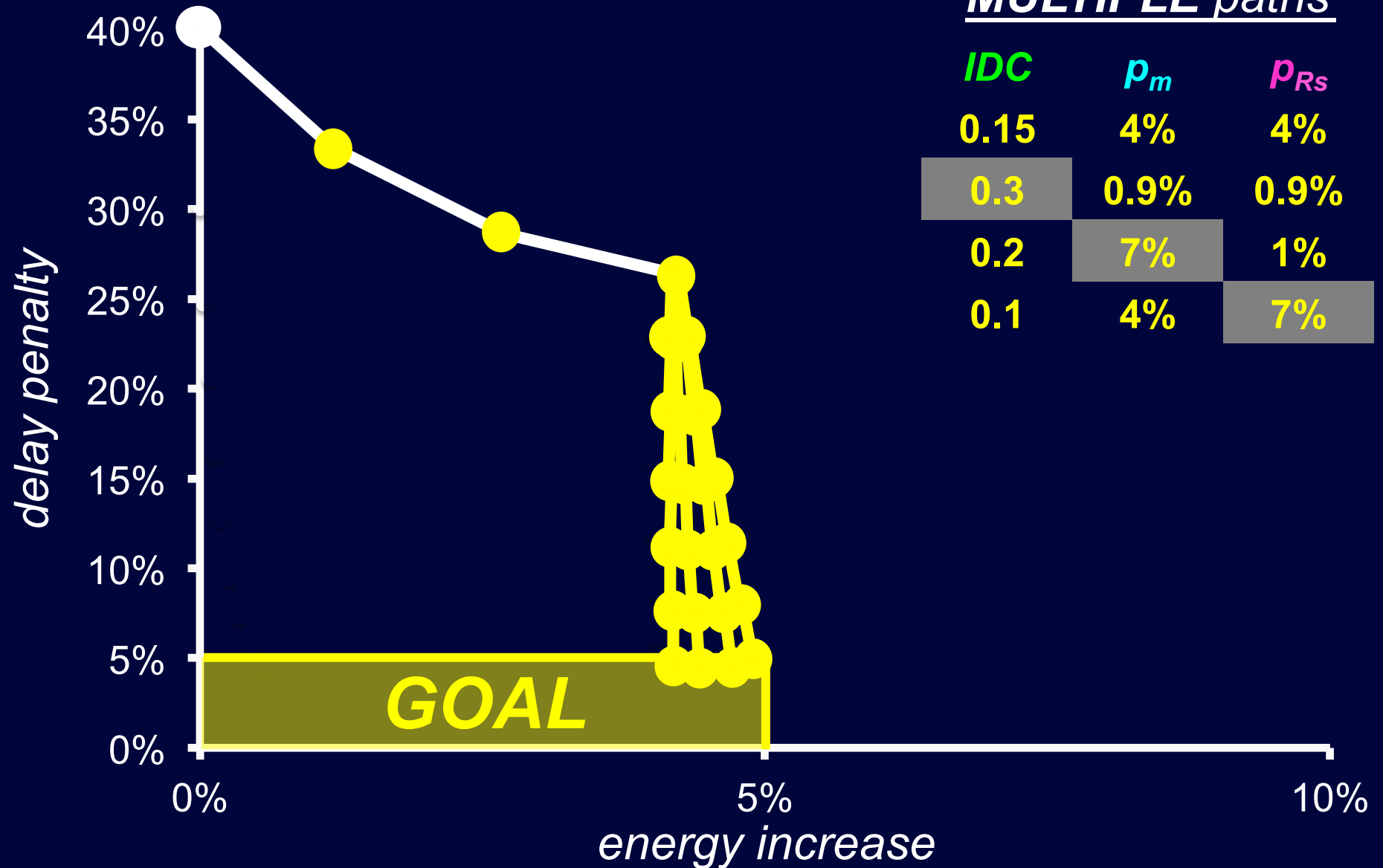


Accuracy within 2.5% of brute-force

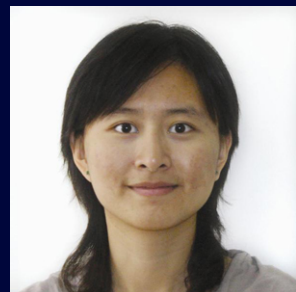
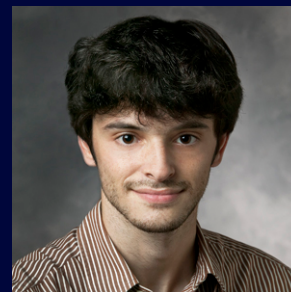
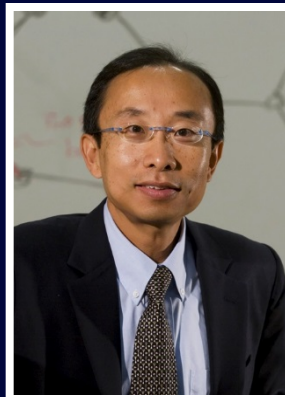
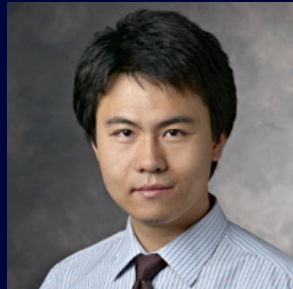
Example

MULTIPLE paths

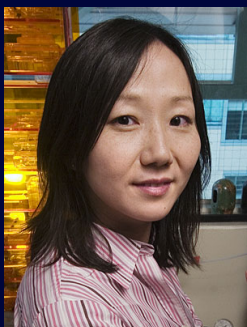
<i>IDC</i>	<i>p_m</i>	<i>p_{Rs}</i>
0.15	4%	4%
0.3	0.9%	0.9%
0.2	7%	1%
0.1	4%	7%



Thanks to “Carbon” Group



“Carbon” Sponsors & Collaborators



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Stanford



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EPFL



G. Gielen
KU Leuven



J. Rabaey
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