3DIC System Design Impact, Challenge and Solutions

ISPD 2014

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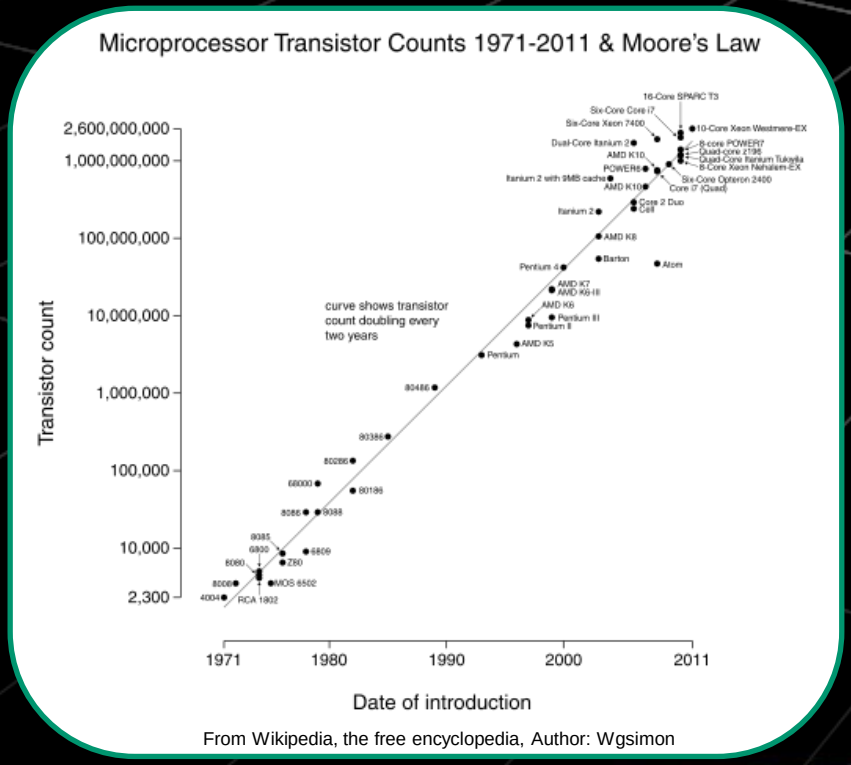
TSMC 300mm Wafer with WideIO-1 Parts

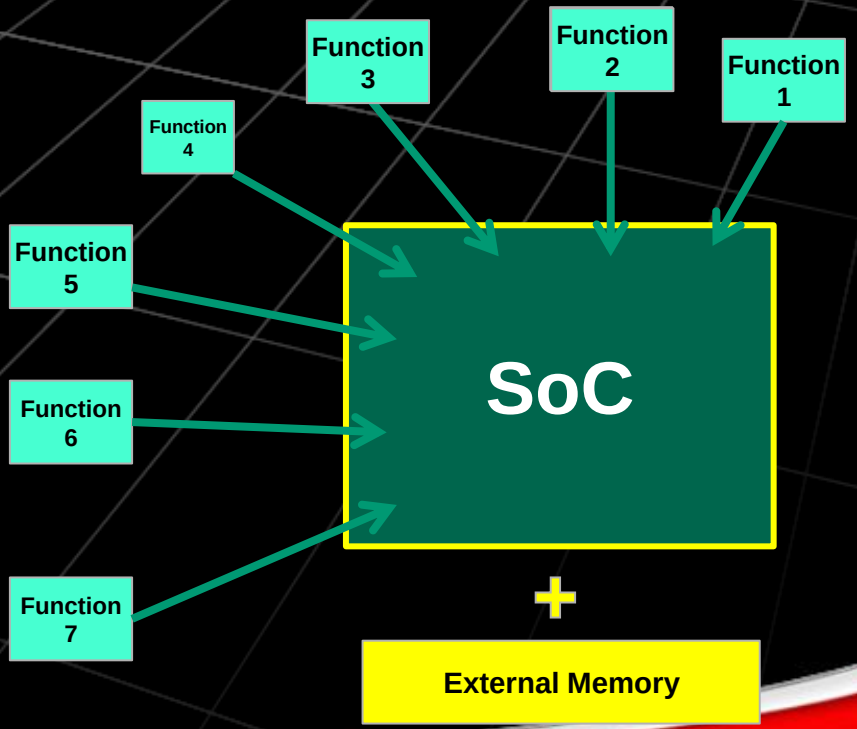
Agenda

- From 2D to 3DIC Design
- TSMC CoWoS™ Test Vehicle Platform
- Design Challenges in 3DIC
- Next Steps and Design Flow Support
- Lesson Learned and Suggestions
- Summary

SoC Integrations Trend

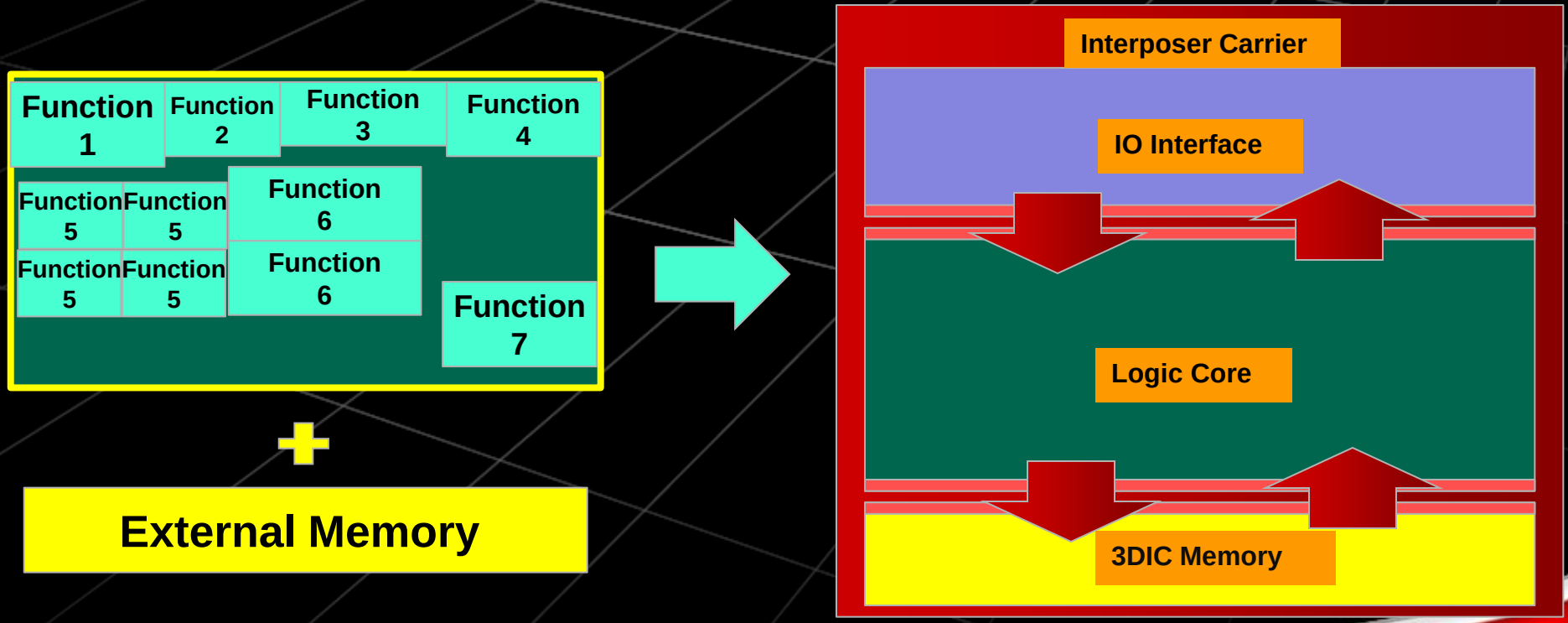
- As Moore's law predicted, semiconductors density doubled every two years in last two decades
- Logic die can host more and more functions



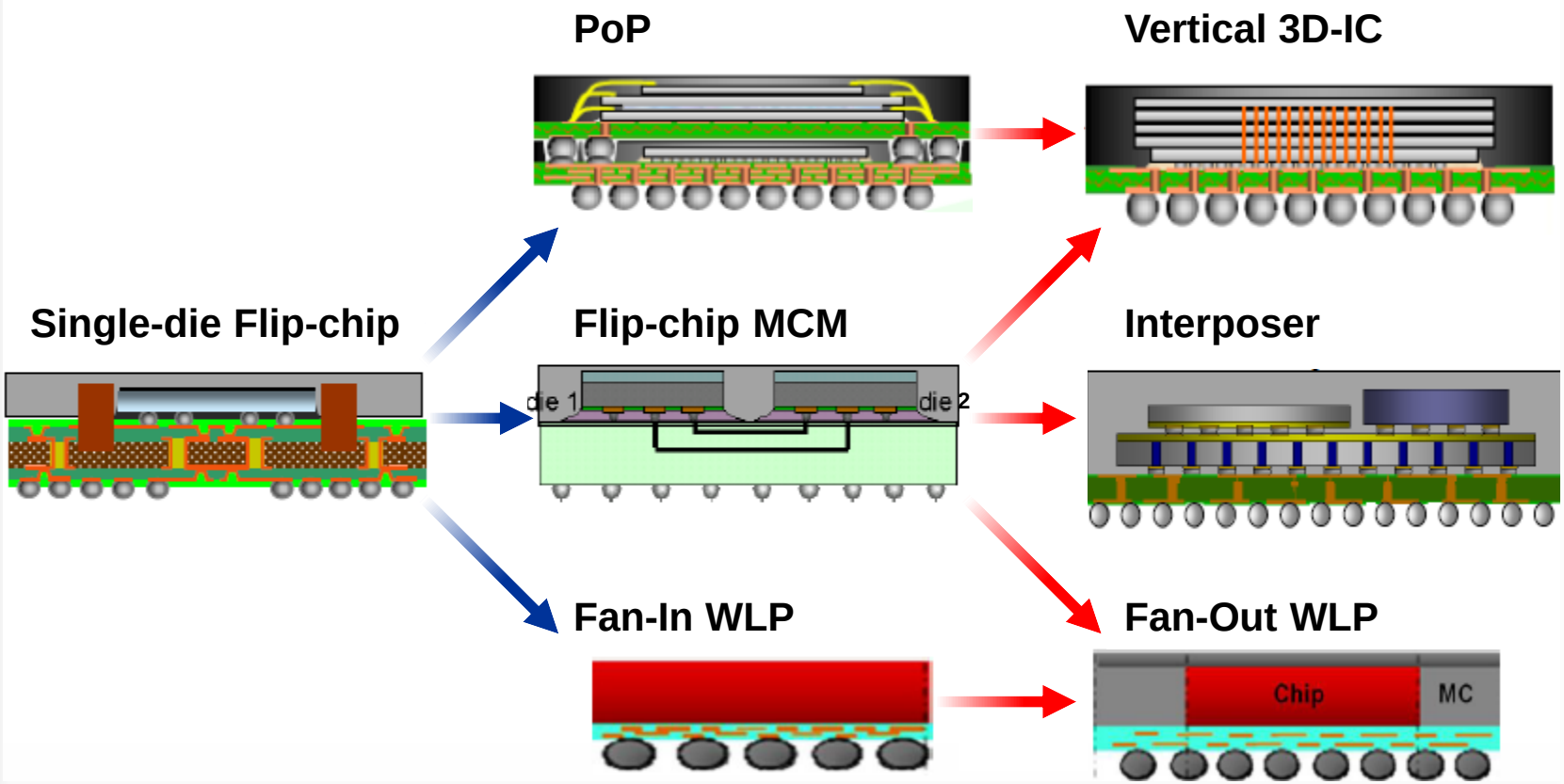


Trend for Future SoC Partition

- Driven by Cost & Yield
- Driven by bandwidth, power and form factors

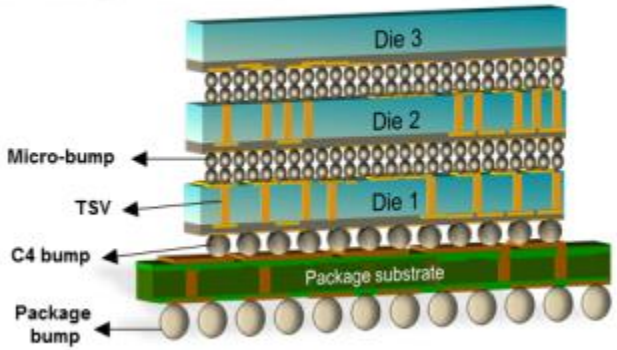


System Packaging Evolution Trend

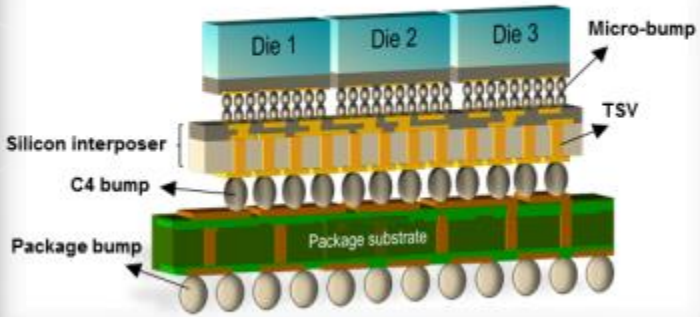


3D IC Design Paradigm

3D IC
(TTS: Through TSV Stack)



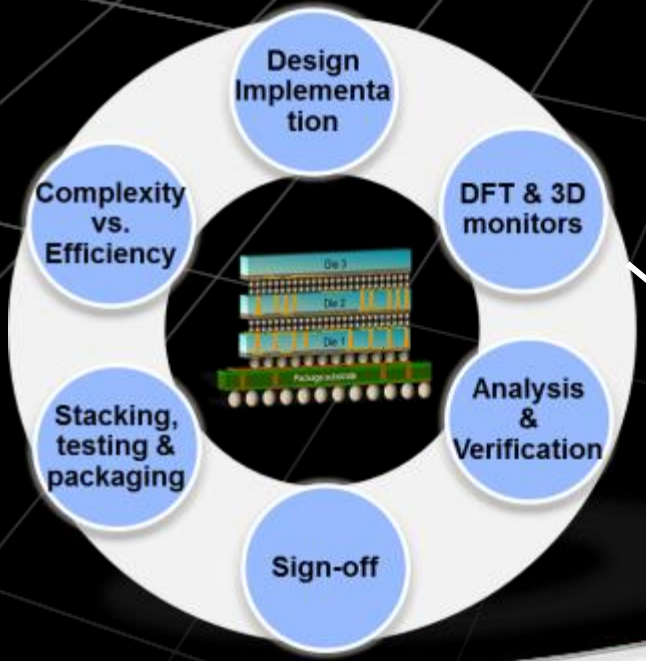
CoWoS™ IC
(TIS: Through Interposer Stack)



Advantages

- Integration of dies with individually optimized processes
- Better performance, lower power and higher bandwidth
- Yield enhancement through logic die partitioning
- Reduced system form factor
- Shorter time to market through heterogeneous integration

Challenges



Partners & Eco systems

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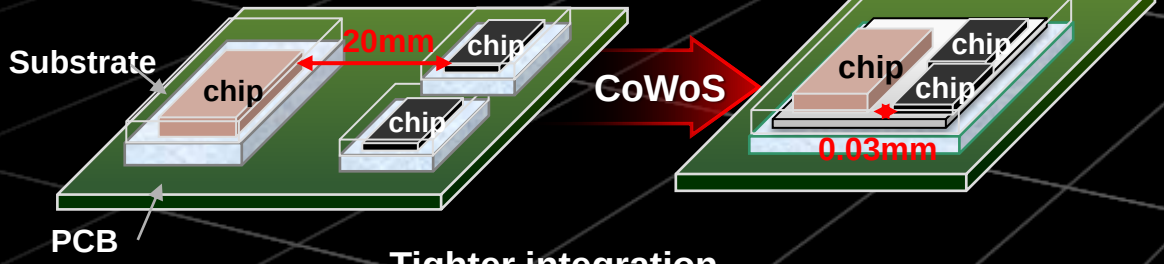
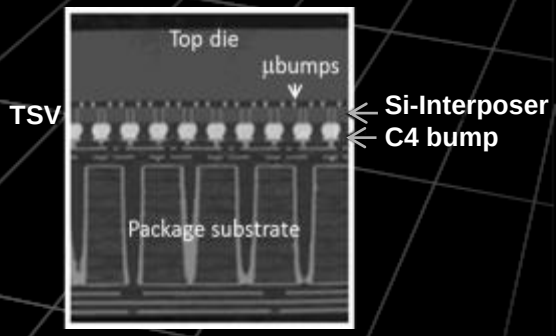
CoWoS Technology

- Integrate multiple chips into one single package using a sub-micron scale silicon interface (interposer)

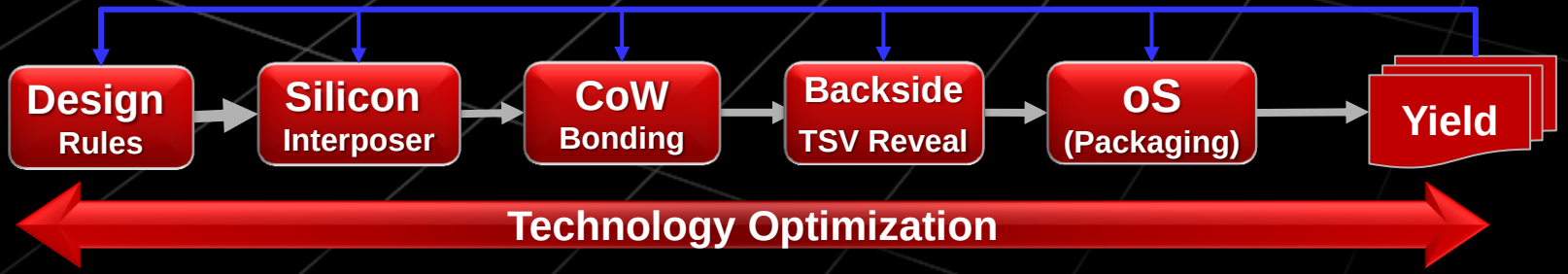


Tighter integration



Cross section view of CoWoS system

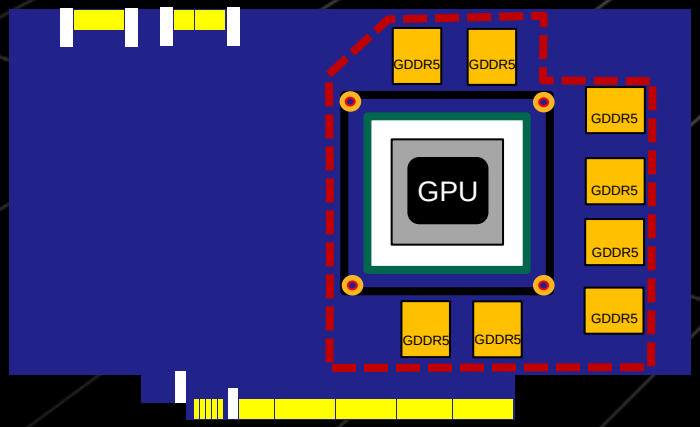
- Collaborate with customers to shorten time to market



2D - 3D Improvements

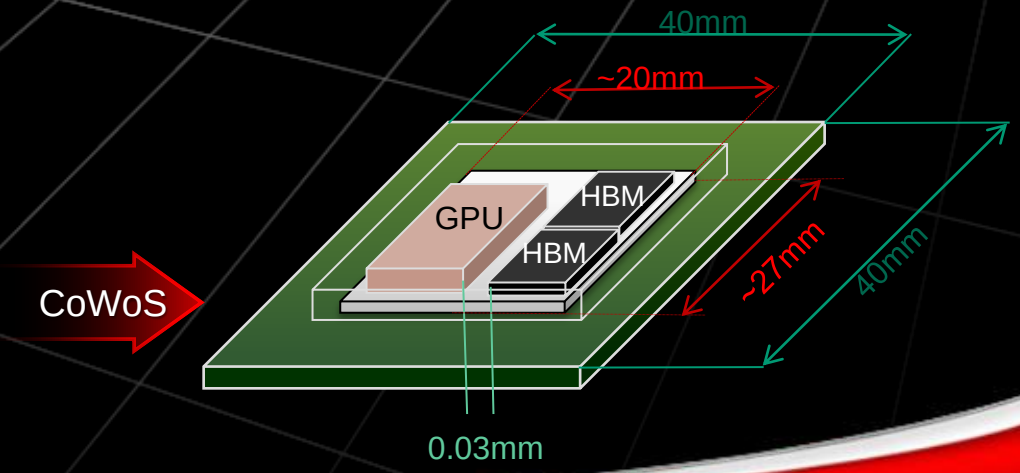
- Provide wider interface, boost performance
  - 2x HBM stack, BW up to 256GB/s
- Save space, wiring distance and power
  - Est. each HBM ~3.5W, total power ~7W
  - PCB area reduction from 120x120mm to 40x40mm

8GByte GDDR5 + GPU on 40x40mm substrate
PCB area ~12cmx12cm
8 GDDR5 BW=192GB/s, Power 42W



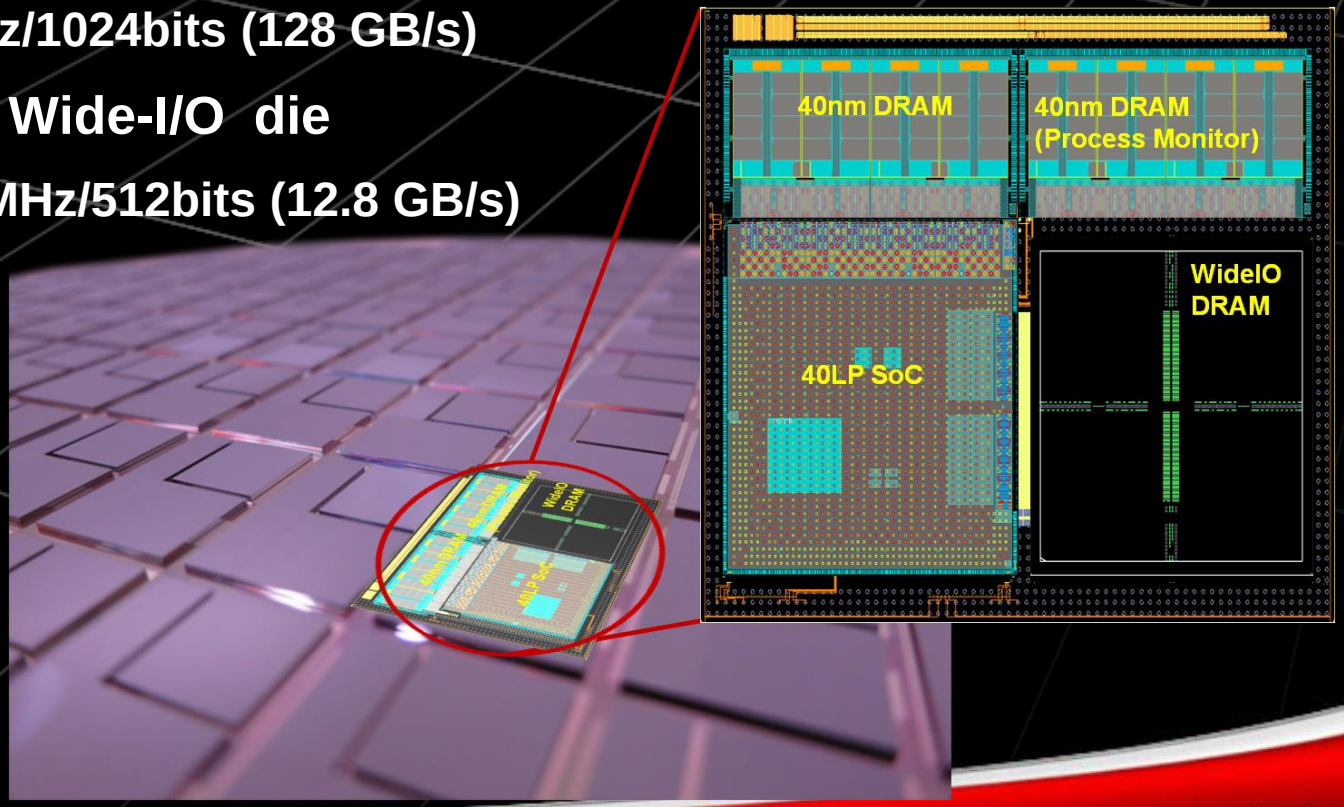
High end Graphic Card Example

GPU (10x18mm) with 2 HBM stack on interposer 40x40mm substrate
2 HBM, 8 die total, 8GByte, BW 256GB/s, Est. power 7W



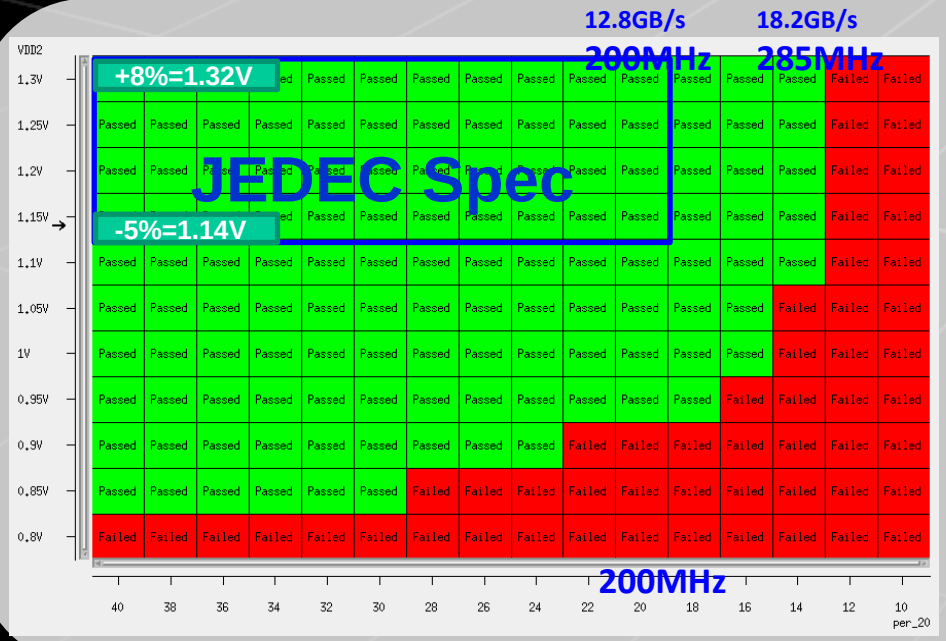
CoWoS Platform Test Chip with WideIO DRAM

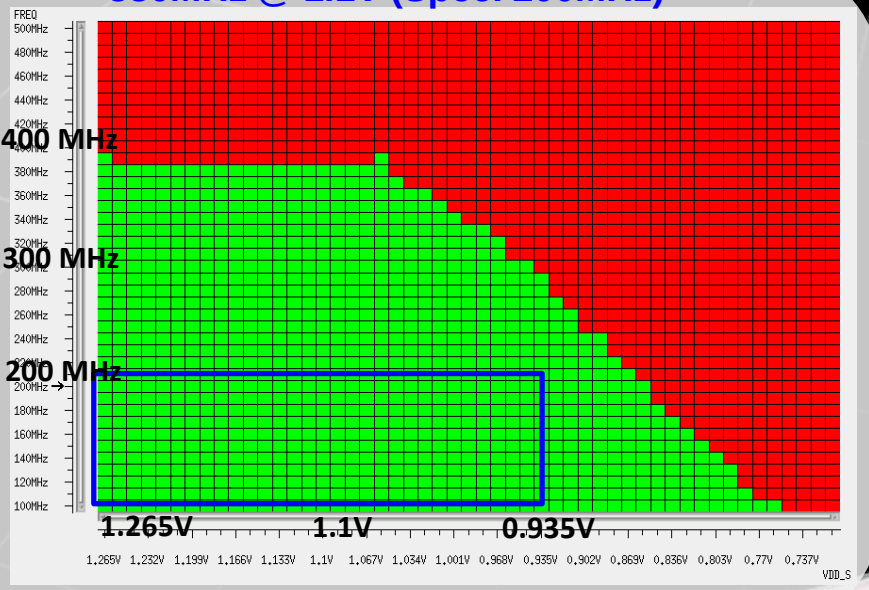
- Integration of third party die on interposer
  - Logic die (40nm)
  - TSMC DRAM (40nm)
    - 1GHz/1024bits (128 GB/s)
  - JEDEC Wide-I/O die
    - 200MHz/512bits (12.8 GB/s)



WideIO DRAM in TSMC CoWoS

- WideIO-1 DRAM performs very well on CoWoS structure
  - At test chip set up, 200Mhz DRAM was overdriven up to 285MHz with full operations
  - With limited address and pattern, memory interface reached 380Mhz





Uncertainty with Third Party Die

- Wide-I/O DRAM is JEDEC compliant die
  - JEDEC standard defines the physical foot print of the die
- Key Barriers
  - µbump size, material & density matching between Wide-I/O DRAM and interposer
  - Matching of location of support pillars/µbumps
  - Signal routing and power delivery to Wide-I/O DRAM
    - Long/short wire/trace analysis to calculate signal/power integrity affect
  - Silicon to Standard matching
    - How to ensure die is compliant to JEDEC standard?
- TSMC CoWoS design methodology and routing kit to address the above challenges

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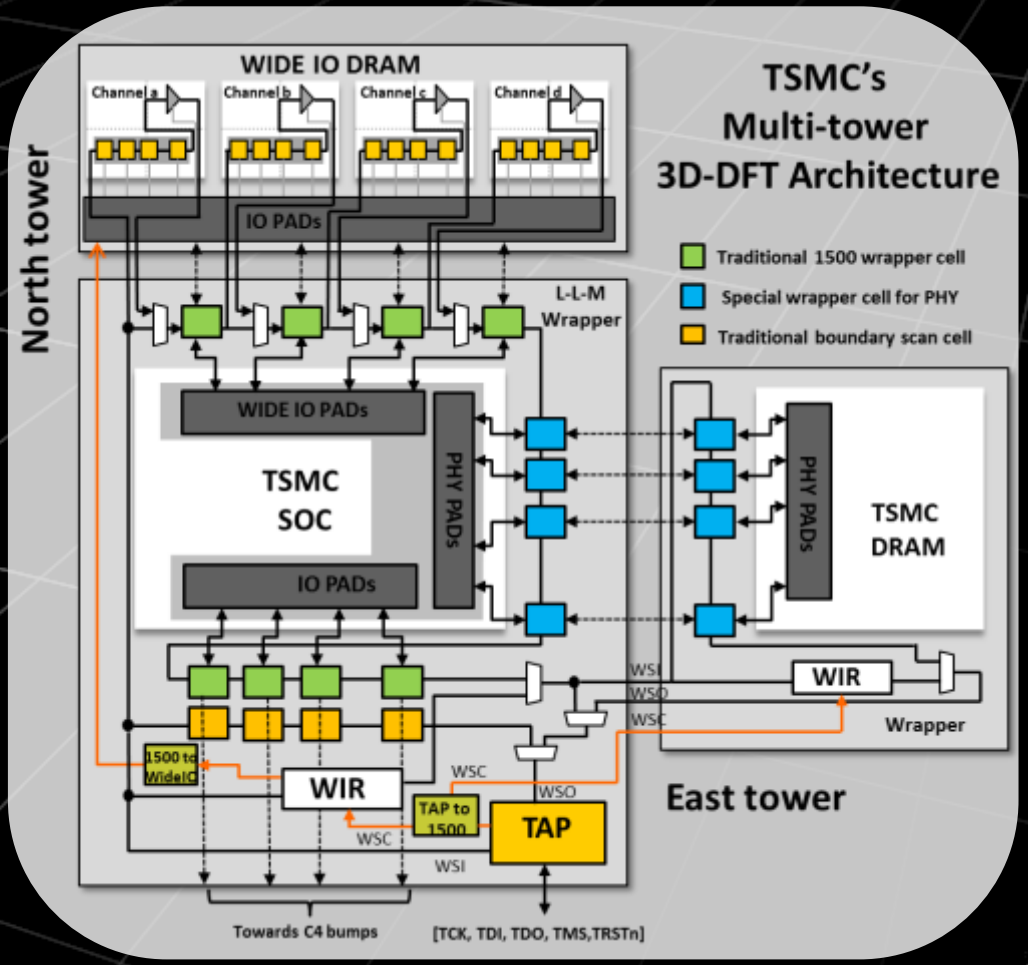
Design Challenge & Solutions

- Complexity vs. Efficiency
  - Footprint, Power, Performance
  - 3D IC or CoWoS
- DFT and Monitors
  - Testing of dies and stacks (Logic-Logic & Logic-Memory), plug-n-play
  - Sensors for thermal and other 3D effects
- Test for Packaging
  - Reliability and testing flow
  - Thin wafer handling, mechanical stress
- Partner and Ecosystem
  - First time EDA flow adoption, 3D IC specific IPs and IP quality
- Analysis and Verification
  - Heterogeneous dies integration knowhow
  - Verification of 3D elements, stack-level STA

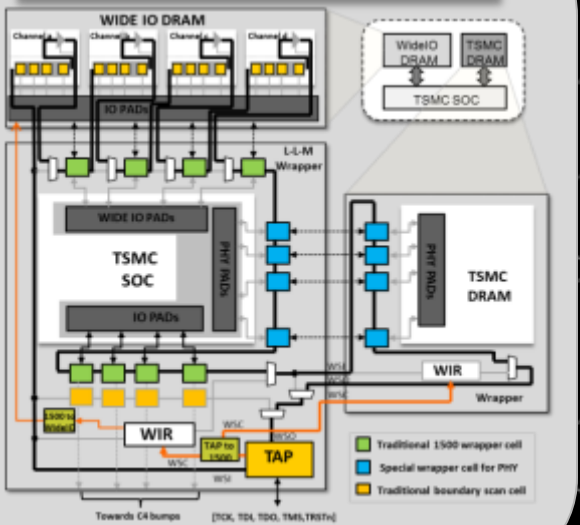
Multi-Tower 3D-DFT Architecture

- **Industry's first multi-tower architecture based on IEEE 1500 Std.**
  - **Position of PAD cells and wrapper cells is swapped for clarity**
- **Features**
  - **Low-pin count: TAP-based control from package pins**
  - **Complete tower can be bypassed during test**
  - **Each channel in wide-IO DRAM can be bypassed**

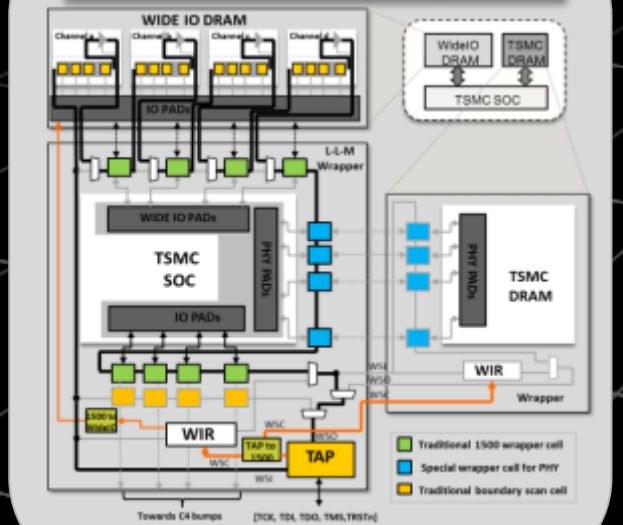


Supported Modes Example

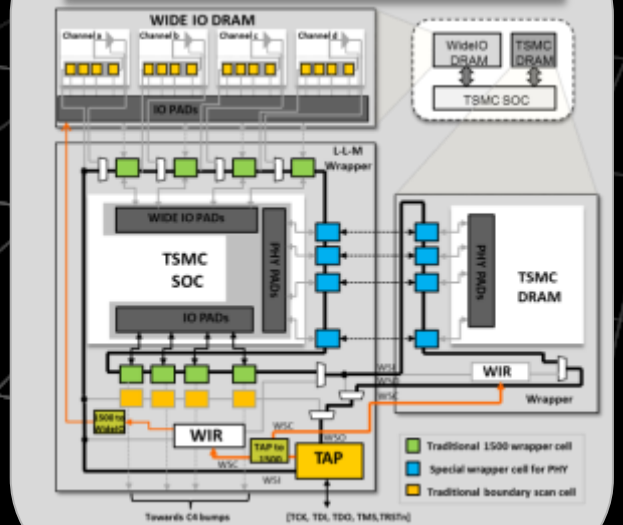
Three die Interconnect Test



(SOC-Wide-I/O DRAM) Test

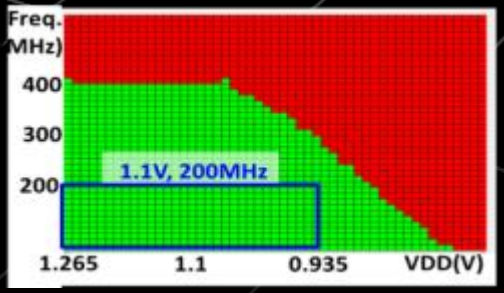


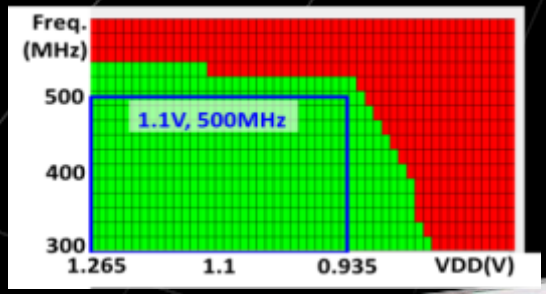
SOC-DRAM Test



- High-speed interface test with the reduce function Instruction set
  - Exceeds the specification for both interfaces

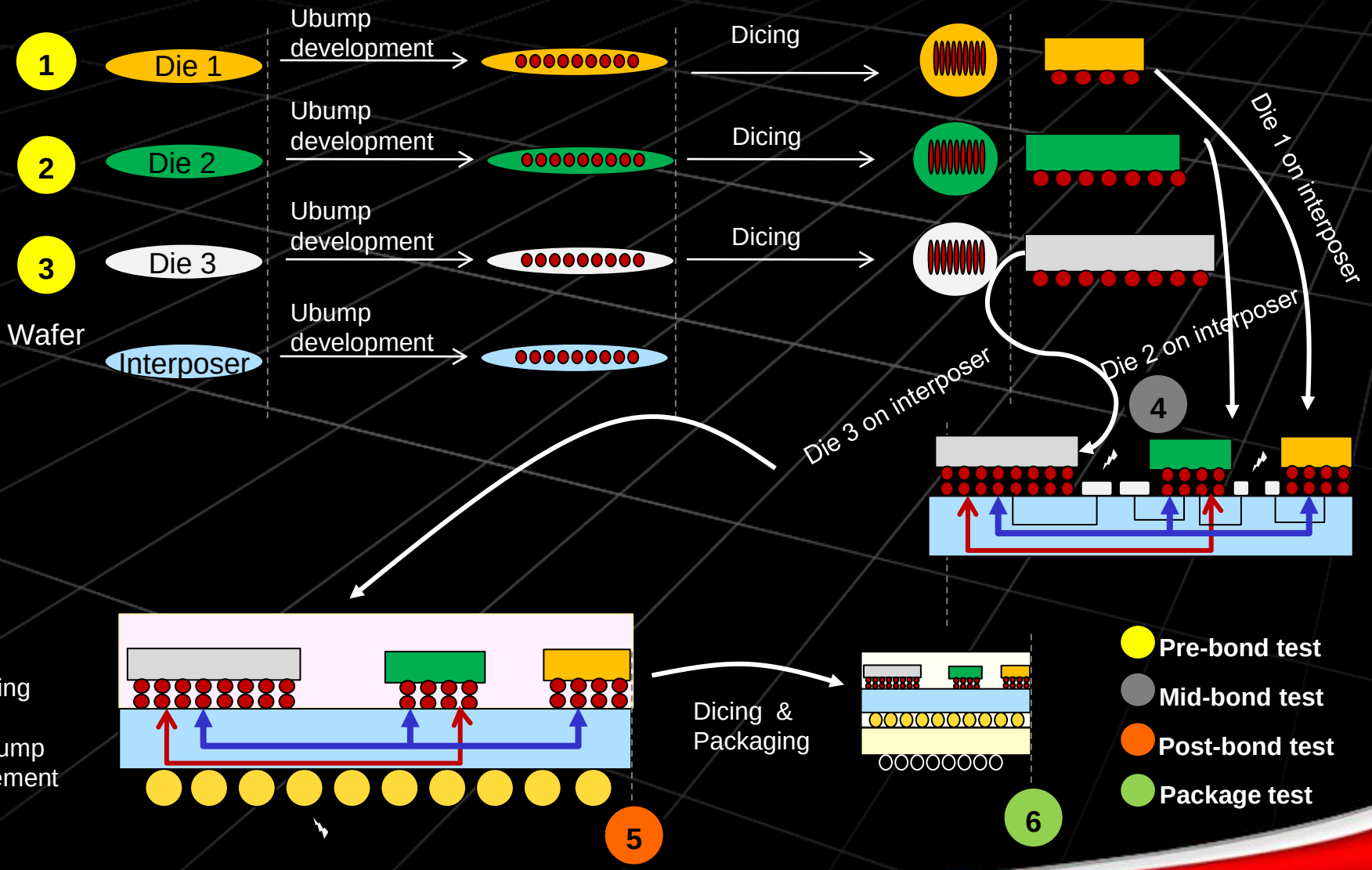
SOC-to-Wide-I/O





SOC-to-TSMC DRAM

Test Flow Optimization



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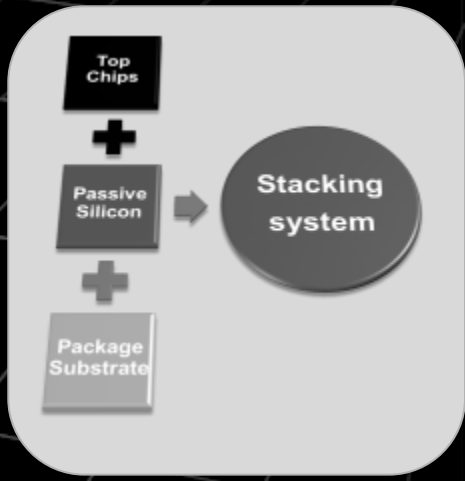
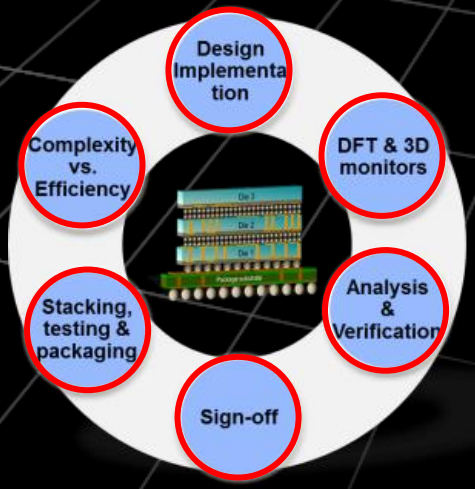
CoWoS and 3D IC Design Solutions

Top Chips	Passive Silicon	Package Substrate	Stacking System
Bump assignment	Implementation (Micro-bump alignment Routing, MiM)	Substrate routing	Inter-die LVS/DRC
RDL routing	RC Extraction	Substrate RLC extraction	Integrated IR/EM
Wafer level DFT & BIST	LVS/DRC		Thermal analysis
Micro-bump DRCB	SSN(SI/PI) RLC extraction		Package level DFT & BIST
	PDN RLC extraction		Stacking STA & post-simulation
			SSN(SI/PI)/PDN simulation



TSMC 3D / CoWoS IC Readiness

CoWoS	Capability	Readiness
Top Chips	Bump Assignment / RDL Routing	●
	Wafer-level DFT & BIST	●
	μbump DRC	●
Interposer	Bump Alignment & Interposer Routing	●
	RCX	●
	LVS/DRC	●
	SSN (SI/PI) RLC Extraction	●
	PDN RLC Extraction	●
Substrate	Substrate Routing	●
	Substrate RLC Extraction	●
Stacked System	Inter-die LVS/DRC	●
	Concurrent IR/EM	●
	Thermal Dissipation Analysis	●
	Package-level DFT & BIST	●
	Stacking STA / Post-sim	●
	SSN (SI/PI) / PDN Simulation	●
Memory IP	Controller, PHY	●

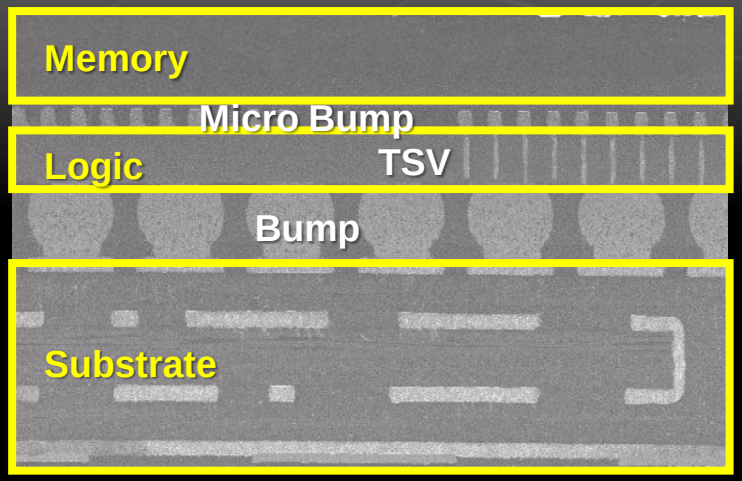


● Complete

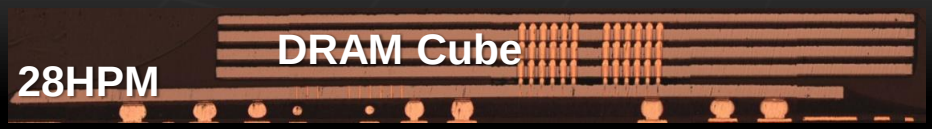
TSV / 3D-IC Vertical Stacking

- Demonstrated vertical stacking of memory on 28nm logic for mobile applications
- Characterized TSV (Through-Silicon-Via) design rule for customer's test vehicle design and functional verification

DRAM on 28HPM Logic



Memory cube on 28HPM

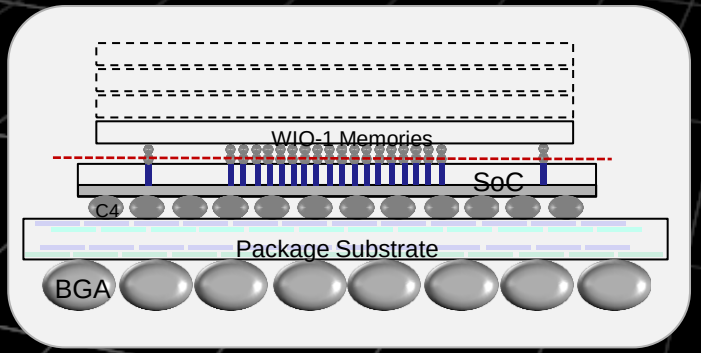


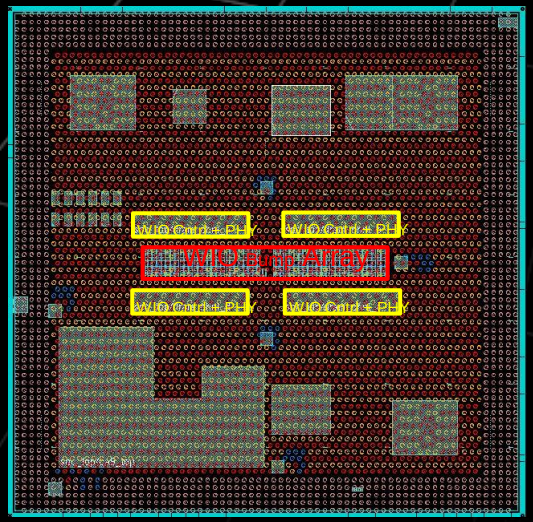
3D IC TTS Design Solution

3D IC	Capability	Readiness
Silicon Chips	Bump Assignment / RDL Routing	●
	Wafer-level DFT & BIST	●
	µbump DRC	●
	Cu-pillar Bump Implementation	●
	Custom Design Support	●
	TSV-to-TSV Coupling RCX / TSV RLC Subckt Replacement	●
Substrate	Substrate Routing	●
	Substrate RLC Extraction	●
Stacked System	Inter-die LVS/DRC	●
	Concurrent IR/EM	●
	Transient Thermal Analysis	●
	Integrated DFT & BIST	●
	Cross-die STA / Post-sim	●
	System PDN Simulation / TSV SSN	●
	Decap/Mimcap Co-optimization	●
	Chip-Package Bump Co-optimization	●
Memory IP	Controller, PHY	●

● Completed

Validated with 3DIC TTS Test Vehicle





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Lesson Learned and Proposal - ESD

- JEDEC has a very good ESD specification for all chip IO pins. However in 3DIC, interconnect pins are not ESD protected to reduce the input loading capacitance
  - Only the direct access test pins are ESD protected
  - DA functions are vendor specified. Different vendor may use different DA pins and may not protect the unused pins with ESD

- Proposed JEDEC to standardize DA pin set. All DA pins have to be ESD protected per Human Body Mode at any time

Lesson Learned and Proposal – Boundary Scan needs

- JEDEC has adopted different Boundary Scan standard or a simplified version of standard
  - WIO1 and WIO2 have used a portion of IEEE1149 like design but not a complete package.
    - The EDA tools have to be adjusted from IEEE std to adapt the DRAM interface
  - HBM has adopted the complete IEEE 1500 package
- Do not have a standard software interpretation on DRAM portion of Boundary Scan logic
  - On WIO1, a small variation generated on one vendor's software package may not fit the other vendor's parts
- Suggestion:
  - Specification has to be carefully defined to avoid ambiguity, which may cause adoption of different logic interpretations
  - Continue to encourage adopting full IEEE standard instead of partial standard

Lesson Learned and Proposal – Support balls

- JEDEC has defined all signal ball and part of support ball in the MO file with detailed mechanical drawings
  - Other mechanical support balls are vendor defined
  - This makes the over all footprint mismatch one vendor parts to others

- JEDEC has started standardizing all support ball positions

Summary

- Semiconductor industry will continue to drive the technology evolution per Moore's law
- The 3D IC transition is here
  - Better performance, lower power, smaller form factor
  - Die partitioning improves yield
  - It has create different dimension from Moore's law
- More than Moore system integration enabled by TSMC 3DIC and FOWLP solutions
  - CoWoS Reference Flow released at OIP 2012
  - 3DIC TTS Reference Flow released at OIP 2013

Thank You