Physical Design for Debug: Insurance Policy for IC's

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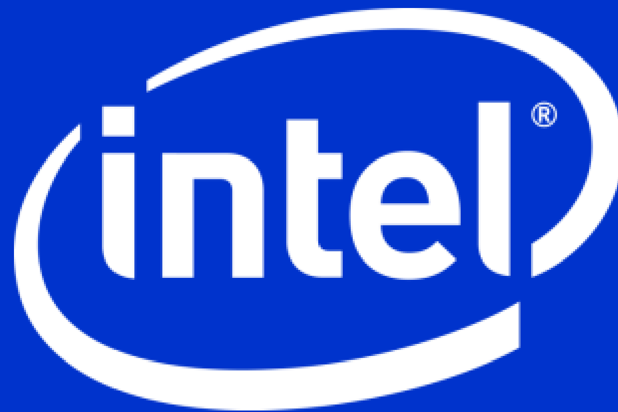

Purpose

Learn about PDFD Features

Find out Why PDFD is Critical to Post Si Debug

Discover Ways to Insert and Meet Coverage

How to Build PDFD into Standard Library Cells (Stealth DFD)

Outline

- Overview
- Physical Debug Equipment Overview and Challenges
- PDFD Features
- Insertion and Placement
- PDFD Utilization for Product Steppings
- Conclusion

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Overview

- Problem Statement: Perform root cause analysis and validation of Engineering Change Orders (ECO's)/bugs during physical debug of IC's (SoC, microprocessor, …) for faster time-to-market with high quality.

- Industry Standard Solution => Physical Debug: The use of analytical and debug equipment to physically analyze and root cause ECO's using Focused Ion Beam (FIB) and Optical Probe equipment.
  - Bugs can be root caused and validated in a few days compared to weeks or months required for an ECO in a new mask set.
  - Can reduces the number of steppings/masks required to qualify for high volume manufacturing.
  - Caveat: XYZ scaling, layout efficiency, and new technologies (e.g. trigate) have reduced physical debugs ability to access transistors and metal signals.

Overview

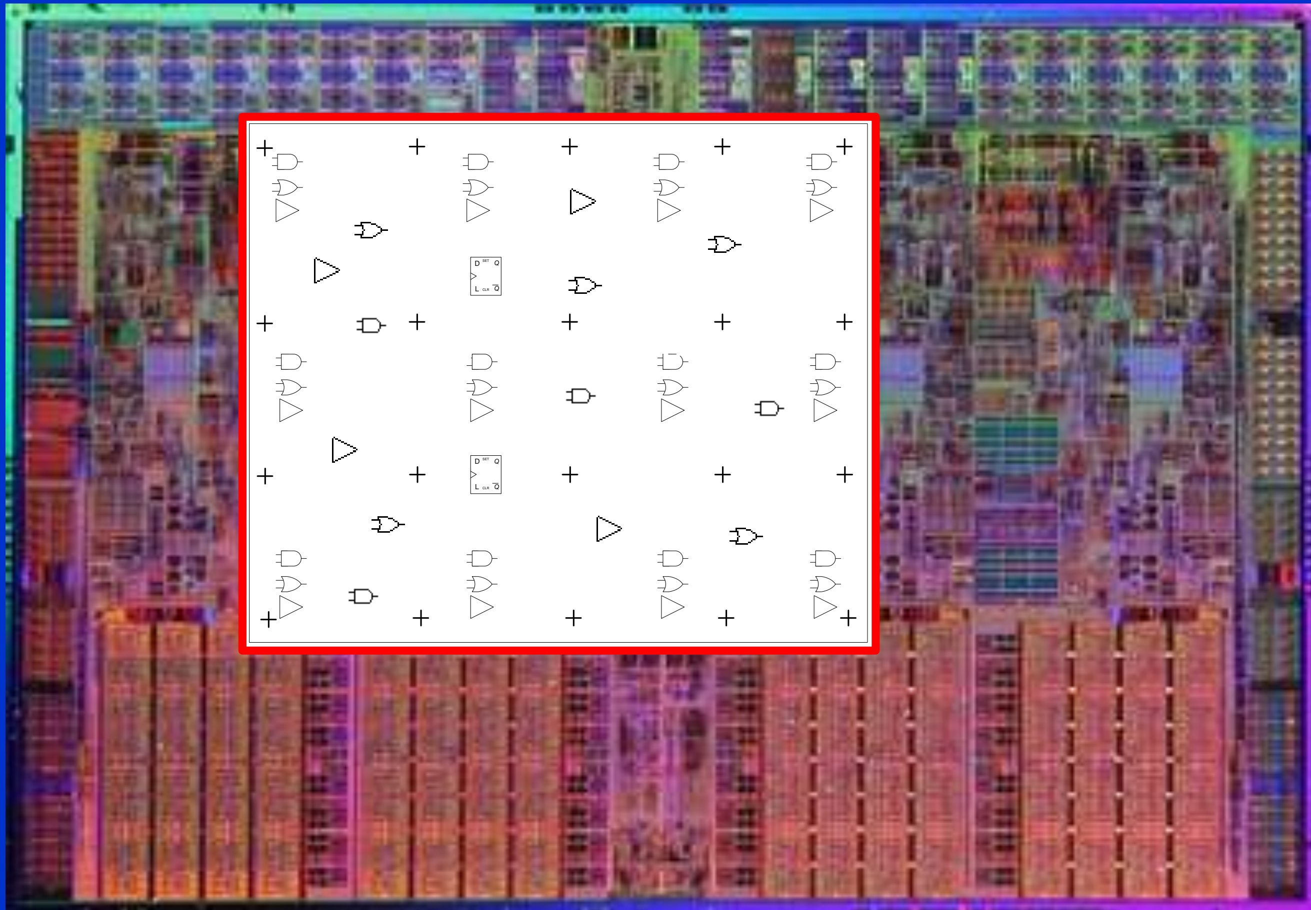
Yes – Enter P (DFD)

What is PDFD? = Physical Design for Debug

- Design hooks placed in layout to enable / optimize access to nodes during silicon debug. -e.g., FIB probe/access, backside circuit edit, optical probing.
- Typical Features: Bonus and spare cells (logic and sequential), mechanical probe points, navigation features, FIB cut / Connect cells, spacing between transistors, etc…
- Also used in conjunction with or to enable Design for Test (DFT) features.
- Built as standard library cells or incorporated into cells. Must meet Design Rules (DRC's).
- Inserted using standard place and route tools in combination with (Design for Manufacturing) DFM features.

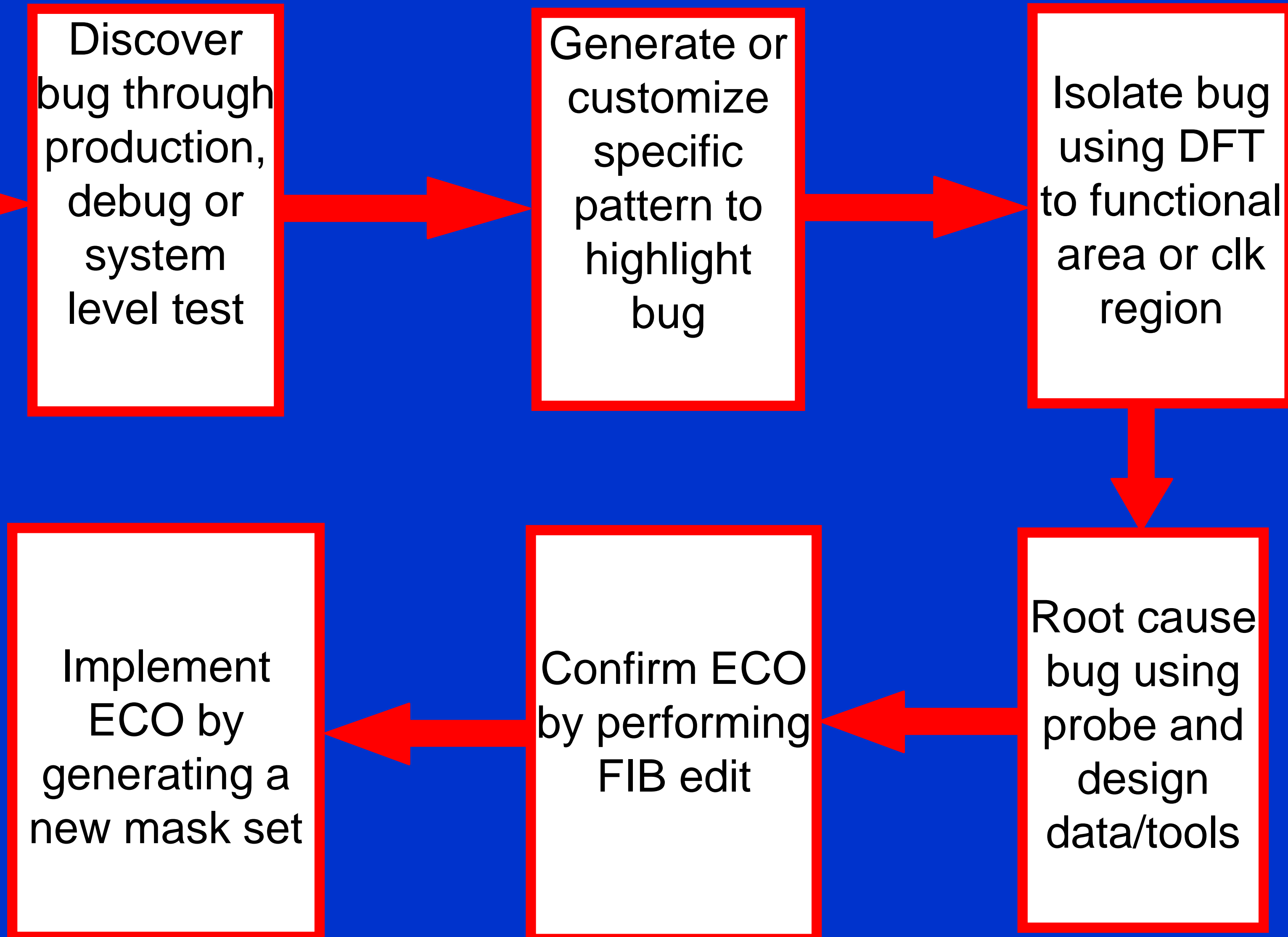
Overview

Example Cell Placement



Intel Core i7 Processor

Overview



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First Step of Physical Debug

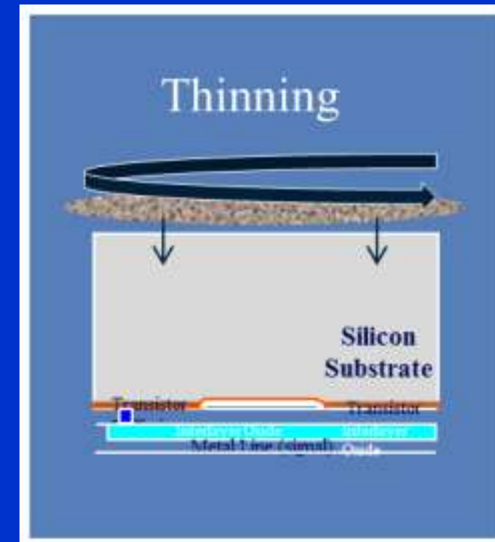
Gain access to tx's and metal routing through the backside of Si.

Intel Core i7 Processor

Circuit Edit Review and Challenges

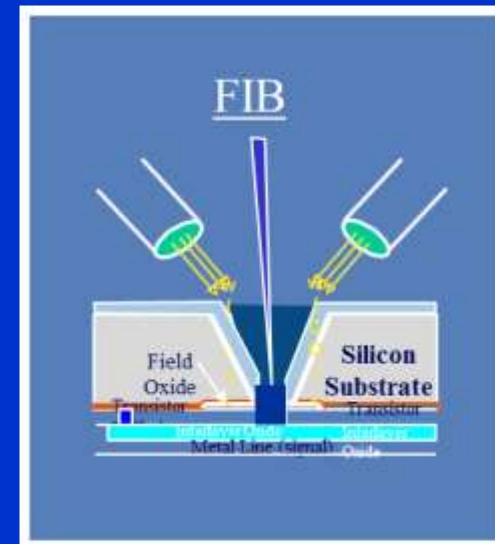
Sample Preparation:

- What: global and local thinning, IHS removal, global dielectric
- Purpose: prepare packaged devices for all debug tools
- **Challenges:** mechanical stability, invasiveness



Focused Ion Beam (FIB):

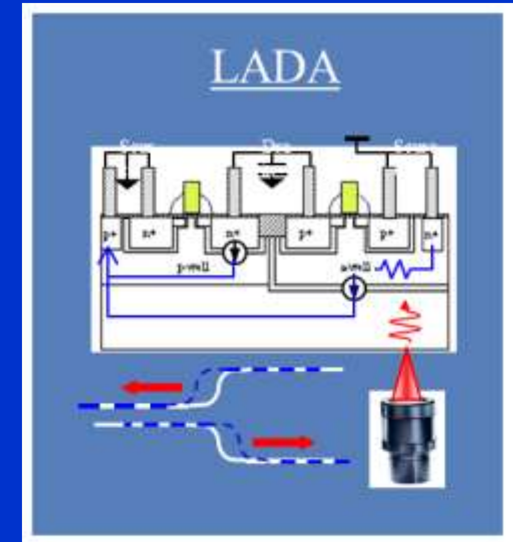
- What: scanning Ion beam with Gas assisted etching and deposition
- Purpose: circuit changes, defect introduction
- **Challenges:** mill selectivity, resolution, end pointing, invasiveness



Optical Probe Review and Challenges

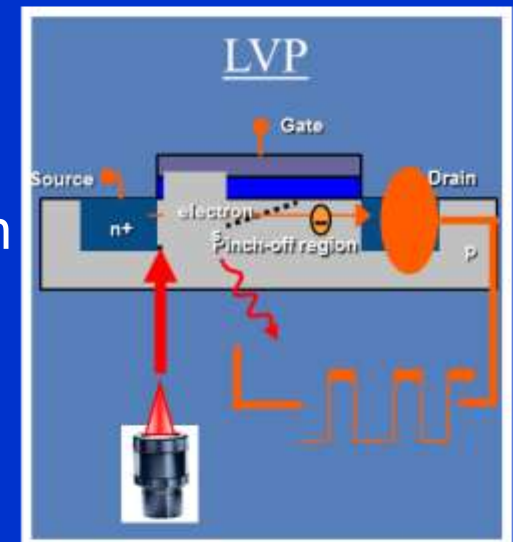
LASER Assisted Device Alteration (LADA):

- What: near IR LASER scanned over circuit/FUB while running failing pattern
- Purpose: highlights failing speedpath circuits, fault isolate marginal fails
- **Challenges:** spatial resolution, invasiveness, timing shift correlation, thermal



LASER Voltage Probe (LVP):

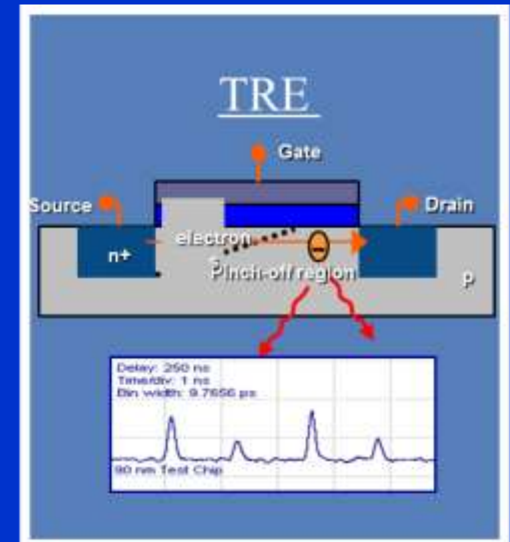
- What: near IR pulsed LASER samples transistor while running a pattern
- Purpose: obtain high-speed voltage waveforms on individual transistors
- **Challenges:** spatial resolution, S/N, thermal



Optical Probe Review and Challenges

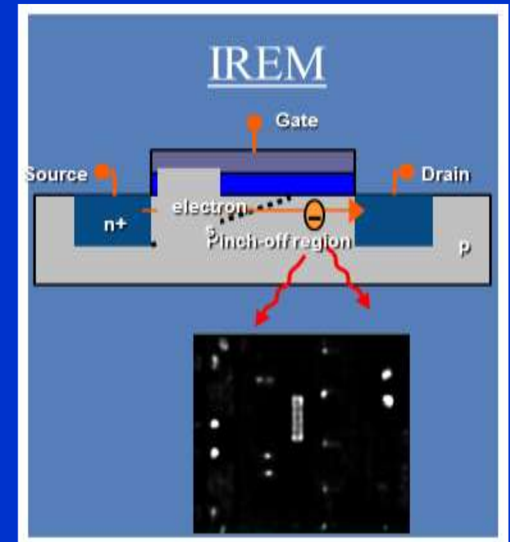
Time Resolved Emission (TRE):

- What: emission microscope with integrated high-bandwidth detector
- Purpose: obtain switching histogram on individual transistors
- **Challenges:** sensitivity, resolution, bandwidth, crosstalk, thermal



Infra-Red Emission Microscope (IREM)

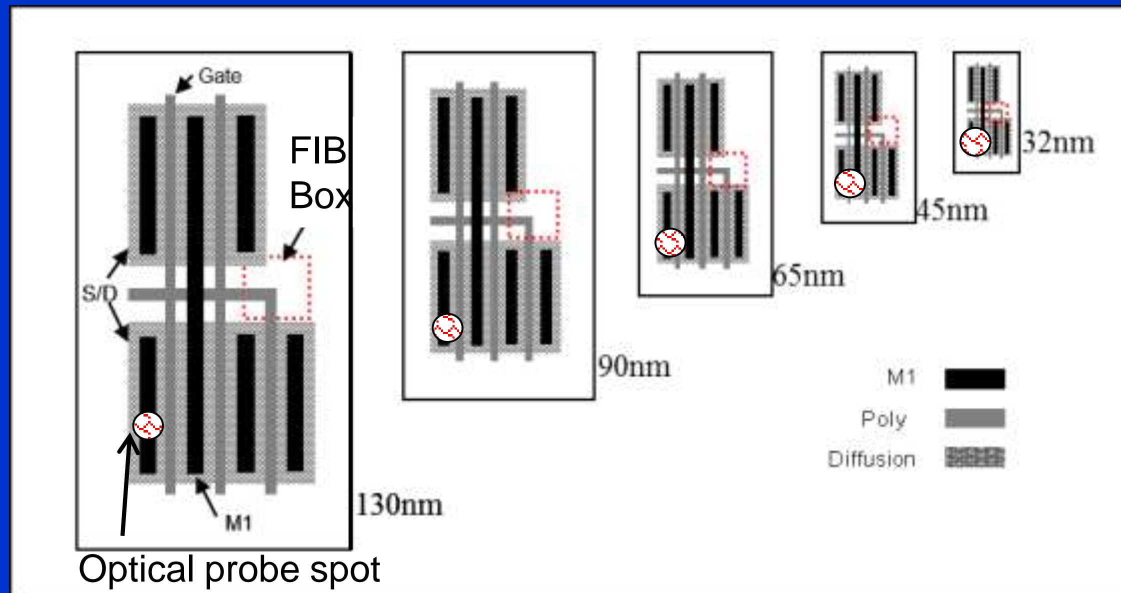
- What: NIR imaging microscope
- Purpose: logic state imaging, defect detection, power mapping
- **Challenges:** resolution, sensitivity, thermal



Physical Debug Scaling Challenges

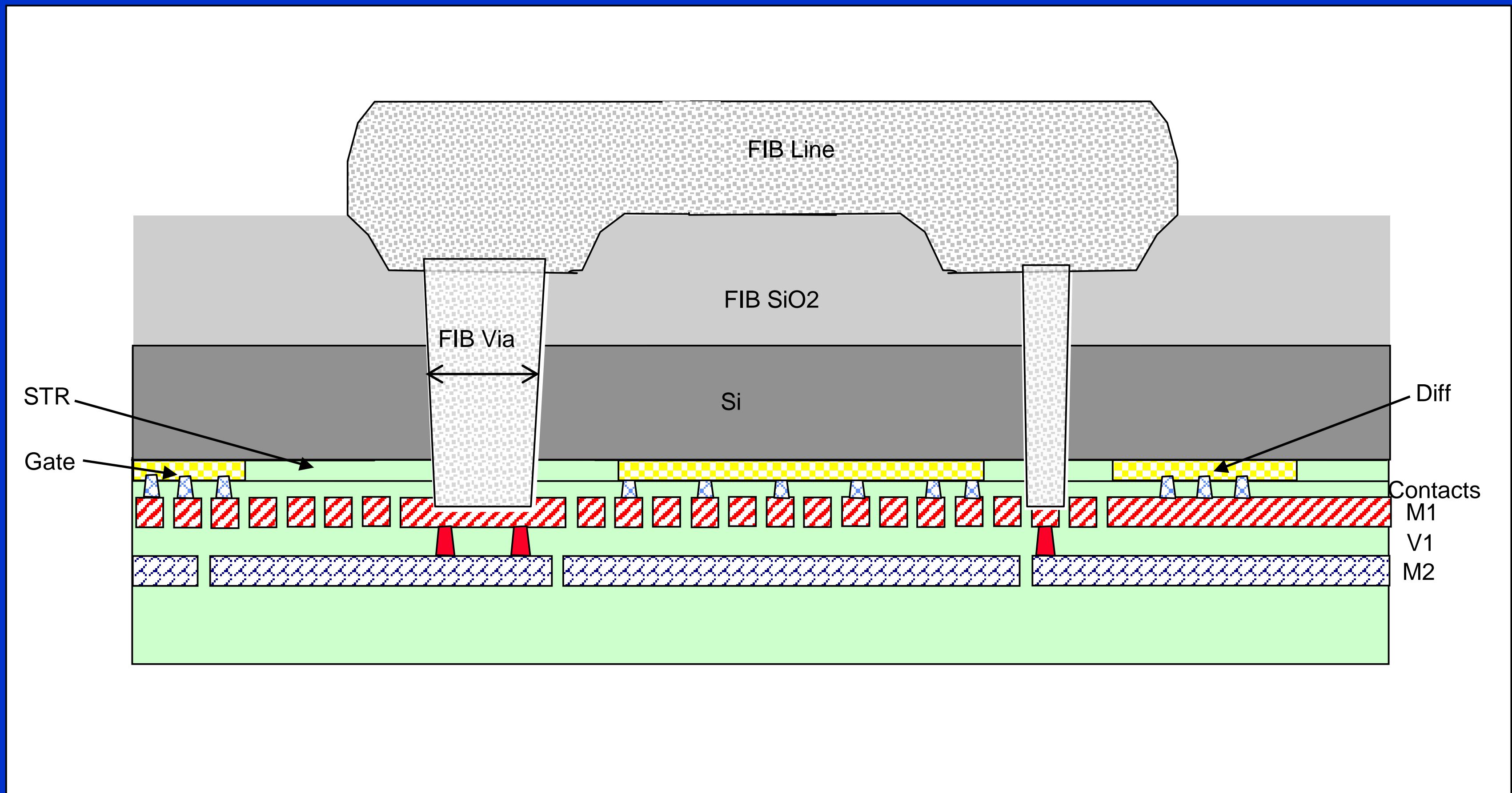
- Device geometry scaling and layout efficiency improvements have reduced physical debug's ability to access transistors and metal signals.
  - From 130nm to 45nm there was ~32x reduction in white space.
- This limit in technology scaling has resulted in a greater need for features to be placed in the silicon to enable access to internal nodes (i.e., PDFD).

Cell Height Scaling



Circuit Edit Geometry

- PDFD features provide guaranteed access to critical signals.
  - Excellent correlation between aspect ratio and success rates.
  - Shown here on the left is a metal 1 PDFD connection point and on the right is an opportunistic metal 1.



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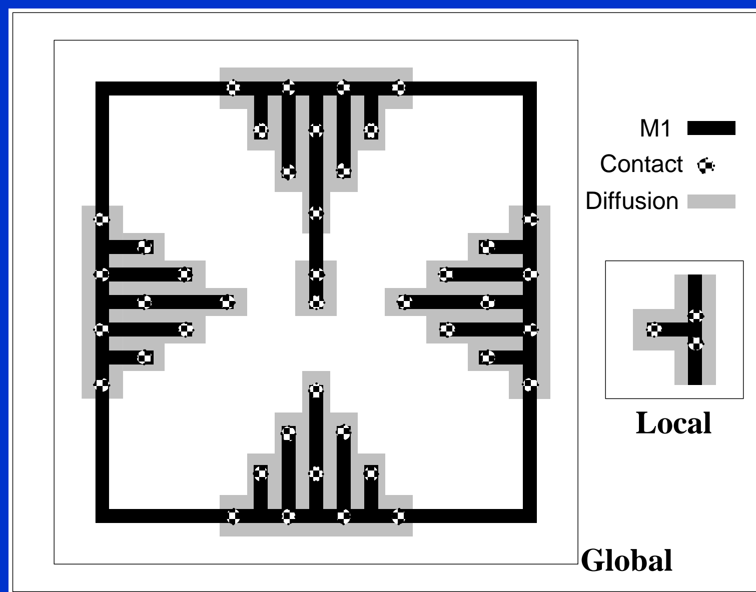
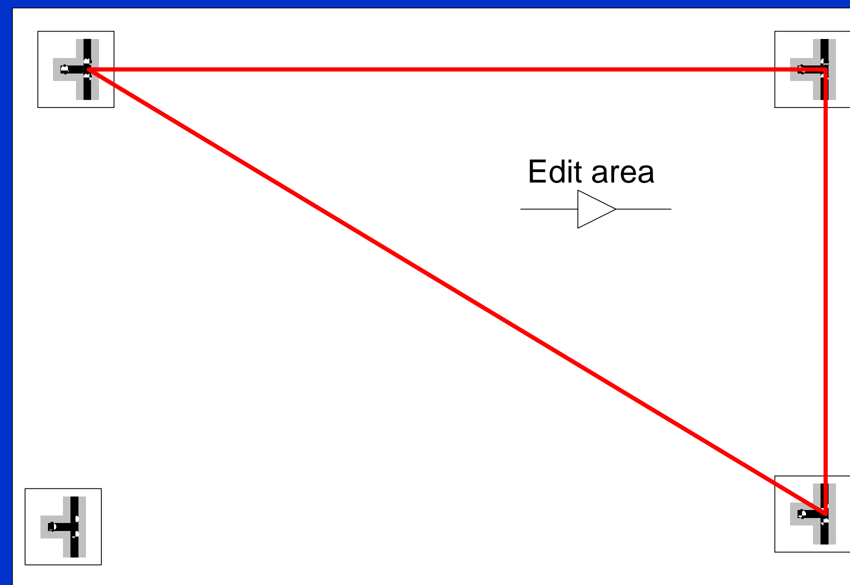
Navigation Features

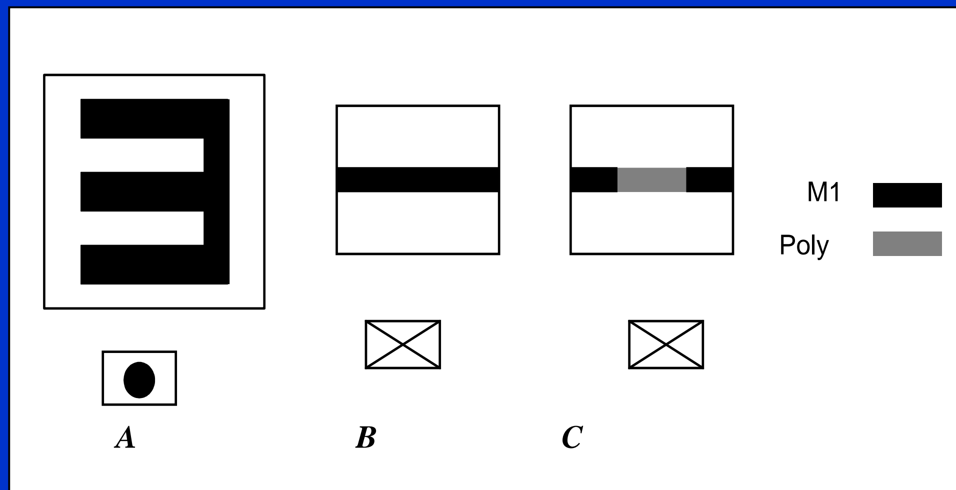
- Fiducial alignment points are the most utilized PDFD features as they are used every request.
  - The larger version referred to as a global fiducial is placed with a 5mm-10mm pitch and provides the 1st level of navigation (sub 1um)
  - The smaller or local fiducial has a much higher pitch typically around 100um and is used to achieve sub 100nm accuracy.
- Both have an array of contacts and diffusion that are locked to a CAD database of the chip.





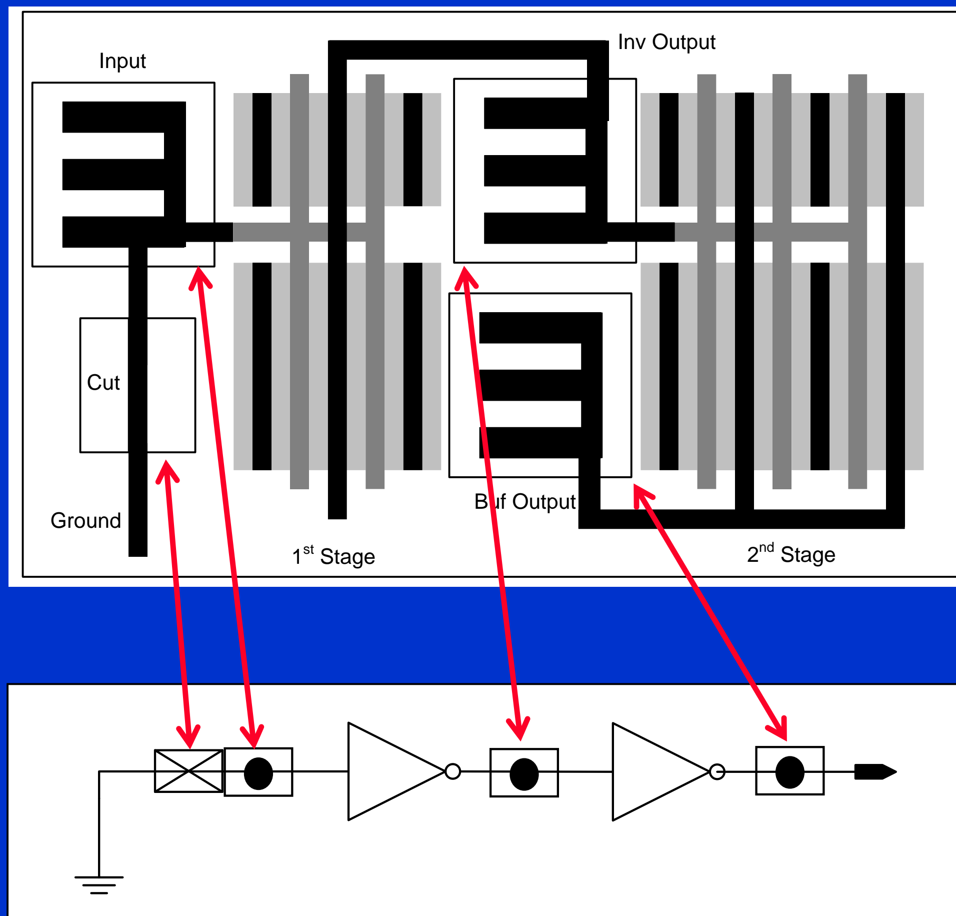
PDFD Building Blocks

- Basic building block features are designed to meet FIB access guidelines.
  - The features are created as cells that can be abutted.
- The Metal 1 connection pad provides guaranteed access to signals for mechanical probing or re-routing.
  - Optimized to keep the FIB via resistance in the 10-20ohm range.
  - Cell area driven by aspect ratio requirements.
  - Metal 1 area maximized to decreases contact resistance.
- Cut cells provide guaranteed access to signals that need to be disconnected from their driver.
  - Metal 1 version typically used for active signals that can not be routed in poly.
  - Poly cut cell was introduced when metal signals migrated from Al to Cu.



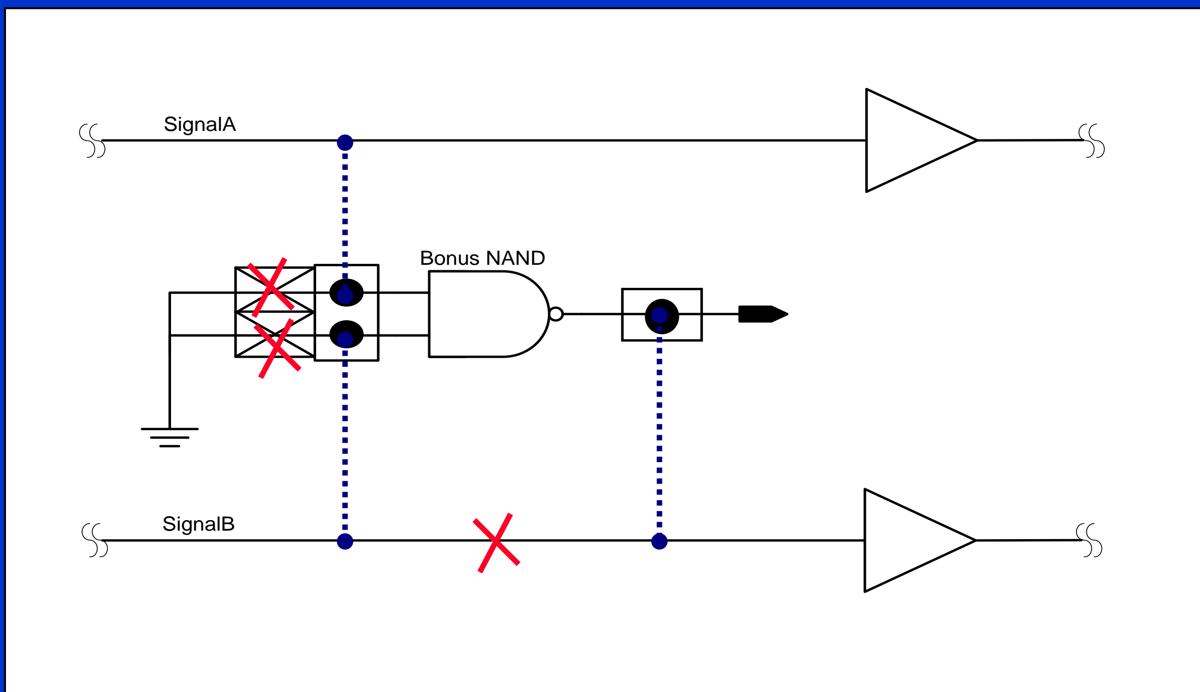
Bonus Combinational and Sequential Cells

- Bonus logic and sequential elements are added to a design to validate functional and speed path bugs.
  - Typical cells include NAND, NOR, Buffer, latch, and Flop.
  - They are also used in dash steppings.
- A cell is chosen from a standard library that has the ability to drive FIB metal ~100-200um.
  - The cell is enlarged so that building block cut and connect cells can be inserted.
  - Input tied to ground and output left floating.



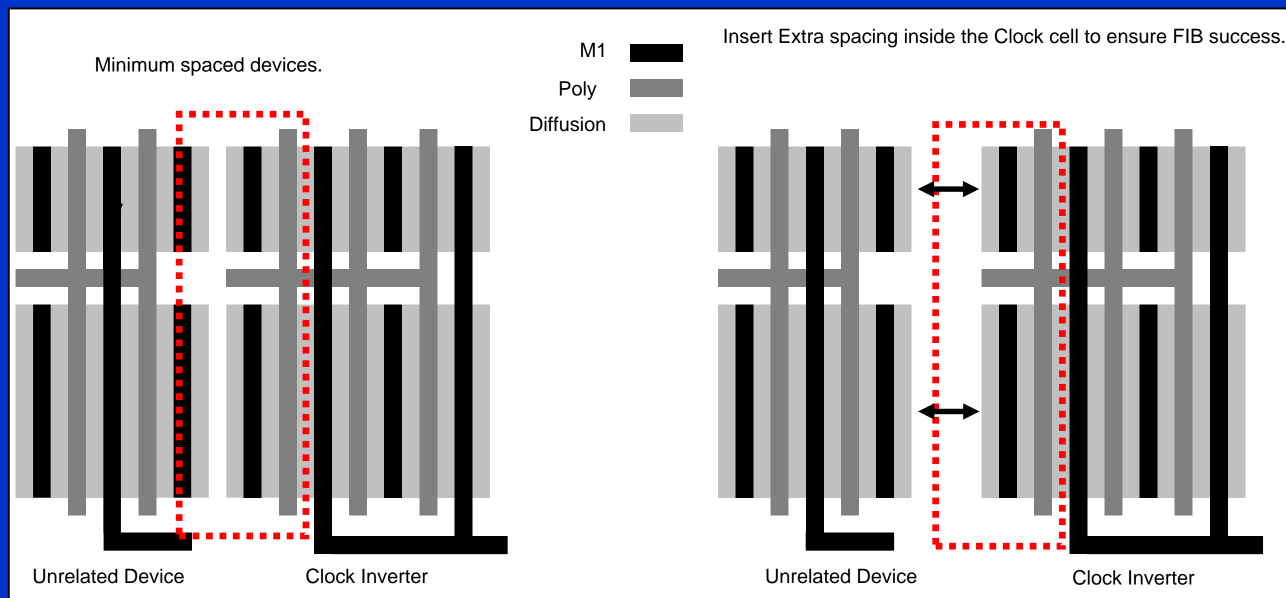
Bonus Combinational and Sequential Cells

- In the below example Signal-B is driving a buffer but should have been the NAND of Signal-A and Signal-B.
- The FIB connects Signal-A and Signal-B which are then routed using FIB metal to the inputs of a bonus NAND. The output of the NAND is connected back to Signal-B before the input to the next stage.
- Once the routing and connecting are complete the FIB will cut Signal-B as shown by the "X" and the FIB cut cells at the NAND's input.



PDFD In Clock Elements

- The ability to alter the timing of clocks is one of the main activities performed during speed path debug.
  - On current generation processes it has become essential to design PDFD features and accessibility into the clock elements themselves.
- To provide FIB access in such small geometries clock elements are designed with increased spacing's between adjacent transistor's.
  - In this case a multi legged clock inverter can be trimmed successfully without damaging the unrelated adjacent device.
- For optical probe access the separation helps minimize cross talk.



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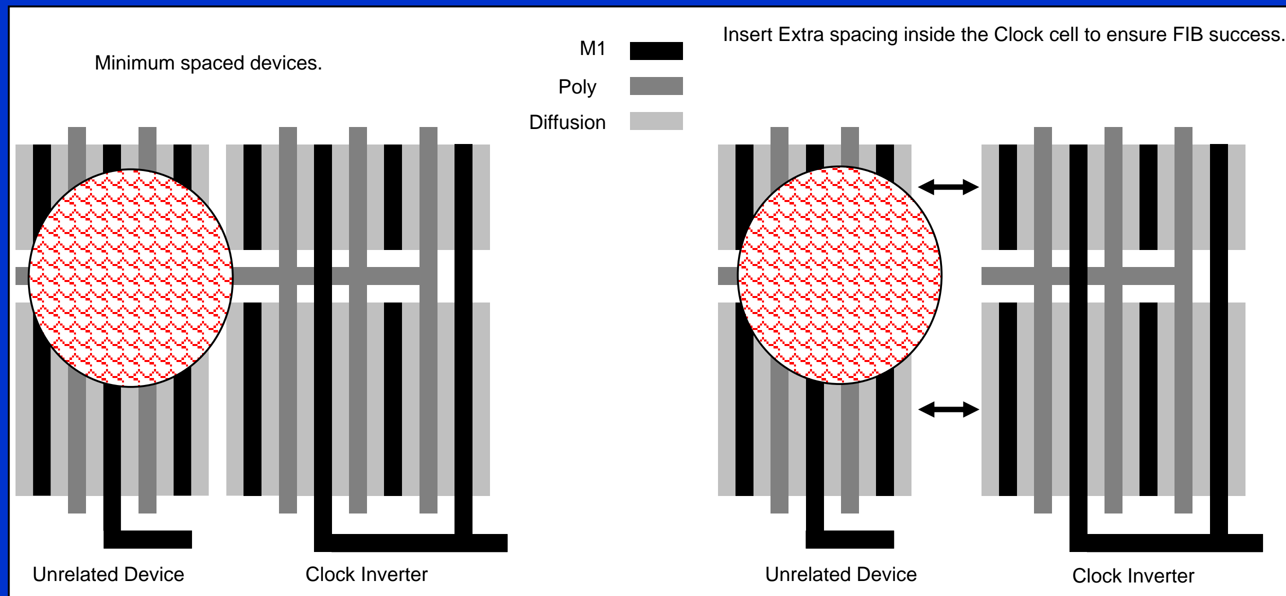
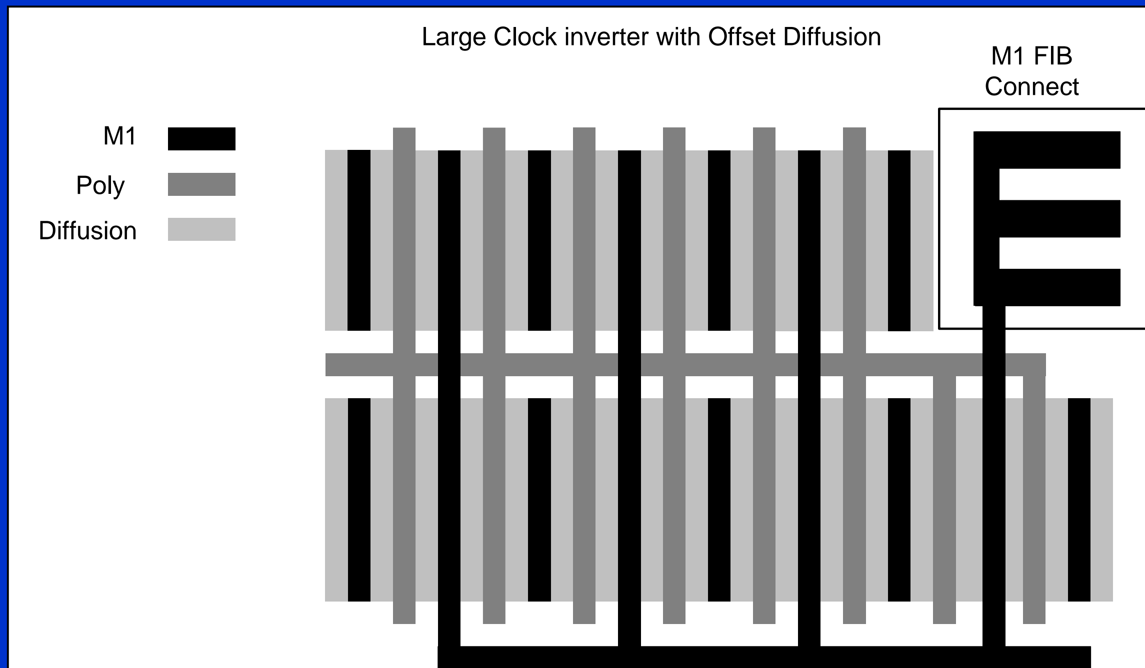


PDFD In Clock Elements

- A second type of PDFD feature designed into clocks are mechanical probe points/FIB access cells.
  - A building block connect cells is placed in opportunistic space.
  - The connection point allows for a FIB load capacitor to be connected thus delaying the signal.
  - It also allows for the output to be routed to another circuit using FIB.



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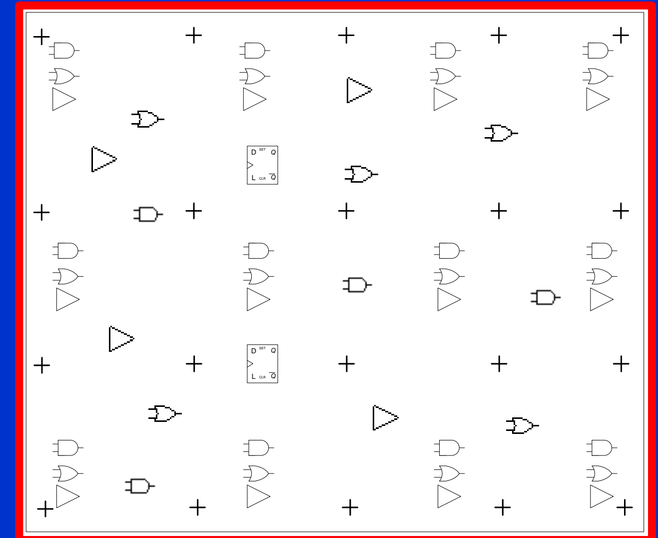
Insertion and Placement

- Historically, each area or functional block owner had to manually insert PDFD features resulting in wasted effort and inconsistent implementation.
- Today the use of automated scripts and customized flows are utilized.
  - The scripts are developed by central DA teams that incorporates them into the standard design flows (DFM).
  - The scripts cab be customized to meet the individual product's needs for cell types and pitches.
  - A mix of pre and post P&R can be used to meet coverage needs.

- The bonus cell pitch is determined by FIB routing technology and RC requirement.
- The pitch for the fiducial is based on required FIB and probe navigation accuracy.



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PDFD Utilization for Product Steppings

- The production of a IC's requires multiple iterations or stepping's.
  - A full stepping requires a complete set of masks and is very expensive.
  - Products use dash or sub stepping's which requires only new backend masks (typically metal 1 and above).
    - This reduces time to market as product can be held in the FAB at a specific layer until the new backend masks are generated.
  - For simplistic timing or electrical issues a dash stepping typically can be performed at metal layers only since they do not require additional transistors.
  - This is not the case when a product has logic or complex issues that requires modifying multiple signals through additional combinational and/or sequential elements.

- The implementation of strategically placed PDFD features allows these type of logic or complex bugs to be fixed in a dash stepping.

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Conclusion

- PDFD implementation in IC's is a critical part of the overall DFD (design for debug) methodology employed by product design teams today.
- Placing design access hooks into the silicon and specifically on critical nodes and cell types has resulted in higher productivity and capability for physical debug equipment.
- The utilization of PDFD results in fewer stepping's and faster time-to-market.
- Optimal placement coverage of PDFD will become even more critical as the semiconductor industry ramps up on 22nm process technology and beyond.
- Insertion of PDFD is performed using standard DFM insertion tools and flows.

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Q & A