Circuit and PD Design Challenges at the 14nm Technology Node

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Session: Advanced Technologies and Design for Manufacturability

ISPD 2013

IBM Systems and Technology Group

Outline

- Introduction
- Classical CMOS Scaling: The End of the Road
- New Device Structures
  - What do these structures mean for circuit designers?
- Wire Interconnects
- Reliability
- Conclusions

Introduction

- 14nm technology will pose many challenges, for many types of designs…
- This talk will focus on:
  - High-frequency digital CMOS design, ie for high-performance microprocessors
  - New PD issues
  - Circuits, wires, reliability, variability…
- Issues related to manufacturing, yield, etc: not covered here
- Why is 14nm so difficult?
- What will designers be facing at the 14nm technology node?

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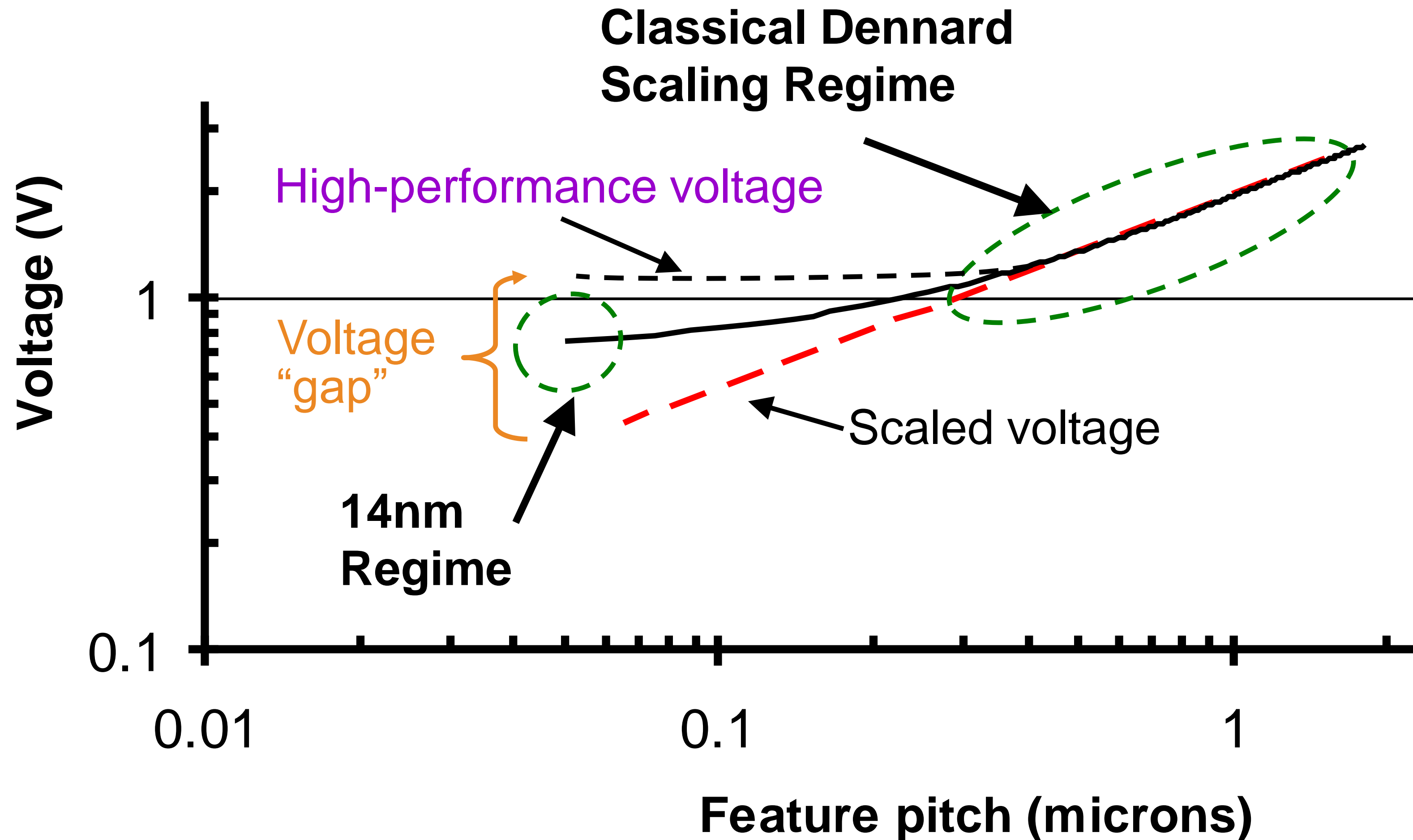
CMOS Supply Voltage Scaling Difficulties

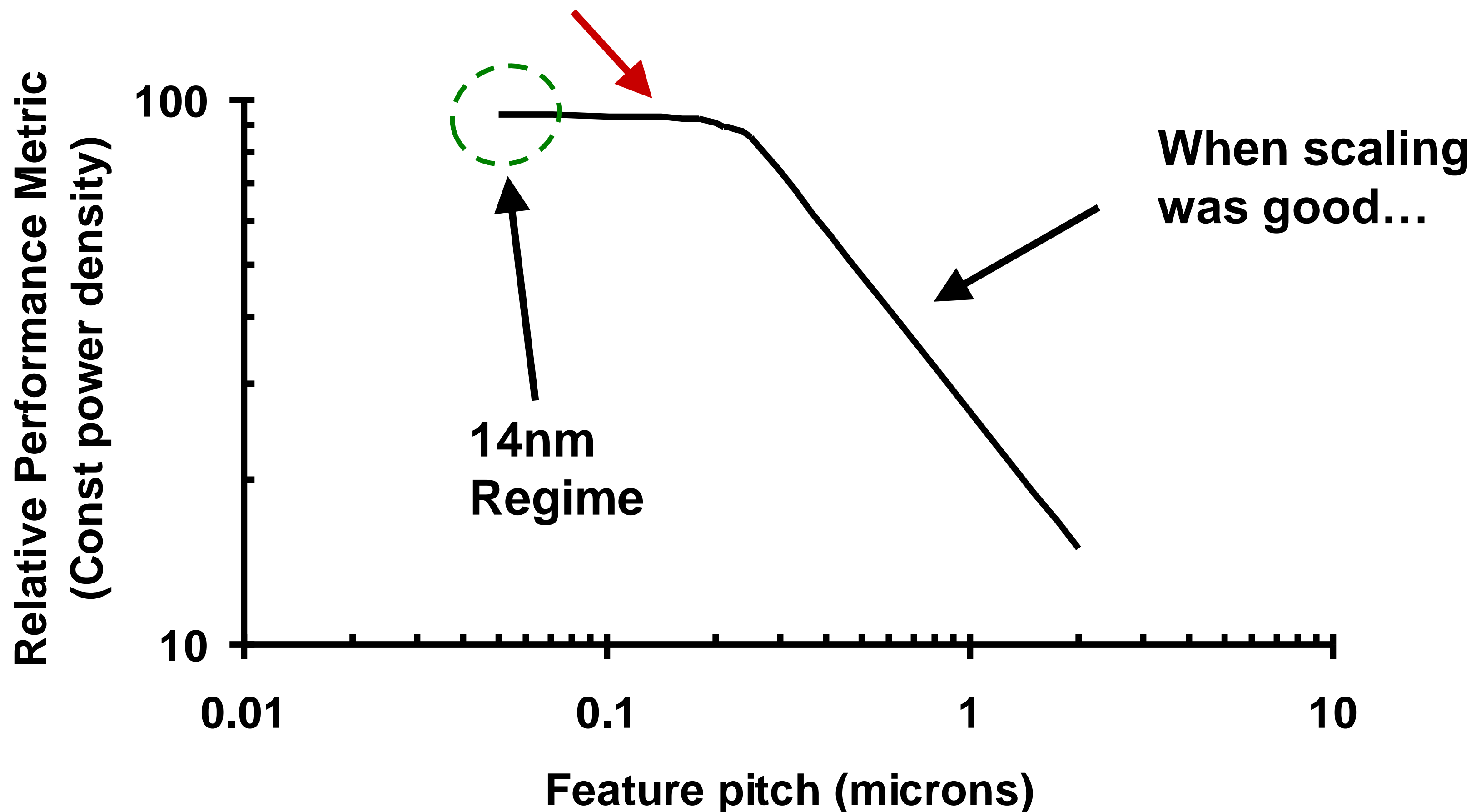


Voltage Scaling Difficulties

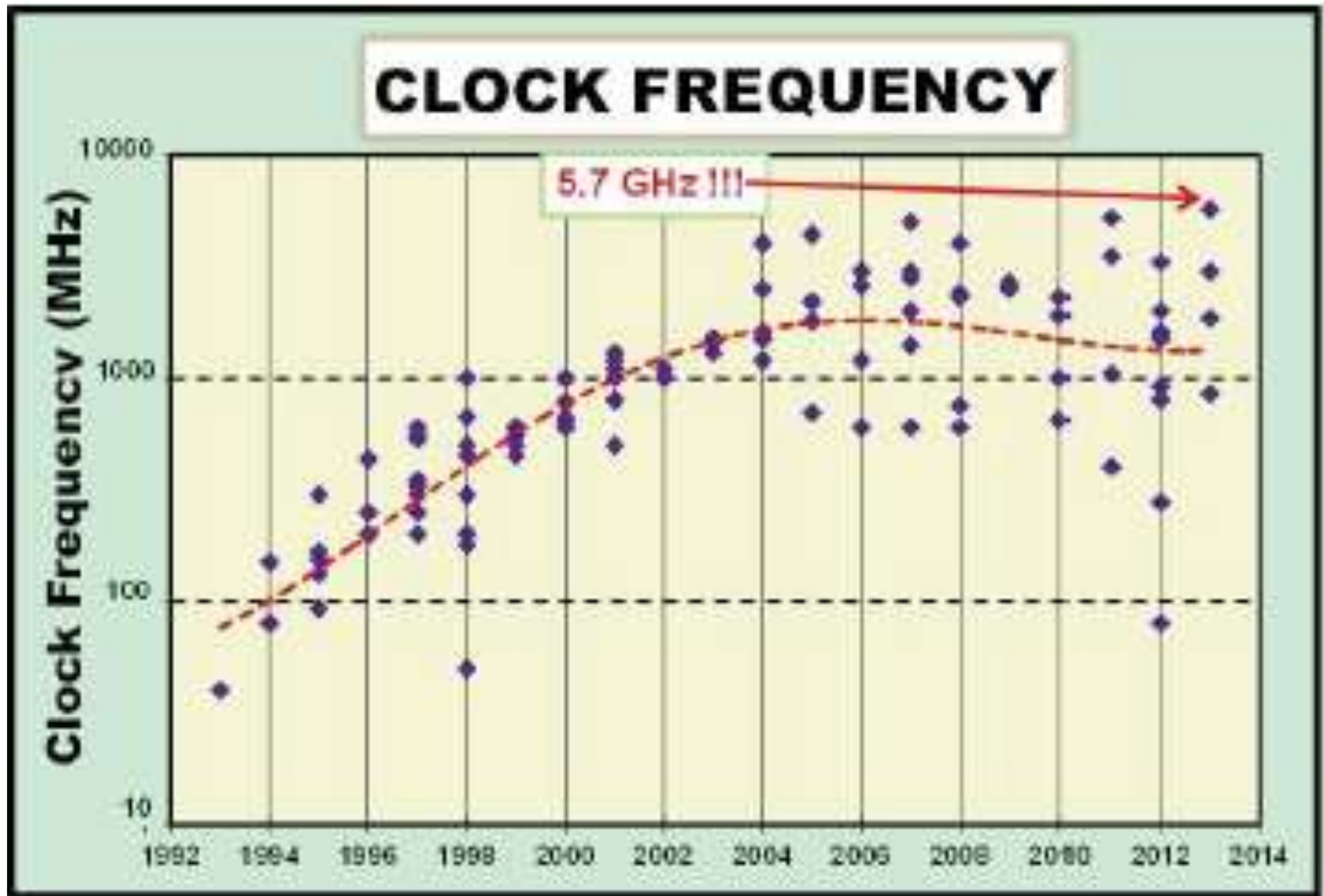
- "The End is Near"…ish
  - Maybe not the end, but things are sure getting tough…
- Voltage scaling for high-performance designs is limited
  - Limited by leakage issues: can't reduce threshold voltages
    - Need steeper sub-threshold slopes…
  - Limited by variability, esp VT variability
    - Need to minimize random dopant fluctuations (RDF)…
  - Limited by gate oxide thickness
    - Some relief from high-K materials (postpones the problem for a couple of generations)
- Limited voltage scaling + decreasing feature sizes
  => Increasing electric fields
  - New device structures needed (short channel control)
  - Reliability challenges (devices and wires)

CMOS Power-performance Scaling

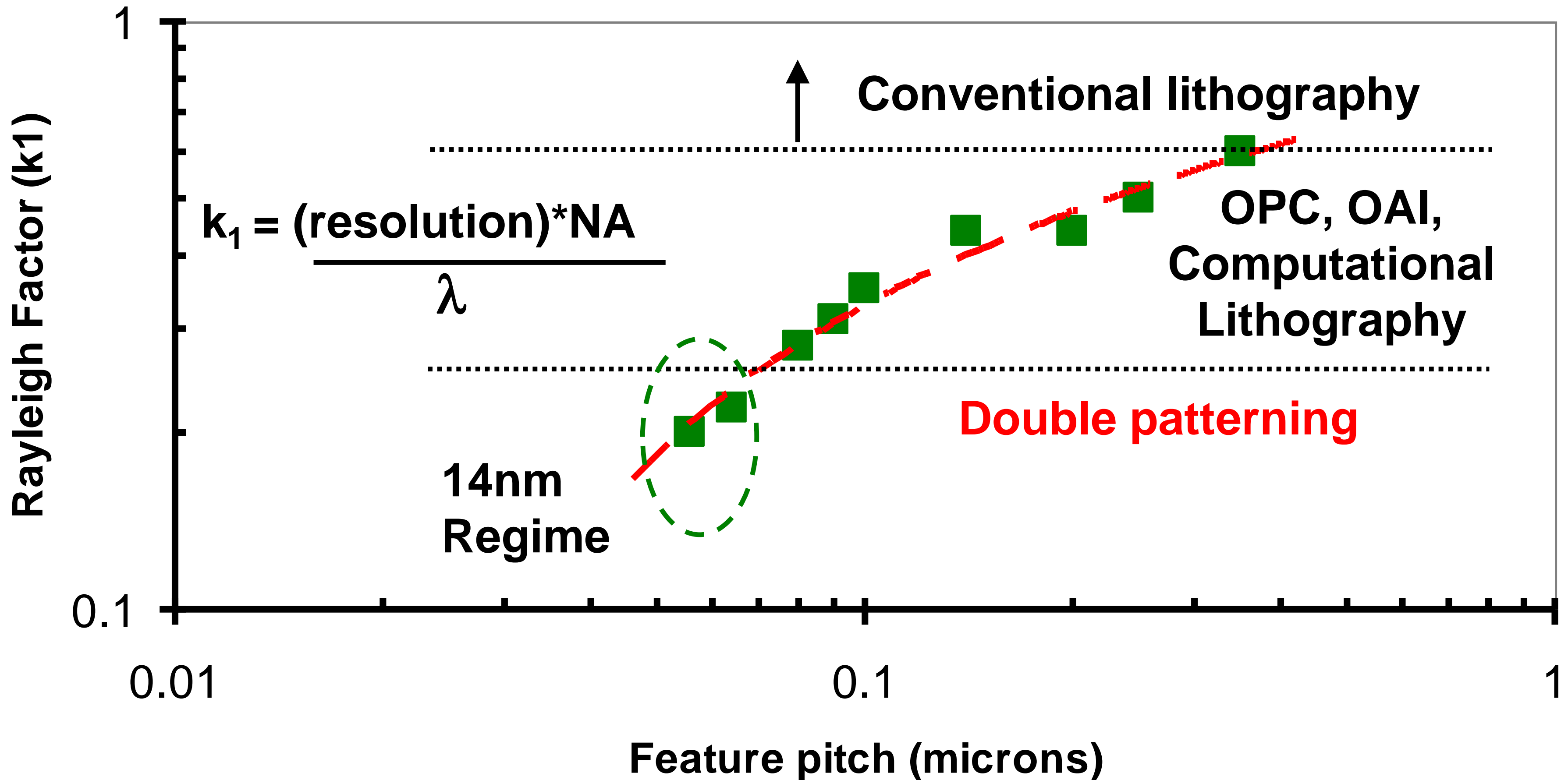
Where this curve is flat, can only improve chip freq by:
a) pushing core/chip to higher power density (tough these days…)
b) design power efficiency improvements (low-hanging fruit all gone)



From IEEE ISSCC 2013 Supplement:



Lithography Scaling



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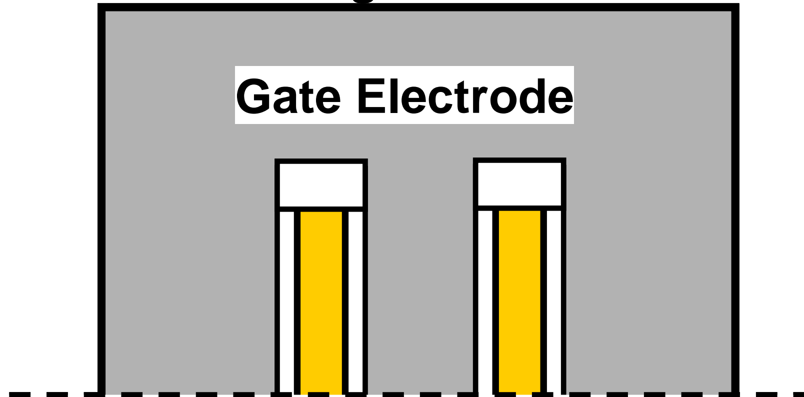
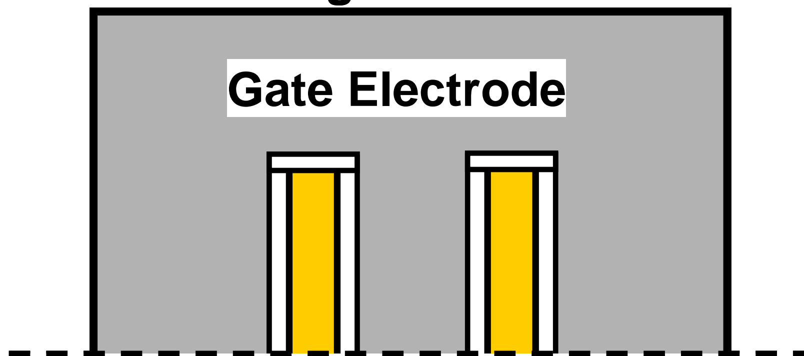
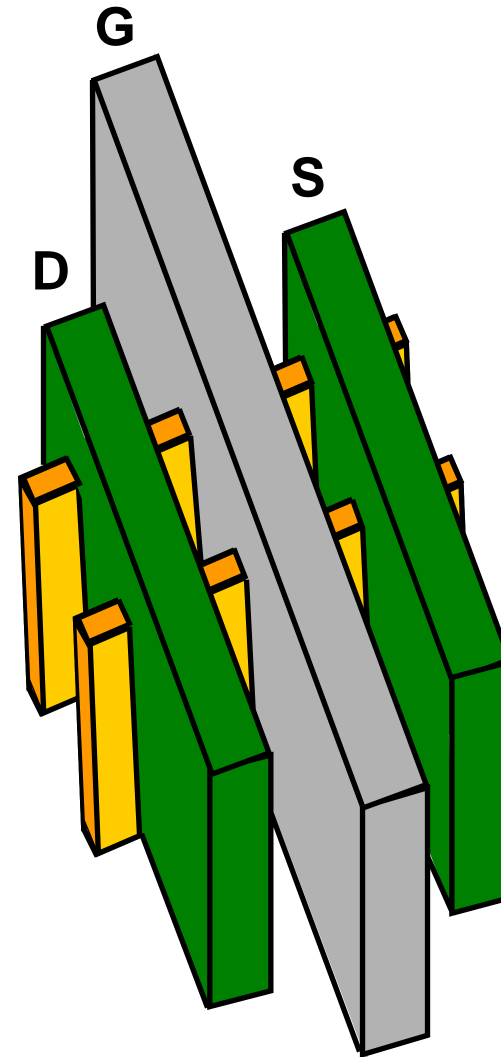
Multigate/FinFET Devices



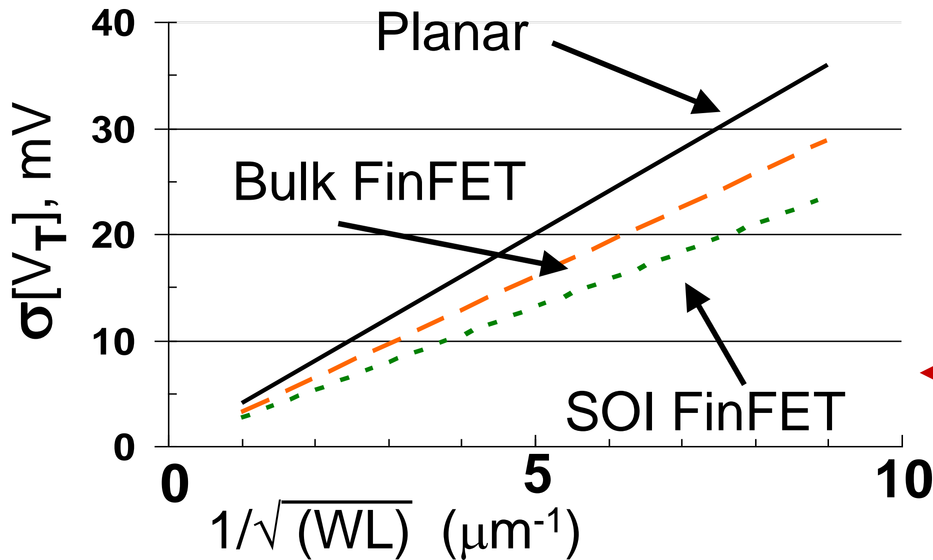




Trigate/FinFET Devices

- The good news:
  - Expect improved subthreshold slope
  - Expect improved RDF-induced variability
  - Above could help to enable lower voltage operation
- What designers have to worry about:
  - New sources of variability
    - Fin width will have a significant impact on VT: Expect global, local and random effects/correlations
    - Fin height -> width variability: can't amortize over wider fingers…
  - Some of the same old variability issues (continuing to worsen…)
    - Gate line-edge roughening (LER), channel length variability
    - May be exacerbated by 3D effects
  - "Quantization" of device widths
    - Can only have integer numbers of fins
  - Changes in device parasitic R, C compared to usual expectations
    - G-S cap (Miller cap), S, D contact resistance

Trigate/FinFET Devices: Variability

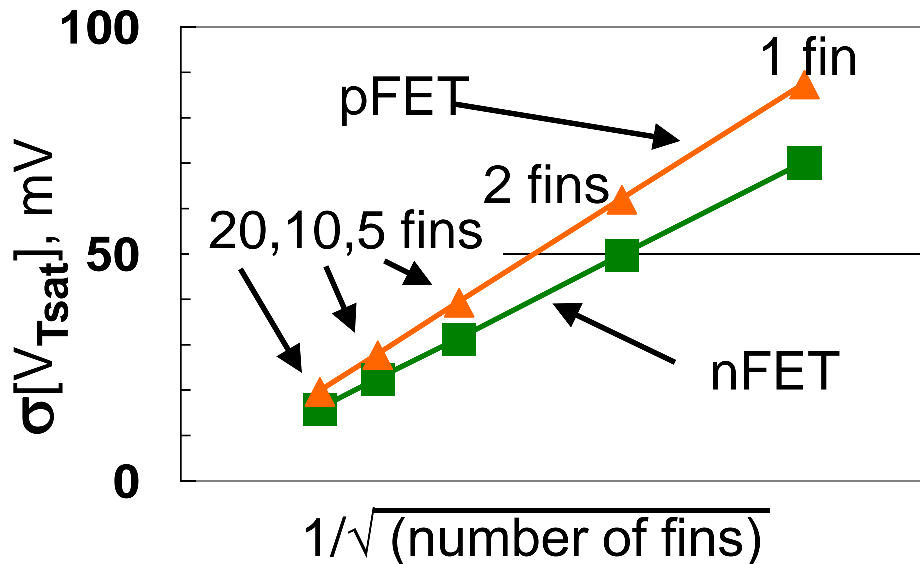


Reduced RDF-related VT variability for FINFETs

(~25-50% depending on design)

eg. M. Jurczak et al,

Proc. 2009 IEEE Int, SOI Conf.

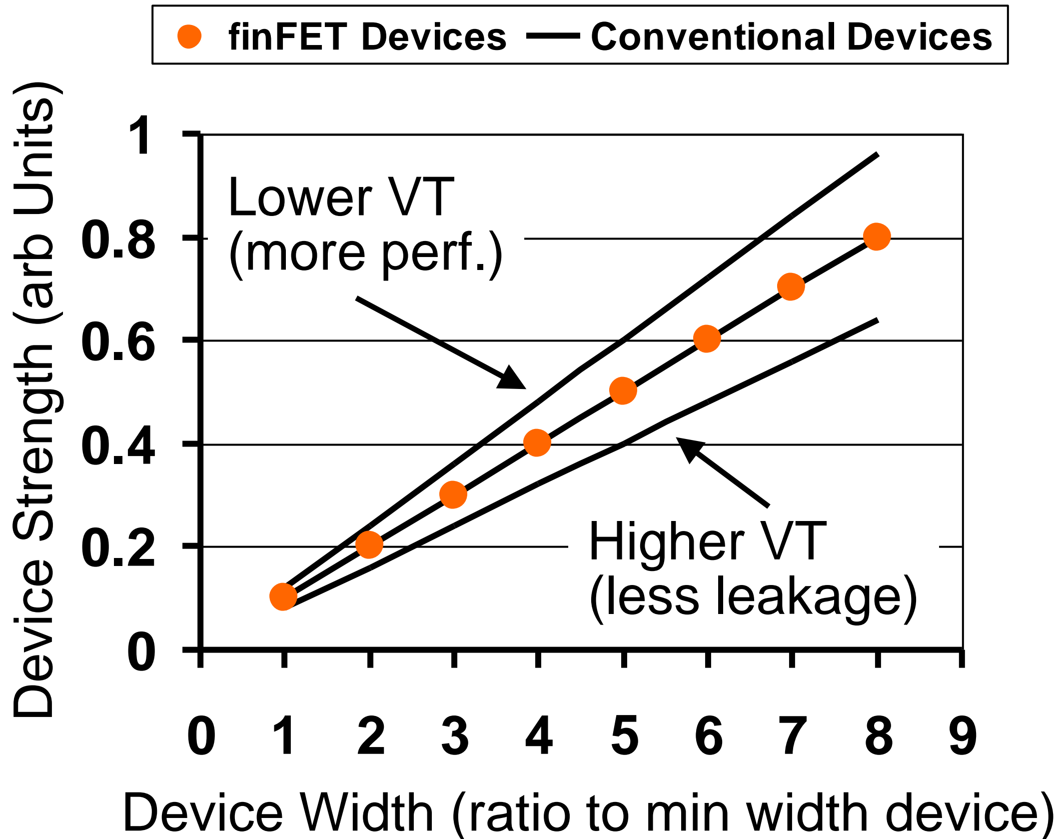


LER-related VT variability for FINFETs

eg. E. Baravelli et al, IEEE T. Nanotechnol. 7, p. 291 (2008).

Warning: considerable spread in reported literature: your mileage may vary

Trigate/FinFET Devices: Quantization



Example: min size finFET INV

Can have p:n ratio = 1, 0.5, 2 (nothing in between)

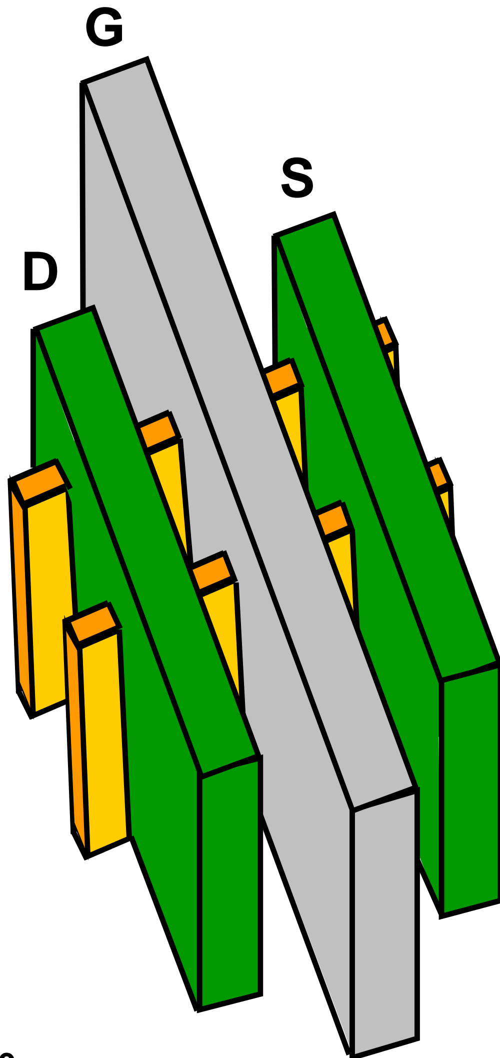
Also, even a “wide” device will always be just a collection of very narrow devices…

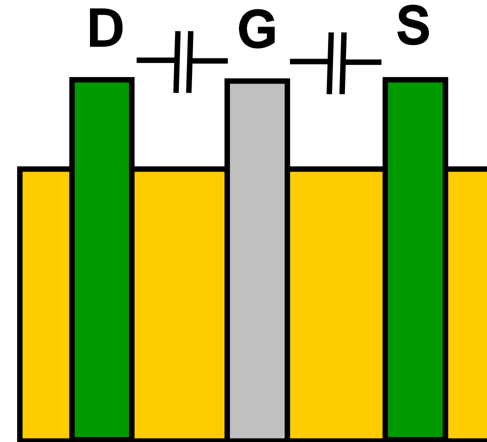
Plus, expect difficulty to create multiple VT offerings in a fully depleted device scenario

- Likely to create most difficulty for SRAM, register file designs
- Also small feedback devices, keepers, etc.
- Issue for any device tuner, other tools expecting continuous width ranges

Trigate/FinFET Devices: Parasitics

- Resistance in contacts to fins might be tricky: assume it can be handled by device engineers! What about G-S cap?

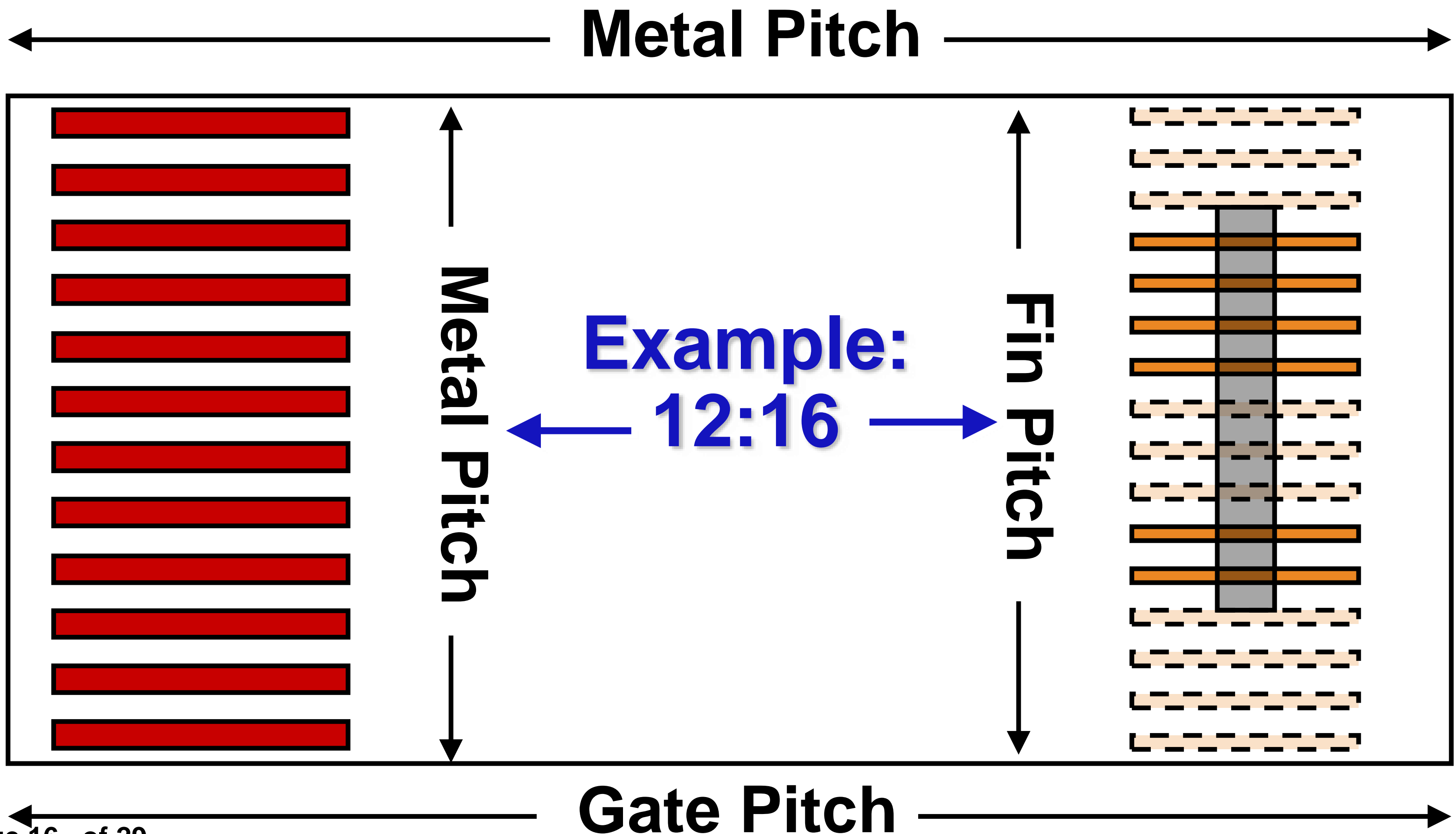




- Expect increase in Cgs compared to planar structures
- Details will depend on fin vs trigate, fin pitch, height, thickness, etc.
- Might have to watch out for certain types of noise issues
- Might decrease static timing accuracy

Trigate/FinFET Devices: PD Issues

- Sea-of-fins technology is attractive: offers tightest fin pitch
- Additional constraint on PD cell image
  - Vertical: **Fin**, metal pitches ⇔ Horizontal: gate, metal pitches



FinFET PD Implications

- Higher fins -> more current drive per unit area
  - But technology minimum device width grows
  - Quantization issues tougher to deal with
- Finer fin pitch -> more current drive per unit area
  - Can trade off shorter fin height with finer fin pitch
  - Sea-of-fins constraints, other litho-related constraints
- Net: stronger technology <-> PD interaction
  - Library cell definition likely to be dependent on technology fin pitch
  - Will need to find gear ratios (metal pitch vs fin pitch) that work well together

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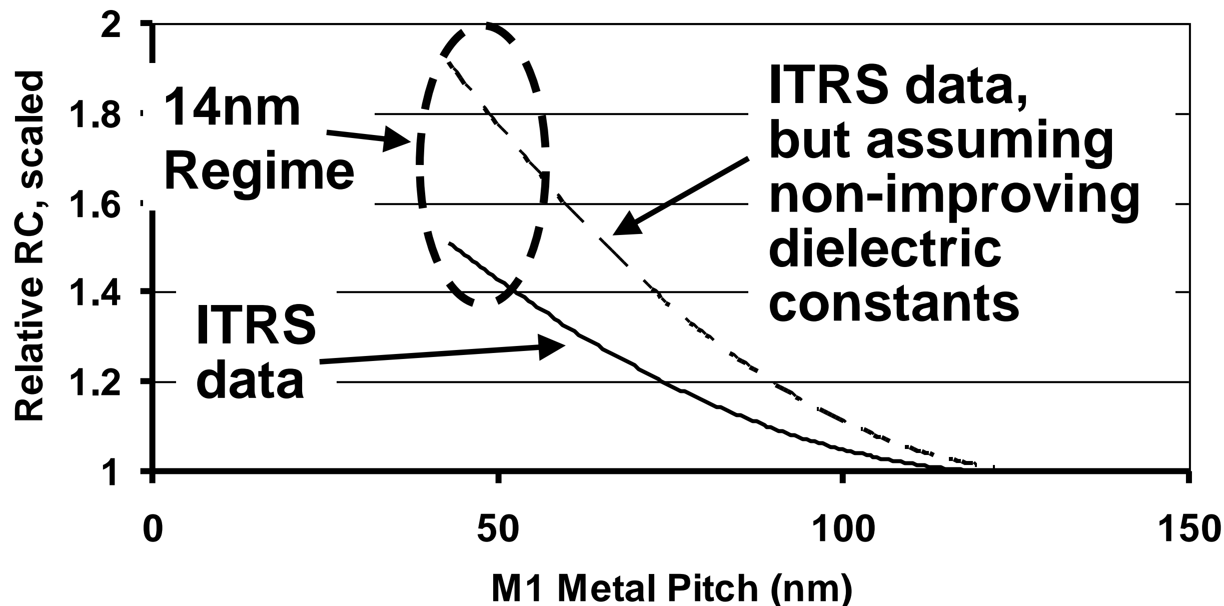
Wire Interconnect Scaling (or lack thereof…)

- Assume all logic scales with litho shrink factor
  - Wire lengths then also would scale
  - Best case scenario: RC stays constant ("perfect scaling")
    - This is already painful, chip area generally hasn't been shrinking!
- Data below shows expectations that wire delays will grow significantly, even in scaled designs.

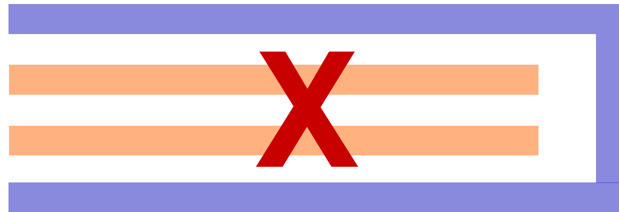


Wire Scaling Implications

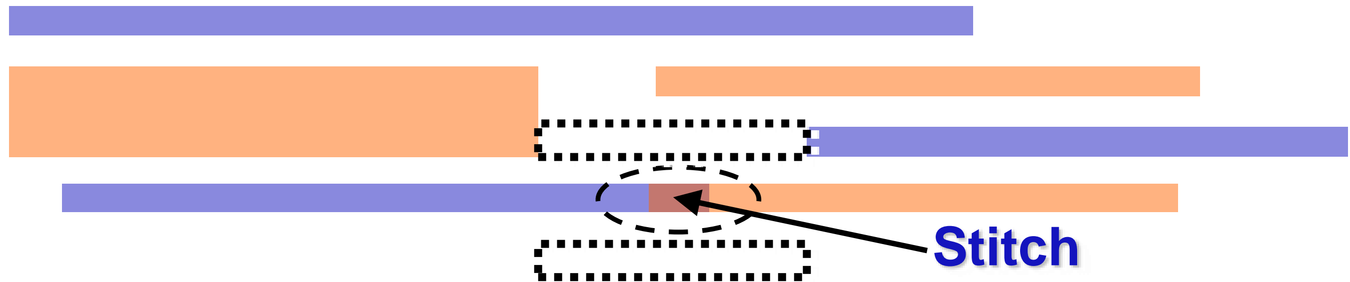
- High-performance designs will not be able to tolerate such large RC increases
  - Will need coarser-pitch, faster wires (ie non-scaled wires)
- But also need fine-pitched wires to leverage technology density
- Result: push for more wiring interconnect layers (coarse-pitch)
  - Will still need some number of fine-pitch layers as well for short-run local connections
- Improved DA tools (routers) needed
  - Optimize wire plane usage to limit technology complexity
  - Negotiate through special design rules for the finest levels
  - Via optimization, especially at driver end
  - Tricky performance vs wireability tradeoffs
  - Many wires will need “special” treatment
    - Increase width, push higher, add buffers, etc.

14nm Wires: PD Implications

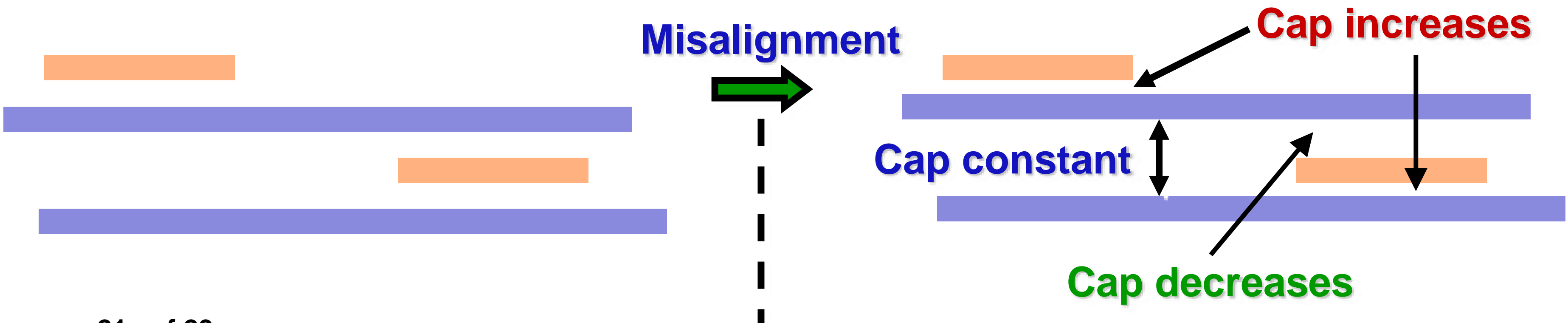
- Complications from double-patterning lithography!



- High-performance fat wires lead to local disruption…



- Need to understand coloring for proper analysis…



14nm Wires: DPL

- How to make sure designs can be colored properly?
  - Rules to guarantee colorability complicated, non-local
  - Coloring solution may be subject to external factors…
- Need color-aware analysis for highest accuracy
  - Correlated capacitance shifts
- Solution: color-aware toolset & design methodology
  - Build in coloring info as design is constructed
  - Correct, DPL-aware solutions, by construction

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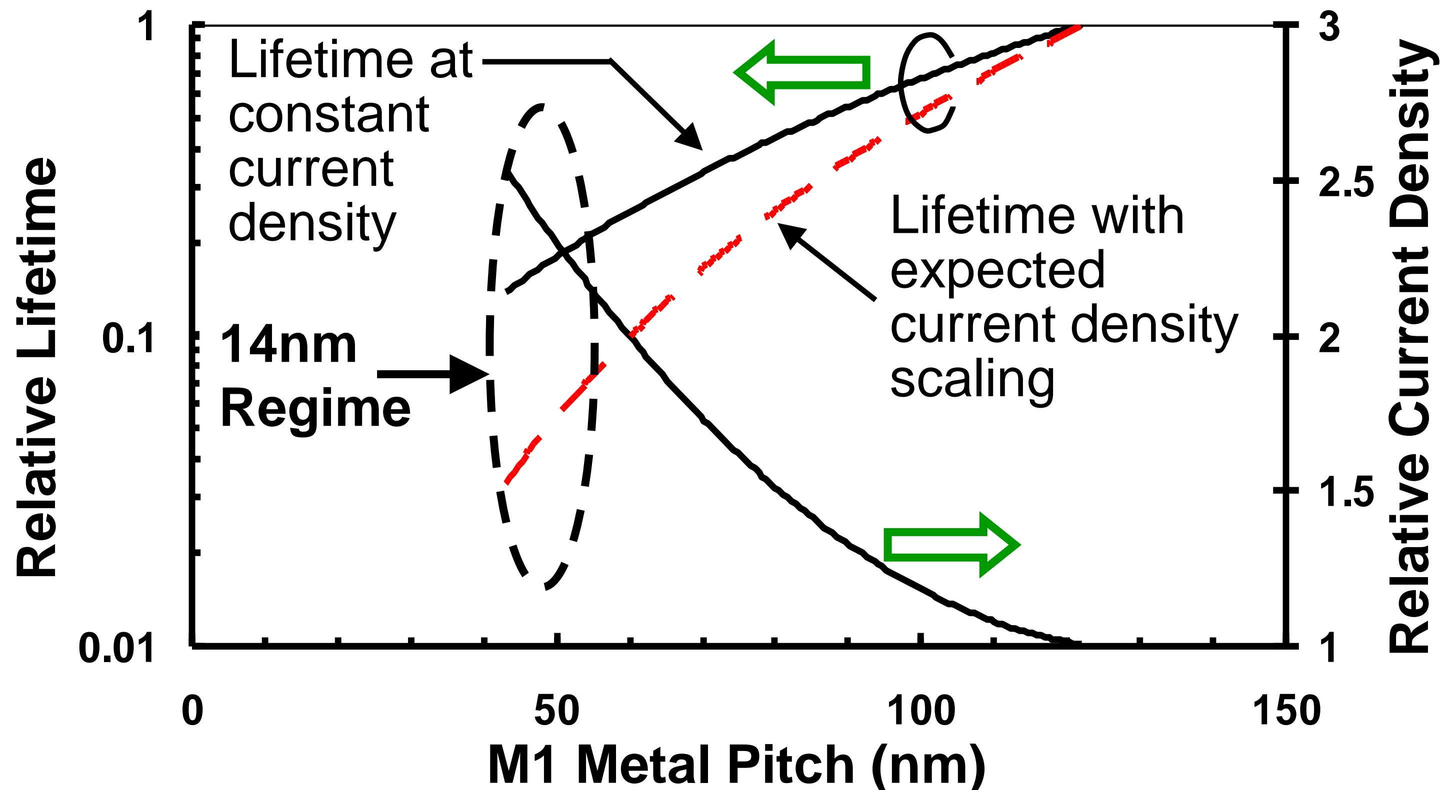
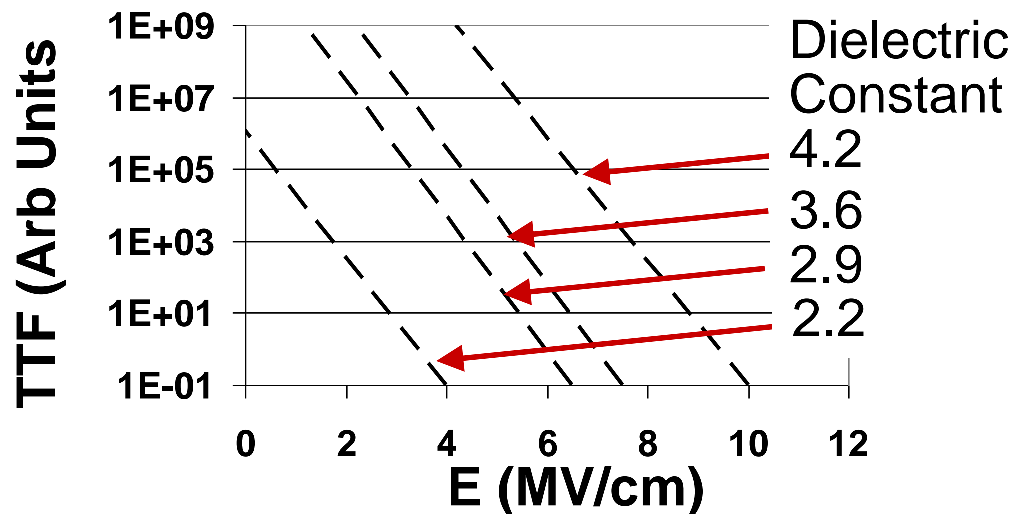
Interconnect Reliability

- Reliability will become a significant focus item for designers in 14nm technology
- Parameters below taken from ITRS, plotted WRT 2009 data
  - Assume constant voltage, const frequency for simplicity



Interconnect Reliability

- New materials likely needed for the finest-pitch planes
  - Resistance increases likely
  - More impetus to push signal wires higher in the stack
- TDDB concerns likely to push technology to higher K materials
  - Higher dielectric constant materials tend to have better reliability
  - Wire cap increase drives higher power, increased RC
  - Concern again for finest-pitch planes…



Ogawa et al,

2003 IRPS

- LER, defect-narrowing likely to exacerbate EM concerns

Interconnect Reliability: Implications

- Will need efficient design tool solutions for robust reliability
  - Likely many elements with current pushing close to reliability limits
  - May need detailed understanding of local switching factors
- Local thermal effects likely significant for high-frequency logic
  - IR heating by currents in fine wires
  - EM effects very sensitively dependent on temperature
  - What happens when hot wires are placed in close proximity?
    - Answer: they get even hotter (and they heat up the surroundings)
  - Need design tools to help avoid bad thermal situations
  - Need thermal analysis tools to detect problematic local situations
- Increased overhead from error checking & recovery expected
  - For high-reliability systems, checking alone is not enough!
  - Need to be able to recover from hard errors
  - Ability to take processor cores offline gracefully
    - Replace with spare core?

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Conclusions

- Breakdown in scaling is pushing technology in new directions
  - Limited voltage scaling for high-performance chips
    - Power/power-density limited performance
  - More constraints from lithography (DPL)
- FinFET device structures => new circuit/PD design challenges
  - VT variability still likely to be a challenge…
  - Constraints from fin pitch, width quantization
- Biggest challenges for high-performance designs: wires
  - Non-scaling RC
  - Reliability
  - DPL makes everything tougher…
- Circuit/system-level check/recovery features will need extra emphasis for high-reliability systems

Acknowledgements

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