

A Structured Routing Architecture and its Design Methodology Suitable for High-throughput Electron Beam Direct Writing with Character Projection

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Agenda

- ❑ **Introduction**
- ❑ **Structured Routing Architecture and Stencil Design**
- ❑ **SRA Design Methodology**
- ❑ **Experimental results**
- ❑ **Conclusion**

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Introduction

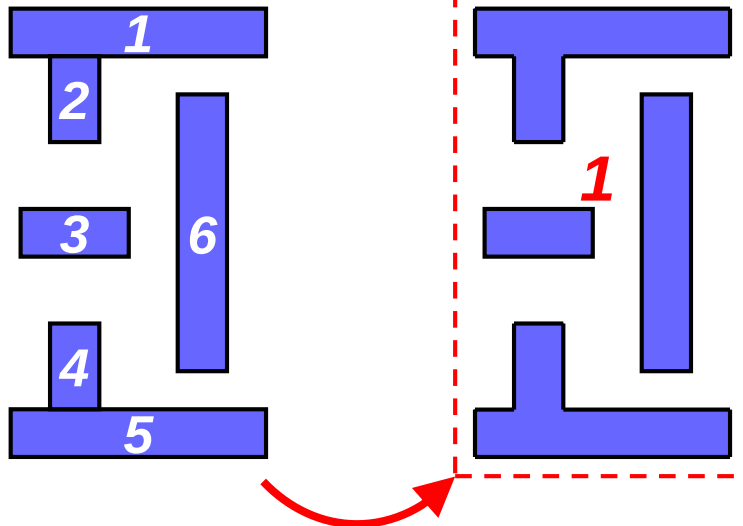
- ❑ **Electron-Beam Direct Writing (EBDW)**
 - ❑ **Low-cost** 'maskless' exposure solution
 - ← Mask cost explosion in high-resolution lithography
 - ❑ **Low exposure throughput**
 - ← One figure per one EB shot (dot, rectangle, ..)
 - ❑ **Limited applications**: low-volume products, test chips, ...

- ❑ **EBDW with Character Projection (CP) technique**
 - ❑ Promising **high-throughput EBDW** in 14nm and beyond
 - ❑ Shooting **multiple figures** at once as a **character**
 - ❑ **Characters** = "Frequently-appeared layout patterns"
 - Prepared on **character stencil**
 - ❑ Higher CP throughput = More figures in 1 EB shot
 - More character varieties required!

Overview of Character Projection (CP) EBDW

Shot count comparison

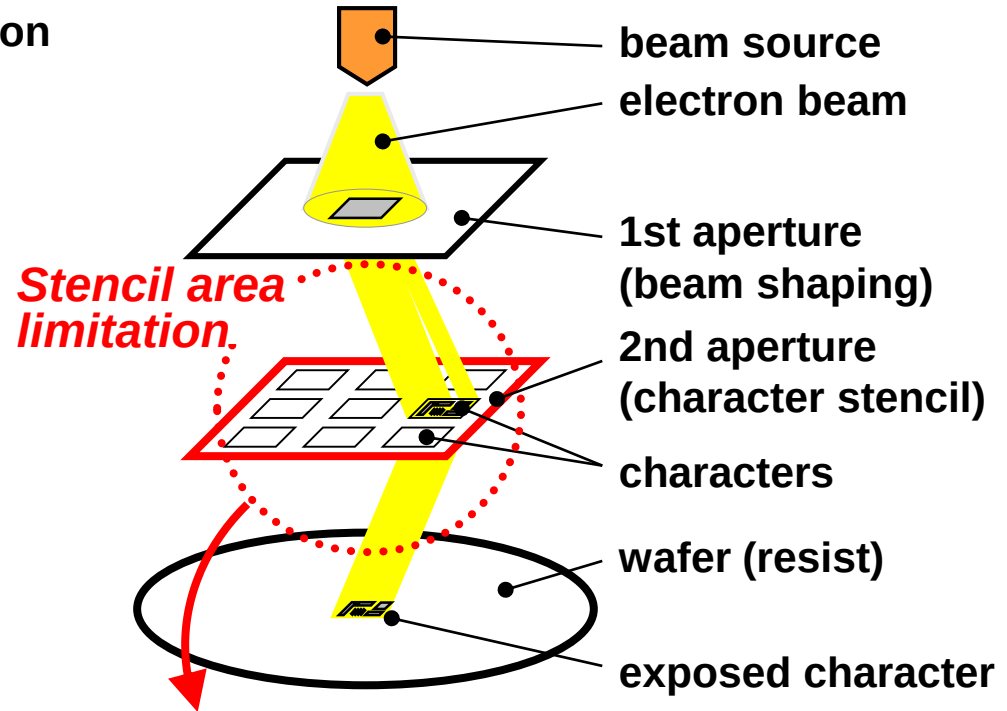
Variable Shaped Beam (VSB) Character Projection (CP)



6x faster throughput

CP efficiency (E_{CP}) = 6.0

CP EBDW equipment



Limited character variety (number)

Challenges toward the practical CP EBDW use:

Shot# reduction: >1000 G-shot/wafer (VSB) → ~100 Gs/w (= $E_{CP} > 10$)

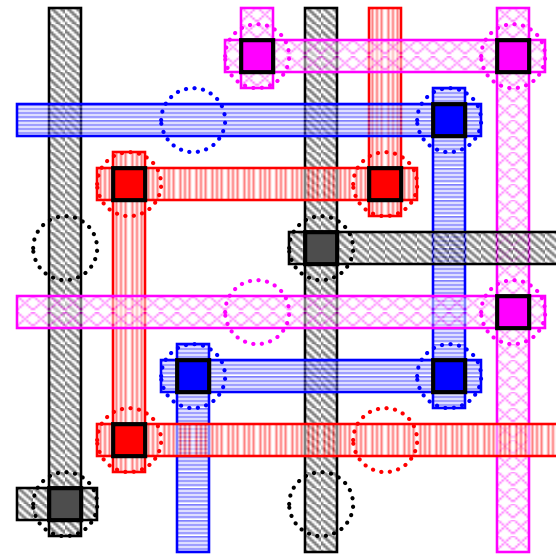
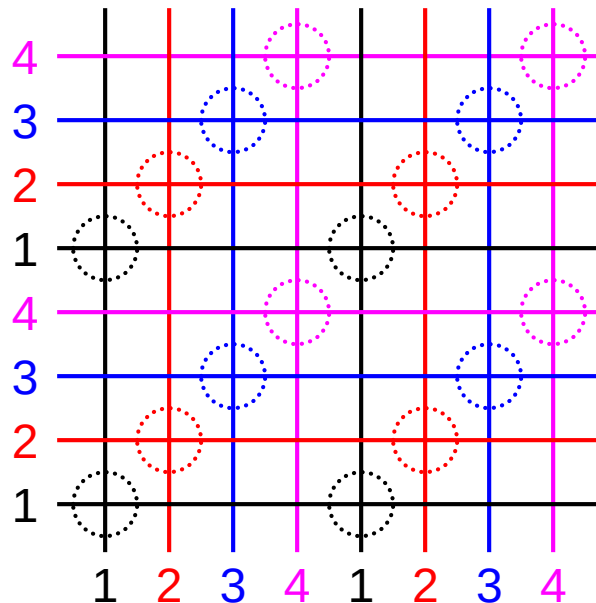
Char# suppression: covering **any layout patterns** with limited characters

Agenda

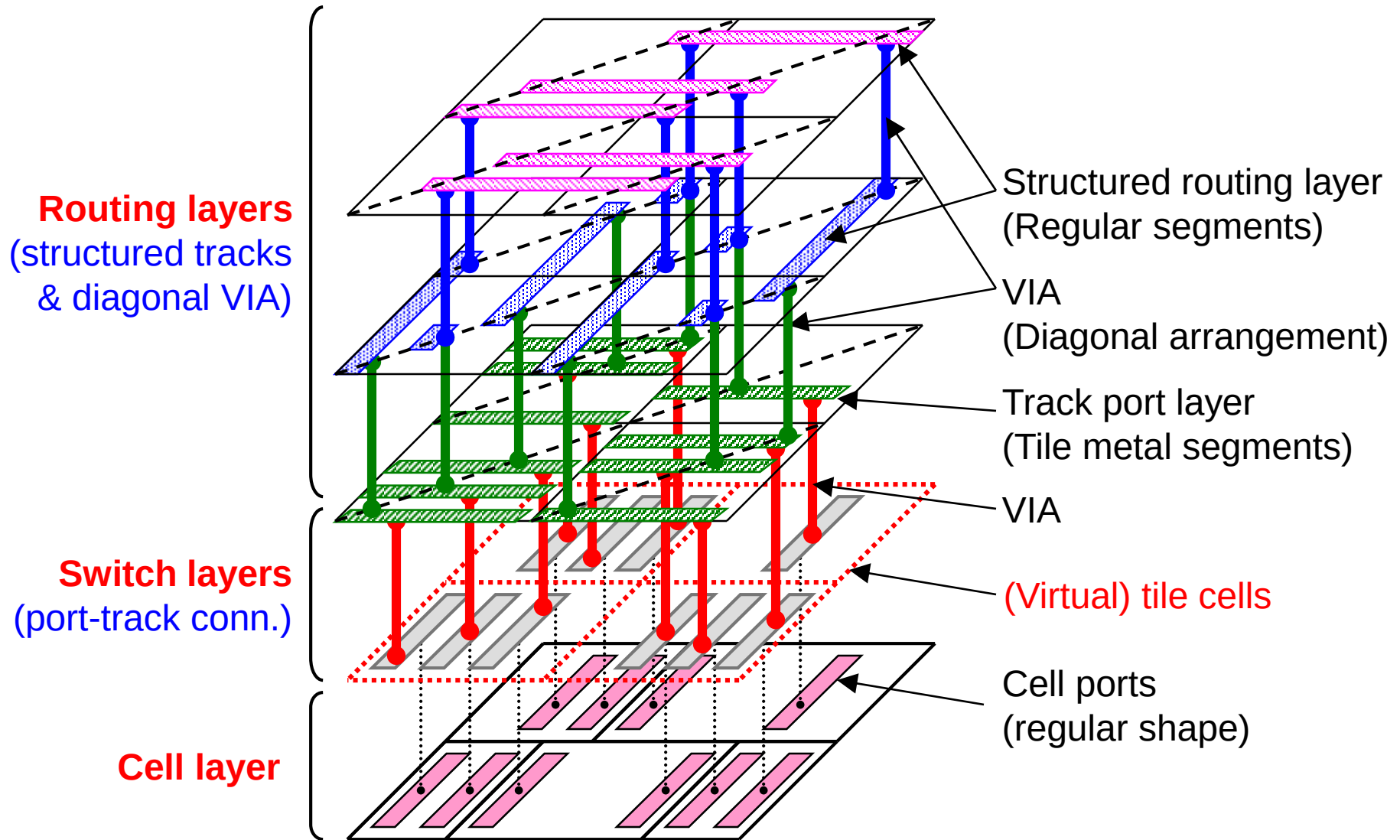
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Structured Routing Architecture (SRA)

- **Purpose:** to reduce VIA/metal CP character variations while increasing the figure# in each EB shot
- **Periodic track grouping, and restricted track exchange**
 - VIA placement on diagonal lines → Less VIA characters
 - Limited metal segment shapes → Less metal characters
- **Limitations in routing flexibility & cell port accessibility**
→ **Track-assign-first flow / switch layer insertion**



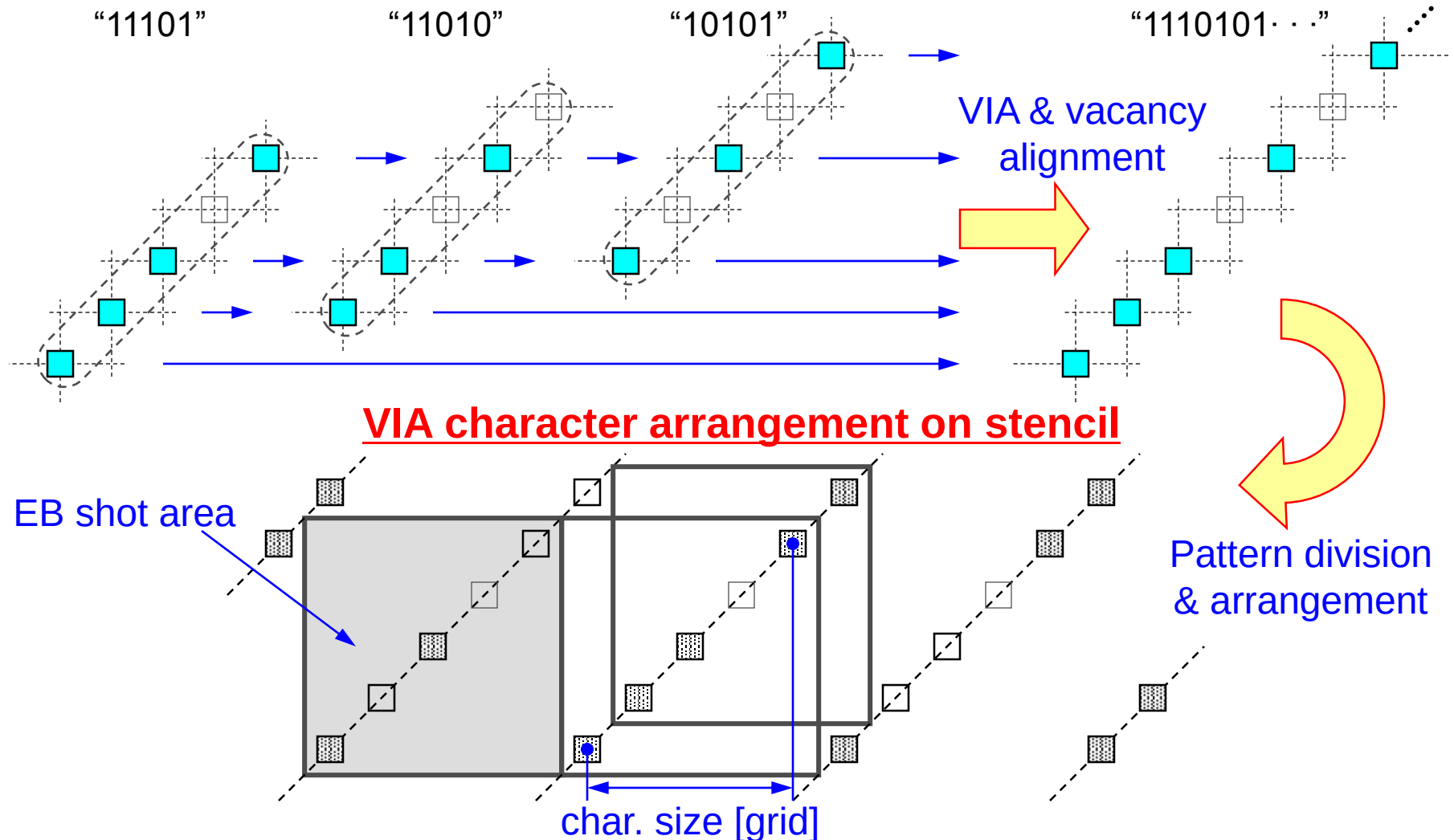
Metal and VIA Layer Usage in SRA



VIA Array Characters and Stencil Design

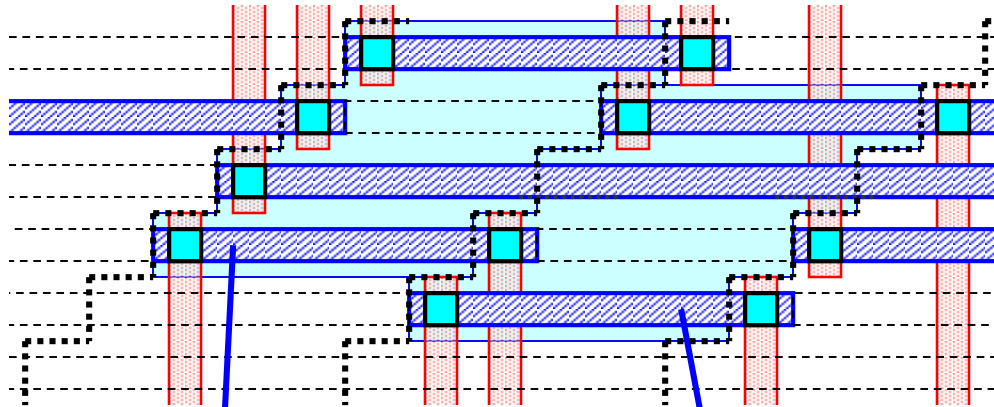
Diagonal VIA array characters (binary codes)

Overlapped pattern

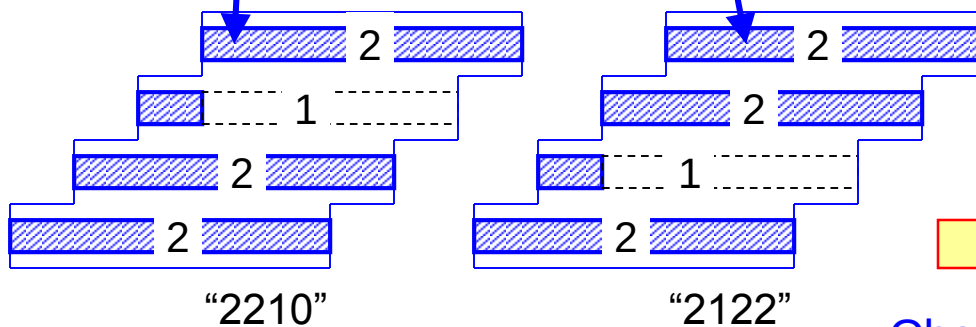


Metal Segment Characters and Stencil Design

Metal wire layout with diagonal VIA



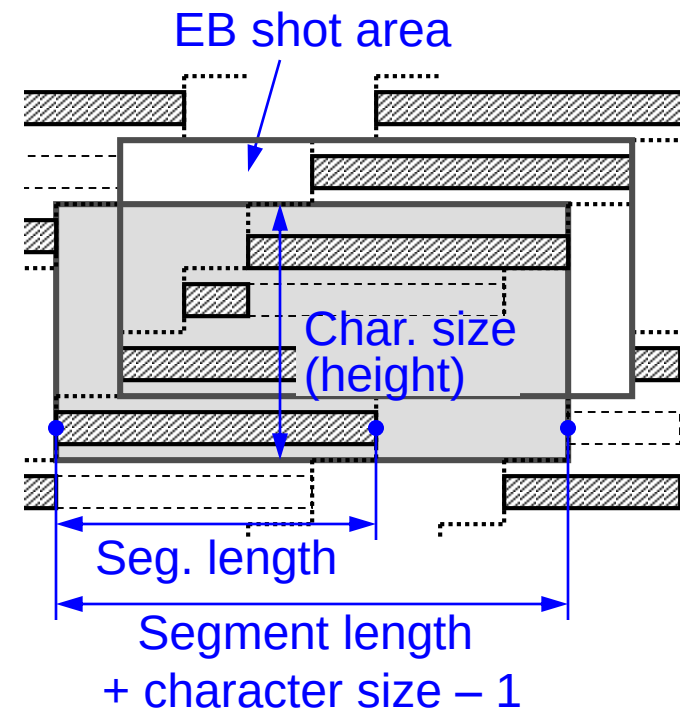
Metal segment character examples



'0'		blank pad span
'1'		
'2'		

Character overlap

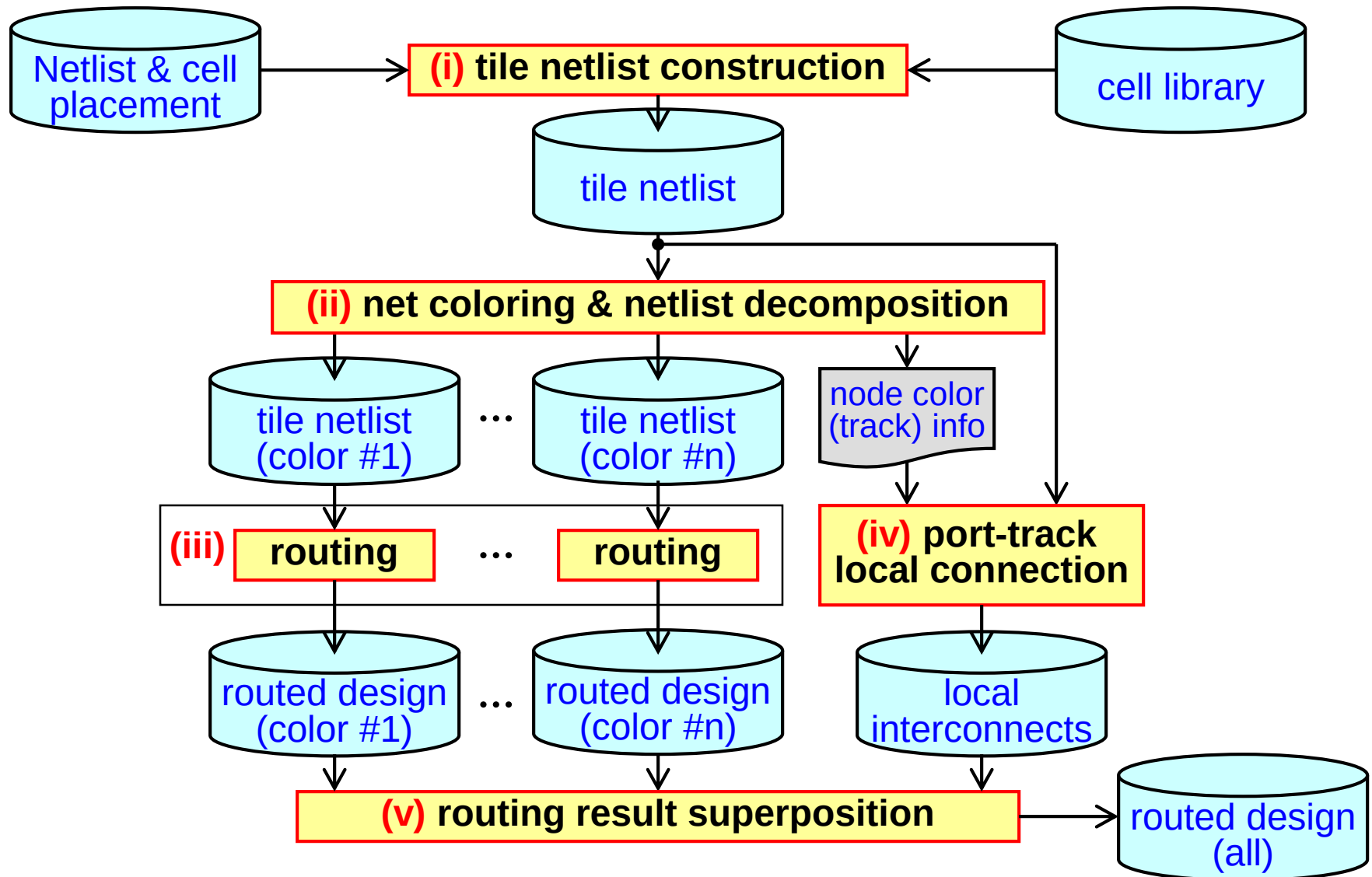
Metal segment character arrangement on stencil



Agenda

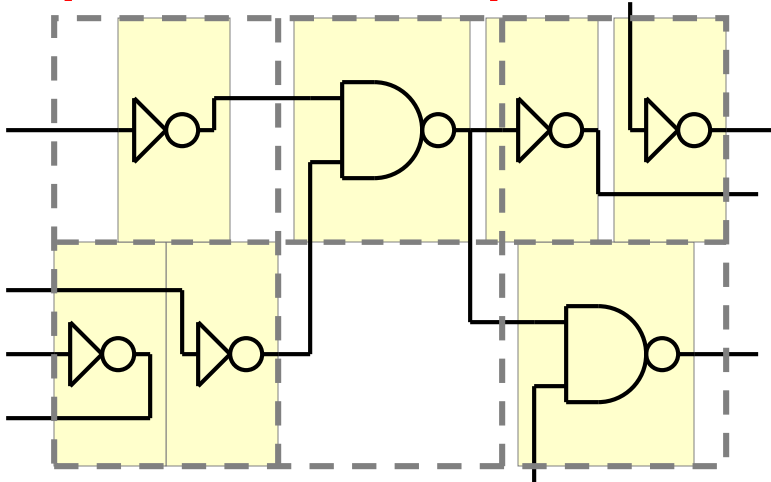
- ❑ Introduction
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- ❑ Experimental results
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Overview of Routing Design Flow for SRA

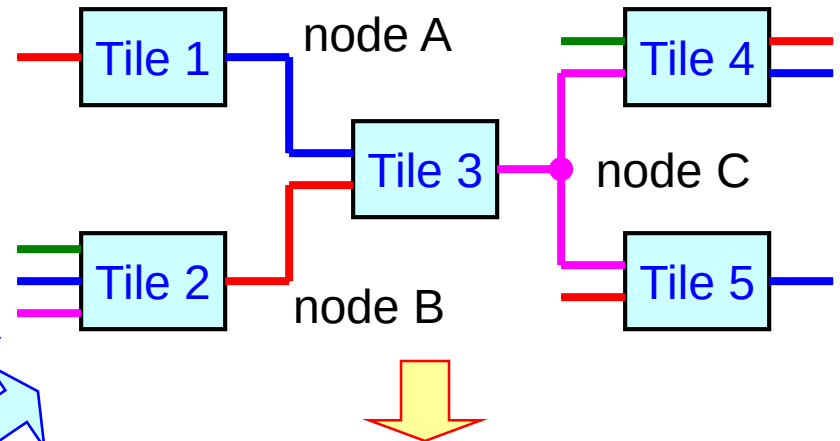


Track Assignment by Tile Netlist Coloring

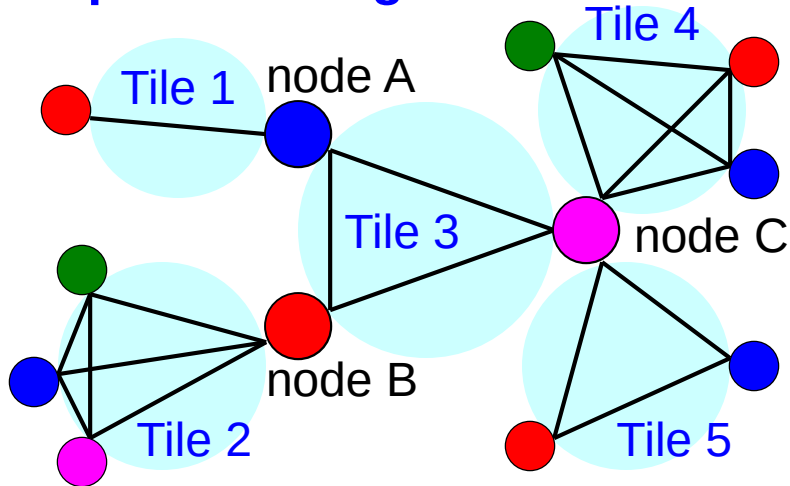
Input netlist & cell placement



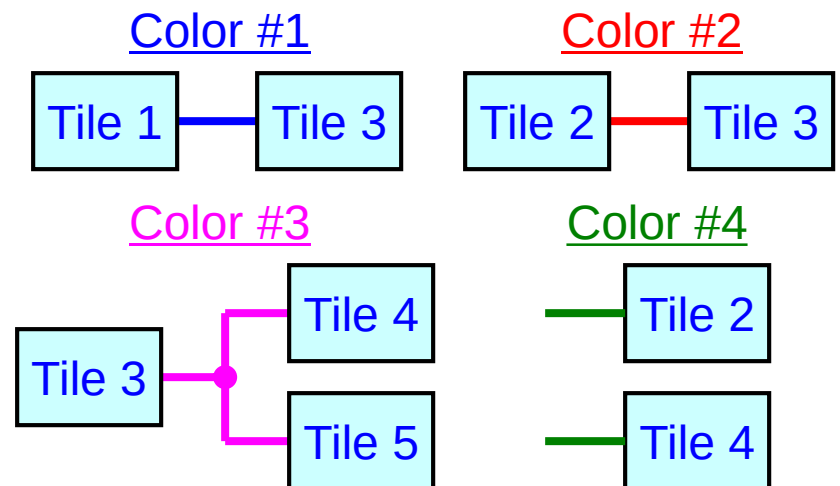
Tile netlist generation & coloring



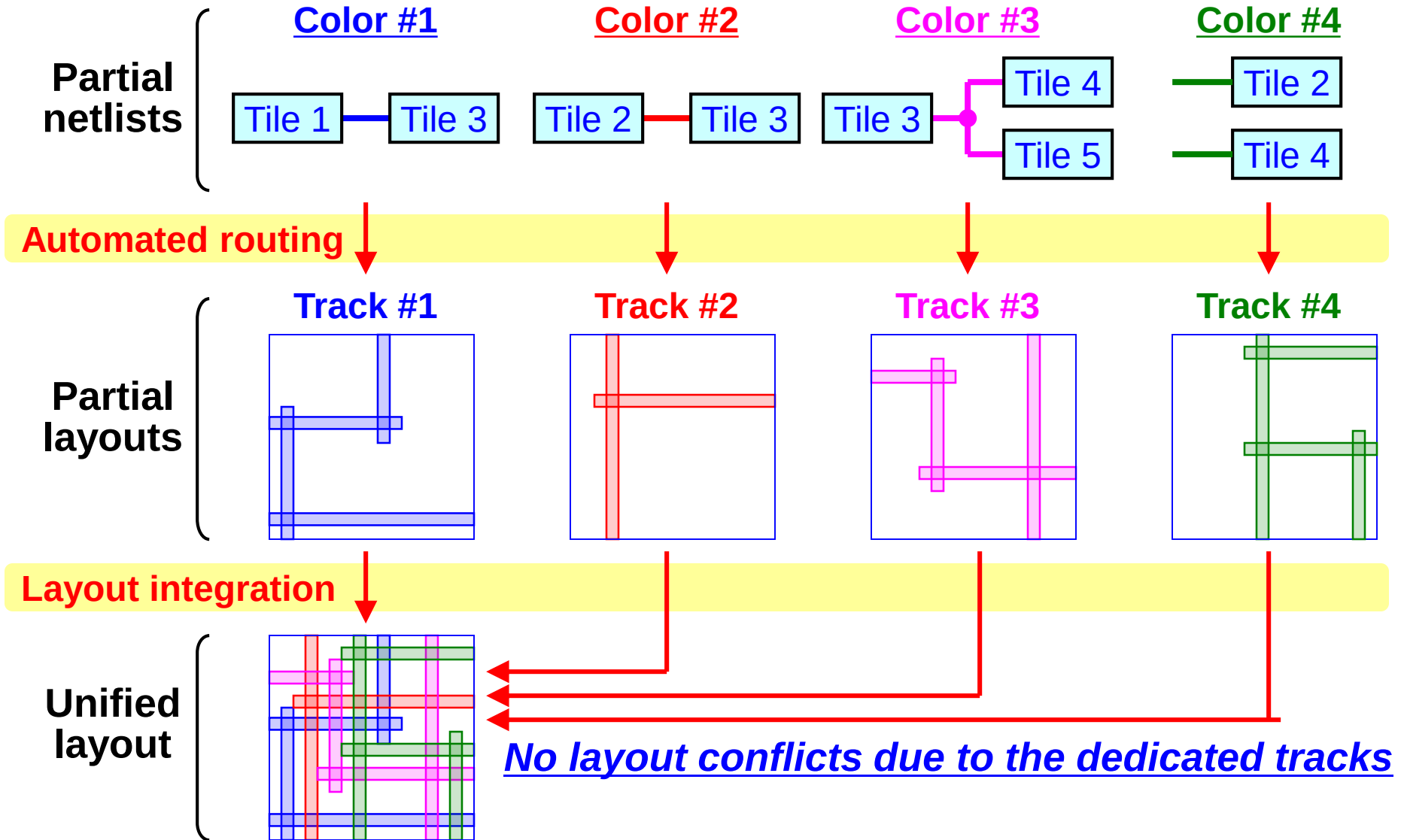
Graph modeling & node coloring



Partial netlist generation



Partial Netlist Routing and Layout Integration



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Experiments and CP Throughput Evaluation

❑ Experiments:

Reference designs (Conventional P&R / 65nm)

- Netlist & cell placement
- SRA design flow
- CP throughput evaluation

❑ CP throughput evaluation:

Shot count estimation per wafer

$$(\text{Gshot/wafer}) = \frac{10.0 \times 100}{(\text{lay out area})} \times (\text{shot\#})$$

average shot area (100Gs/w)
× target shot count
= total shot area

❑ Evaluation criteria:

Practical shot count in 14nm = 100~173 Giga shot/wafer

- ❑ 173 Gs/w: the minimum throughput requirement
- ❑ 100 Gs/w: the target to allow margins of other factors

Tile-cell Netlist Generation and Node Coloring

Design name		8080 Compat. CPU	USB 2.0 Function Core	AES (Rijndael) IP Core	Discrete Cosine Trans.
Logic cell#		4,326	7,708	16,755	13,880
Tile cell#		3,479	8,316	16,859	17,597
Signal net#		4,346	8,077	17,014	14,297
Net# per color	1	829	1,747	4,115	3,623
	2	787	1,554	3,720	3,048
	3	726	1,311	3,122	2,438
	4	665	1,299	2,407	2,068
	5	597	1,114	1,795	1,496
	6	523	745	1,338	1,063
	7	204	261	502	414
	8	15	38	14	133
	9	0	8	1	14
Max. color		8	9	9	9

Tile size = 9 grid (= lib cell height)

SRA design steps:

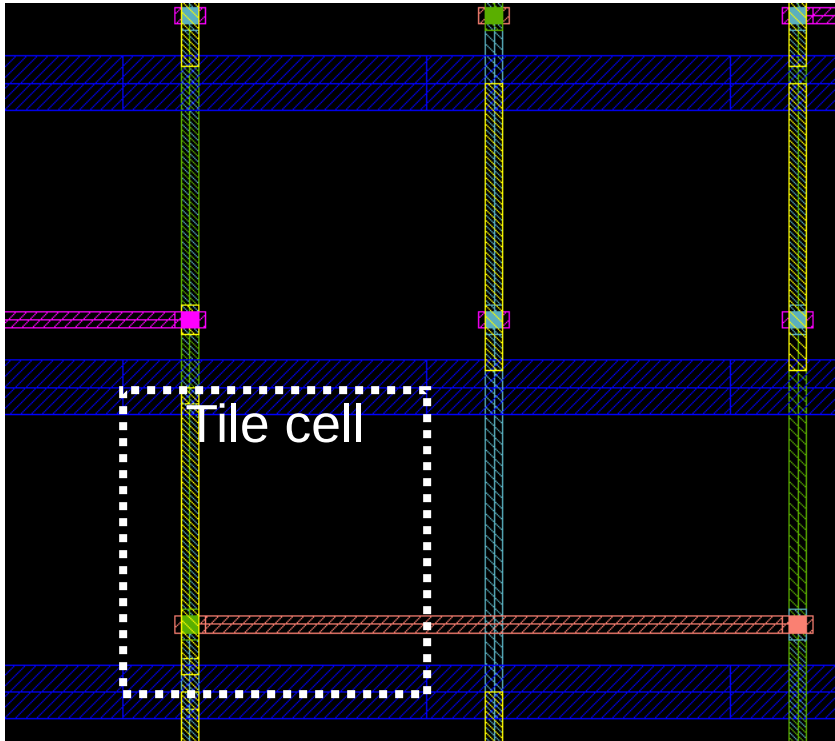
- ❑ Tile-cell netlist gen.
- ❑ Graph modeling
- ❑ Graph (net) coloring
(Brelaz, et. al, 1979)
→ Track assignment
& Partial netlist gen.

Coloring results:

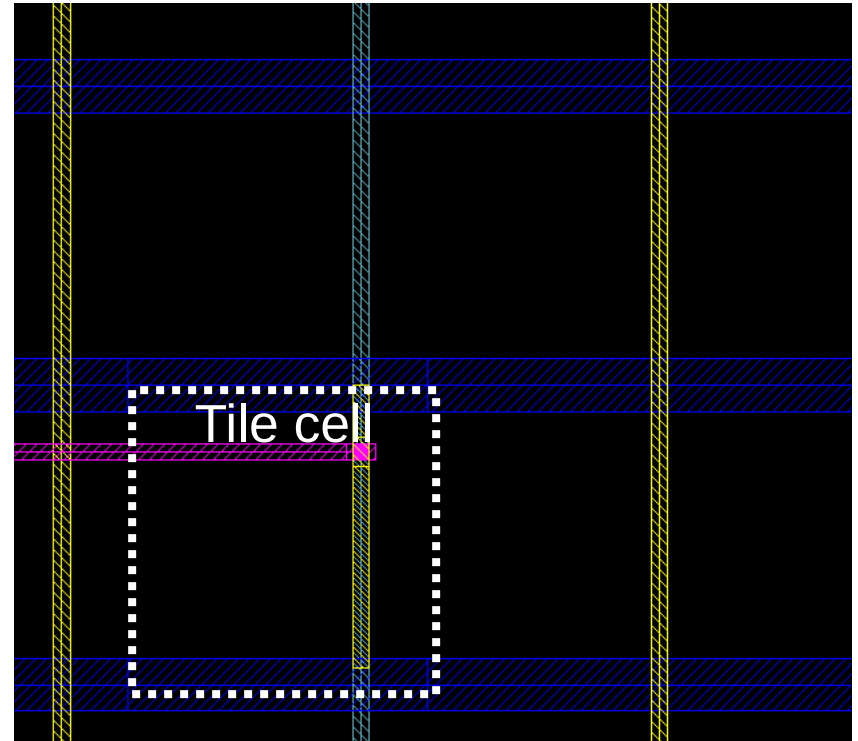
- ❑ Successful coloring
with the limited track
colors (Tile size L=9)
- ❑ Unbalanced net# for
each assigned color
- ❑ Partial netlists: to be
used in the next step
(partial routing)

Partial Netlist Routing Results

Track #2



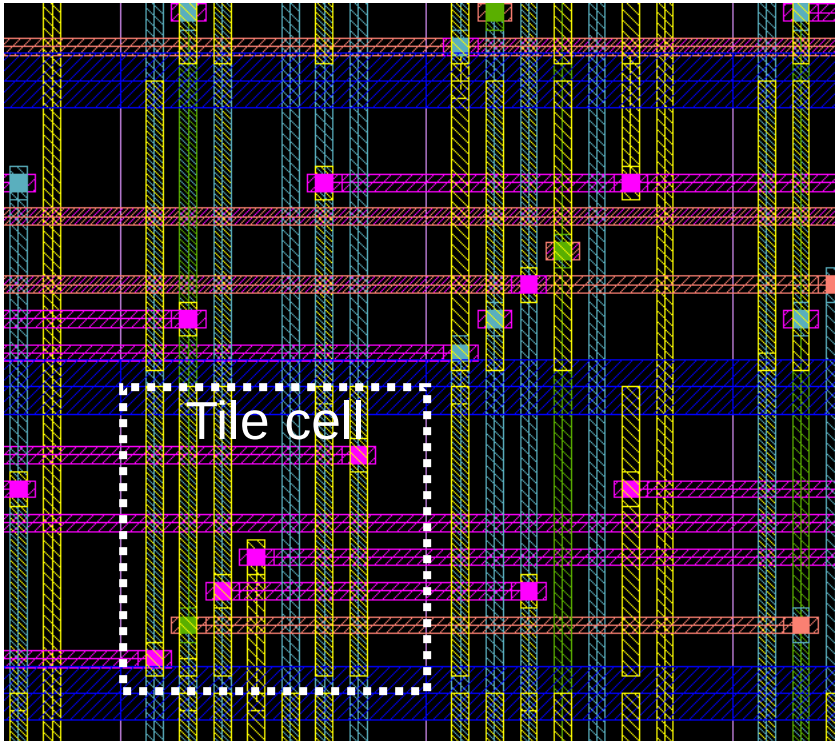
Track #7



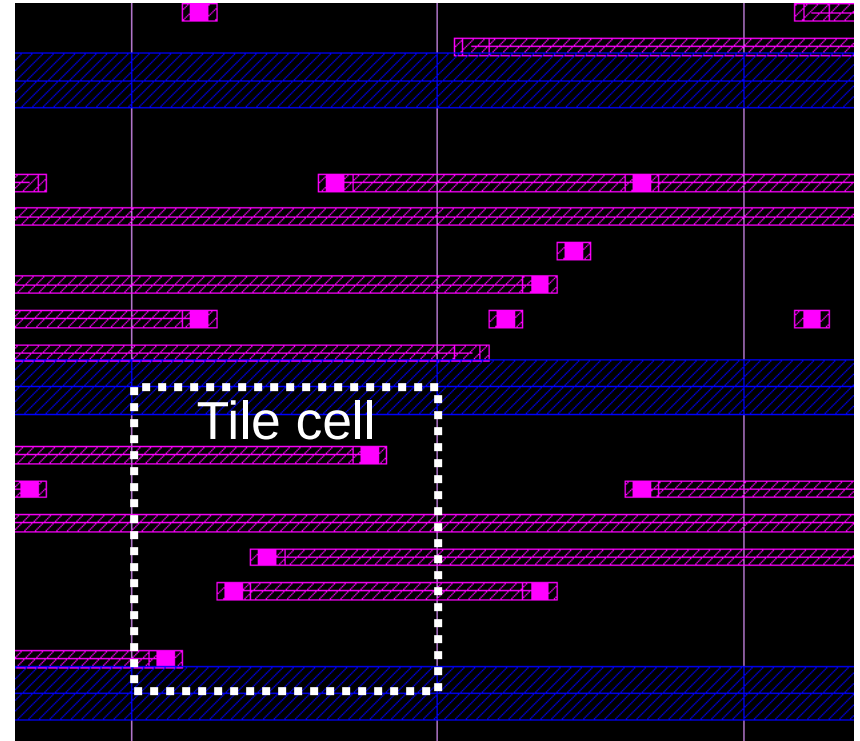
- ❑ Separate interconnect routing (ICC) results of the partial netlists
- ❑ Routing only on the assigned tracks
- ❑ Sparse routing results on the square grids

Routing Result Superposition for All Tracks

All tracks (all layers)



All tracks (VIA4, Met5)



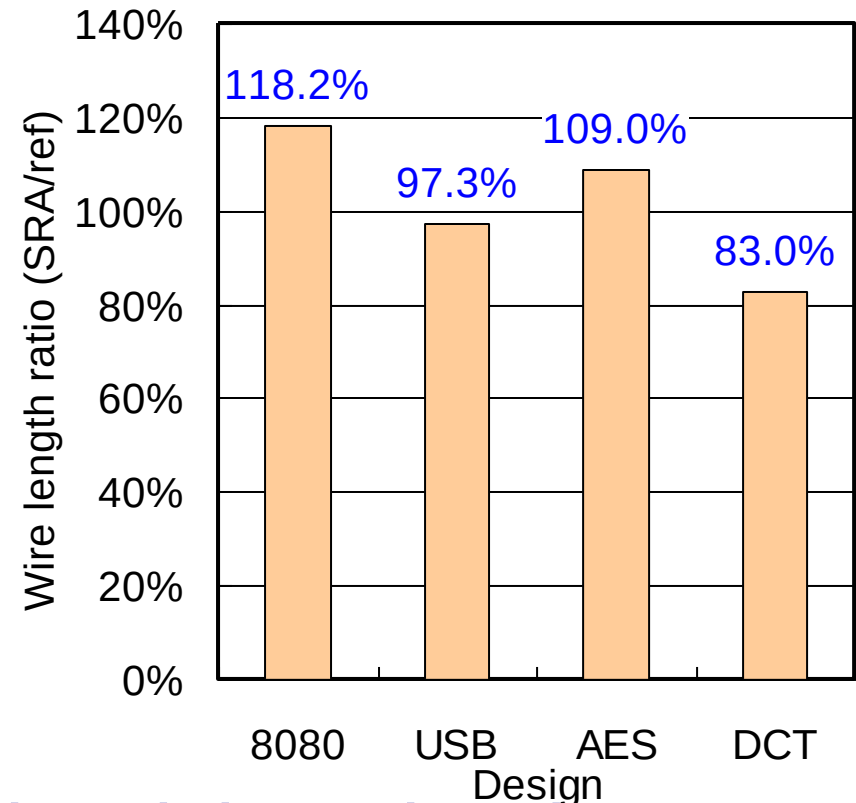
- ❑ Superposition of the routing results of the partial netlists
- ❑ No conflicts due to the dedicated tracks for each partial results
- ❑ Diagonal VIA arrangement
- ❑ Regular-length metal segments with diagonal arrangement

Routing Length Comparison: Ref vs. SRA

Wire length in each layer (USB 2.0)

Reference		SRA	
Layer	Length [um]	Layer	Length [um]
MET1	1,079.6	<MET4	43.2
MET2	15,879.8	MET4	17,398.8
MET3	37,475.9	MET5	40,914.0
MET4	31,732.7	MET6	34,495.2
MET5	30,313.6	MET7	25,819.2
MET6	18,980.9	MET8	15,049.8
>MET6	9,573.9	>MET8	7,374.6
Total	145,036.3	Total	141,094.8
Ratio (SRA/reference)		97.3%	

Total wire length: SRA/Ref



- ❑ **Higher layers used in SRA** due to the switch layer insertion
- ❑ As for the routing layers, **slightly shorter wires in SRA (USB 2.0)** despite the coarse routing grids and the reduced routing flexibility
- ❑ SRA required **-20~20% wires** than ref in the 4 example designs

EBDW Throughput Improvement by SRA

Layer	VIA			Metal		
Design	G-shot/wafer			G-shot/wafer		
	VSB (VIA2)	CP (VIA4)		VSB (MET3)	CP (MET5)	
8080	1303.0	152.3	8.55	1121.2	219.2	5.11
USB	1035.2	138.8	7.46	832.4	204.6	4.07
AES	970.9	136.9	7.09	826.6	197.9	4.18
DCT	847.6	120.3	7.05	684.3	168.8	4.05
Average	1039.2	137.1	7.58	866.1	197.6	4.38

- ❑ **Estimated EB shot count [G-shot/wafer) in the most dense layers**
 - ❑ VIA shot#: 120~152 Gs/w → Hitting the target shot#/wafer
 - ❑ Met shot#: 169~219 Gs/w → Missing the target shot#/wafer
- ❑ **Comparison Reference design with VSB vs. SRA design with CP**
 - ❑ VIA performance improvement: ~7.5x shot# reduction
 - ❑ Metal performance improvement: ~4.4x shot# reduction

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Conclusion

❑ Structured Routing Architecture

- ❑ CP throughput limitation by stencil area (= character#)
- ❑ Periodic track grouping & restricted track exchange
- ❑ Restricted VIA placement & metal shape → less CP char.
- ❑ Area-efficient stencil design by overlapped characters
- ❑ SRA design flow (track-assignment first) development

❑ Experimental results

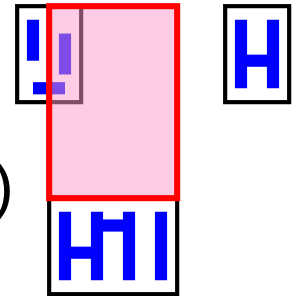
- ❑ SRA design flow demonstration with example circuits
- ❑ CP performance evaluation (shot#/wafer, figure#/shot):
100~220 Gs/w (VIA & metal), 4~9 figures/shot
- ❑ Improvement from VSB: VIA: 4.4x, Metal: 7.5x
- ❑ Target throughput achievement:
VIA: achieved, Metal: not → tile size optimization, etc.

Thank you!

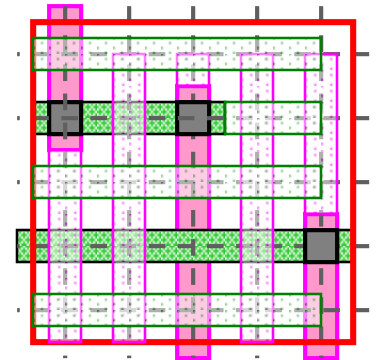
Appendices

Earlier Efforts for CP Efficiency Improvement

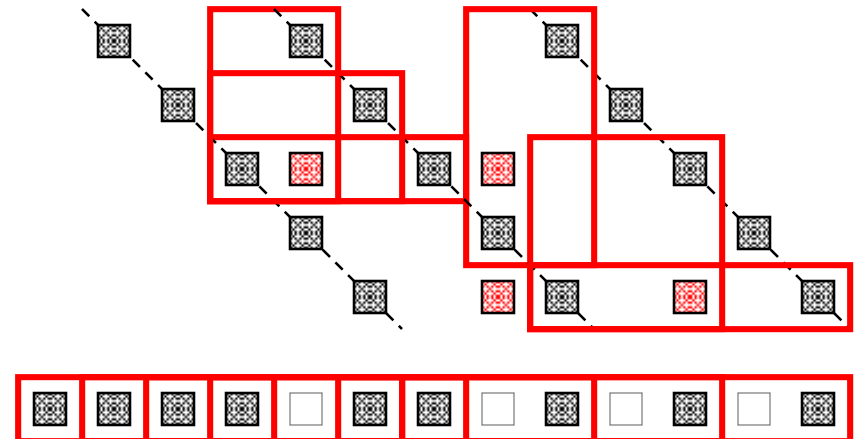
- ❑ **Cell layer (transistors & local wires)**
 - ❑ 1 cell/shot (major cells only) $\rightarrow E_{CP} > 10$
 - ❑ > 1 cells/shot (cell clusters as the characters)
cluster extraction / rearrangement



- ❑ **Metal layers (interconnect)**
 - ❑ Tile routing: normalized wire segments
 - ❑ Matching to predefined characters



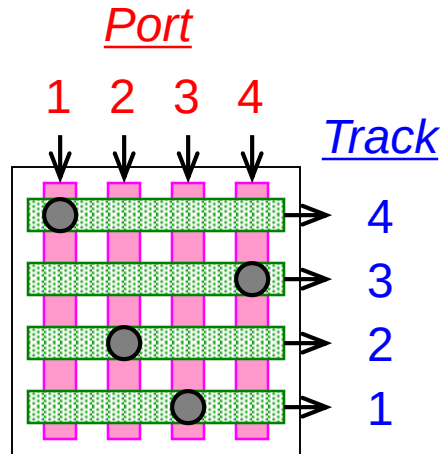
- ❑ **VIA layers (interconnect)**
 - ❑ Area-efficient stencil design
 $\rightarrow$ Max. 3 via/shot
(Du et al./ASP-DAC2012)
 - ❑ 1D VIA character stencil
 $\rightarrow$ 4~6 via/shot in average
(Ikeno et al./ASP-DAC 2013)



Cell-Port to Routing-Track Switch Connections

1-step switching

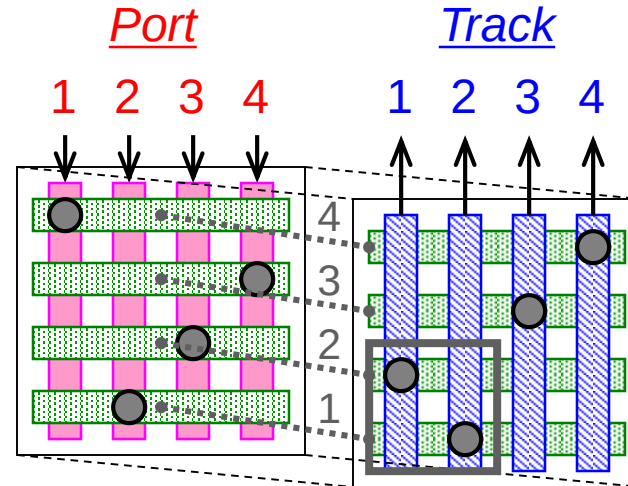
(1234) → (4213)



$4! = 24$ patterns

2-step switching

(1234) → (4123) → (4213)



$4!/2! + 2! = 14$ patterns

- ❑ If all 1-step VIA patterns (= $N!$) can not be integrated in the stencil, 2 (or more) steps are required for VIA pattern reduction
- ❑ If limiting the permutations in one layer as $m!$, the other layer requires only $N!/m!$ patterns

Stencil Design under Area & Size Constraints

- ❑ Character set planning for stencil design to be adopted to 14nm CP-EBDW equipment specifications

Stencil area: 3.6×10^6 grids / Shot size: 30 grid x 30 grid

VIA array character

- ❑ **M**: character size (max. VIA# in 1 character)
- ❑ Character number = 2^M (= number of M-bit binary codes)
- ❑ Average area for 1 character = **M** [grid]
- ❑ $2^M \times M < 3.6 \times 10^6 \rightarrow \boxed{M=17}$

Metal segment character

- ❑ **L**: Segment length $\rightarrow \boxed{L=9}$ (Tile size = cell height = 9 grid)
- ❑ **M**: Character size (# occupied tracks)
- ❑ Character number = 3^M (= number of M-digit ternary codes)
- ❑ Average area for 1 character = **M+L-1** [grid]
- ❑ $3^M \times (M+L-1) < 3.6 \times 10^6 \rightarrow \boxed{M=11}$

Example Circuits & Reference Design Summary

Design name	8080 Compat. CPU	USB 2.0 Function Core	AES (Rijndael) IP Core	Discrete Cosine Trans.
Clock period [ps]	600	300	600	1,000
Layout area [μm^2]	11,750	29,309	60,270	63,907
Cell area [μm^2]	11,321	26,997	51,956	55,013
Logic cell#	4,326	7,708	16,755	13,880
Signal net#	4,346	8,089	17,014	14,295
Layout figure# statistics (most dense layers)				
VIA2	15,311	30,340	58,513	54,170
Met3	13,174	24,398	49,818	43,732
EB shot count estimation [Gshot/wafer]				
VIA2	1303	1035	971	848
Met3	1121	832	827	684

- ❑ The most dense layers (VIA2 & Met3) define the overall throughput
- ❑ The estimated shot count: ~1000 Giga-shot/wafer by VSB
- ❑ Increase of the actual shot# due to multi-shots for long wires, etc.

VIA and Metal CP Performance Estimation

Design	VIA#	VIA4 util.	Shot#	EB shot# [G-s/wafer]	VIA#/shot
8080	11,861	36.3%	1,790	152.3	6.63
USB	22,288	27.4%	4,068	138.8	5.48
AES	46,266	27.6%	8,253	136.9	5.61
DCT	29,914	16.9%	7,689	120.3	3.89
Design	Seg#	Met5 util.	Shot#	EB shot# [G-s/wafer]	Seg#/shot
8080	15,563	47.7%	2,576	219.2	6.04
USB	35,482	43.6%	5,998	204.6	5.92
AES	64,850	38.7%	11,928	197.9	5.44
DCT	46,602	26.3%	10,785	168.8	4.32

- ❑ EB shot count estimation in the most dense layers of VIA & metal
- ❑ VIA shot#: **120~152 Gs/w** → Hitting the target shot#/wafer
- ❑ Met shot#: **169~219 Gs/w** → Missing the target shot#/wafer
- ❑ CP efficiency: **4~9 figures/shot** in average