

Tribute to Professor Yoji Kajitani

Dawn of Computer-aided Design **- from Graph-theory to Place and Route -**

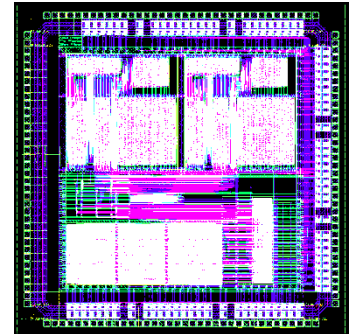
Atsushi Takahashi
Tokyo Institute of Technology

Atsushi Takahashi

- Tokyo Institute of Technology
 - B.E. 1989
 - Switch-box Routing
 - M.E. 1991, D.E 1996
 - Graph-Theory, Path-Width
 - Research Associate 1991-1997
 - Associate Professor 1997-
(Osaka Univ. 2009-2012)
 - Physical Design, Algorithm
 - Routing, Clock, etc.

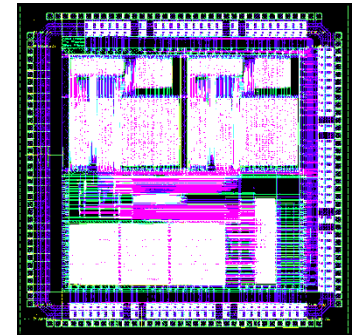
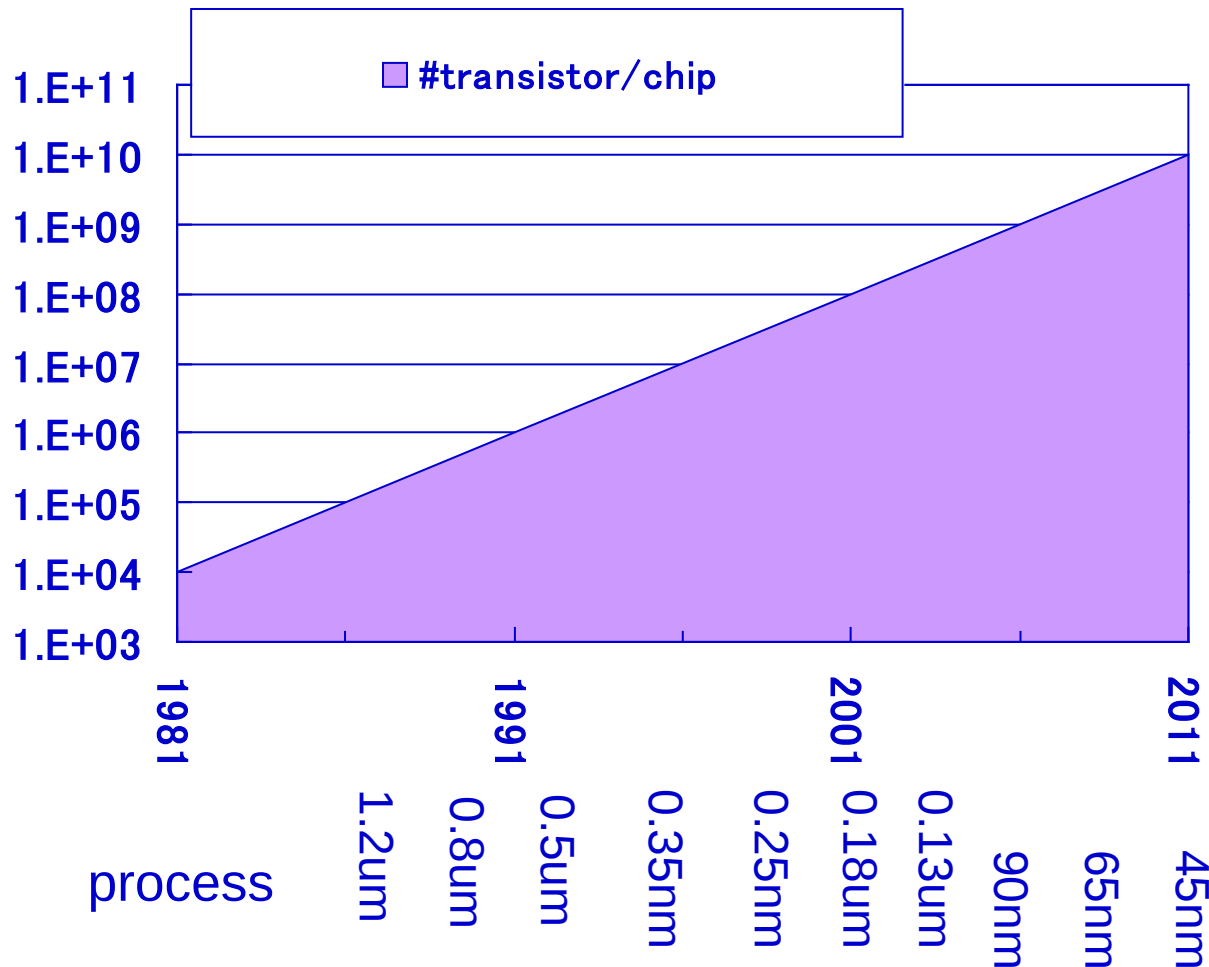
History of VLSI

- 1959
 - Transistors, diffusive resistances, wires are fabricated on a silicon substrate by using lithography and etching technology
 - Few elements are in one chip
 - **Robert Noyce** (A founder of Intel)
 - **Jack Kilby** (Nobel Prize in Physics, 2000)
- Moore's Law: #elements in one chip
 - Twice in 1.5 year
- Now
 - More than 1G elements in one chip



#Transistors in one chip

- Increases +58%/year



by SEMATECH

Change of Names

- IC: Integrated Circuit (1960-)
- LSI: Large Scale IC (1970-)
- VLSI: Very Large Scale IC (1980-)
- ULSI: Ultra Large Scale IC (1990-)

- System LSI
- SoC (System on Chip)
- SiP (System in Package),...

Historical Computers in Japan

- Relay Computer, Fujitsu
 - Relay-elements from telephone exchange equipment
 - Toshio Ikeda
 - FACOM100, 1954
 - FACOM128A, 1956
 - FACOM128B, 1958
 - Commercial computer
 - Still working model was manufactured in 1959
 - IPSJ Information Processing Technology Heritage

Historical Computers in Japan

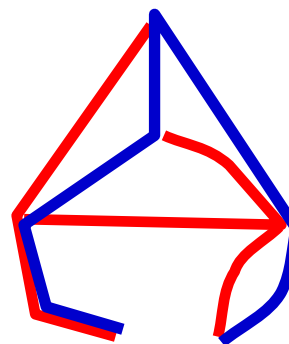
- Parametron Computer, NEC
 - SENAC-1(NEAC1102), 1958
 - First commercial computer by NEC
 - Hitoshi Watanabe
 - IEEE Kirchhoff Award 2010
 - » Filter design theory and computer-aided circuit design
 - IPSJ Information Processing Technology Heritage

Historical Computers in Japan

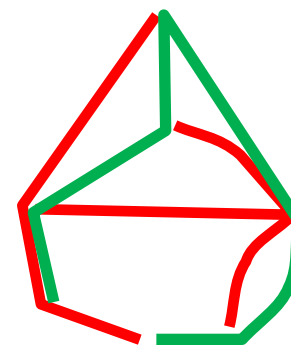
- Electronic Calculators, Sharp
 - CS-10A, 1964
 - Germanium-Transistor
 - First all-transistor diode electronic desktop calculator in the world
 - 25 kg
 - 535,000 Yen (= 1,500 US\$)
 - Initial monthly salary of graduate = 21,526 Yen
 - Toyota Corolla 1100cc = 432,000 Yen (1966)
 - IEEE milestone 1964-1973
 - IPSJ Information Processing Technology Heritage

Principal Partition (1969)

- Genya Kishi & Yoji Kajitani
 - Maximally Distant Trees and Principal Partition of a Linear Graph
 - IEEE Trans. CAS 1969
 - Most Distant (Reliable) Pair of Sub-trees
 - Unique Graph Partition, Sparse, Dense, and Other
 - The minimum set of voltages and currents that describes all variables in a circuit



$D = 4$



$D = 5$

Original Principal Partition Papers

- Genya Kishi, Yoji Kajitani
 - Maximally Distant Trees in a Linear Graph (in Japanese)
 - IEICE Trans. Fund. 1968 (Japanese Edition)
 - Best Paper Award
- Tatsuo Ohtsuki, Yasutoshi Ishizaki, Hitoshi Watanabe
 - Network Analysis and Topological Degree of Freedom (in Japanese)
 - IEICE Trans. Fund. 1968 (Japanese Edition)
 - Best Paper Award
- Masao Iri
 - A Min-Max Theorem for the Ranks and Term-Ranks of a Class of Matrices – An Algebraic Approach to the Problem of the Topological Degree of Freedom of a Network (in Japanese)
 - IEICE Trans. Fund. 1968 (Japanese Edition)
 - Best Paper Award

Graph Theory for Network

- Yoji Kajitani

- The Semibasis in Network Analysis and Graph Theoretical Degree of Freedom
- IEEE Trans. CAS 1979
- Basis of Independent variables

- IEEE Fellow 1992

- IEEE CASS Golden Jubilee Medal 1999

- IEEE CASS Technical Achievement Award 2009

Principal Partition

- ISCAS 1982
 - Session: Theory and Application of Principal Partition

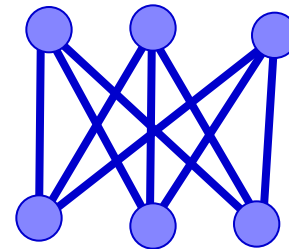
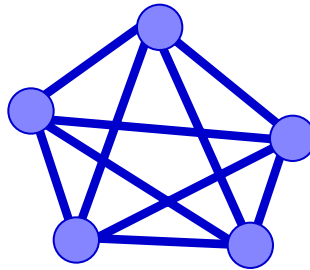
- Theory of Principal Partitions Revisited
 - Satoru Fujishige
 - Research Trends in Combinatorial Optimization
 - Springer, pp.127-162, 2009

- A Faster Algorithm for Computing Principal Sequence of Partitions of Graph
 - Vladimir Kolmogorov
 - Algorithmica, vol.56, pp.394-412, 2010

- On Variants of the Matroid Secretary Problem
 - Shayan Oveis Gharan, Jan Vondrak
 - ESA 2011, LNCS 6942, pp.335-346, 2011

Planarity Testing

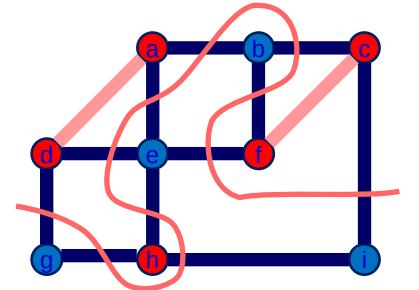
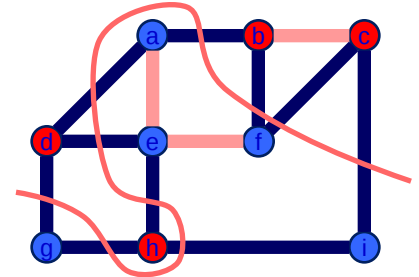
- Kuratowski's Theorem (1930)
 - Planar iff K_5 , $K_{3,3}$ are not contained



- Linear Time Algorithm (1974)
 - Hopcroft & Tarjan
 - Efficient planarity testing, J.ACM, 1974

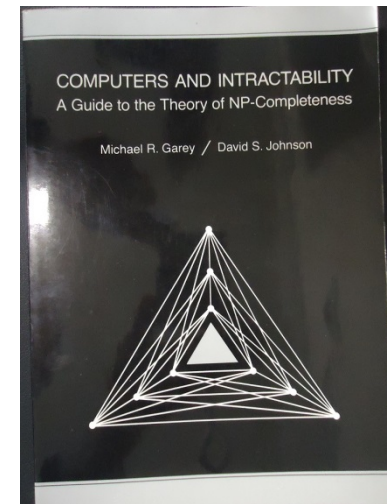
Maximum Cut

- NP-hard in general (1972)
 - Karp
 - Reducibility among combinatorial problems
 - Complexity of Computer Computation, Plenum Press, 1972.
- Polynomial in planar (1975)
 - Hadlock
 - Finding a Maximum Cut of a Planar Graph in Polynomial Time
 - SIAM J Comput, 1975
 - $O(n^2 \log n)$



NP-Completeness (1979)

- Garey & Johnson
 - Computers and Intractability
 - A Guide to the Theory of NP-Completeness



- Heuristic should be introduced after proving that the problem is NP-hard

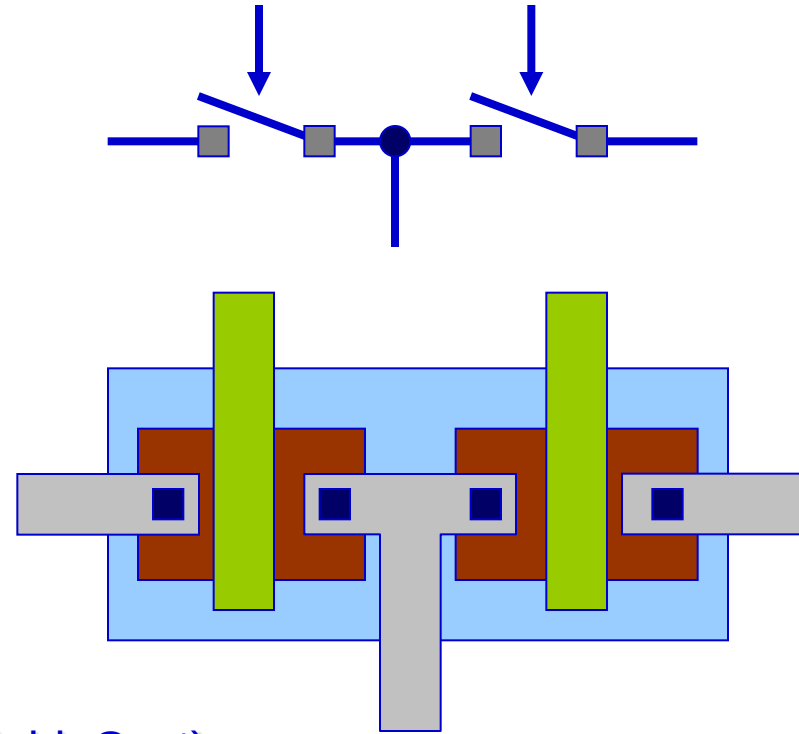
Change of Design Method

■ Design Method

- Manual Design
 - Circuit Diagram, Mask
- Computer Aided Design
 - Boring simple tasks
- Design Automation
 - Inferior quality but used since a circuit is too big to design manually

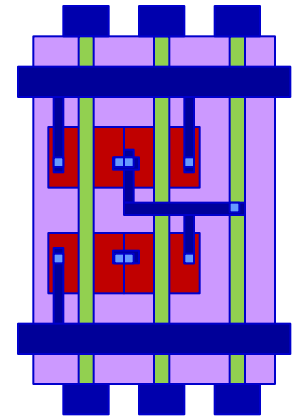
■ Design Objectives

- Area (Request from manufacturing, Yield, Cost)
- Speed (Request from market, Emergence of PC)
- Power (Emergence of Mobile products)
- Noise (Influence to TV, Medical products)



Change of Design Style

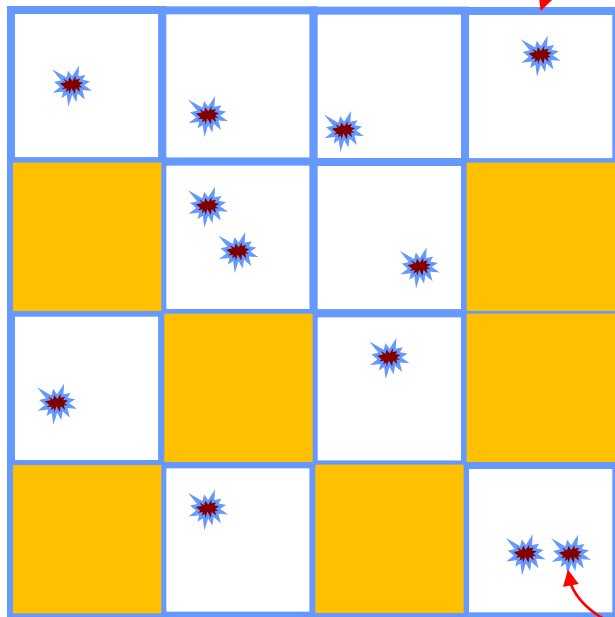
- Full Custom Design
- Semi Custom Design
- Standard Cell
 - Same cell height
- Gate Array
 - Same transistor layout
- FPGA (Field Programmable Gate Array)
 - Same logic elements
- Reconfigurable
- IP base



Chip Area Reduction

More chips and more earnings

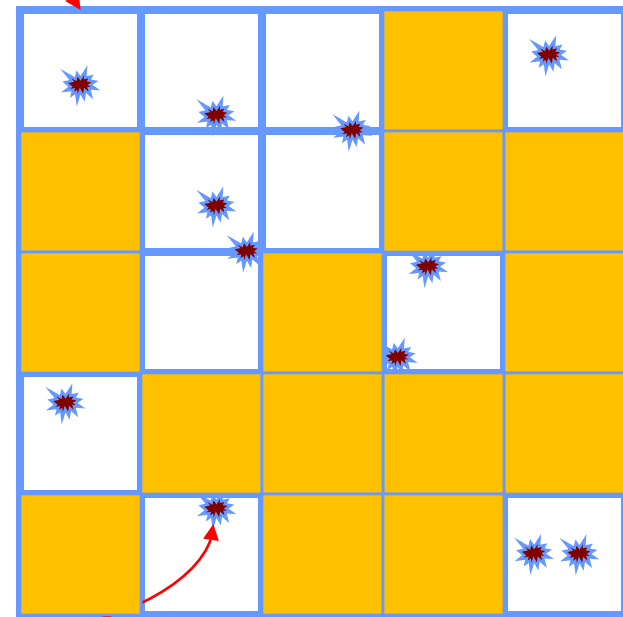
Chip Area: Large



16
6

#chip
#actual chip

Small

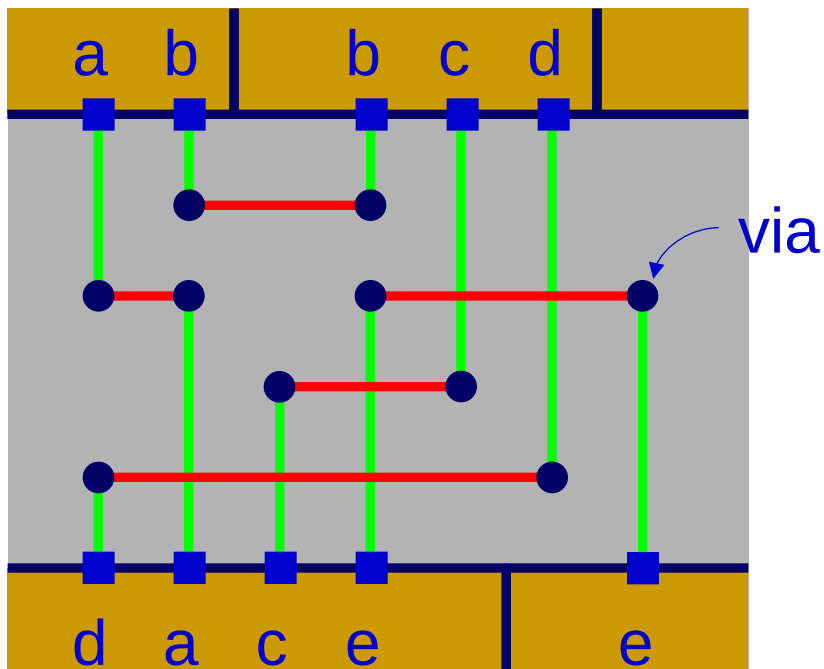


25
14

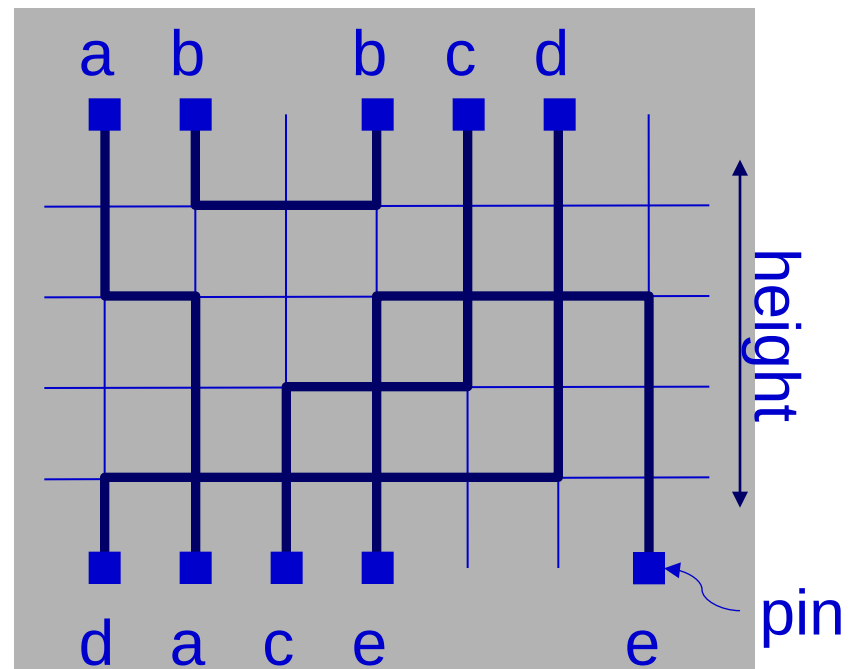
Channel Routing

■ 2-Layer Channel Routing

- Connect pins on the boundary of routing area using 2-layer
- Minimize the number of tracks (height, width) of channel



HV rule



Left-Edge Algorithm (1971)

- Hashimoto & Stevens
 - Wire Routing by Optimizing Channel Assignment within Large Apertures
 - DAC 1971
 - Minimum tracks when no vertical constraint

Minimum Tracks in Channel (1979)

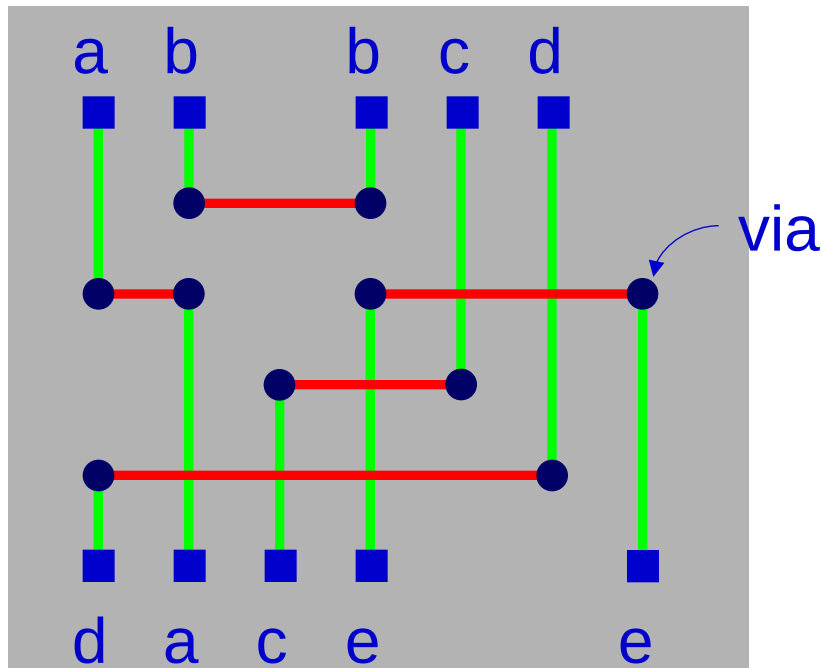
- Tatsuya Kawamoto & Yoji Kajitani
 - The Minimum Width Routing of a 2-Row 2-Layer Polycell-Layout
 - DAC 1979
 - Minimum tracks

Via Problem

■ Via Minimization

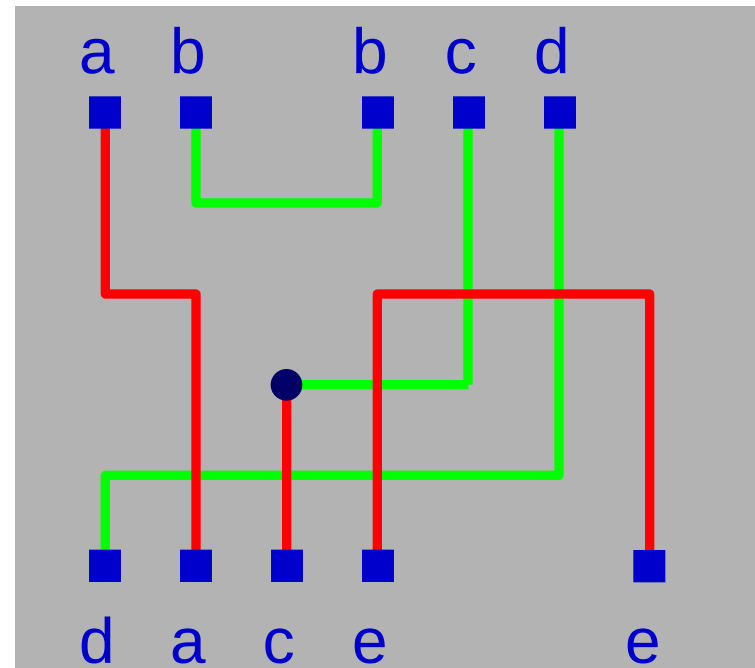
- Minimize #via by assigning wires into proper layer

#via = 10



HV rule

#via = 1



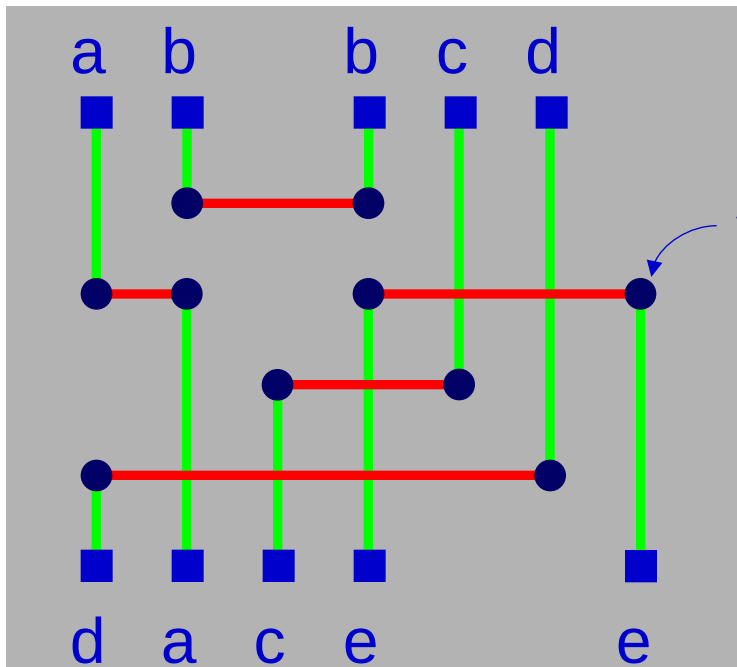
arbitrary rule

Via Problem (2)

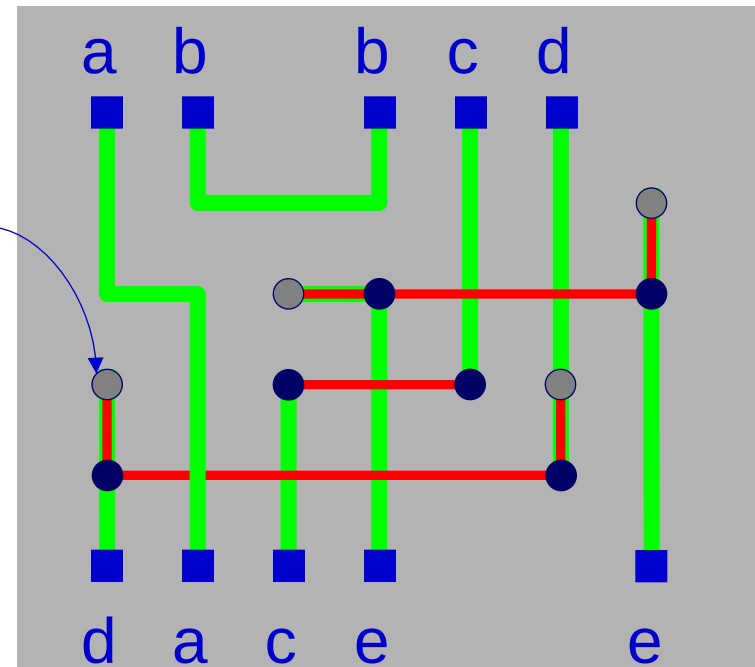
■ Double Via Insertion

- Minimize #single-via to improve the reliability

#single-via = 10



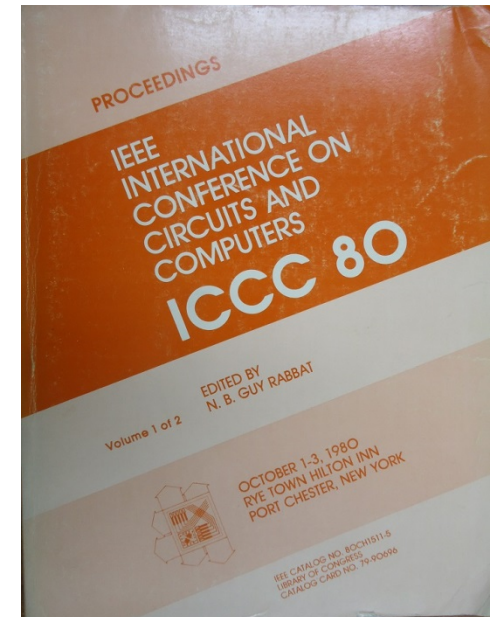
#single-via = 2



Via hole Minimization (1980)

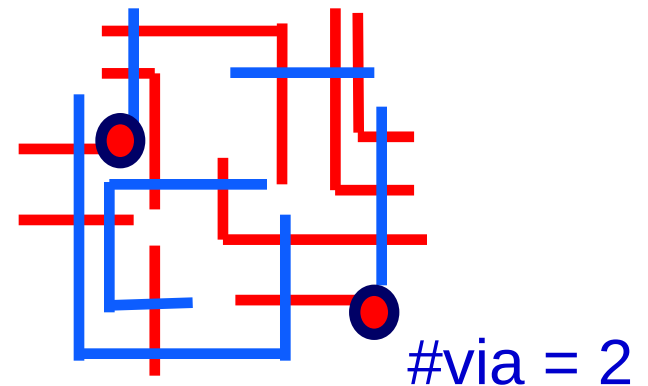
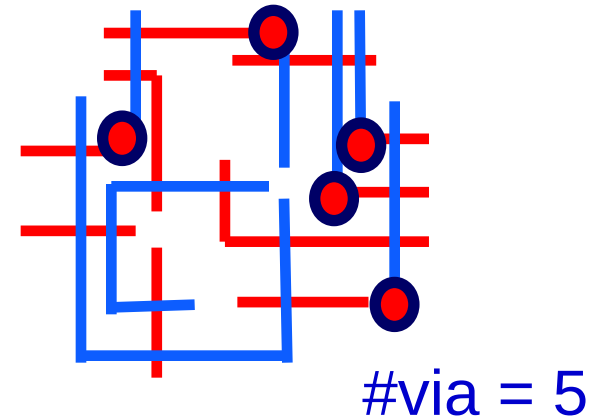
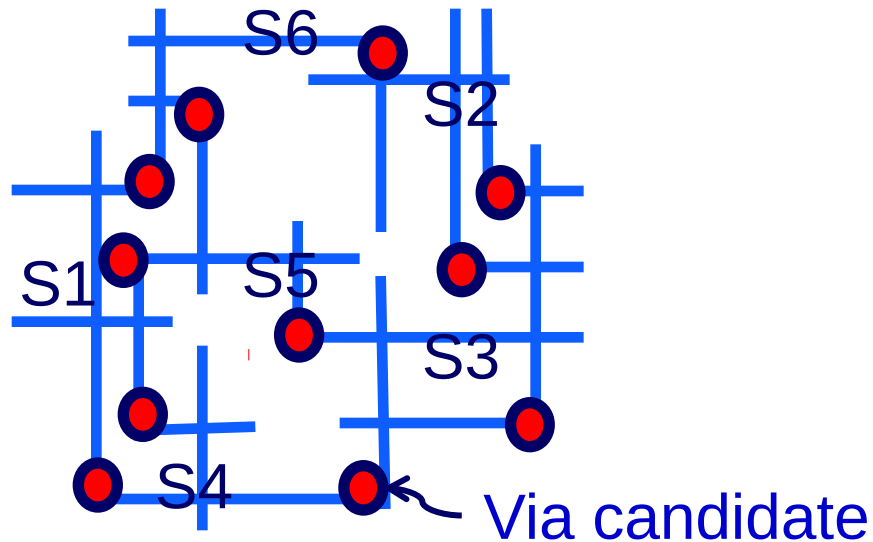
■ Yoji Kajitani

- On Via Hole Minimization on Circuits and Computers
- IEEE International Conference on Circuits and Computers, ICC80
- Assignment of wires into 2-layer that minimize the number of vias



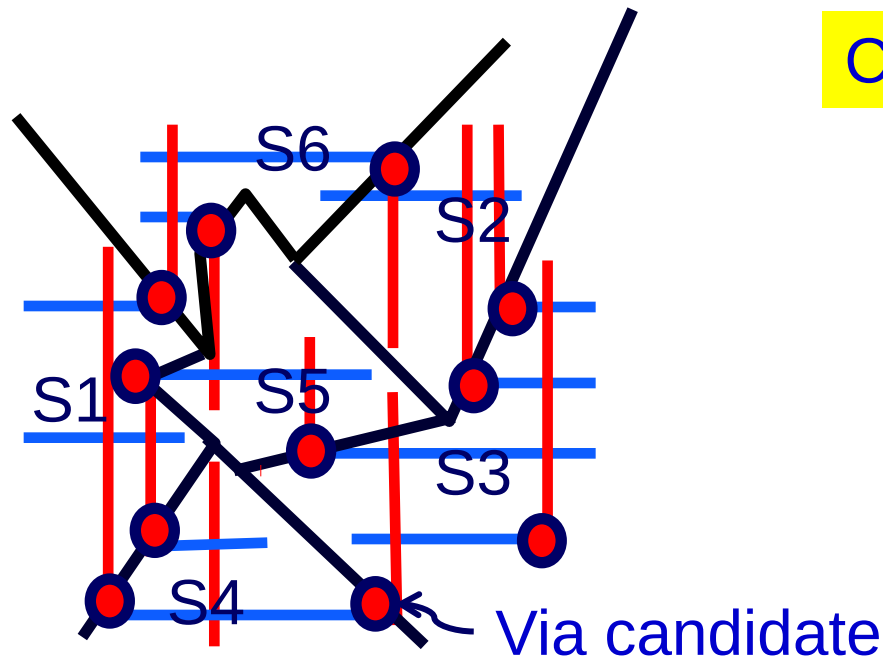
Wire Assignment and Vias

■ 2-Layer wire assignment



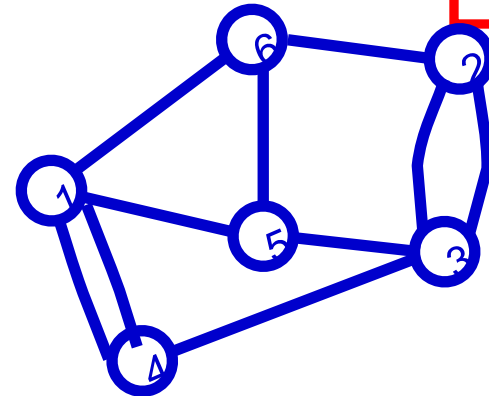
Wire Clustering and Constraint Graph

- Clustering by crossing relation between wires



Constraint Graph

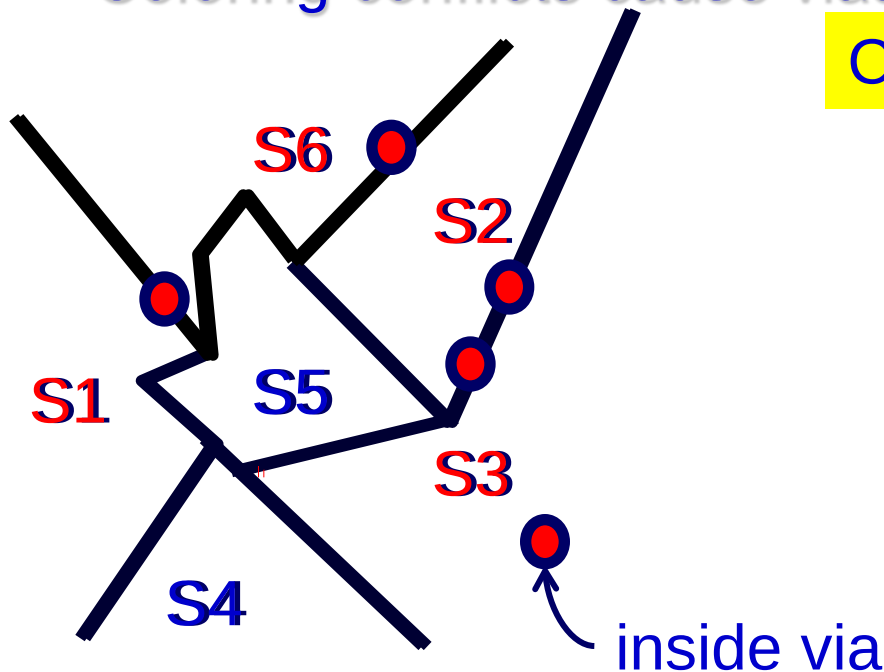
Planar



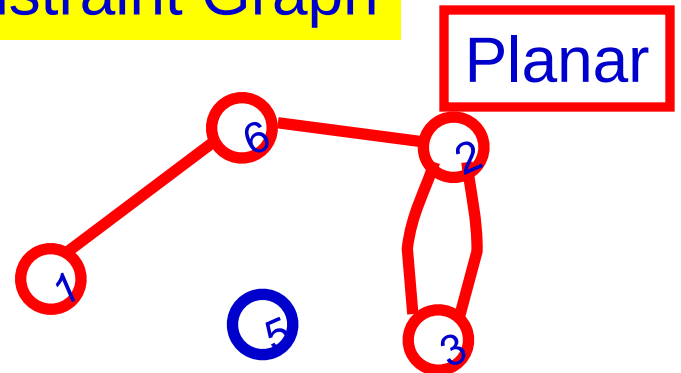
Vertex : Cluster
Edge: Via candidate

Constraint Graph 2-Coloring and Vias

- 2-coloring of constraint graph
 - Coloring conflicts cause vias



Constraint Graph

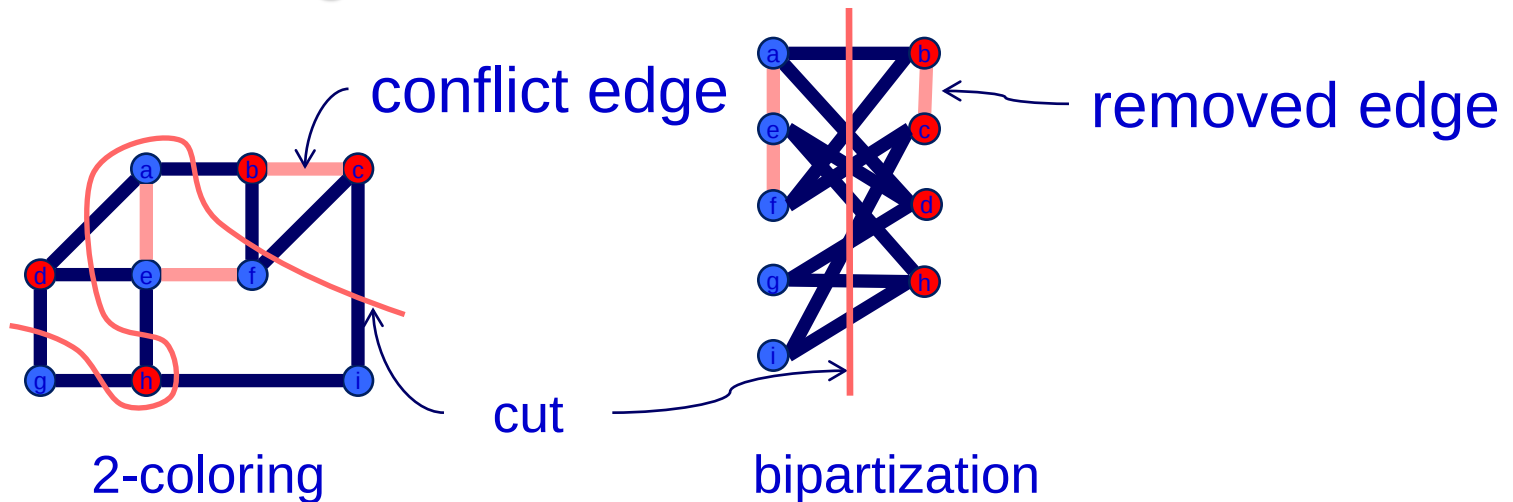


Vertex : Cluster
Edge: Via candidate

#via between clusters = 4
#via inside cluster = 1

Minimum Via Problem

- #via = #conflict edges in 2-coloring
= #edge that needed to be removed
to make the graph bipartite
 $\Leftrightarrow$ #edge in cut



Minimum Via Problem = Maximum Cut Problem

(NP-hard in general)

Planar Graph and its Dual Graph

■ Planar Graph $\Leftrightarrow$ Dual Graph

– Vertex $\Leftrightarrow$ Face

■ Vertex degree $\Leftrightarrow$ Face Degree

– Face $\Leftrightarrow$ Vertex

■ Face degree $\Leftrightarrow$ Vertex degree

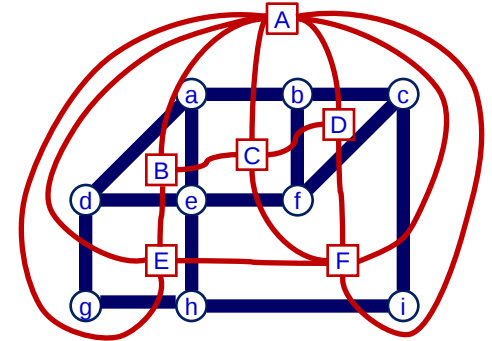
– Edge $\Leftrightarrow$ Edge

– Cycle = Symmetric difference of faces

– Two colorable = Bipartite graph

= No odd cycle = No odd face

$\Leftrightarrow$ No odd vertex degree (Euler Graph)



Maximum Cut of Planar Graph

■ Min Via Problem

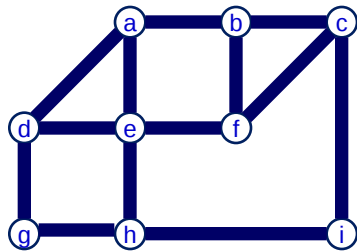
⇔ Max Cut Problem of Planar Graph

⇔ Min Conflict 2-coloring Problem of Planar Graph

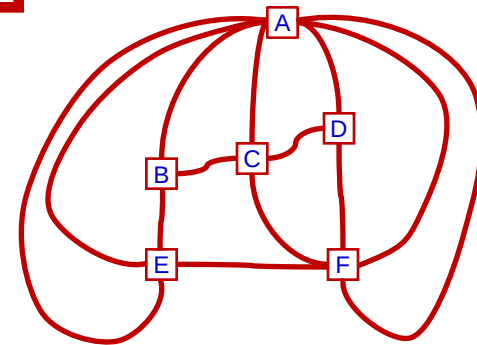
⇔ Euler Graph Problem in Dual

- Make each vertex degree even by removing the minimum number of edges

Constraint Graph



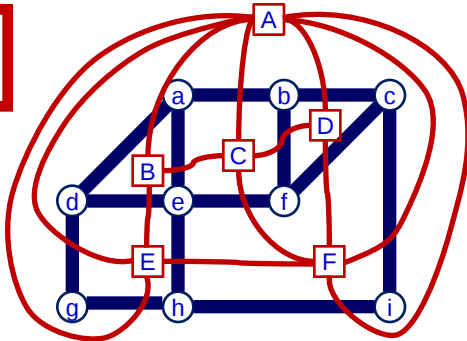
Dual



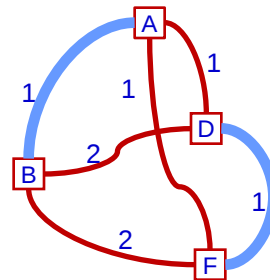
Euler Graph Problem

- Make each vertex degree even by removing the minimum number of edges in **Dual**
 - Construct complete graph K_d from constraint graph
 - Vertex: odd degree vertex of **Dual**
 - Edge weight: shortest path length in constraint graph
 - Find a minimum cost perfect matching of K_d
 - Remove edges corresponding to the obtained matching

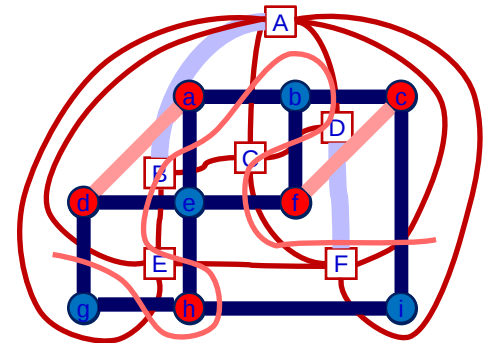
Dual



Constraint Graph



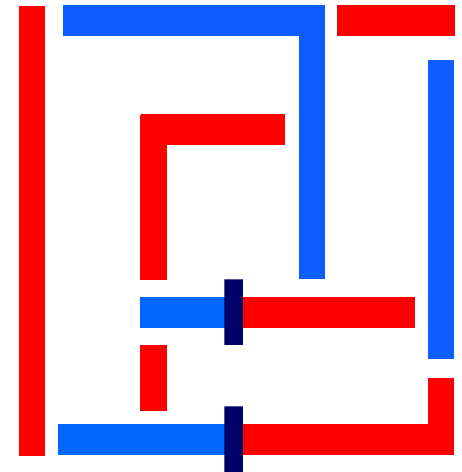
K_d



Minimum Stitch in Double Patterning

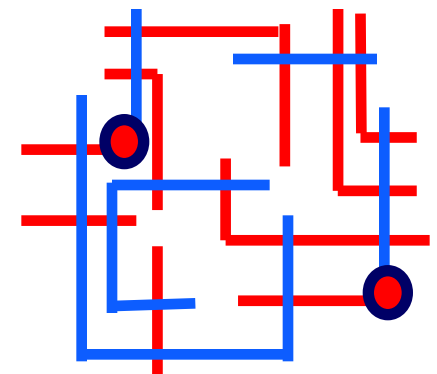
■ Minimum stitch insertion in double patterning

- Feature assignment into two masks
- Constraint graph is planar
 - Vertex: primitive feature
 - Edge : stitch candidate



■ Minimum via insertion in two-layer routing

- Wire assignment into two layers
- Constraint graph is planar
 - Vertex: wire segment cluster
 - Edge: via candidate



Conclusion

- Computational power enhancement is achieved
 - computer-aided design
 - proper graph theoretical problem analysis
 - sophisticate combinatorial algorithms
- To attack new problems
 - Powerful computation might not be enough
 - more proper graph theoretical problem analysis
 - more sophisticate combinatorial algorithms
 - latest and historical overview to find clue

Tribute to Professor Yoji Kajitani