Scope and Limit of Lithography to the End of Moore's Law

Burn J. Lin

tsmc, Inc.

What dictate the end of Moore's Law

- **Economy**
- **Device limits**
- **Lithography limits**

Litho Requirement of Critical Layers

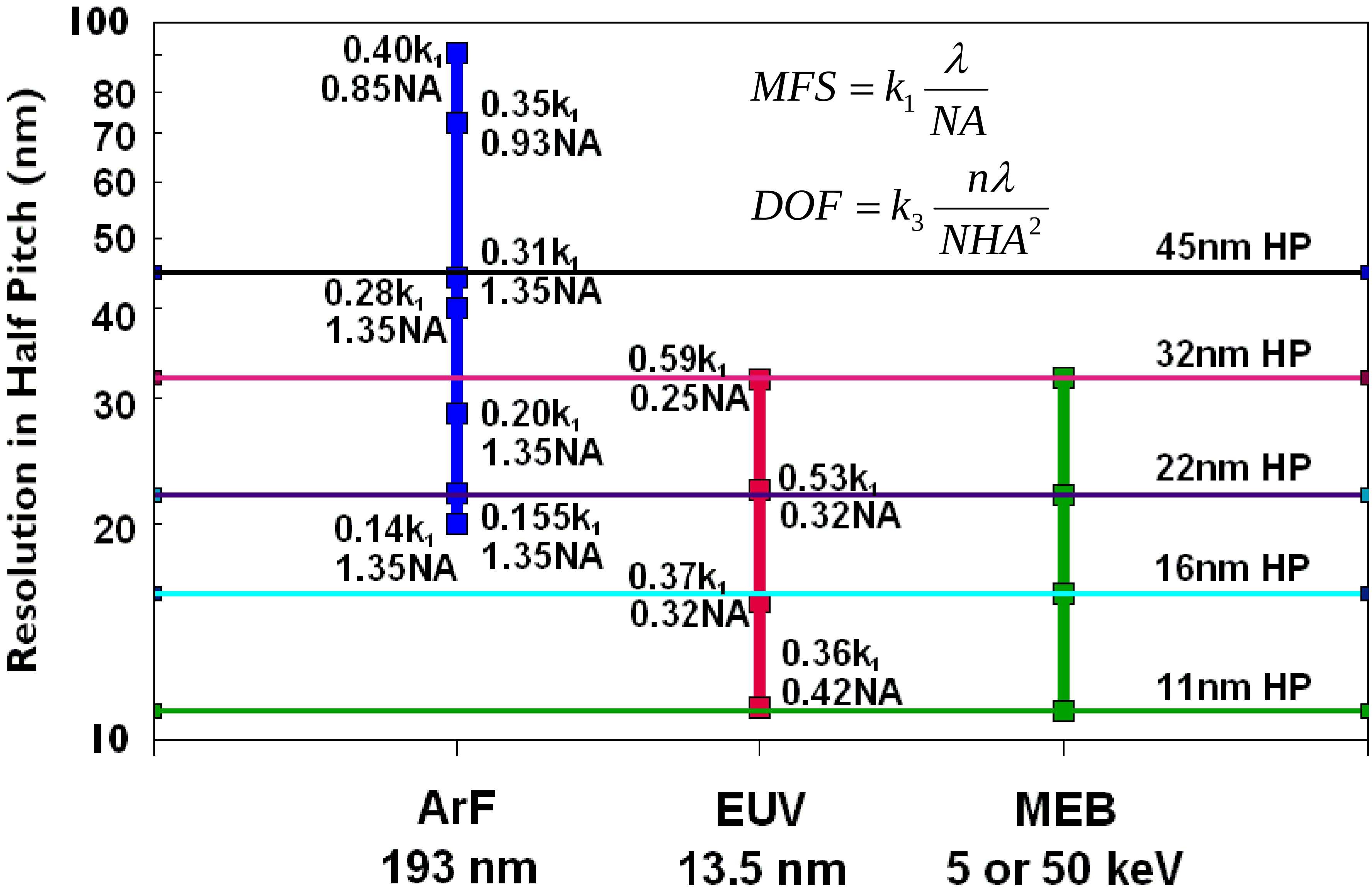
Logic Node (nm)	32	22	16	11	8
Poly Half Pitch (nm)	45	32	22	16	11
CD Uniformity (nm)	3.2	2.2	1.6	1.1	0.8
Overlay Accuracy (nm)	9.6	6.6	4.8	3.3	2.4

These are generic technology nodes that have no correlation to TSMC nodes

Pushing the Limits of Lithography

- **Pitch splitting with ArF water immersion**
- **Further wavelength reduction to EUV**
- **Multiple E-Beam Maskless lithography**

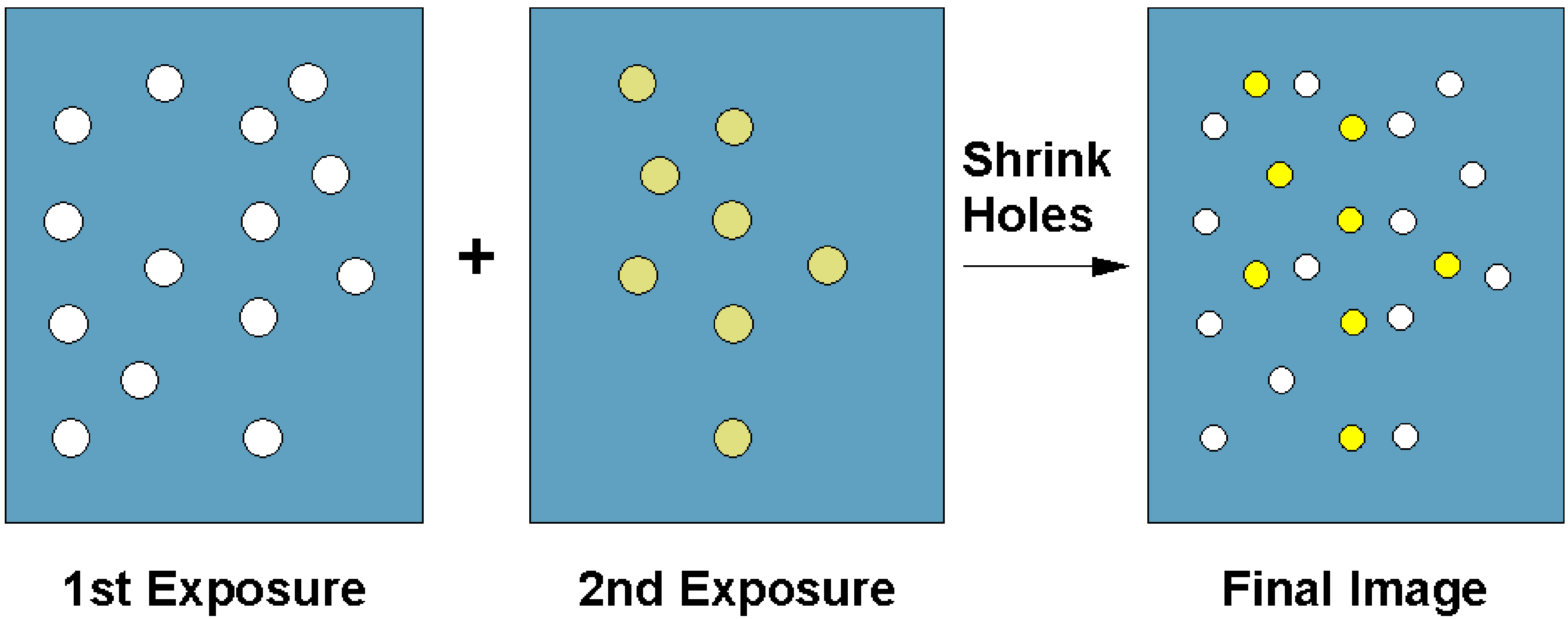
Resolution of Tools from ArF to MEB



Multiple Patterning

- **Double patterning => L + E + L + E = 2L2E**
  Triple patterning => 3L3E
- **Multiple patterning can be used for**
  - ***Pitch splitting***
  - ***Pattern trimming***
  - ***Spacers***

Pitch Splitting
Combining two patterns and shrink

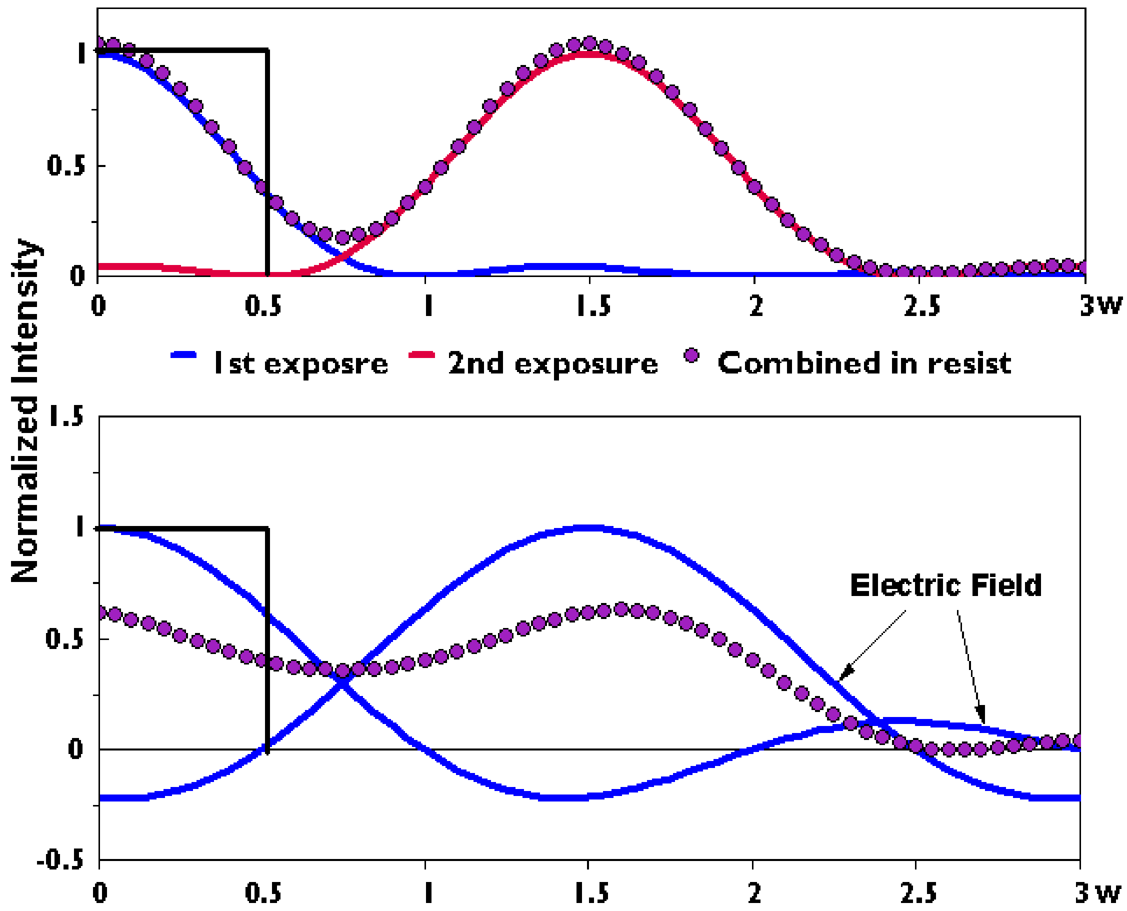


Combined Intensity in Resist

Incoherent combination of light with double exposure

Coherent combination with single exposure.

Partial coherence is better than coherence but still worse than incoherence.

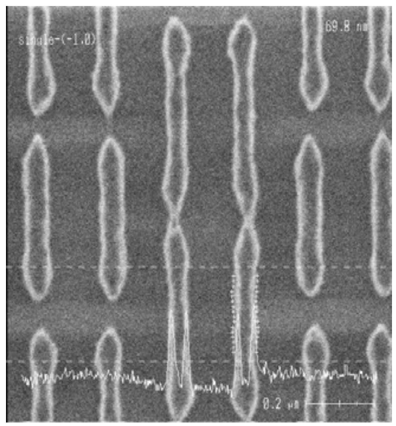


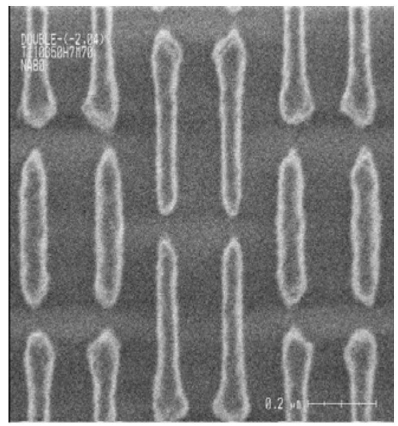
Better End Caps With Double Exposures

	Single exposure	Double exposures in resist	Double exposures through etch.

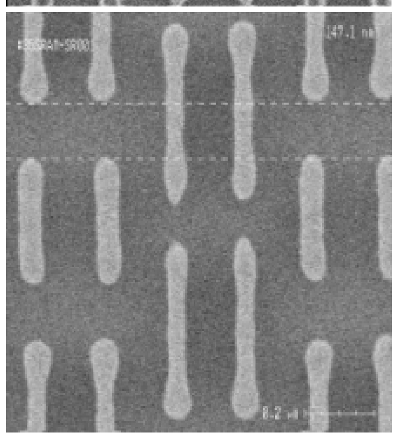
2 coatings
2 exposures
2 developments
2 etches

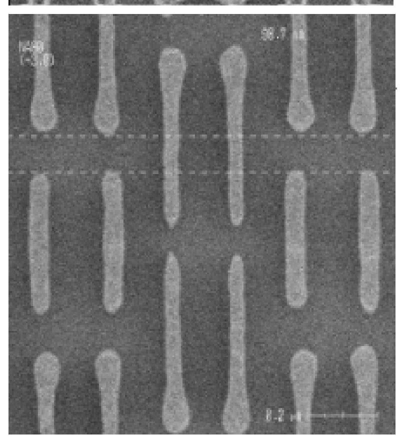
ADI

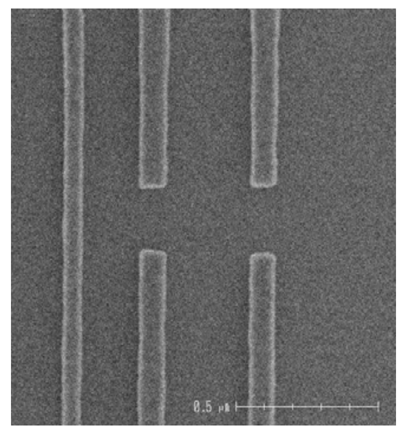




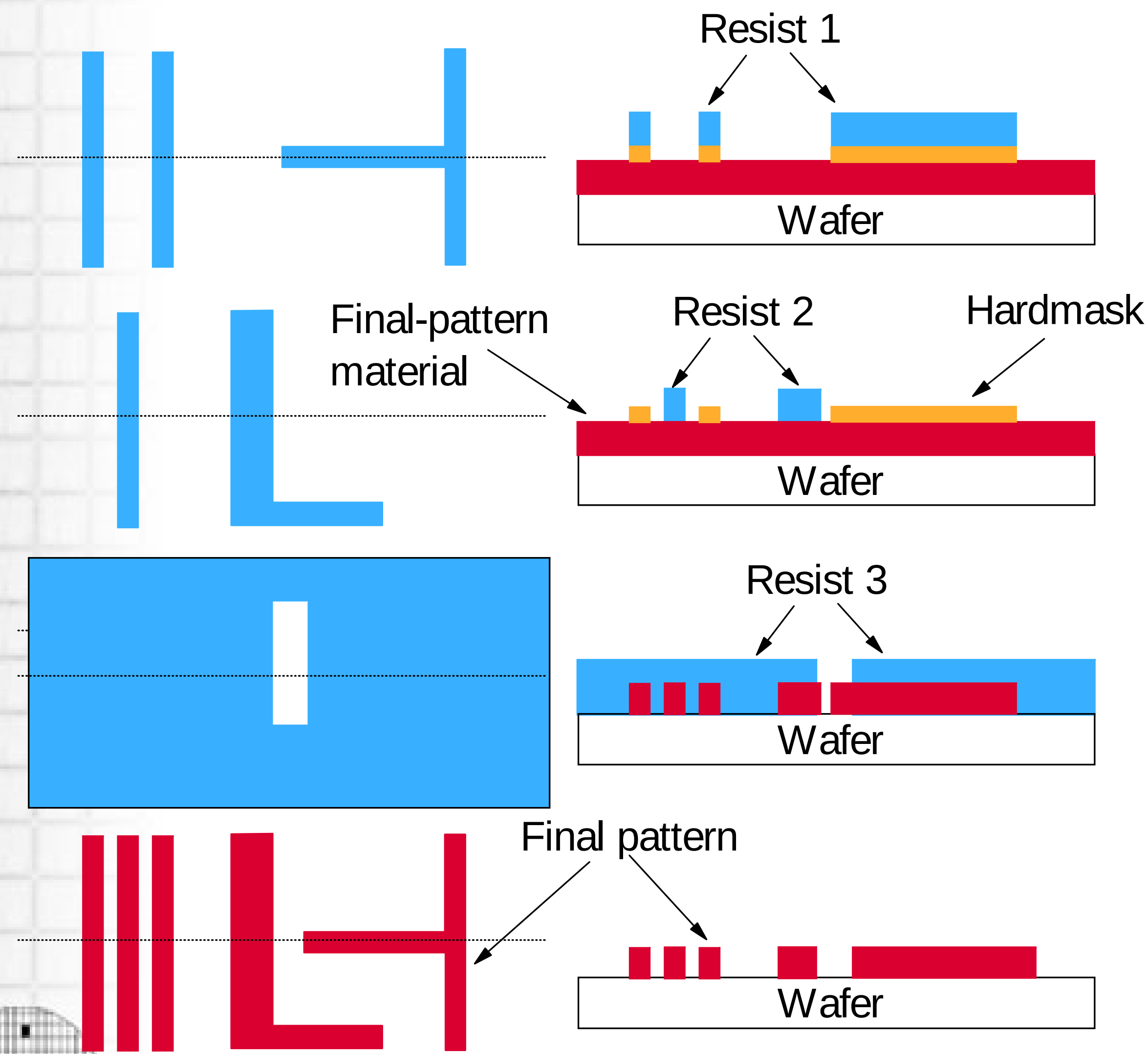
AEI







Triple Patterning Using Split Pitch and End Cutting



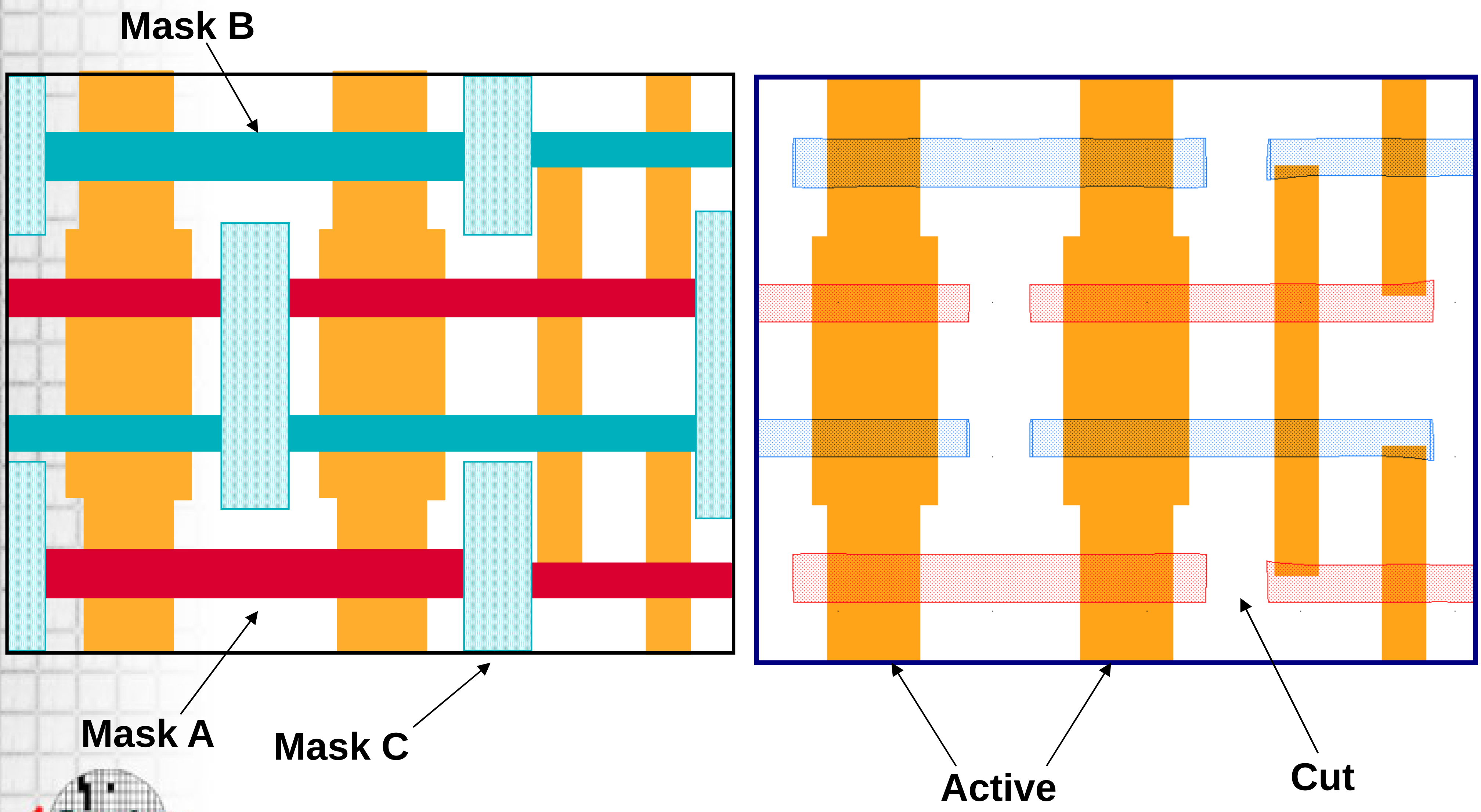
Resist-1 and etchd hardmask images

Strip resist 1, coat and image resist 2

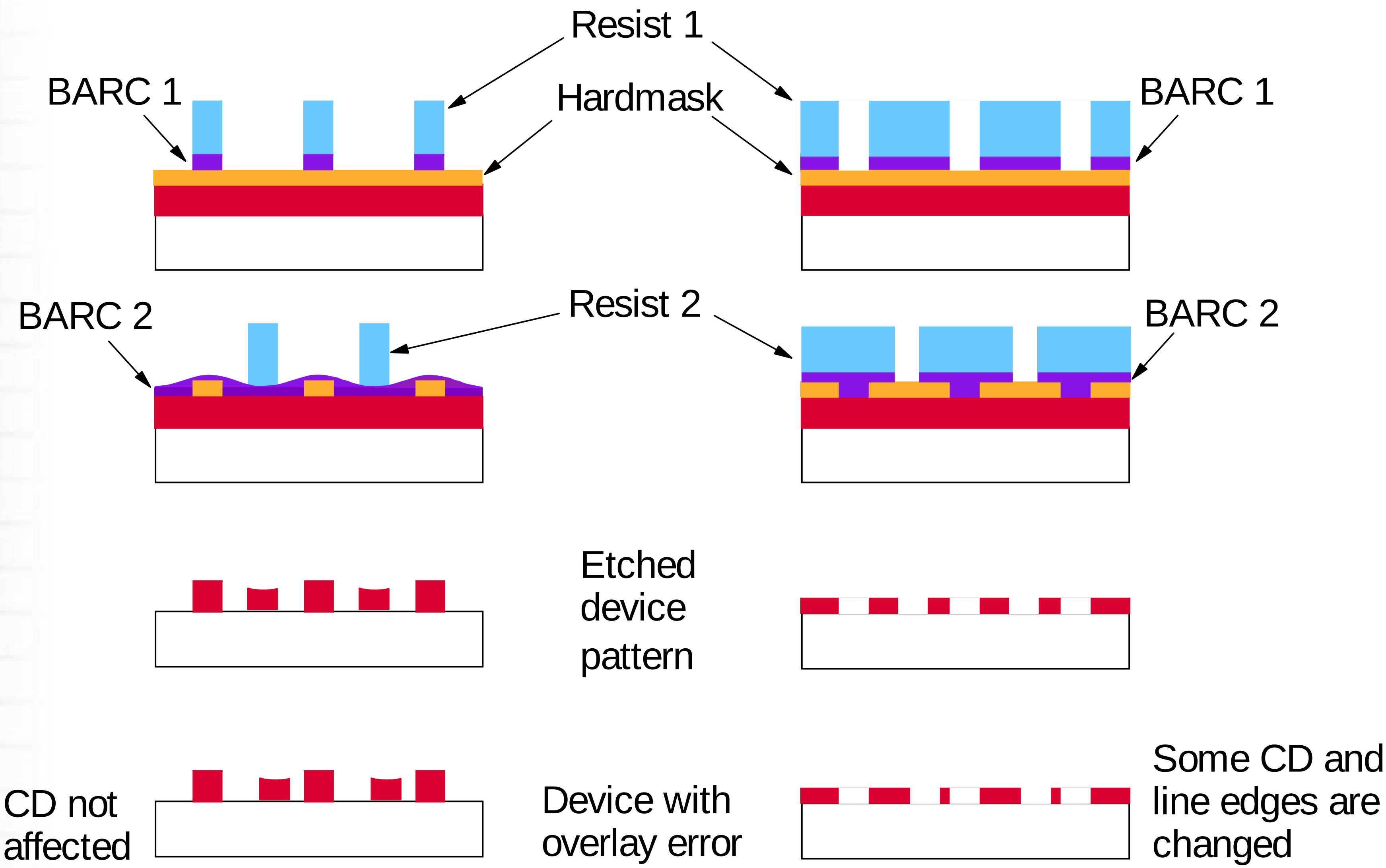
Etch final-pattern layer. Coat and image resist 3 to cut line end.

Final pattern from the end-cutting resist mask.

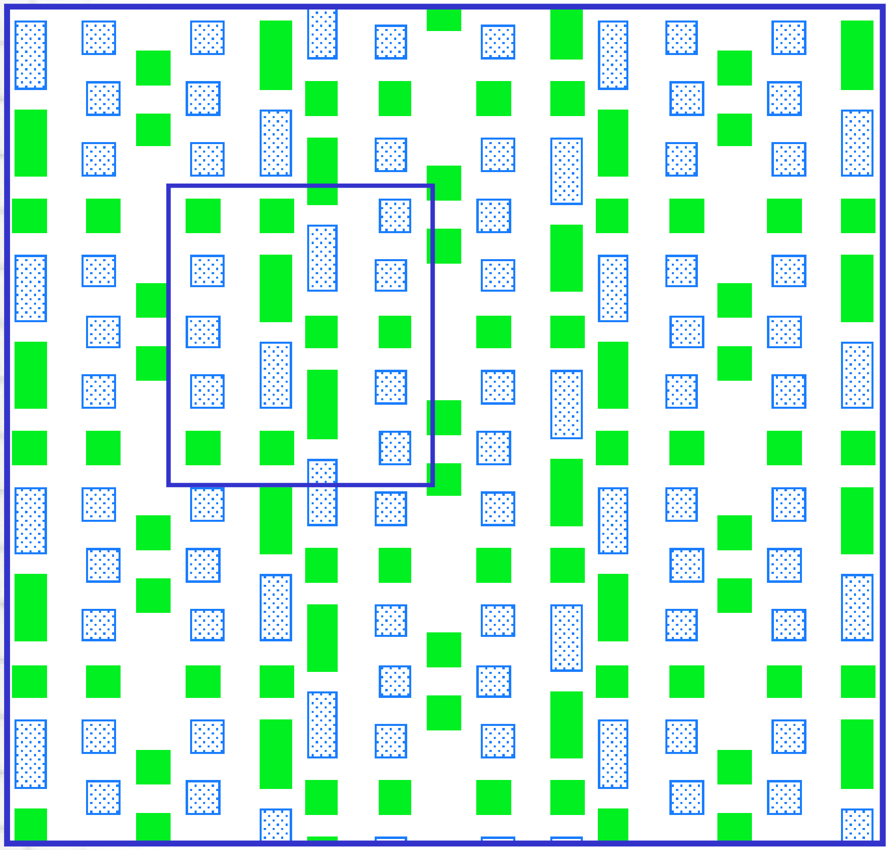
Split Pitch with Line-End Cutting



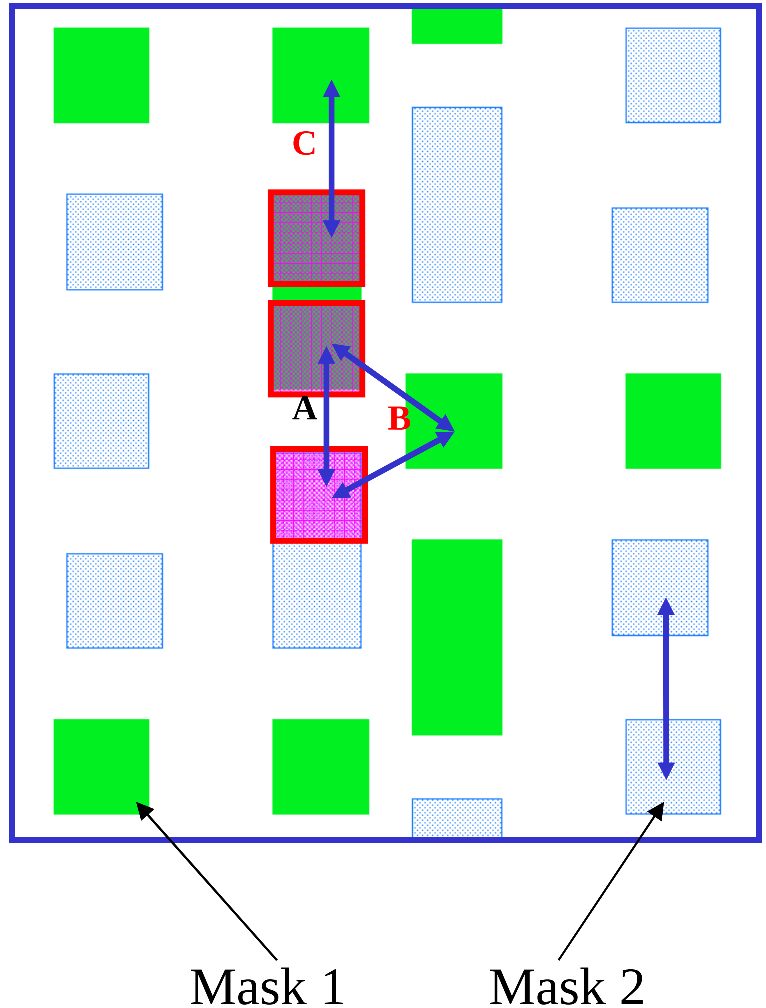
Realistic Considerations on DPT



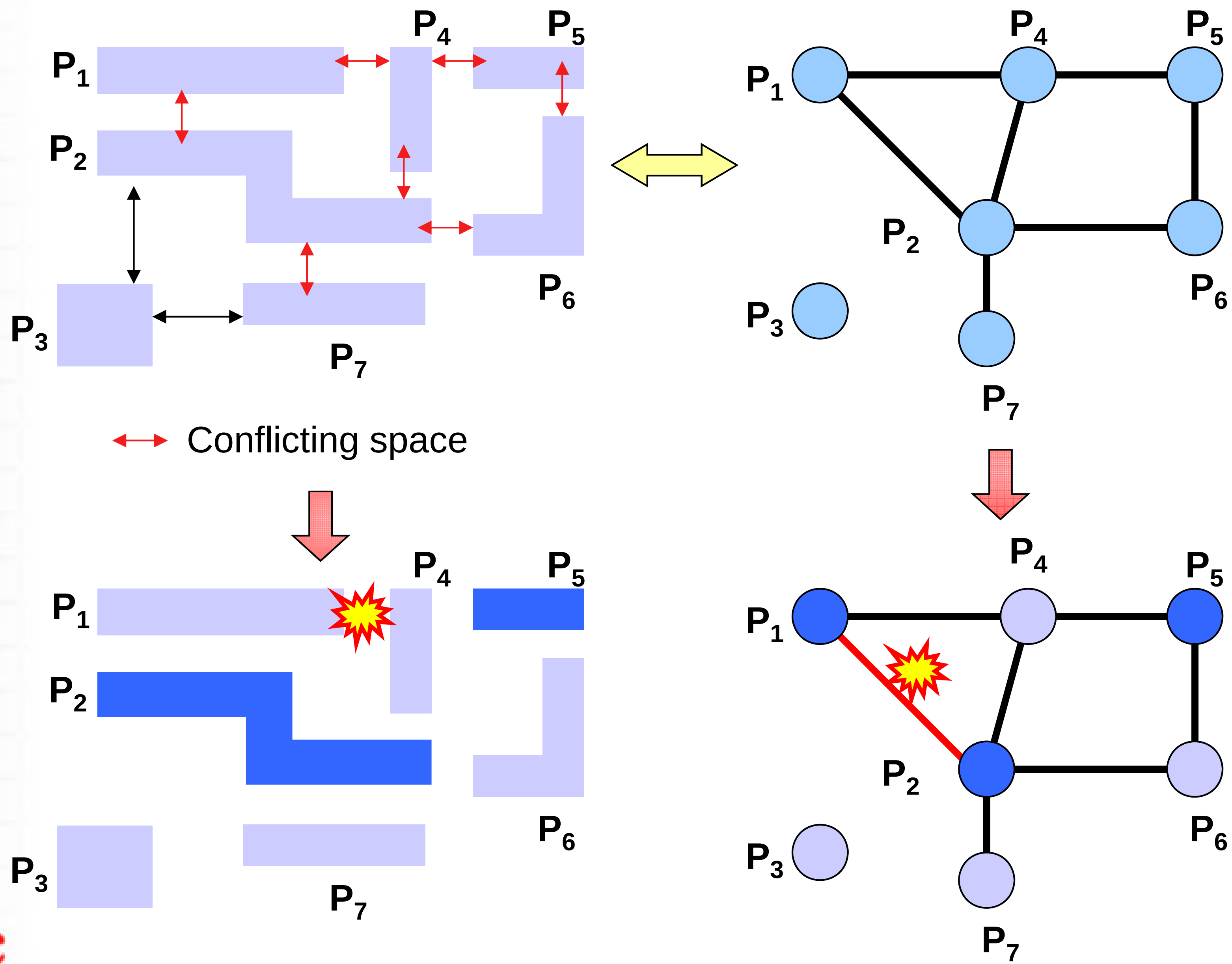
Contact Pitch Splitting



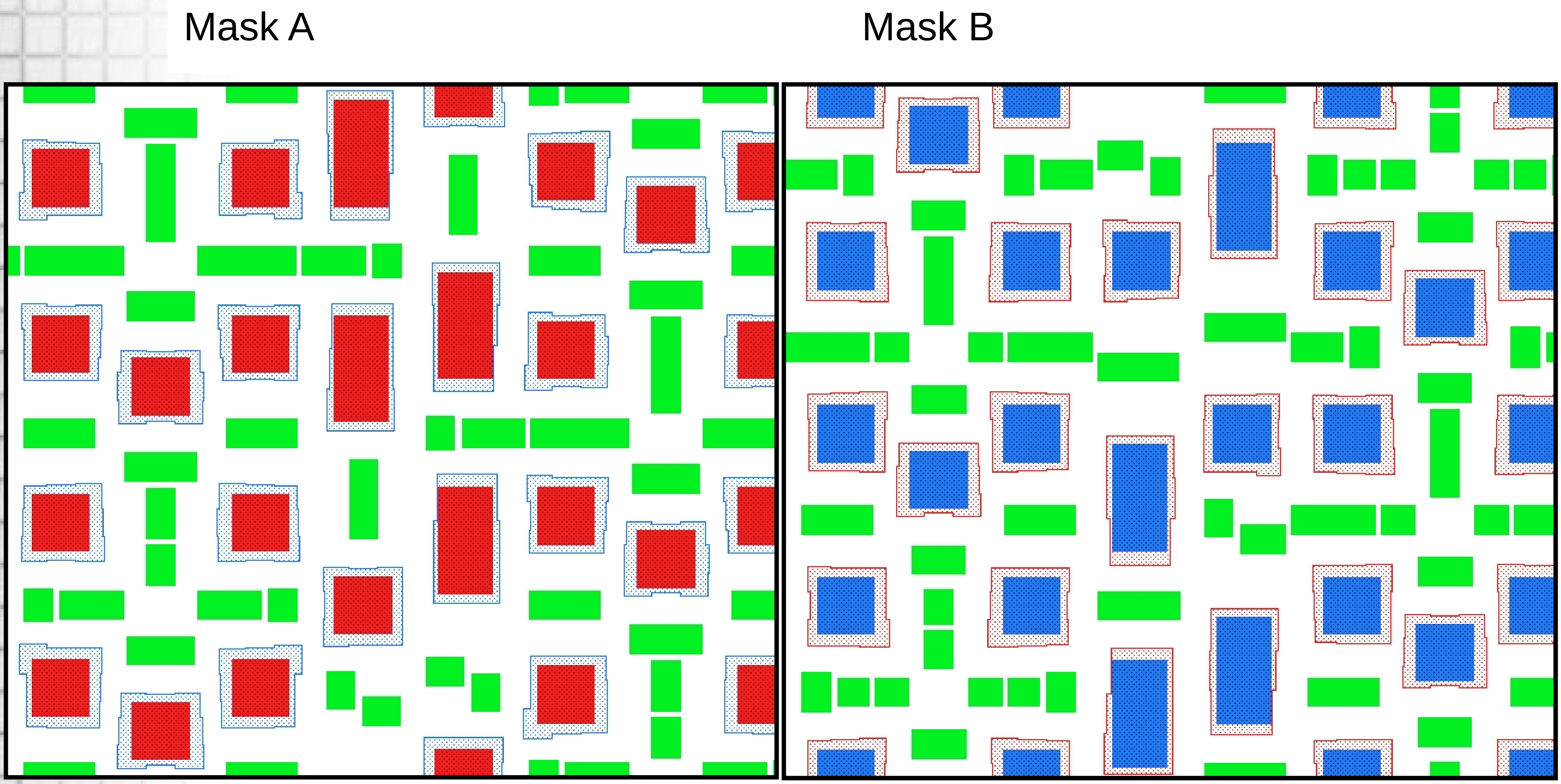
Watch out for G-rule violation



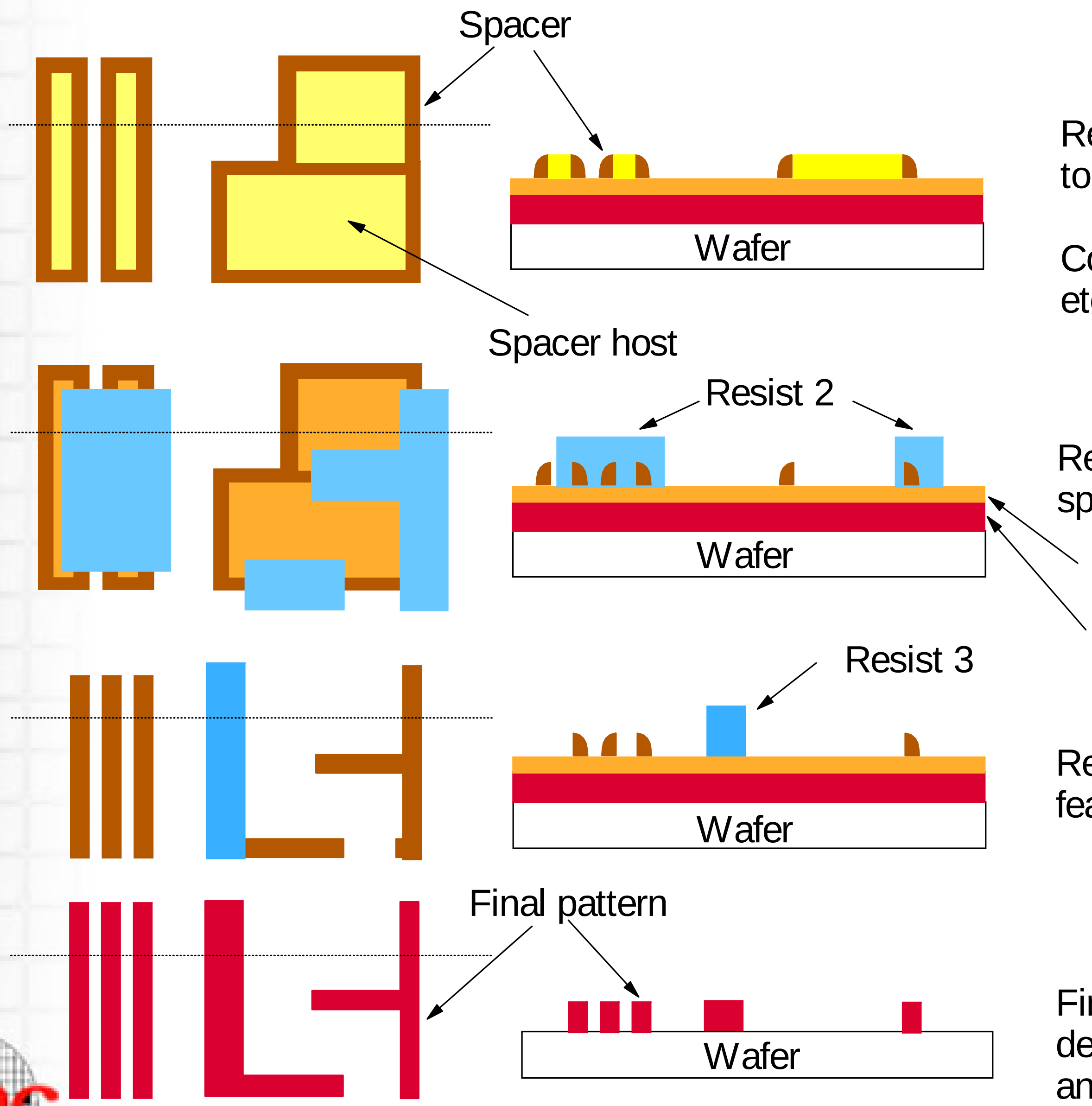
More G-Rule Violations



Split Masks with Hollow SB and OPC



Triple Patterning Using Spacers



Resist-1 image (not shown) is used to delineate the spacer host pattern.

Conformable coating & anisotropic etching produce sidewall spacers.

Resist-2 image protects selected spacers.

Resist-3 image is the etch mask for features larger than the spacer width.

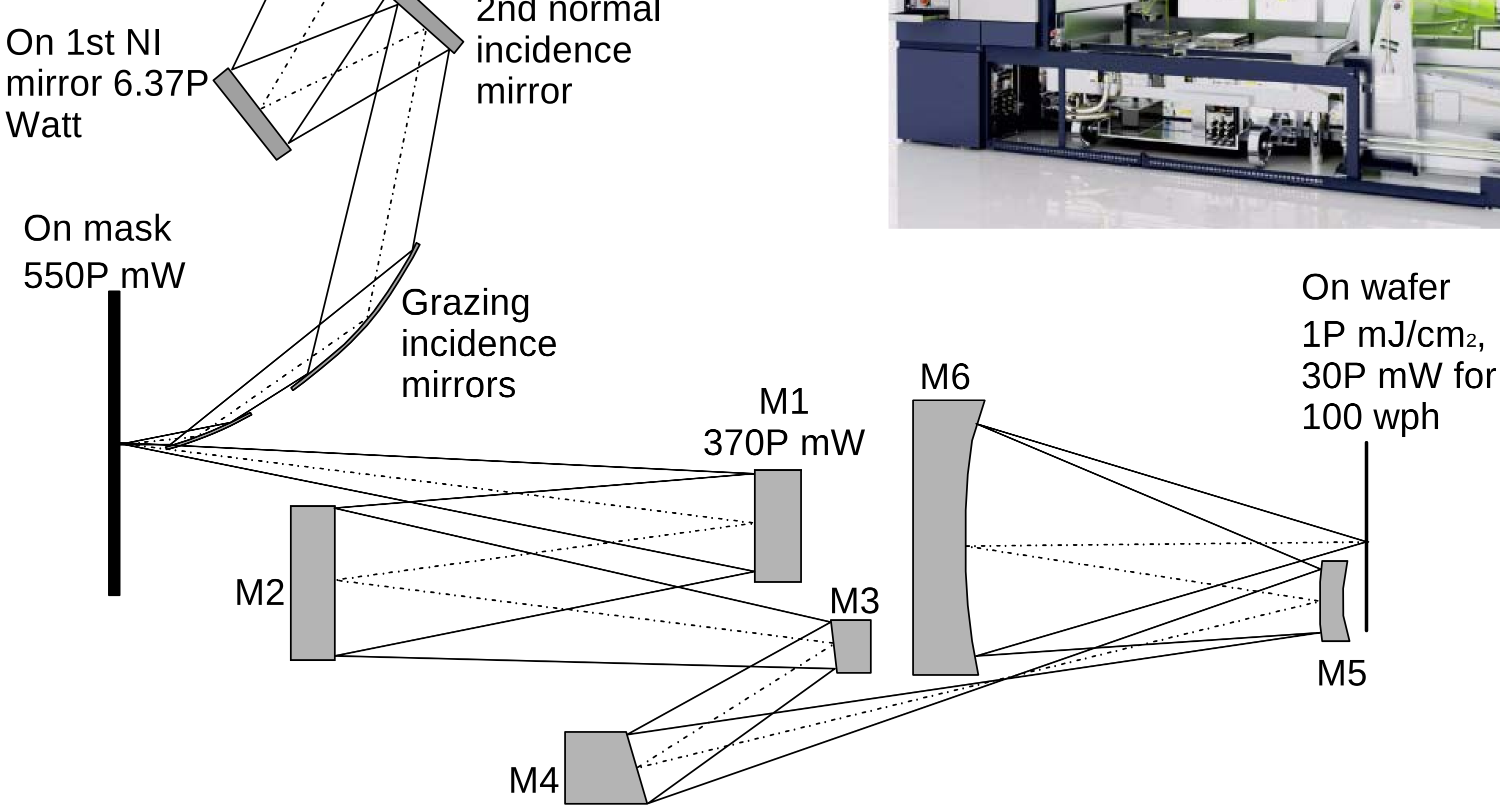
Final pattern from hardmask that was delineated with the composite spacer and resist-3 images.

Multiple Patterning in ArF Immersion

Logic Node	32nm	22nm	16nm	11nm	8nm
Poly Half Pitch (nm)	45	32	22	16	11
Contact Half Pitch (nm)	50	35	25	17	12
Metal Half Pitch (nm)	45	32	22	16	11
Immersion k_1 for Poly	0.31	0.22	0.15	0.11	0.08
Immersion k_1 for Contact	0.35	0.24	0.17	0.12	0.08
Immersion k_1 for Metal	0.31	0.22	0.15	0.11	0.08
Multiple Patterning	1	2	2	3	4
Immersion k_1 for Poly	0.31	0.45	0.31	0.34	0.31
Immersion k_1 for Contact	0.35	0.49	0.35	0.36	0.34
Immersion k_1 for Metal	0.31	0.45	0.31	0.34	0.31

EUV Lithography

EUV Illuminator and Imaging Lens

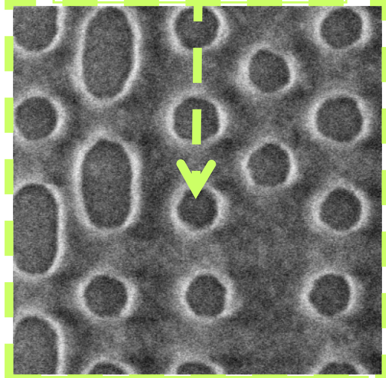


EUVL Results

SRAM192	7	7.6	8.2	8.8	9.4	10	10.6	11.2	11.8	12.4	13
-0.12											
N-node			56.94	60.14	62.31	61.47	60.82	63.63	64.77		
Vcc			58.18	60.83	67.31	61.13	68.38	68.87	66.21		
-0.08											
N-node			58.85	55.98	63.52	57.41	63.57	63.96	64.63		
Vcc			61.65	61.40	66.16	64.53	65.69	69.50	67.32		
-0.04											
N-node	51.22	53.20	56.71	55.74	61.53	59.83	62.01	63.02	63.33	65.64	67.30
Vcc	57.27	62.16	57.09	61.61	64.91	59.83	63.86	68.54	68.80	69.24	72.79
0											
N-node	53.06	57.13	59.56	63.41	59.31	62.25	60.33	61.39	65.43	65.65	72.09
Vcc	59.20	57.11	59.17	65.76	62.28	68.12	67.42	68.64	68.43	64.19	70.55
0.04											
N-node	51.14	56.45	58.43	58.00	61.07	59.64	61.72	67.67	64.18	70.59	72.64
Vcc	59.34	59.57	59.93	65.42	63.89	66.20	65.95	65.13	71.30	74.14	72.15
0.08											
N-node			59.35	58.44	63.15	64.75	63.34	60.81	63.88		
Vcc			59.40	64.68	68.63	70.89	67.74	66.22	69.56		
0.12											
N-node			56.64	59.16	60.19	61.03	64.82	66.59	65.14		
Vcc			65.44	62.11	64.10	64.43	68.80	68.55	72.57		

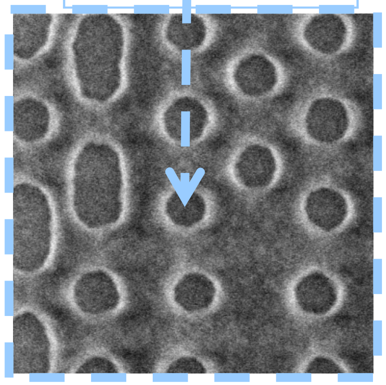
N32 SRAM contact holes

CD = 52 nm



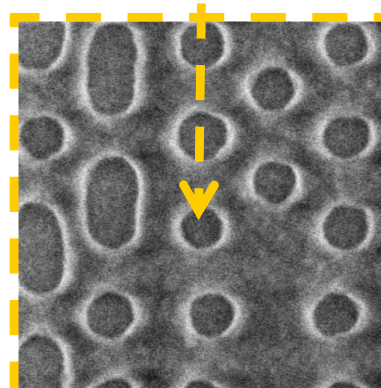
Focus = 0 nm

CD = 53 nm



Focus = - 40 nm

CD = 54 nm



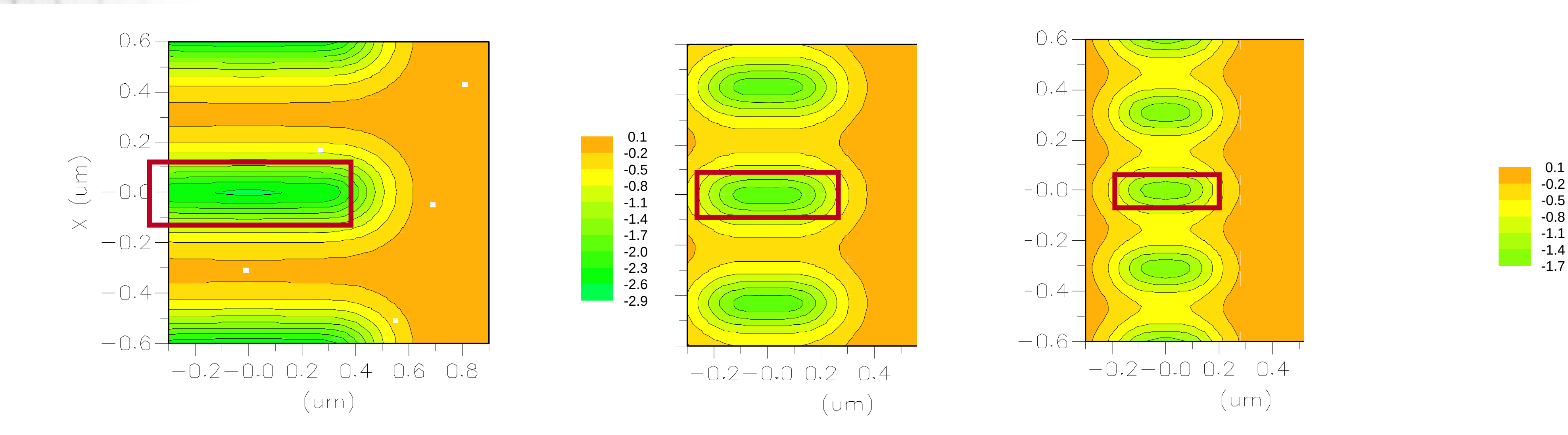
Focus = + 40 nm

k_1 of EUVL

Node	22nm	16nm	11nm	8nm
NA	0.25	0.32	0.32	0.45
EUV k_1 for Poly	0.59	0.52	0.38	0.37
EUV k_1 for Contact	0.65	0.59	0.40	0.40
EUV k_1 for Metal	0.59	0.52	0.38	0.37

One Implication of k_1

Contrast at Line End



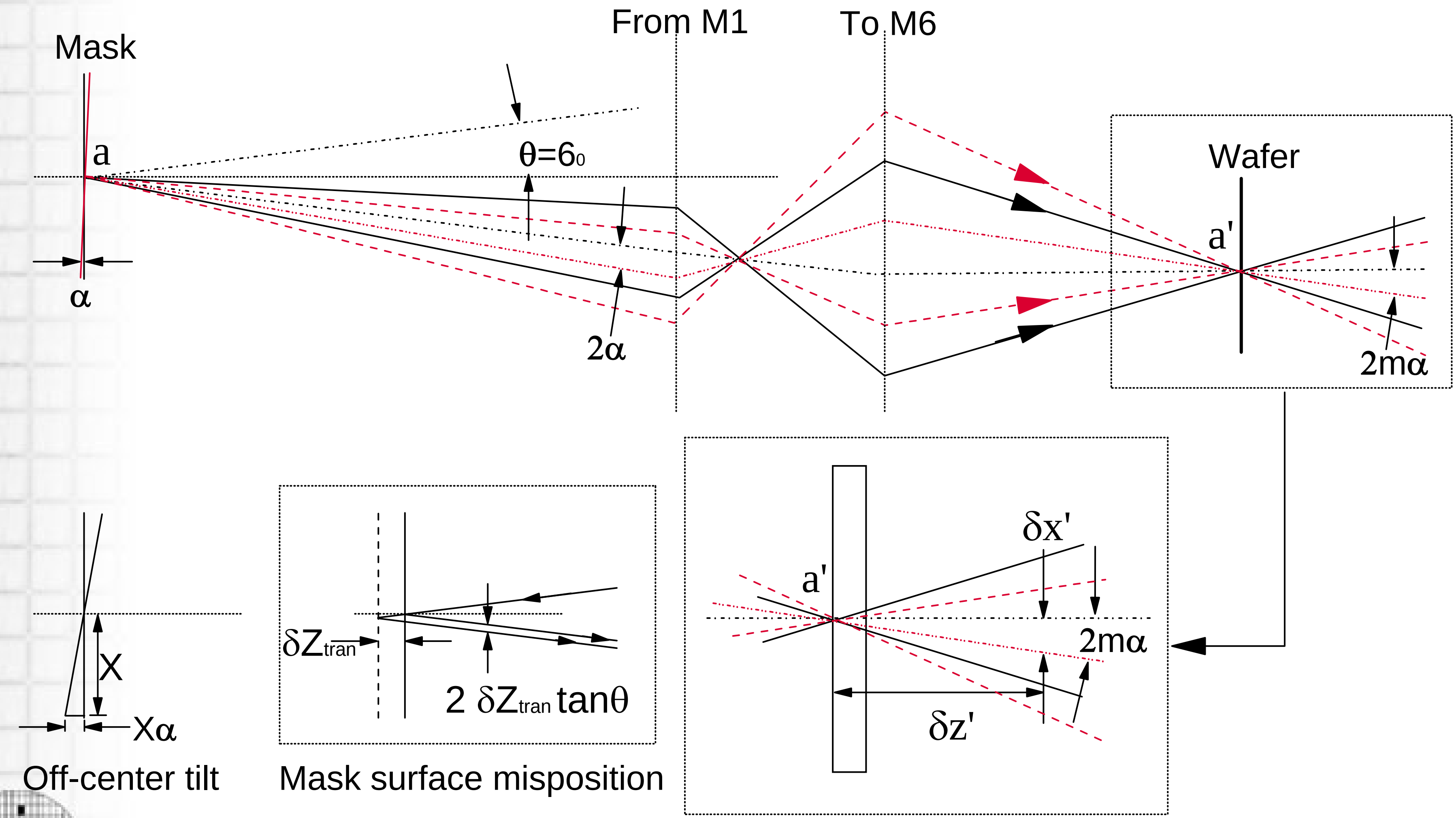
250nm node,
k_1=0.63 λ=248nm
NA=0.5

180nm node,
k_1=0.47 λ=248nm
NA=0.54

130nm node,
k_1=0.42 λ=248nm
NA=0.67

Disk Illumination $\sigma = 0.8$

Positioning Errors due to Mask Rotation and Translation

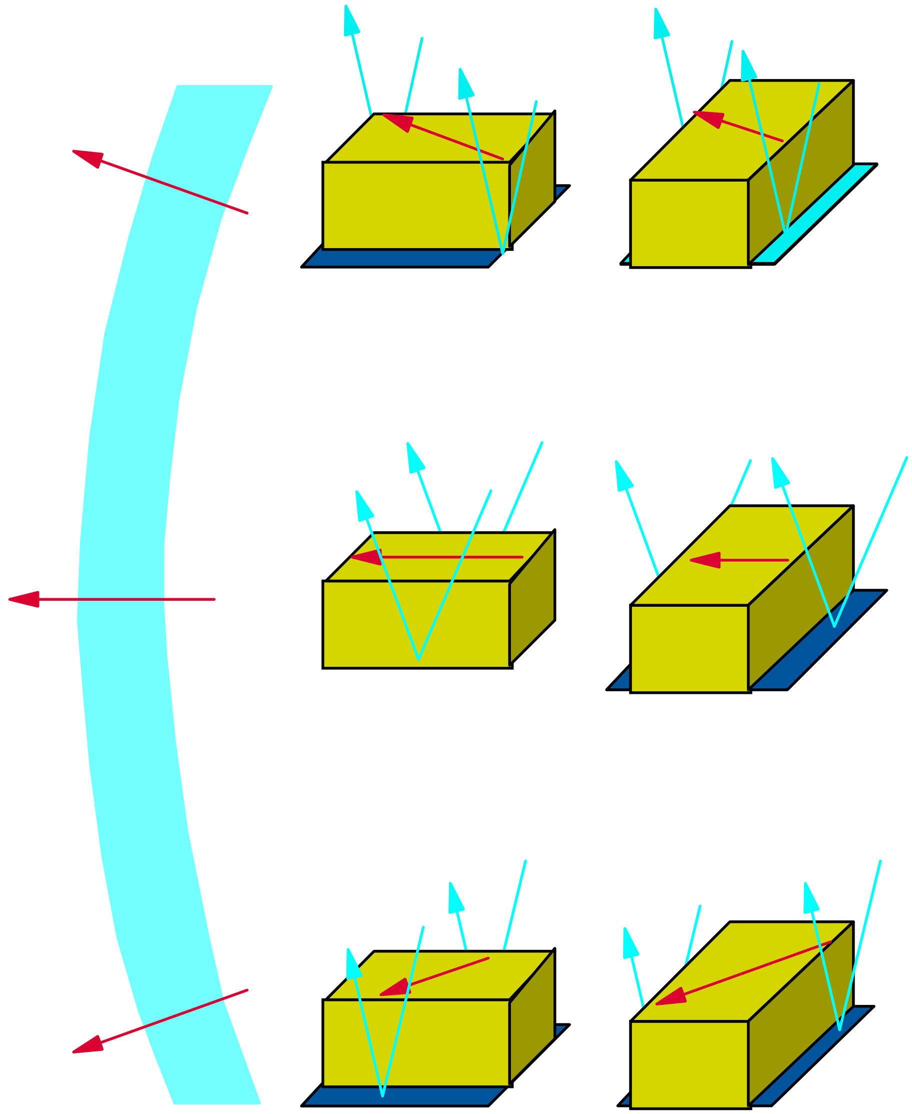


EUV Mask Flatness Requirement

Node	22nm	16nm	11nm	8nm
θ (deg)	6.0	6.0	6.0	8.0
$\tan(\theta)$	0.105	0.105	0.105	0.141
Mask flatness required (nm)	46.5	33.8	23.3	12.6

Flatness of best immersion mask: 500 nm

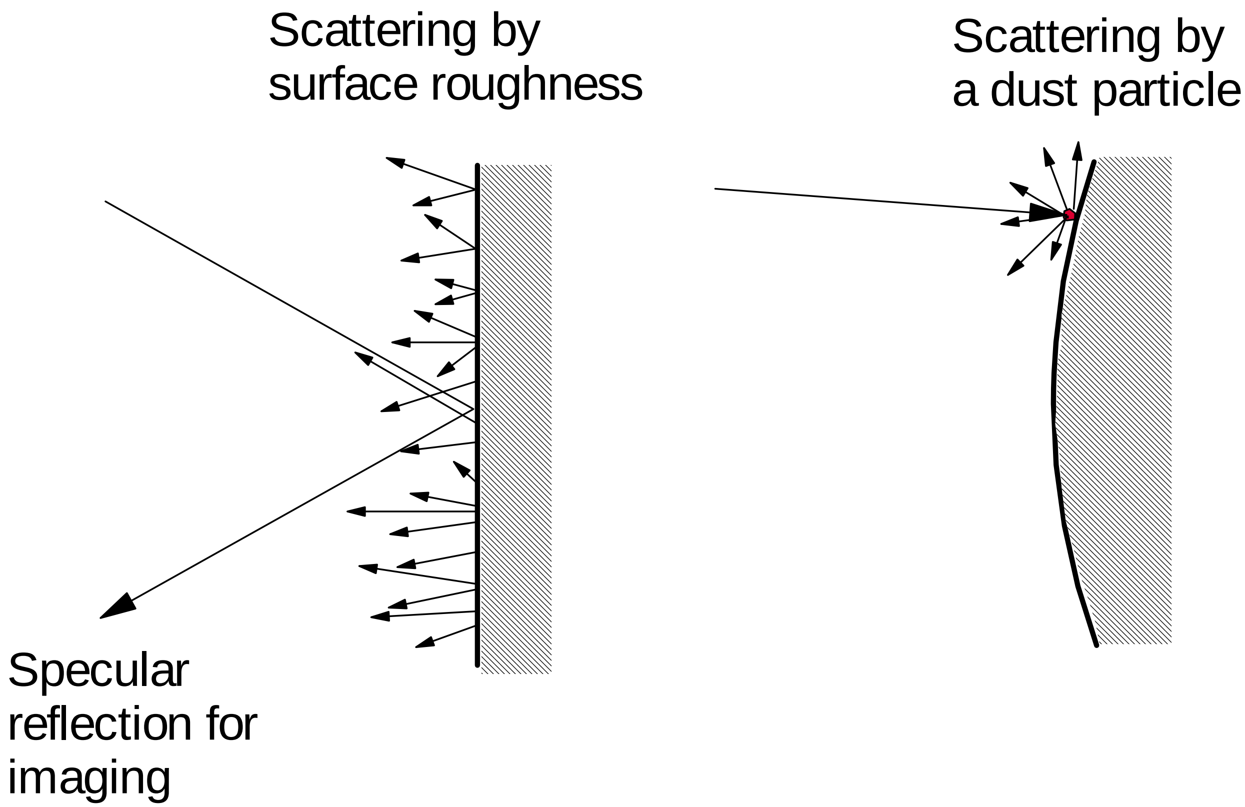
Shadowing from Oblique Illumination



CD needs to be compensated according to feature location and orientation

(Courtesy Lorusso, IMEC)

Stray Light from Lens Surfaces



EUV flare ~10% vs. < 0.1% UV flare

OPC Considerations

- Uneven flare and shadowing effect require **field-dependent OPC**.
- Inter-field flare necessitates **dummy exposures** at wafer edge.
- Flare signature if inconsistent between scanners, requires **dedicated mask**.
- **Flare stability** still unknown.

On Lack of Pellicle

- Developed **reticle box** for freedom from contamination during storage, transportation, loading/unloading.
- Attraction of particulates by the **electrostatic mask chucking** has to be minimized.
- Need to block line-of-sight exposure to **Sn debris** source.
- Maintain high vacuum. Minimize presence of trace **Carbon-containing vapor and H_2O vapor**.

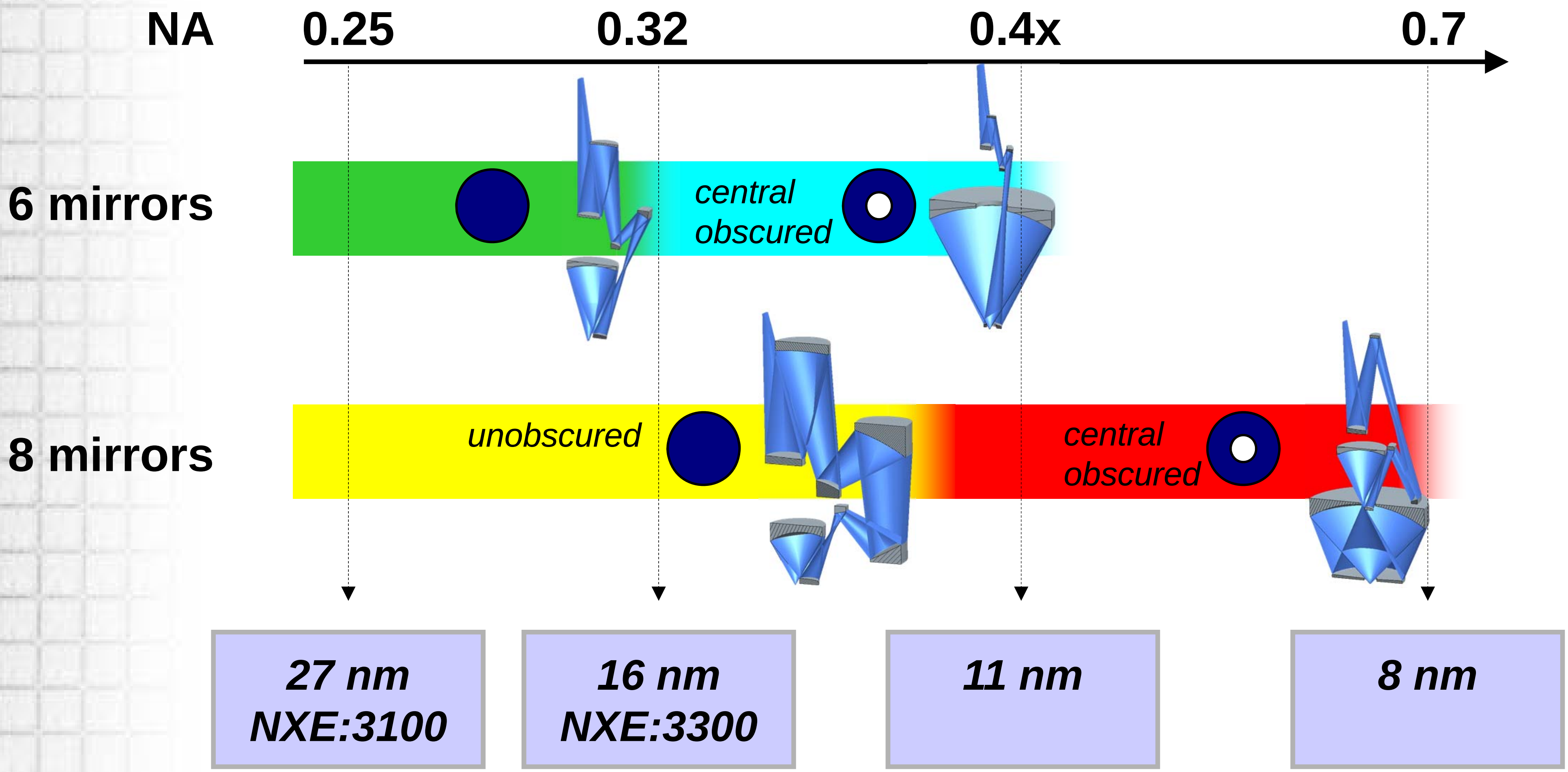
Mask and Pellicle

Summary of EUVL Concerns

- Need 250 W at IF. Currently < 10 watt.
- Mask defect and flatness.
- Field-dependent OPC.
- Time-dependence of OPC can be detrimental.

EUV Extendibility

High-NA EUV Design Solutions



schematic designs – for illustration only.

W. Kaiser et al., SPIE 2008

NA and k_1 of Photon Tools

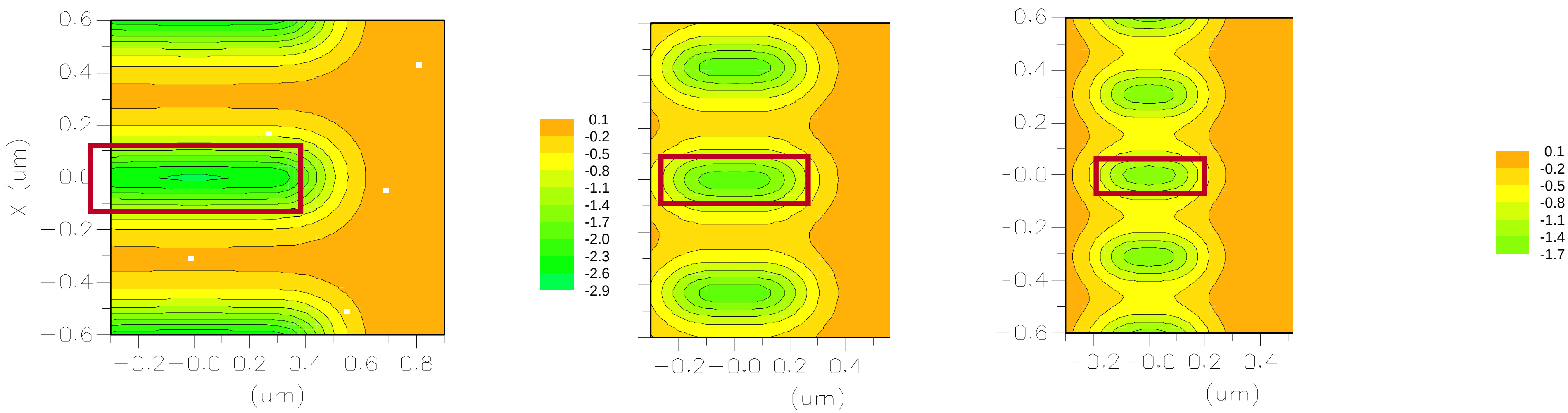
Node		22nm	16nm	11nm	8nm
Half pitch (nm)		32	22	16	11
ArF water immersion	λ (nm)	193	193	193	193
	NA	1.35	1.35	1.35	1.35
	k_1	0.22	0.15	0.11	0.08
EUV at constant k_1	λ (nm)	13.5	13.5	13.5	13.5
	NA	0.25	0.36	0.50	0.73
	k_1	0.59	0.59	0.59	0.59
EUV at diminishing k_1	λ (nm)	13.5	13.5	13.5	13.5
	NA	0.25	0.32	0.32	0.45
	k_1	0.59	0.52	0.38	0.37

Cannot maintain constant k_1 because of

- Diminishing DOF
- Expensive NA

One Implication of k_1

Contrast at Line End



250nm node,
k_1=0.63 λ=248nm
NA=0.5

180nm node,
k_1=0.47 λ=248nm
NA=0.54

130nm node,
k_1=0.42 λ=248nm
NA=0.67

Disk Illumination σ = 0.8

DOF of EUV

Node		22nm	16nm	11nm	8nm
EUV at diminishing k_1	λ (nm)	13.5	13.5	13.5	13.5
	NA	0.25	0.32	0.32	0.45
	k_1	0.593	0.521	0.379	0.367
DOF (k_3)		0.612	0.557	0.242	0.235
Theoretical (nm)		520	286	124	59
Experimental (nm)		300			

DOF determined with common E-D window

- **0.4:0.6 Resist line : space**
- **Allowance for mixed pitches**

13.5nm light may be reaching physical resolution & DOF limits at 11nm Half Pitch or earlier.

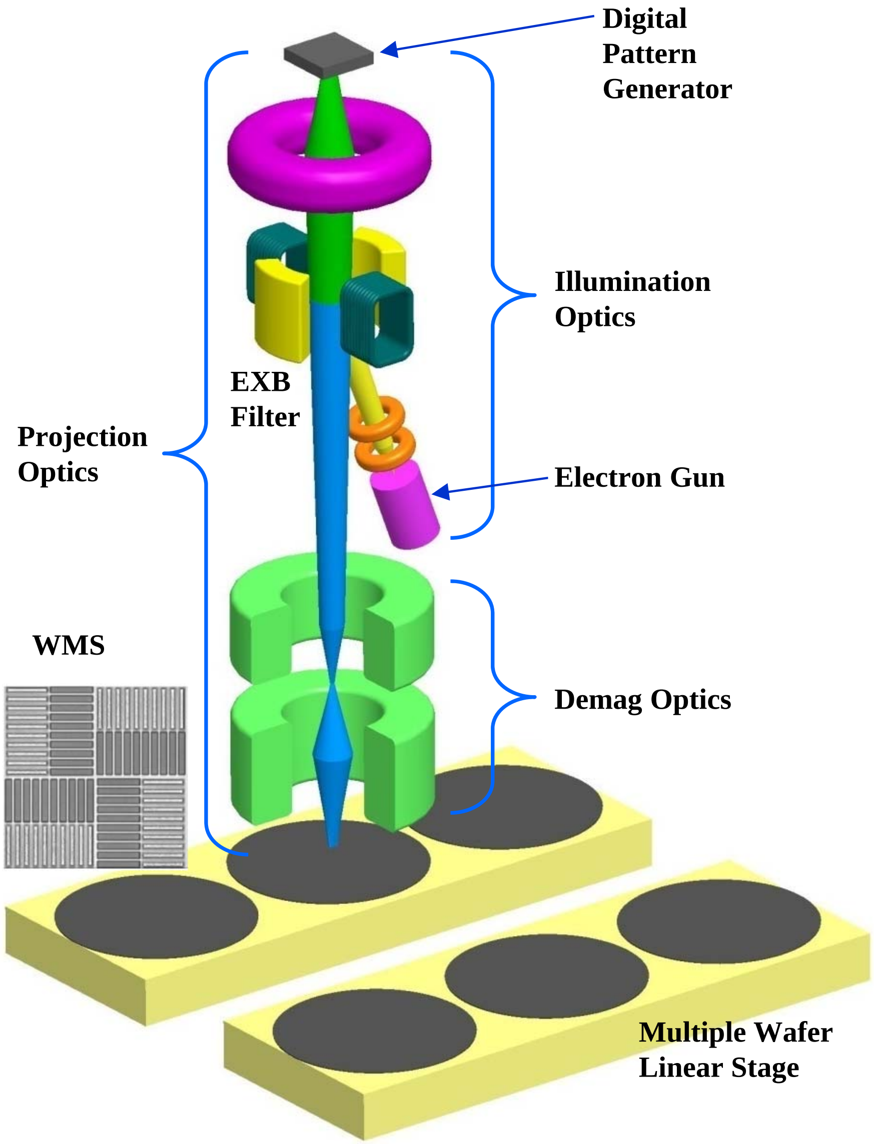
It may reach the economic limit much earlier.

Multiple E-Beam

Maskless Lithography

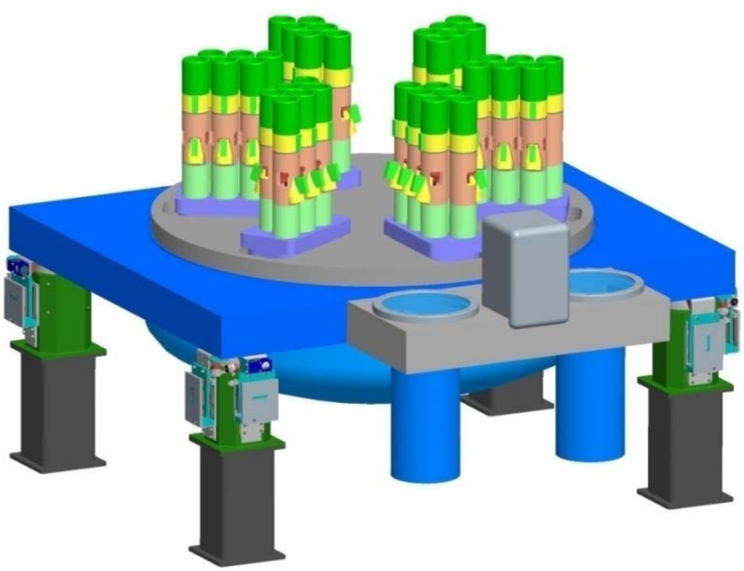
REBL System

- Reflective Electron Optics
- Digital Pattern Generator (DPG)
- TDI (Temporal Dose Integration)
- Optical Wafer Registration
- Maglev Stage Technology

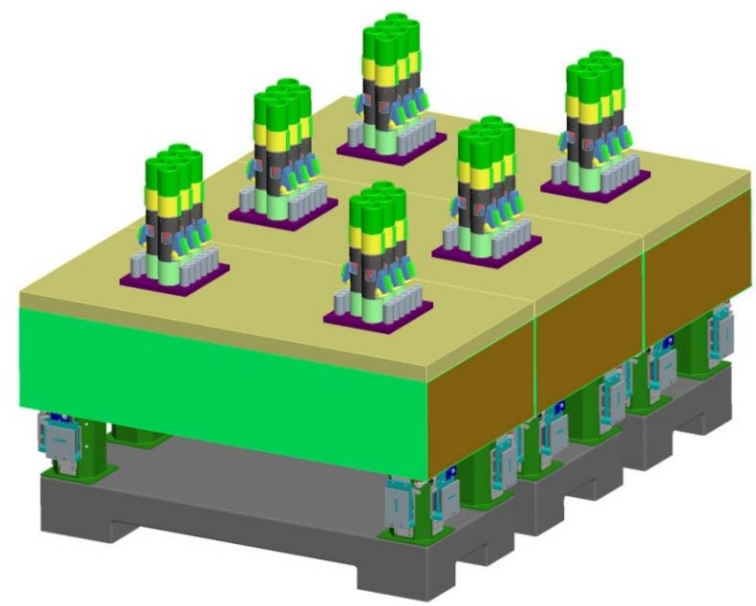


Rotary & New Linear Stages for REBL HVM

- E-beam column has to have 10-cm diameter or smaller.
- HVM throughput goals are similar in both stages.
- Stage design, data path, and rendering algorithms are simpler for linear stage.



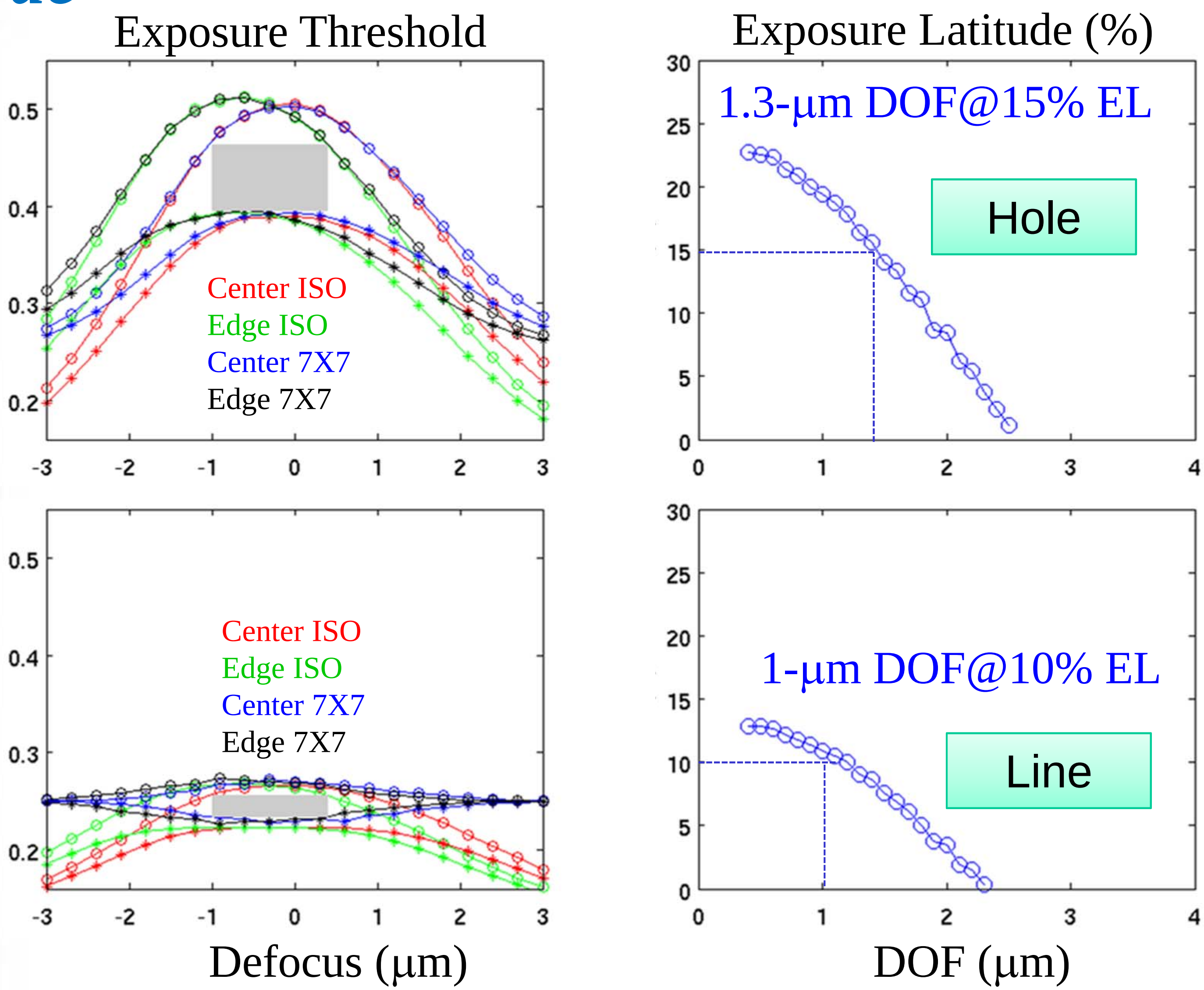
HVM Rotary Design, 36 Columns



HVM Linear Design, 36 Columns

100keV Expo. Lat. & DOF @1.5μA(75 wph)

10nm Node



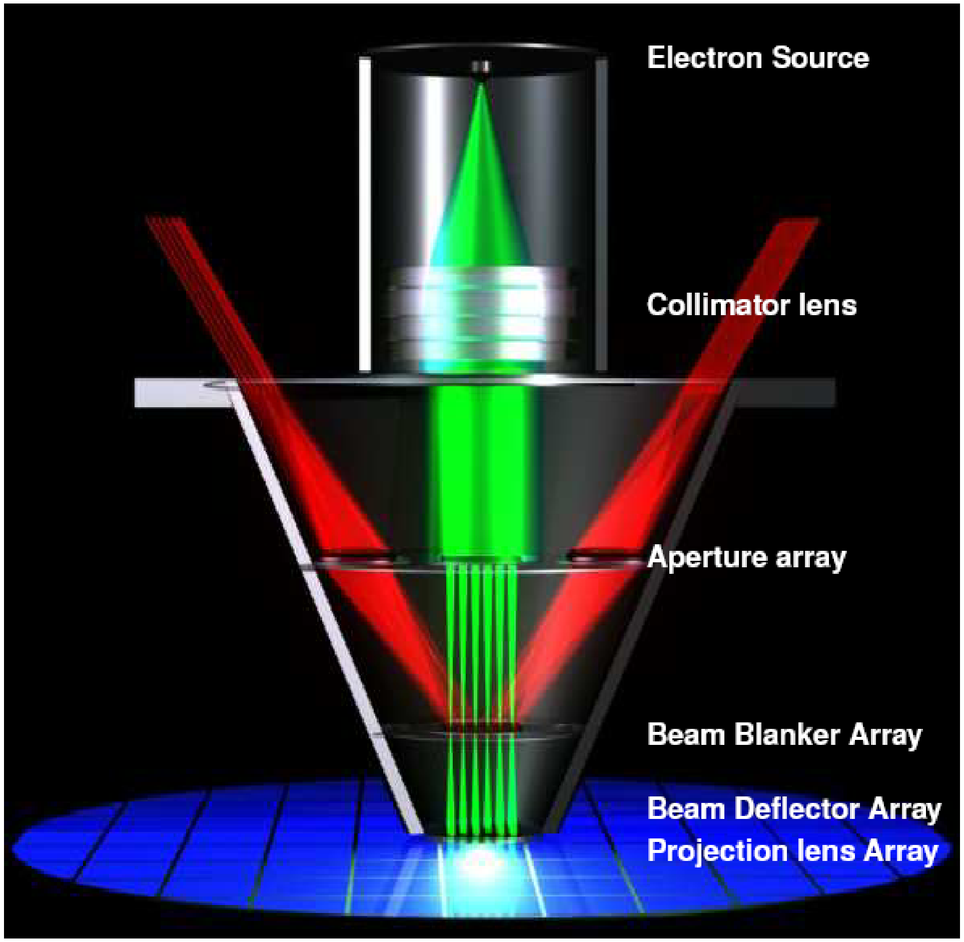
100 keV		
Hole	Iso 7x7	
	HP 21 nm	
	PR 65 nm	
Line	Iso 7	
	HP 15 nm	
	PR 50 nm	

Resist scattering and 10-nm blur by acid diffusion are included.

WCwang & PYLiu

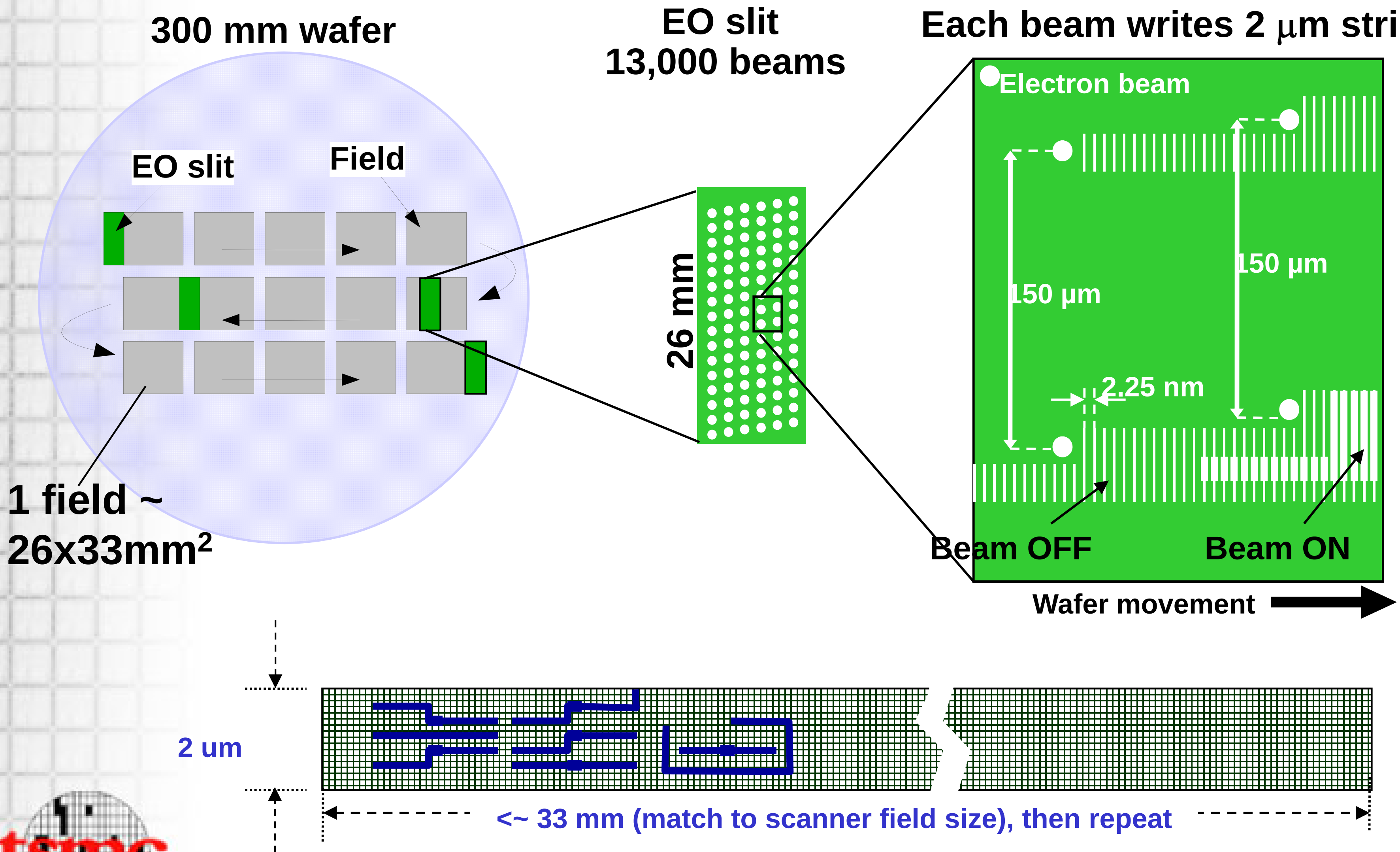
MAPPER Technology

- Single electron source split in 13,000 Gaussian beams
- V_{acc} = 5 keV
- Apertures are imaged on substrate through 13,000 micro lenses
- MEMS-stacked static electric lenses.
- Optical-switch, CMOS-MEMS blanker array
- Simple B&W bitmap data through light signal



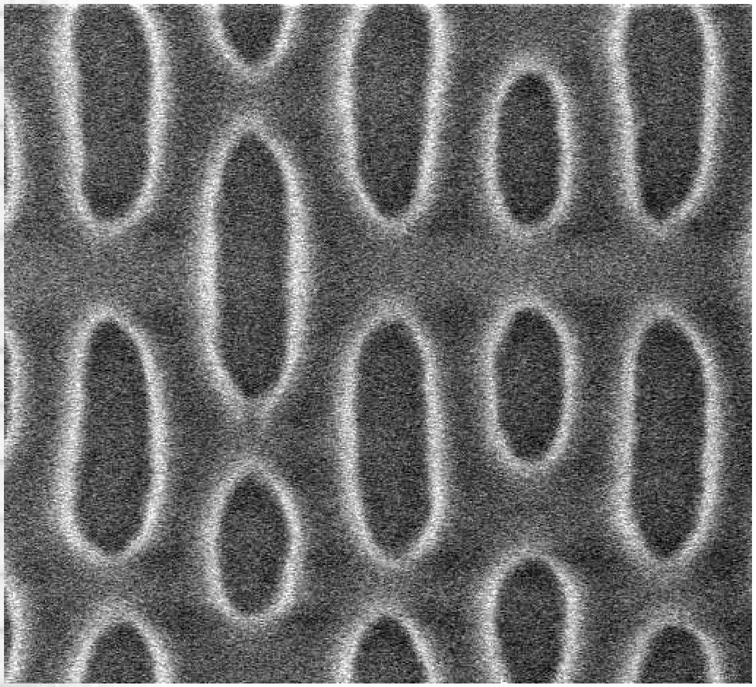
* Infomation from MAPPER Lithography.

Direct Write Scheme

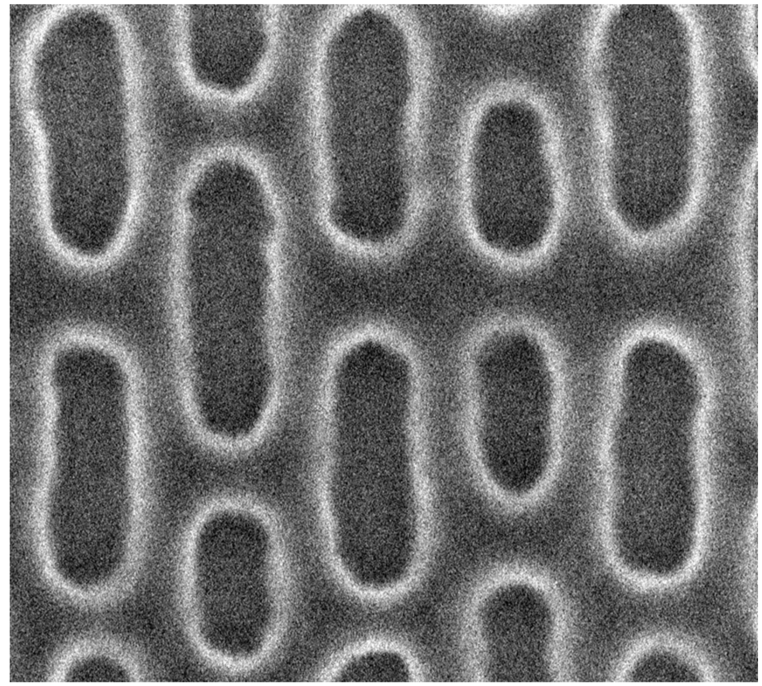


Each beam writes 2µm width by up to 33mm long stripe.

OPCed Immersion Image vs EPCed 5keV Image



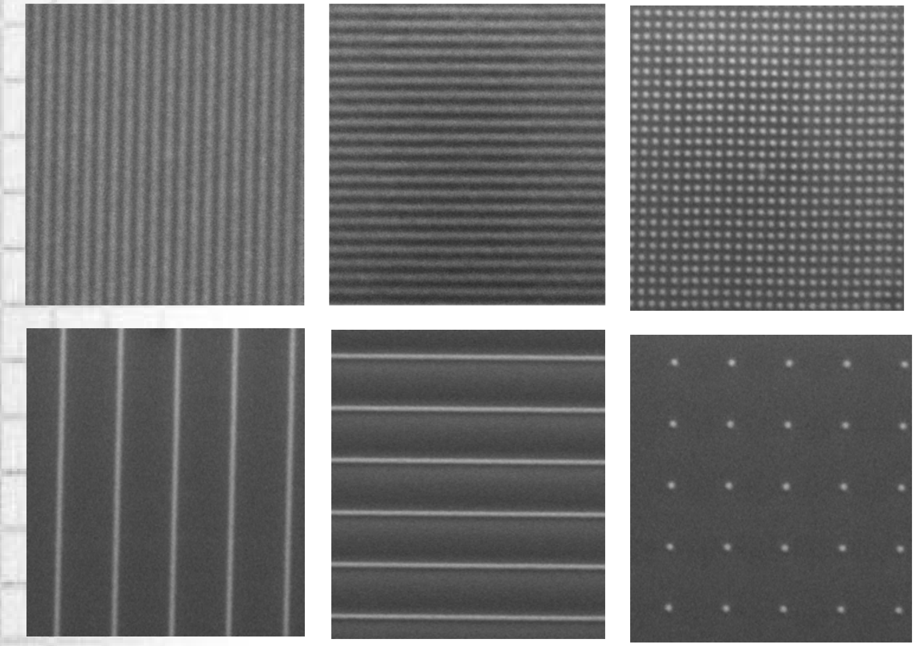
ArF immersion



MAPPER

- *Raster scan exposure @ 15μC/cm^2*
- *P-CAR 45 nm thickness*
- *Pixel size 2.25 nm*
- *EPC by Double Gaussian model*

Multiple-E-Beam Results



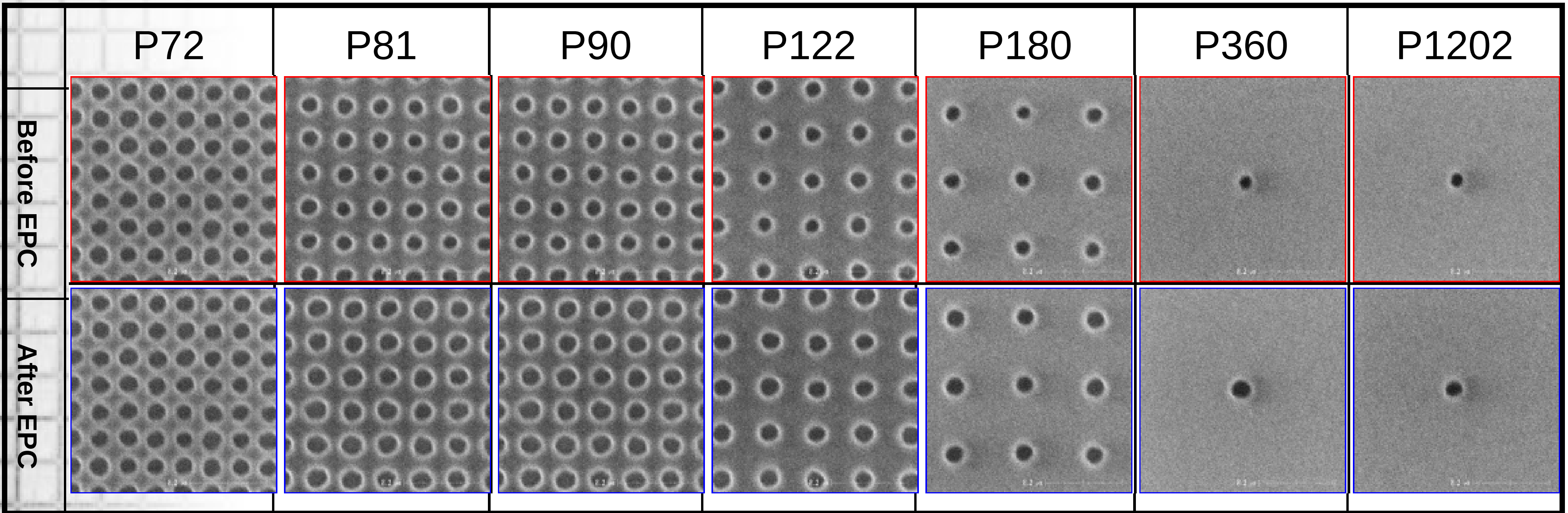
- 110 beams working
- Each beam covers a 2x2μm^2 block
- Met CD mean-to-target & CDU spec

pattern	CD [nm]	CD Mean-to-target [nm]			CDu [nm]	
	Measured	Required	Measured	Required	Measured	Required
Dots dense	43.4	45.0	1.6	3.2	2.5	4.5
Dots-Isolated	46.4	45.0	1.4	3.2	2.8	4.5
Horizontal dense	42.8	45.0	2.2	3.2	1.9	4.5
Horlines-isolated	42.1	45.0	2.9	3.2	3.0	4.5
Verlines-dense	44.9	45.0	0.1	3.2	2.8	4.5
Vertical iso lines	46.5	45.0	1.5	3.2	2.9	4.5

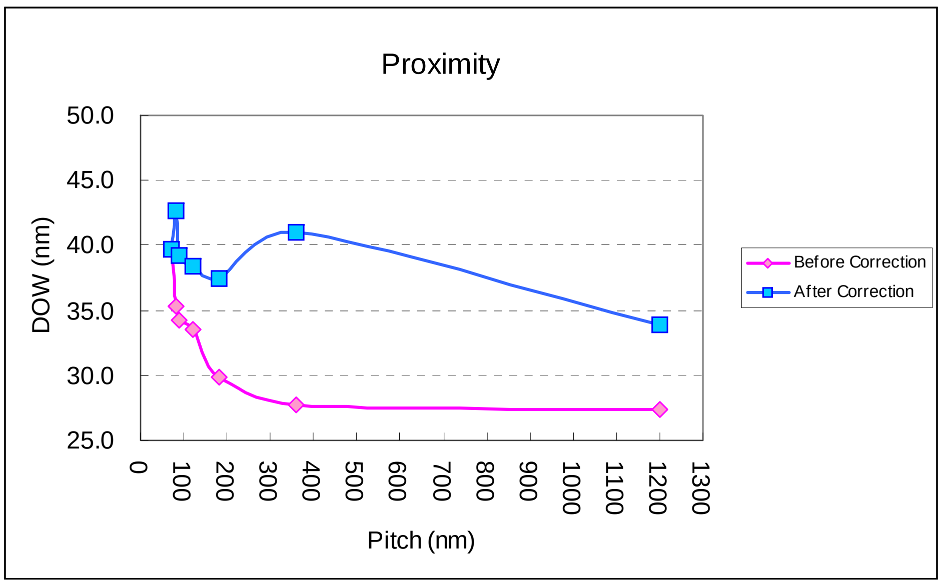
From 11 randomly selected beams. Data from 110 beams are substantially identical.

B.J. Lin, SPIE Proceedings vol. 7379, pp. 737902-1~11, 2009

EPC for MAPPER Pre-α Tool @ TSMC



45-nm CAR-P1@ 30 μC/cm^2



Proximity error:

12.3 nm before EPC,
8.7 nm after EPC (not yet optimized)

Cost Comparison

Tool Cost/(wph*cm^2)				
	ArF Dry	ArF imm SPT	ArF imm DPT	EUV N14
300-mm Scanners	26%	46%	90%	1
300-mm MEB DW	9%	21%	32%	66%
450-mm MEB DW	4%	15%	24%	54%

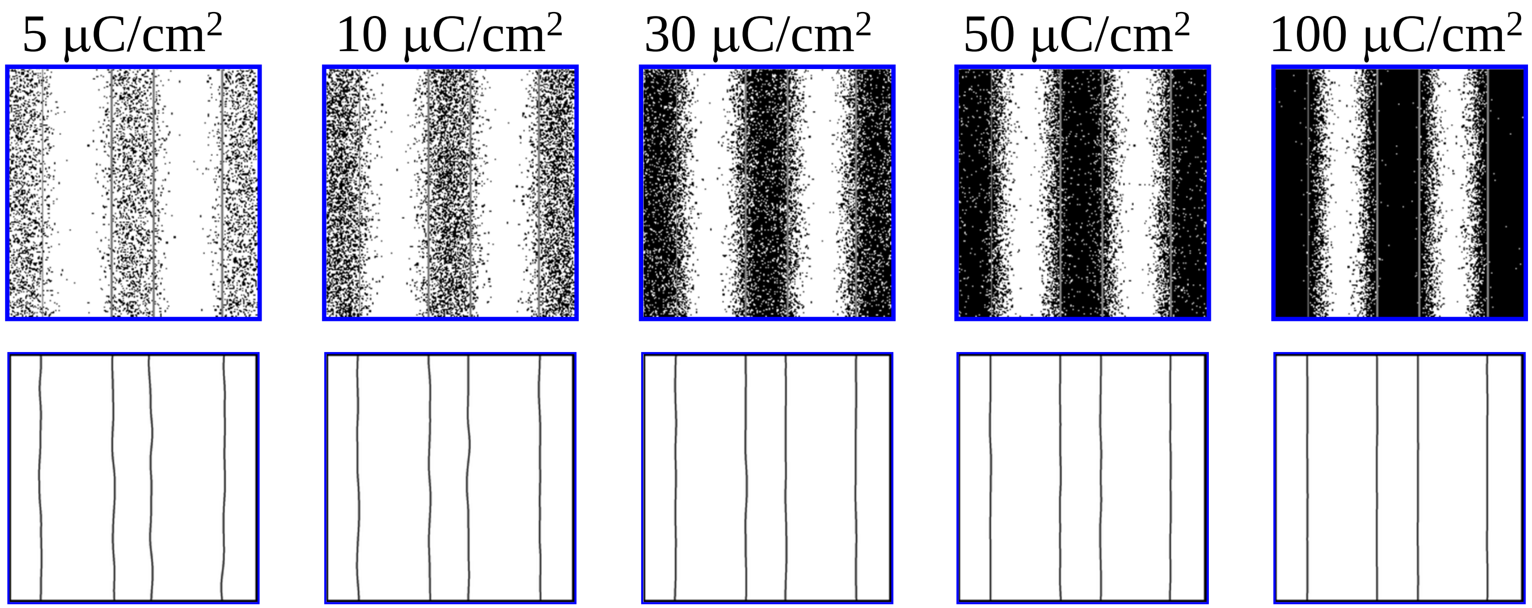
Assumptions for All-Layer REBL System

Node (nm)	130	65	28	20	14	10
Spot(blur) size with 3.5 NILS normalized to 10nm node	12.1	5.9	2.9	2.0	1.4	1.0
Blur-limited beam current / col. normalized to 10nm node	33.9	15.6	6.7	4.1	2.3	1.0
Beam current reduction ratio per node	0.7	0.7	0.6	0.6	0.6	0.4
Throughput loss from stitching (TSMC estimate)	6.1%	6.1%	6.1%	6.1%	6.1%	6.1%
Throughput loss from overhead (TSMC estimate)	2.78%	2.78%	2.78%	2.78%	2.78%	2.78%
Throughput loss from wasted area (geometrical)	31.5%	31.5%	31.5%	31.5%	31.5%	31.5%
Resist sensitivity ($\mu C/cm^2$)	20	20	40	40	60	60

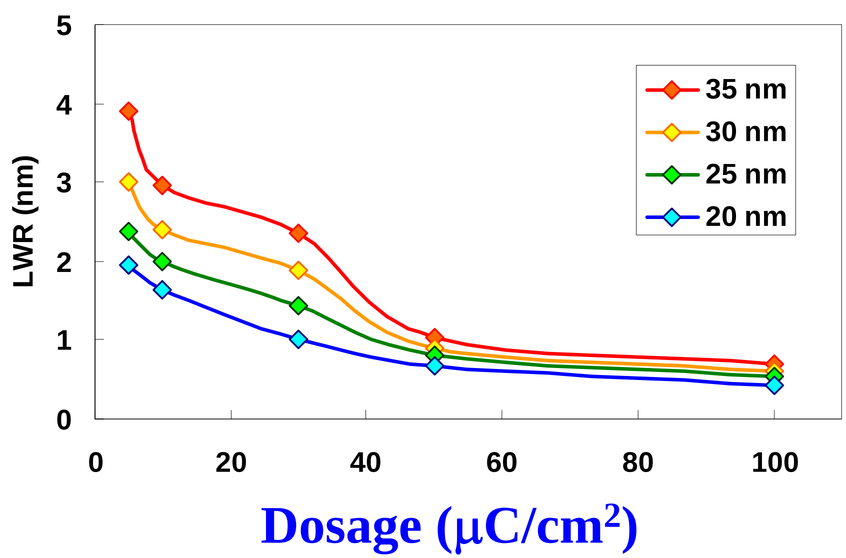
LWR vs. Exposure Dosage

Distribution of incident electrons

Contour of the latent image



LWR vs. dosage at different beam sizes

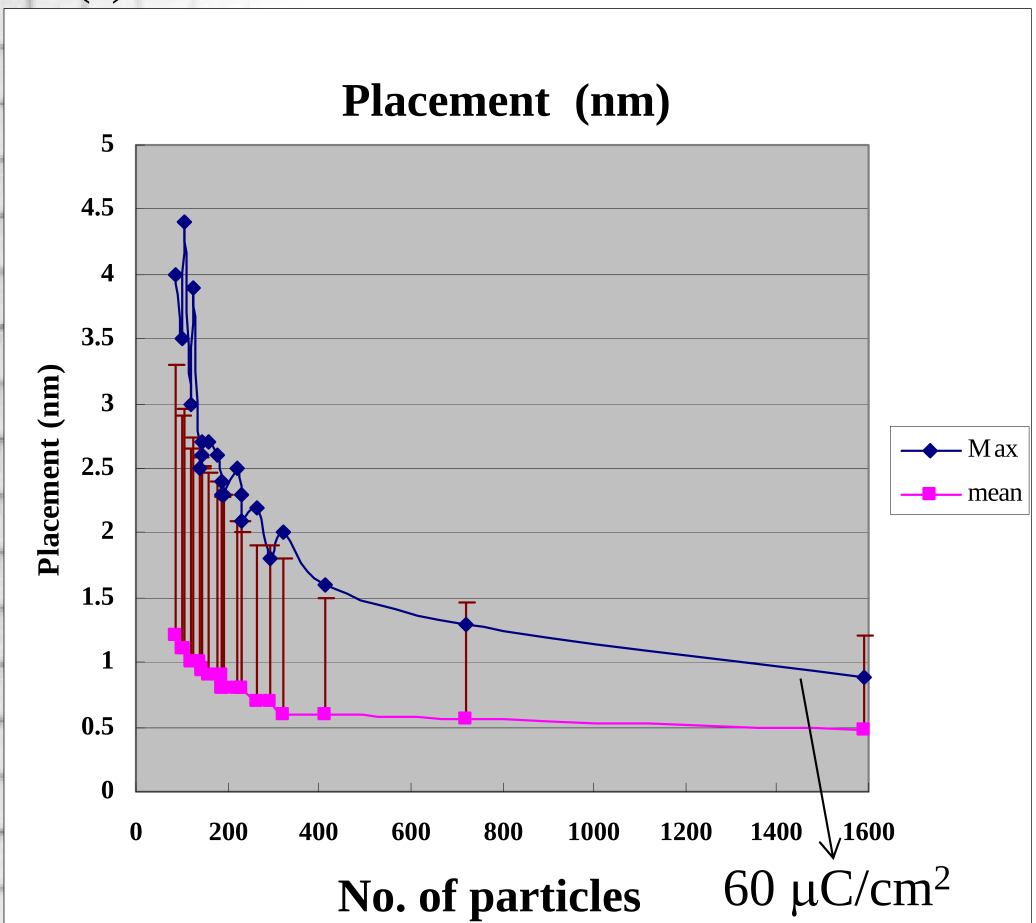


Acid diffusion and electron scattering contribute 10-nm blur.

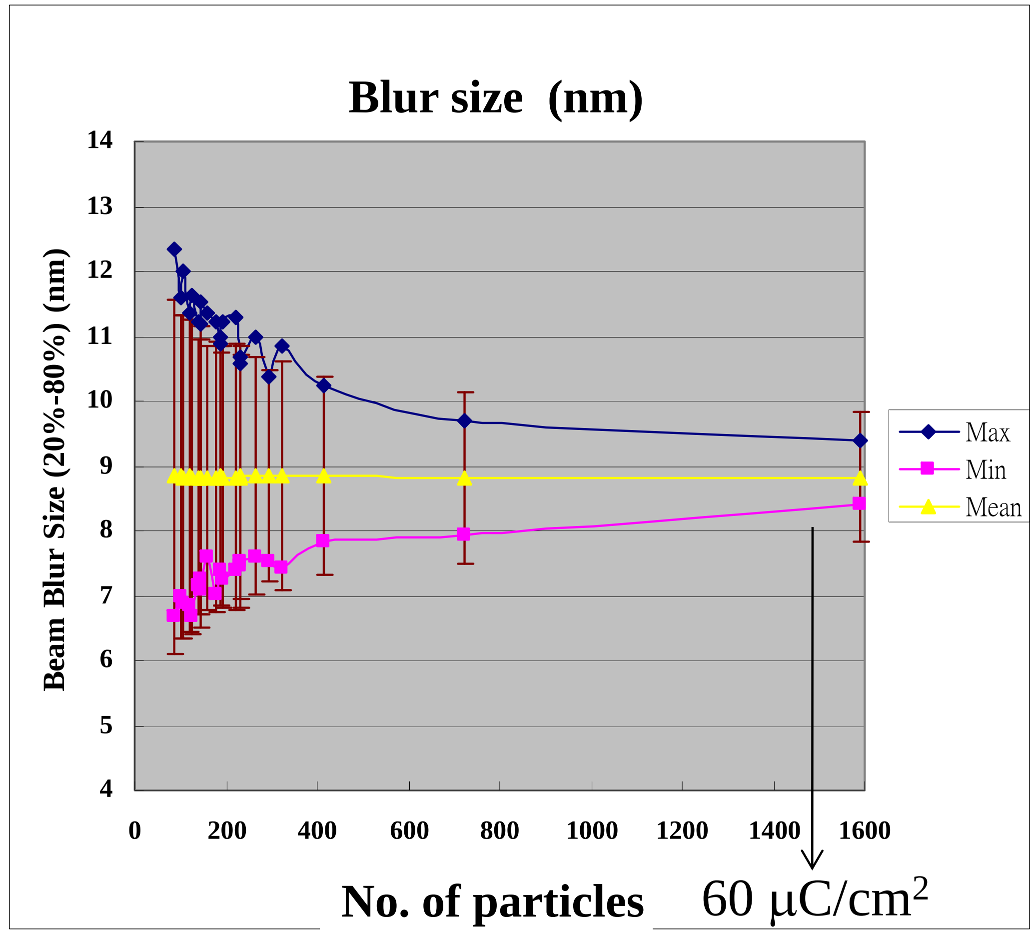
Shot Noise Induced Placement Error

- REBL optics performance by Monte Carlo simulation
- Current = 1.5 μA (100wph@6% pattern density) @ Focus (100 kV on wafer)

(a) Placement after correction



(b) Beam Blur Size (9 nm@100 wph or 1.5 µA)



Shot noise induces ~1 nm placement error.

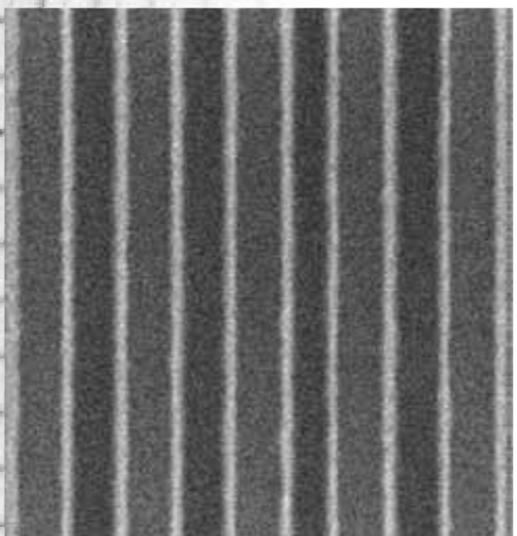
Cost & Throughput For Holes

Node (nm)		130	65	28	20	14	10
Holes pattern density		6%	6%	6%	6%	6%	6%
Required beam current / col. on DPG with respect to 10nm blur-limited beam current		565.1	260.3	111.0	67.9	37.8	16.7
Beam current on DPG not exceeding source brightness limit per col. with respect to 10nm blur-limited beam current		102.1	102.1	102.1	67.9	37.8	16.7
Avail. beam current/col. on wafer for Holes, with respect to 10nm beam current on DPG		6.12	6.12	6.12	4.07	2.27	1.00
Hole CD (nm)		255	125	61	43	30	21
Pixel size for hole (nm) - 1/4 of CD		63.7	31.2	15.3	10.7	7.5	5.3
Grey level		5	5	5	5	5	5
Data rate/column(Gbps) for holes		44.3	184	384	522	395	355
Hardware	wph / column	21.6	21.6	10.8	7.2	2.7	1.2
	No. of Columns	7	7	14	21	28	36
	No. of Platforms	1	1	1	1	2	4
	Total wph	151	151	151	151	149	169
Costs include platforms, columns, datapath, & infrastructure normalized to 14nm EUV	Tool cost normalized to EUV14	9%	10%	14%	19%	35%	72%
	Normalized tool cost / wph	5.6E-04	6.5E-04	9.6E-04	1.3E-03	2.4E-03	4.3E-03
	Normalized Si cost / (wph*cm^2)	8.0E-07	9.2E-07	1.4E-06	1.8E-06	3.4E-06	6.0E-06

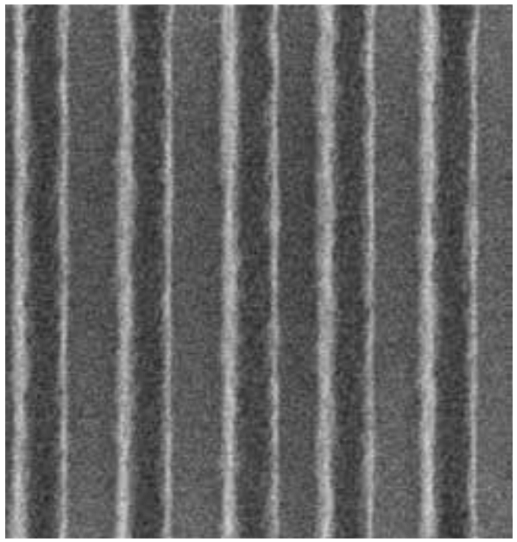
300mm Wafer

IMPLANT Layers Exposed with 50 keV E-Beam

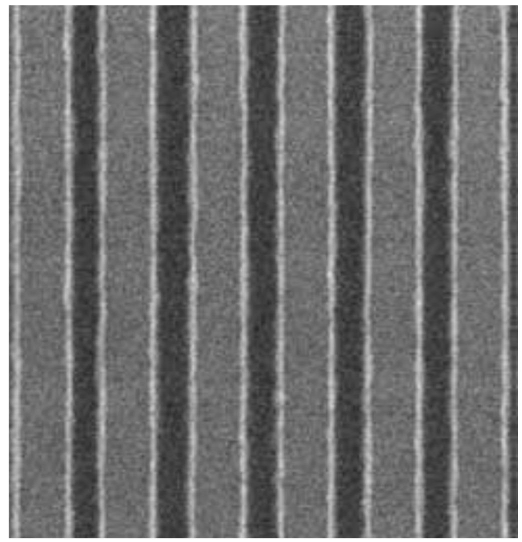
Well implant
PR Thickness: 650 nm
L/S = 180/140 nm
Resist -2, 52 $\mu C/cm^2$



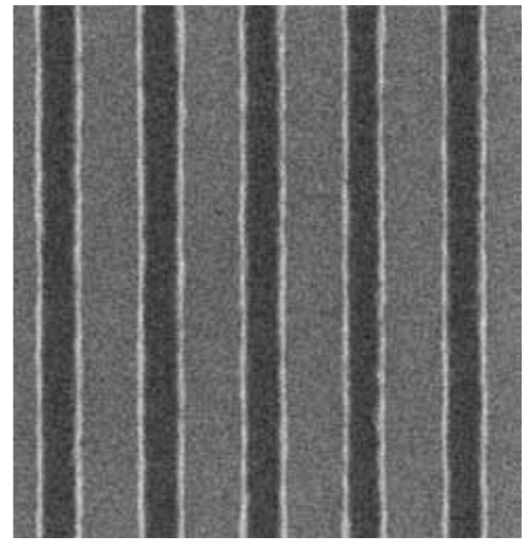
Well implant
PR Thickness: 650 nm
L/S = 152/148 nm
Resist -3, 16 $\mu C/cm^2$



S/D implant
PR Thickness: 150 nm
L/S = 123/137 nm
Resist -1, 52 $\mu C/cm^2$



S/D implant
PR Thickness: 150 nm
L/S = 126/174 nm
Resist -1, 56 $\mu C/cm^2$

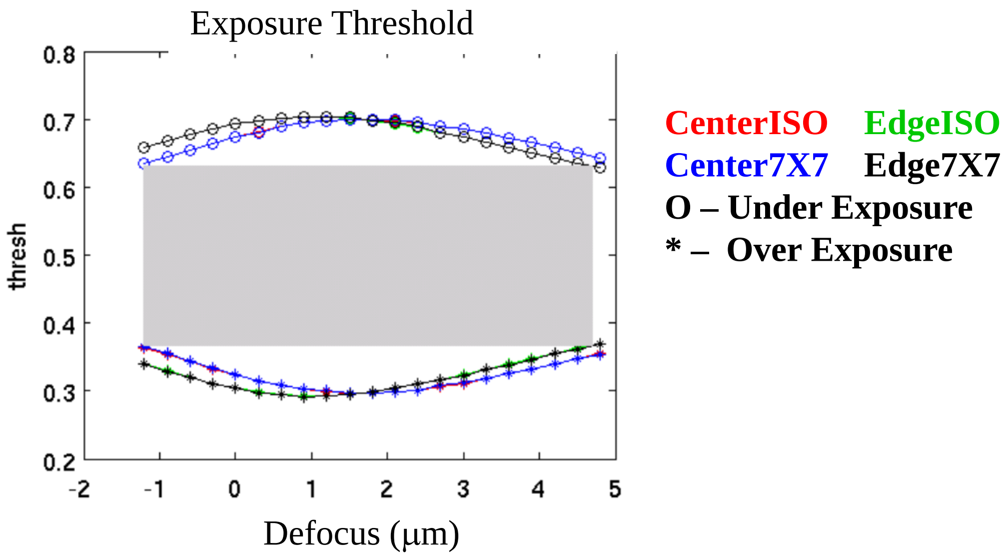


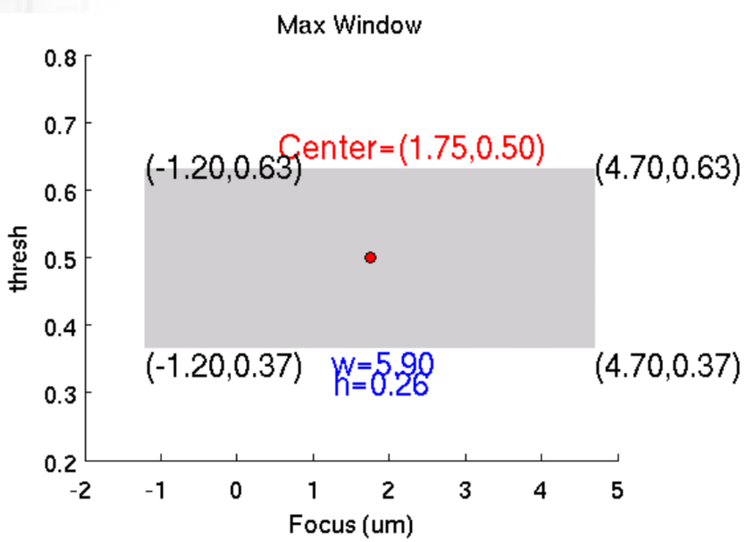
50-KV tool - Hitachi HL-800D
Substrate : Si
Courtesy of Sumitomo Chemical Co., Ltd.

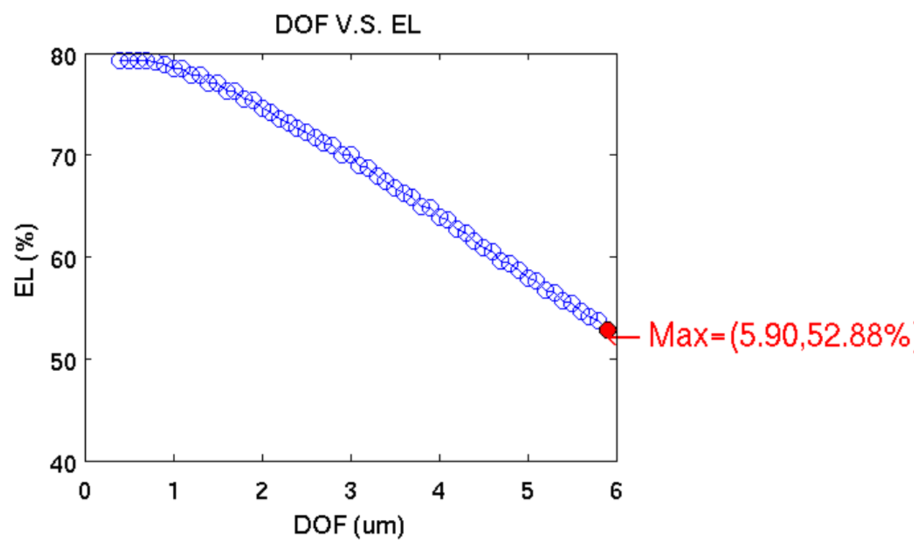
E-D Window of 14nm Node Well Implant

REBL tool provides the much desired overlay accuracy and DOF at low cost

		N14
Column: B-F Curve	Current	7μA 16mrad
	DPG	C, E
M-C Simulation	S/P	150nm/300nm
		PR 700nm
Window Calculation	Acid Diffusio	20nm
		Blur=[(Blur$_{B\text{-}F}$*1.4)^2+20^2]^0.5





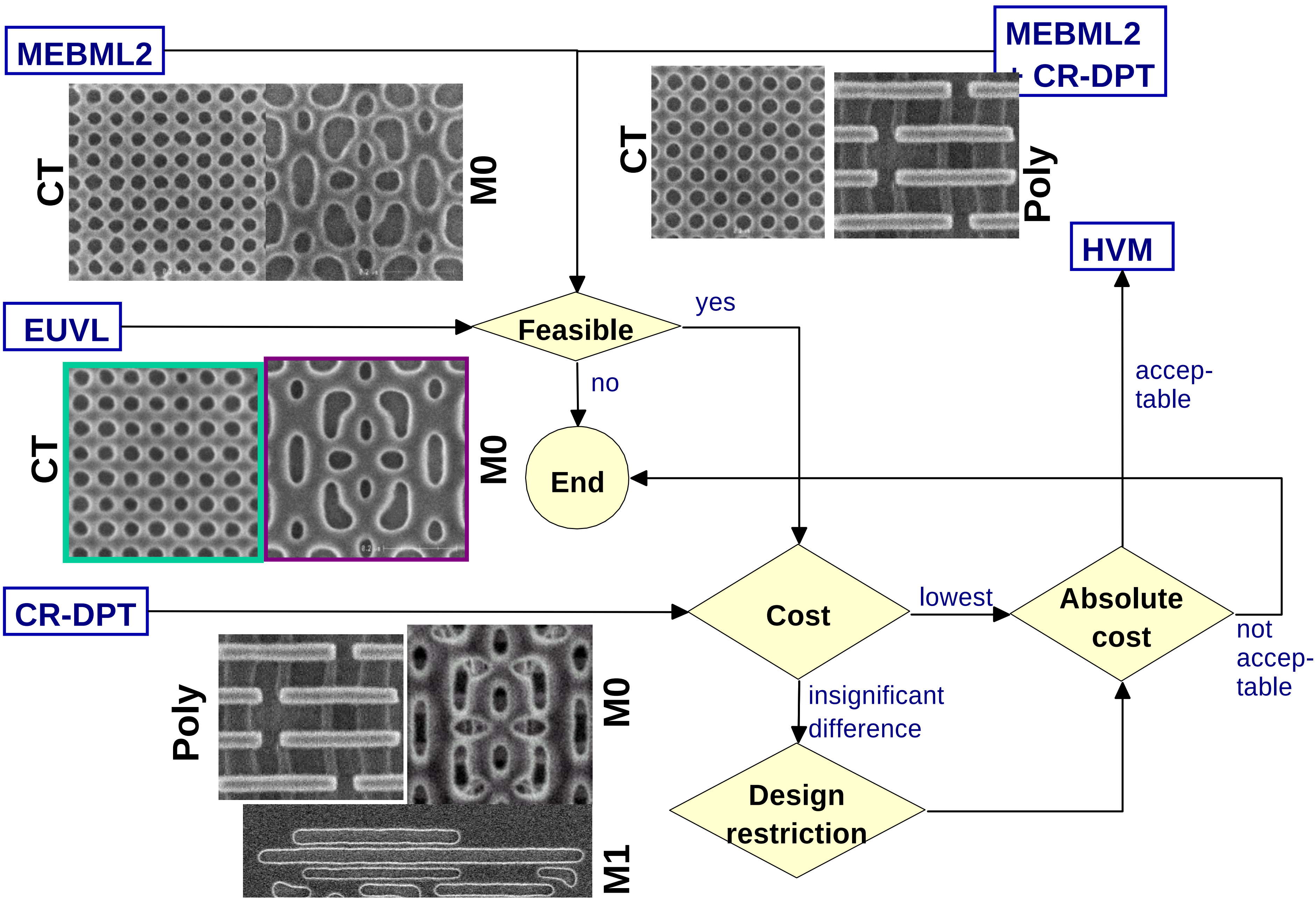


Iso & Dense curves overlap. The proximity effect is negligible.

REBL 450mm All-Layer Systems

- MEB DW is the only known innovation that can save cost by increasing wafer size.
- There is no longer a 26x33mm^2 field size limit.
- Tool matching between layers is much simplified.
- Mask contribution can be removed from wafer CDU and overlay budget.
- Mask cost, contamination, inspection, repair, and cycle time are no longer issues.
- Low-resolution/cost, high alignment accuracy, large DOF for implant layers.
- Low development, operation, and maintenance costs.
- Single platform/column system facilitates resist and academic research.

Litho Decision Tree



March. 2012

End of Presentation

CD Tolerance Considerations

Node	22nm	16nm	11nm	8nm	CD tol budget
Half Pitch (nm)	32	22	16	11	
CD (nm)	22	16	11	8	
Mask CD tol at 1X (nm) 60% of wafer, MEEF=1.5	1.39	1.01	0.69	0.50	6.3%
Wafer litho CD tol (nm)	1.54	1.12	0.77	0.56	7.0%
Wafer non-litho CD tol (nm)	0.74	0.54	0.37	0.27	3.4%
Total EUV CD tol (nm)	2.20	1.60	1.10	0.80	10%
Total maskless CD tol (nm)	1.71	1.24	0.85	0.62	7.8%

Overlay Considerations

Node	22nm	16nm	11nm	8nm	Overlay budget
CD (nm)	22	16	11	8	100%
Overlay requirement (nm) CD/3	7.3	5.3	3.7	2.7	33.3%
Wafer overlay (nm) single tool	6.0	4.2	2.9	2.1	27.3%
Mask edge placement budget (nm) 60% wafer overlay residue	3.6	2.5	1.8	1.2	16.4%
Mask flatness contribution allowed (nm) 1/3 of overlay requirement	2.4	1.8	1.2	0.9	11.1%
EUV CD contribution to overlay (nm) [CD Tol]/√2	1.6	1.1	0.8	0.6	7.1%
Maskless CD contribution to overlay (nm) [CD Tol]/√2	1.2	0.9	0.6	0.4	5.5%
EUV total overlay accuracy (nm)	7.6	5.3	3.7	2.6	34.4%
Maskless total overlay accuracy (nm)	6.1	4.3	3.0	2.1	27.8%

Defect Considerations

MEB

- Electrostatic chuck at wafer, if a proprietary non-static chuck is not used
- Contamination
- Wafer processing

EUV

- Electrostatic chuck at reticle and wafer
- Contamination
- Source debris
- Mask defects
- Wafer processing

Wall Power 1/14/2010

kW	Immer. scanner	EUV HVM			MEB HVM	
	Supplier estimate	Supplier estimate	30 mJ/cm^2 instead of 10 mJ/cm^2	30 mJ/cm^2 resist + conservative collector and source effeciencies	Ten 10-wph columns	Share datapath
Source	89	580	1,740	16,313	120	120
Exposure unit	130	169	190	190		
Datapath					250	53
Total per tool	219	749	1,930	16,503	370	173
Total for 59 tools	12,921	44,191	113,870	973,648	21,830	10,222
Fraction of scanner power in fab	8.61%	29.46%	75.91%	649.10%	14.55%	6.81%

130k wafers per month 12" fab, 150,000 kW

Throughput Loss at Node Advances

MEB

- **2X due to data volume**
  Use next-node datapath
- **2X due to shot noise**
  Increase parallelism or source brightness
- **2X due to lower current for higher resolution**
  Increase parallelism or source brightness

1st method

2nd method

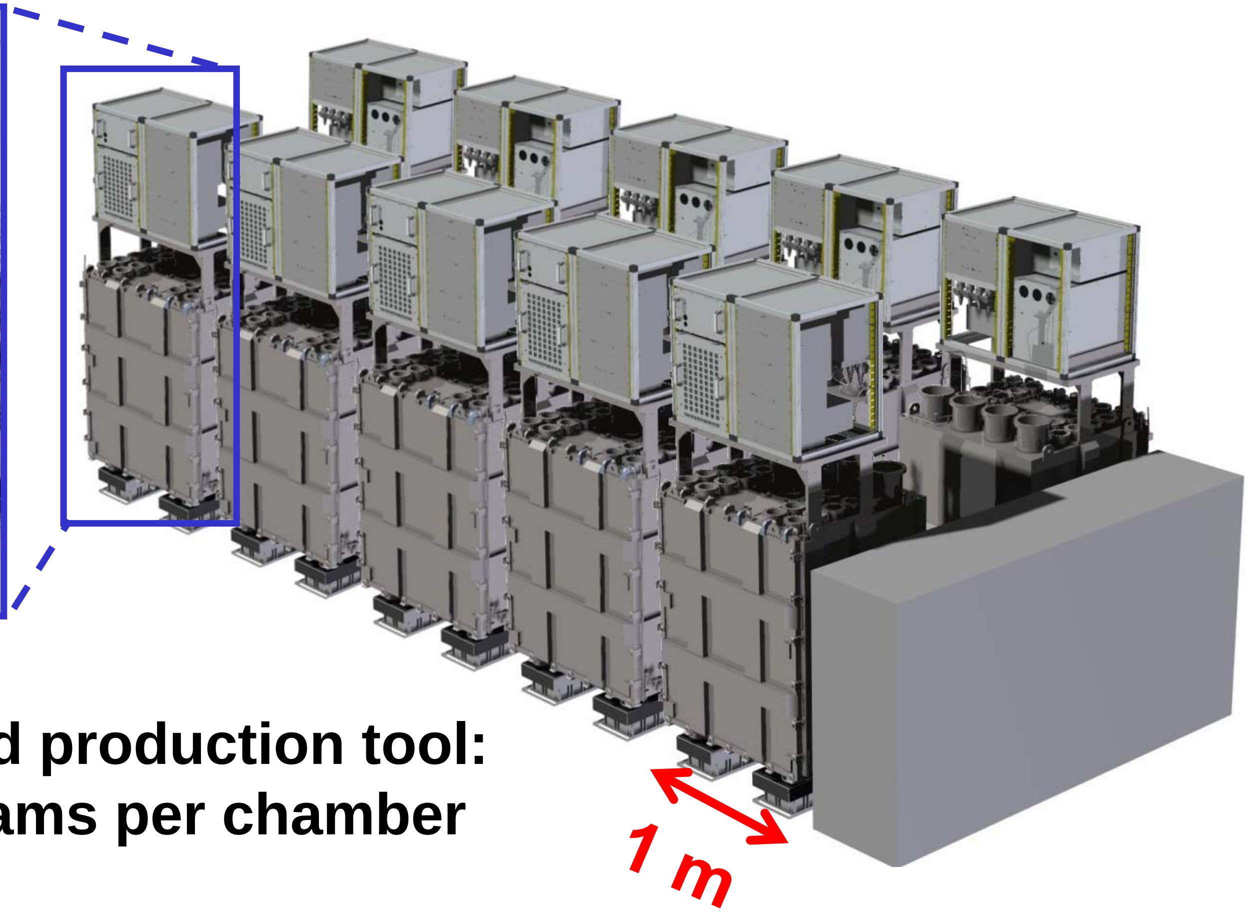
3rd method

EUV

- **2X due to shot noise**
  Increase source power
- **2X due to more mirrors for higher NA**
  Increase source power

1st method

Multiple E-Beam Maskless Lithography for High Volume Manufacturing



HVM clustered production tool:

- **>13,000 beams per chamber (10 WPH)**
- **10 WPH x 5 x 2 = 100 WPH**
- **Footprint ~ArF scanner**

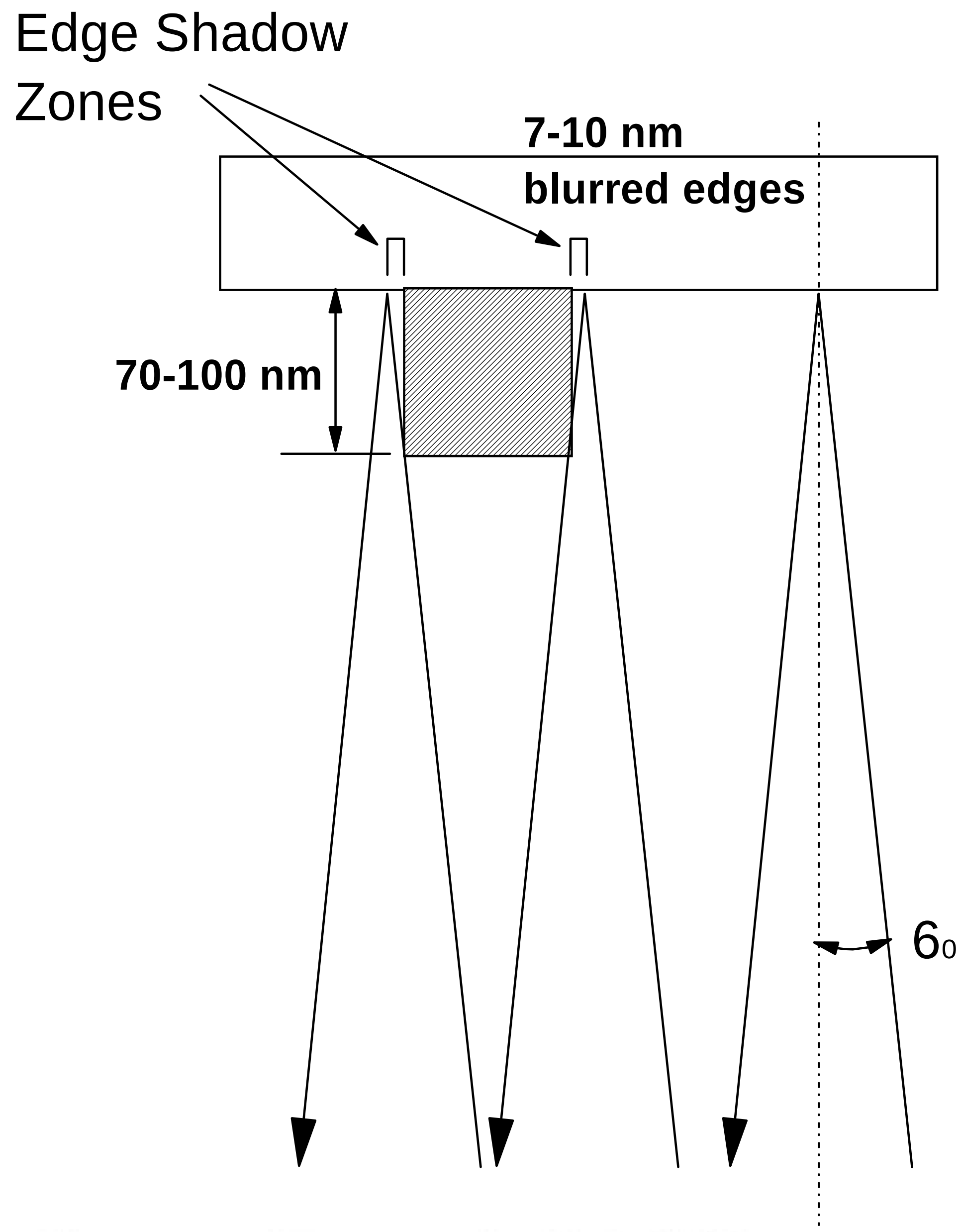
EUV Mask Flatness

- Let 1/3CD be the overlay requirement and 1/3 overlay budget allocated to mask positioning error $\Delta x' < 2.44$ nm.
- When there is no mask rotation, $\Delta z_{tran} < 46.5$ nm. Mask flatness has to be better than 46.5 nm.
- When there is mask rotation, Δz_{tran} has to be even smaller.
- 193-nm mask flatness spec is 500 nm.

Pushing the Limits of Lithography

- **Pitch splitting**
  - *Cost*
  - *Design rule restriction*
  - *Processing complexity*
  - *Requirement of overlay accuracy*
- **Further wavelength reduction – EUV**
- **Multiple E-Beam Maskless lithography**

Shadow of Edges from Oblique Illumination



Portability of Resists to 450mm

- Resists for critical layers have to be developed regardless of wafer size or tool type.
- Even the same resist had to be modified for 200->300 mm transition for scanners.
- It is a golden opportunity to move to better resist systems with scanners anyway.
- We do not expect much difficulty to switch resist, because only the resist thickness is the key parameter for implant layers.