A Size Scaling Approach for Mixed-Size Placement

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Challenges in Physical Design

- High complexity and conflicting objectives
- Large variations in the size of the components on chip
- Pre-placed and fixed macros acting as obstacles
- Elaborate optimization algorithms

Wirelength-Driven Placement

Constrained optimization problem formulation

$$\min WL(x,y)$$

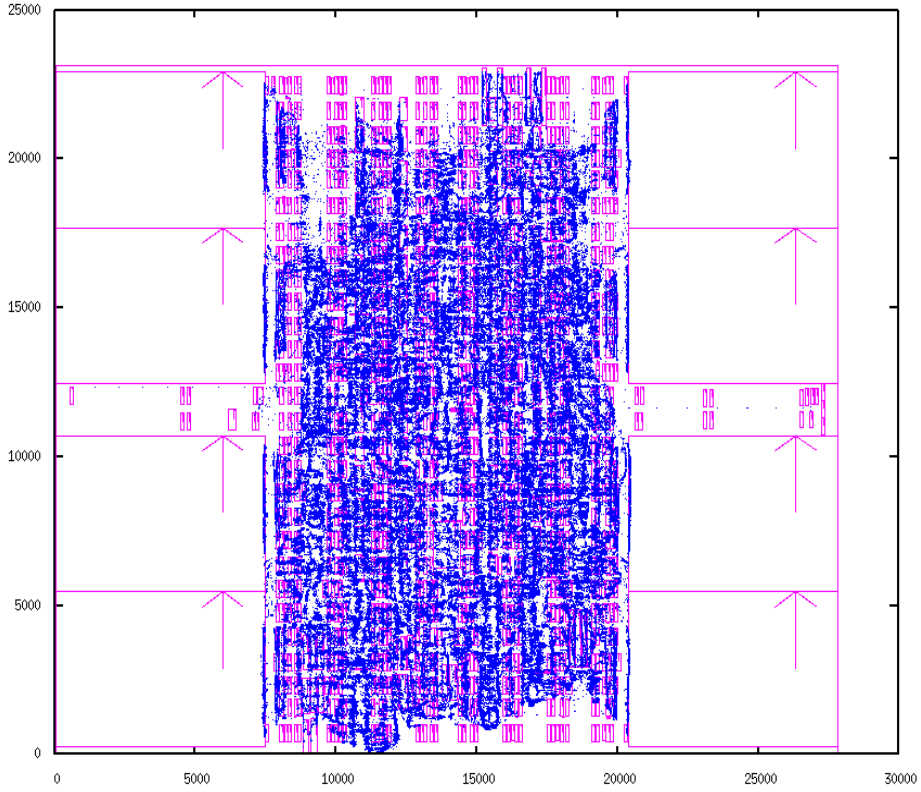
$$s.t.$$

$$SD_b(x,y) \le w_b h_b - SD_{b,fixed}(x,y)$$

Equivalent unconstrained optimization problem

$$\min WL(x,y) +$$

$$\frac{1}{2u}(SD_b(x,y) - (w_b h_b - SD_{b,fixed}(x,y)))^2$$



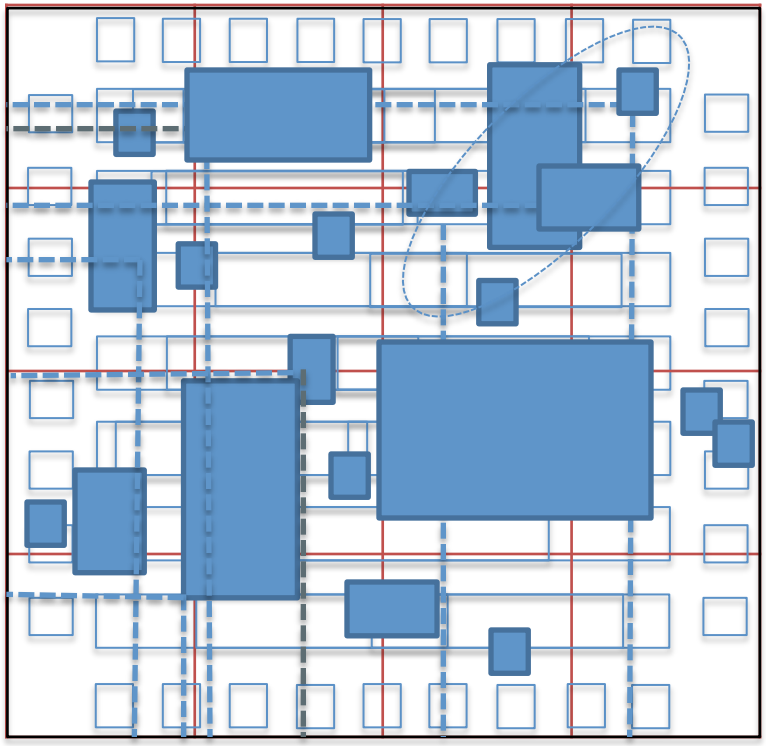
Size Scaling in Placement

Large macros

- Create uneveness of placement region
- Prevent cells from moving to their natural locations

Size scaling

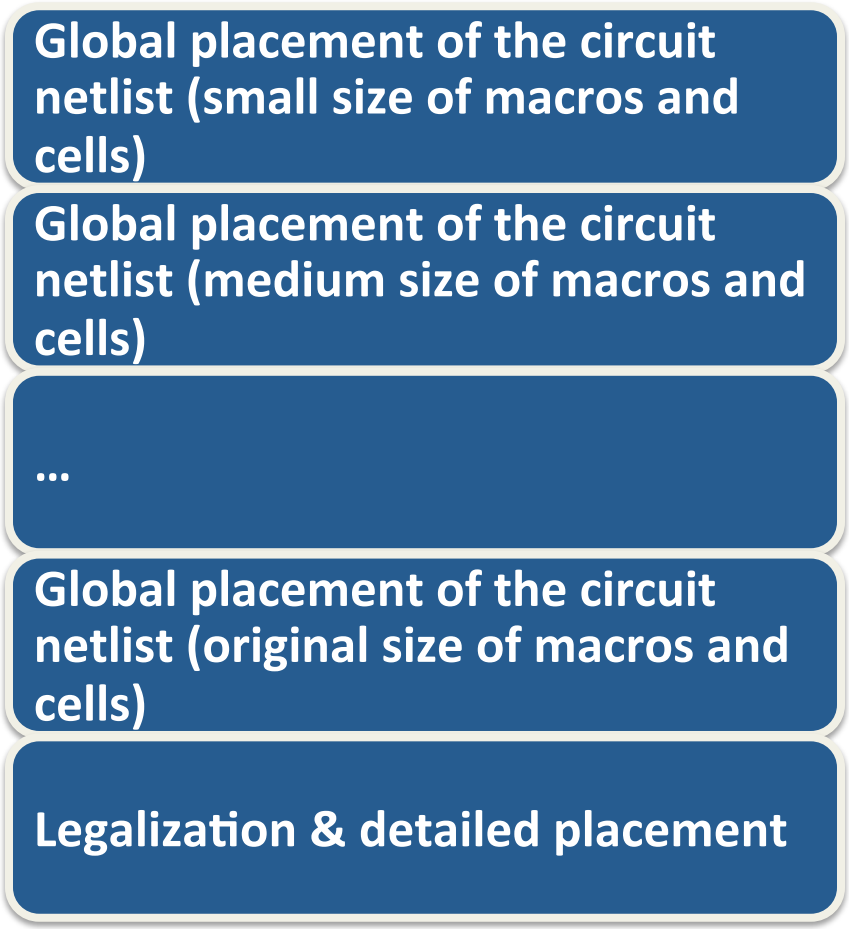
- Preserves smoothness of placement region
- Provides continuity in placement



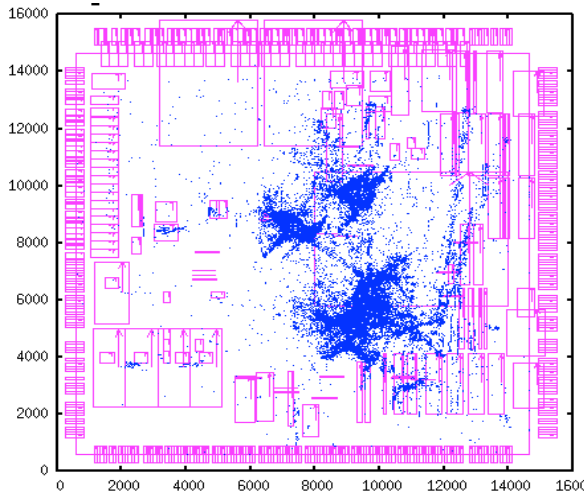
Size Scaling in Placement

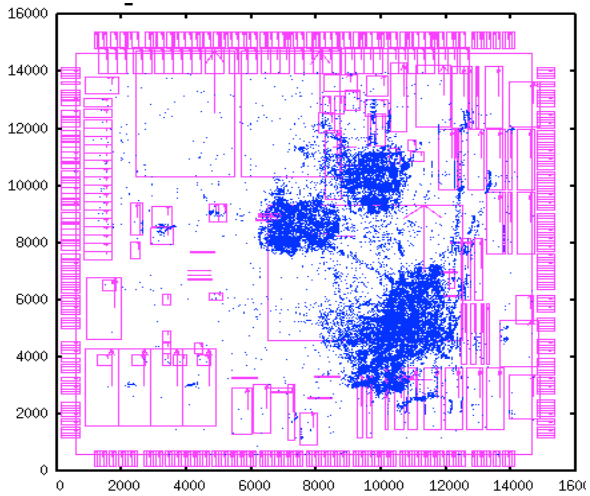
Size scaling

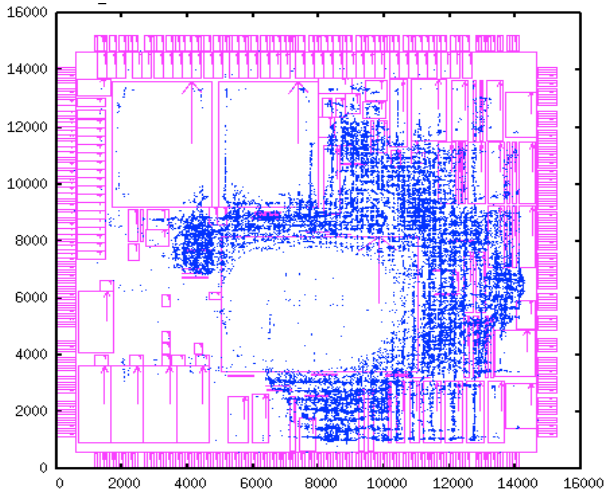
- Flat placement approach
- Original circuit netlist is placed
- Initially, placement components have small sizes
- Gradually, placement components scale up to their original sizes

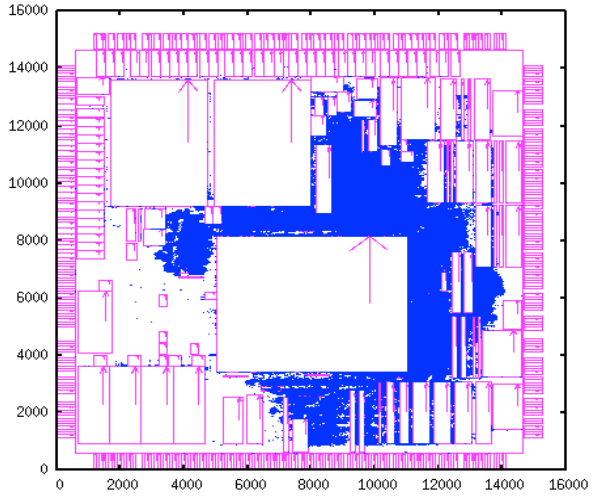


Size Scaling in Placement









Size Scaling in Placement

Size scaling pattern

$$w_{cell} = cell_{width,\min} + (cell_{width,orig} - cell_{width,\min}) \frac{1 + Step}{NumStep},$$

$$h_{cell} = cell_{height,\min} + (cell_{height,orig} - cell_{height,\min}) \frac{1 + Step}{NumStep},$$

$$w_{macro} = macro_{width,\min} + (macro_{width,orig} - macro_{width,\min}) \frac{1 + Step}{NumStep},$$

$$h_{macro} = macro_{height,\min} + (macro_{height,orig} - macro_{height,\min}) \frac{1 + Step}{NumStep}.$$

Experimental Results (ISPD05)

	Ours		mPL6 [Chan et. al.]		NTUPlace3 [Chen et al.]		APlace2 [Kahng et al.]		simPL [Kim et al.]	
	HPWL (x e8)	**CPU (s)**	**HPWL (x e8)**	**CPU (s)**	**HPWL (x e8)**	**CPU (s)**	**HPWL (x e8)**	**CPU (s)**	**HPWL (x e8)**	**CPU (s)**
adaptec1	0.78	1320	0.80	2041	0.81	689	0.78	3164	0.78*	136*
adaptec2	0.90	1398	0.92	2095	0.90	685	0.96	4598	0.90*	209*
adaptec3	1.96	3420	2.14	6196	2.15	1719	2.19	11167	2.09*	472*
adaptec4	1.84	2597	1.94	5705	1.94	2047	2.09	12726	1.87*	318*
bigblue1	9.39	2160	9.68	2531	9.74	1387	1.00	4124	9.74*	241*
bigblue2	1.42	5100	1.52	6338	1.52	4457	1.54	9545	1.46*	497*
bigblue3	3.35	6360	3.44	8720	3.61	5213	4.12	19299	3.40*	827*
bigblue4	8.07	14520	8.29	20062	8.29	10200	8.71	49572	8.08*	2148*
avg.	**1.00**		**1.04**		**1.05**		**1.09**		**1.02***	

Experimental Results (ISPD06)

	Ours		mPL6 [Chan et. al.]		NTUPlace3 [Chen et al.]		APlace2 [Kahng et al.]	
	HPWL (x e8)	CPU (s)	HPWL (x e8)	CPU (s)	HPWL (x e8)	CPU (s)	HPWL (x e8)	CPU (s)
adaptec5	3.32	5564	3.33	10688	3.71	3335	3.54	17592
newblue1	6.15	1850	6.32	2552	6.05	887	6.55	6764
newblue2	1.91	4789	1.99	6253	2.03	2144	1.96	12543
newblue3	2.79	5670	2.84	6701	2.80	1142	2.78	16779
newblue4	2.44	7201	2.47	7430	2.51	3977	2.64	12559
newblue5	4.21	9587	4.23	13693	4.34	8529	4.40	19494
newblue6	4.98	9899	4.99	12591	4.98	7111	5.03	21485
newblue7	N/A	N/A	3.32	5564	N/A	N/A	10.80	53153
avg.	**1.00**		**1.02**		**1.03**		**1.04**	

Conclusion

Placement approach

- Consists of size scaling to handle large variations in size among macros and cells
- Obtained better placement solutions for the circuits of ISPD05 and ISPD06 mixed-size placement benchmark suites